LM4890 Boomer® Audio Power Amplifier Series 1 Watt Audio Power Amplifier

Check for Samples: LM4890

FEATURES

- **Available in Space-Saving Packages: DSBGA, VSSOP, SOIC, and WSON**
- **Ultra Low Current Shutdown Mode**
- **BTL Output Can Drive Capacitive Loads**
- **Improved Pop & Click Circuitry Eliminates Noises During Turn-On and Turn-Off Transitions**
- **2.2 - 5.5V Operation**
- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**
- **Thermal Shutdown Protection**
- **Unity-Gain Stable**
- **External Gain Configuration Capability**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **PSRR at 217Hz, VDD = 5V (Fig. 1): 62dB(typ.)**
- **Power Output at 5.0V & 1% THD: 1W(typ.)**
- **Power Output at 3.3V & 1% THD: 400mW(typ.)**
- **Shutdown Current: 0.1µA(typ.)**

DESCRIPTION

The LM4890 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4890 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4890 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4890 features an internal thermal shutdown protection mechanism.

The LM4890 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4890 is unity-gain stable and can be configured by external gain-setting resistors.

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Connection Diagrams

Top View

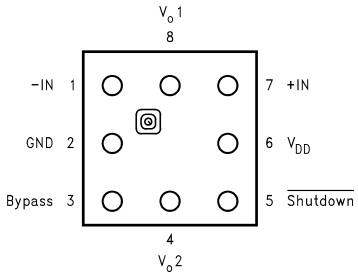


Figure 1. 8 Bump DSBGA Package
See Package Number YPB0008

Top View

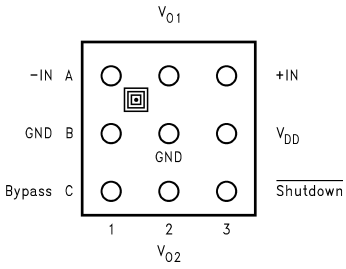


Figure 2. 9 Bump DSBGA Package
See Package Number YZR0009

Top View

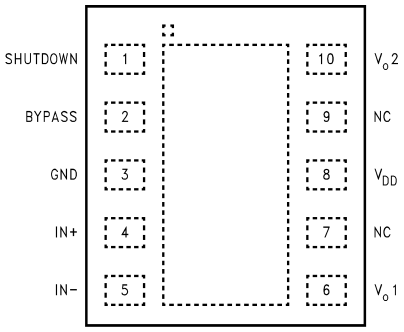


Figure 3. WSON Package
See Package Number NGZ0010B

Top View

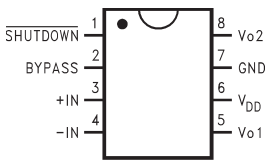


Figure 4. Mini Small Outline (VSSOP) Package
See Package Number DGK0008A

Top View

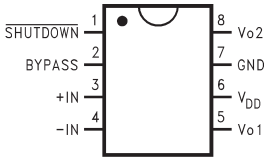


Figure 5. Small Outline (SOIC) Package
See Package Number D0008A

Top View

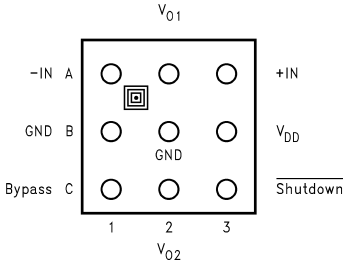


Figure 6. 9 Bump DSBGA Package
See Package Number YZR0009AAA

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Typical Application

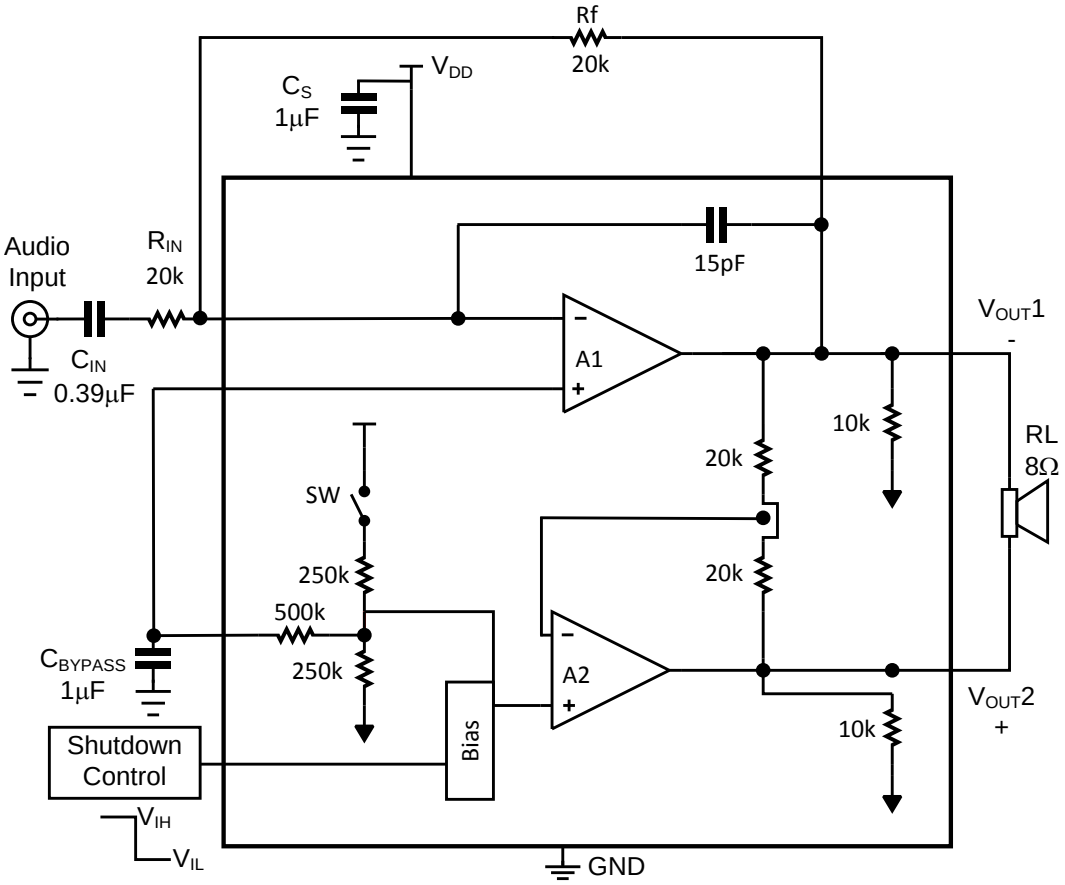


Figure 7. Typical Audio Amplifier Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage[3]		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation[4]		Internally Limited
ESD Susceptibility[5]		2000V
Junction Temperature		150°C
Thermal Resistance	θ_{JC} (SOIC)	35°C/W
	θ_{JA} (SOIC)	150°C/W
	θ_{JA} (8 Bump DSBGA,[6])	220°C/W
	θ_{JA} (9 Bump DSBGA,[6])	180°C/W
	θ_{JC} (VSSOP)	56°C/W
	θ_{JA} (VSSOP)	190°C/W
	θ_{JA} (WSON)	220°C/W
Soldering Information		See AN-1112 (SNVA009) "DSBGA Wafers Level Chip Scale Package." See AN-1187 (SNOA401) "Leadless Leadframe Package (WSON)."

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) If the product is in shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10 ma, then the part will be protected. If the part is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operational life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4890, see power derating curves for additional information.
(5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(6) All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. All bumps must be connected to achieve specified thermal resistance.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage	$2.2V \le V_{DD} \le 5.5V$

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Electrical Characteristics V_{DD} = 5V(1)(2)(3)

The following specifications apply for the circuit shown in Figure 7 unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4890		Units (Limits)
			Typical(4)	Limit(5) (6)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	4	8	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	5	10	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
V_{OS}	Output Offset Voltage		7	50	mV (max)
$R_{OUT-GND}$	Resistor Output to GND(7)		8.5	9.7	kΩ (max)
				7.0	kΩ (min)
P_o	Output Power (8Ω)	THD = 2% (max); f = 1 kHz	1.0	0.8	W
T_{WU}	Wake-up time		170	220	ms (max)
T_{SD}	Thermal Shutdown Temperature		170	150	°C (min)
				190	°C (max)
THD+N	Total Harmonic Distortion + Noise	P_o = 0.4 Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio(8)	V_{ripple} = 200mV sine p-p Input Terminated with 10 ohms to ground	62 (f = 217Hz) 66 (f = 1kHz)	55	dB (min)
T_{SDT}	Shut Down Time	8 Ω load	1.0		ms (max)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(6) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(7) ROUT is measured from each of the output pins to ground. This value represents the parallel combination of the 10k ohm output resistors and the two 20k ohm resistors.
(8) PSRR is a function of system gain. Specifications apply to the circuit in Figure 7 where A_V = 2. Higher system gains will reduce PSRR value by the amount of gain increase. A system gain of 10 represents a gain increase of 14dB. PSRR will be reduced by 14dB and applies to all operating voltages.

Electrical Characteristics V_{DD} = 3V(1)(2)(3)

The following specifications apply for the circuit shown in Figure 7 unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4890		Units (Limits)
			Typical(4)	Limit(5) (6)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	3.5	7	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	4.5	9	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V(min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V(max)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(6) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

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Electrical Characteristics V_{DD} = 3V[1][2][3] (continued)

The following specifications apply for the circuit shown in Figure 7 unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4890		Units (Limits)
			Typical[4]	Limit[5] [6]	
V_{OS}	Output Offset Voltage		7	50	mV (max)
$R_{OUT-GND}$	Resistor Output to Gnd[7]		8.5	9.7	kΩ (max)
				7.0	kΩ (min)
T_{WU}	Wake-up time		120	180	ms (max)
P_o	Output Power (8Ω)	THD = 1% (max); f = 1kHz	0.31	0.28	W
T_{SD}	Thermal Shutdown Temperature		170	150	°C(min)
				190	°C(max)
THD+N	Total Harmonic Distortion + Noise	P_o = 0.15Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio[8]	V_{ripple} = 200mV sine p-p Input terminated with 10 ohms to ground	56 (f = 217Hz) 62 (f = 1kHz)	45	dB(min)

(7) ROUT is measured from each of the output pins to ground. This value represents the parallel combination of the 10k ohm output resistors and the two 20k ohm resistors.
(8) PSRR is a function of system gain. Specifications apply to the circuit in Figure 7 where A_V = 2. Higher system gains will reduce PSRR value by the amount of gain increase. A system gain of 10 represents a gain increase of 14dB. PSRR will be reduced by 14dB and applies to all operating voltages.

Electrical Characteristics V_{DD} = 2.6V[1][2][3]

The following specifications apply for for the circuit shown in Figure 7 unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4890		Units (Limits)
			Typical[4]	Limit[5] [6]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	2.6		mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1		µA (max)
P_0	Output Power (8Ω) Output Power (4Ω)	THD = 1% (max); f = 1 kHz THD = 1% (max); f = 1 kHz	0.2 0.22		W W
THD+N	Total Harmonic Distortion + Noise	P_o = 0.1Wrms; f = 1kHz	0.08		%
PSRR	Power Supply Rejection Ratio[7]	V_{ripple} = 200mV sine p-p Input Terminated with 10 ohms to ground	44 (f = 217Hz) 44 (f = 1kHz)		dB

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(6) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(7) PSRR is a function of system gain. Specifications apply to the circuit in Figure 7 where A_V = 2. Higher system gains will reduce PSRR value by the amount of gain increase. A system gain of 10 represents a gain increase of 14dB. PSRR will be reduced by 14dB and applies to all operating voltages.

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External Components Description

(See Figure 7)

Components		Functional Description
1.	R_{IN}	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_{IN} at $f_C = 1/(2\pi R_{IN}C_{IN})$.
2.	C_{IN}	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_{IN} at $f_c = 1/(2\pi R_{IN}C_{IN})$. Refer to the section, Proper Selection of External Components, for an explanation of how to determine the value of C_{IN}.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_{IN}.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the section, Power Supply Bypassing, for information concerning proper placement and selection of the supply bypass capacitor, C_{BYPASS}.
5.	C_{BYPASS}	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_{BYPASS}.

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Typical Performance Characteristics

THD+N vs Frequency
at V_{DD} = 5V, 8Ω R_L, and PWR = 250mW, A_V = 2

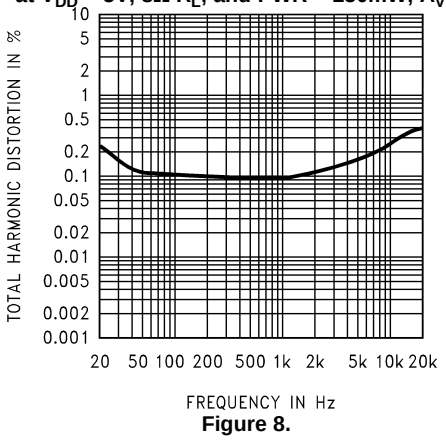


Figure 8.

THD+N vs Frequency
at V_{DD} = 3.3V, 8Ω R_L, and PWR = 150mW, A_V = 2

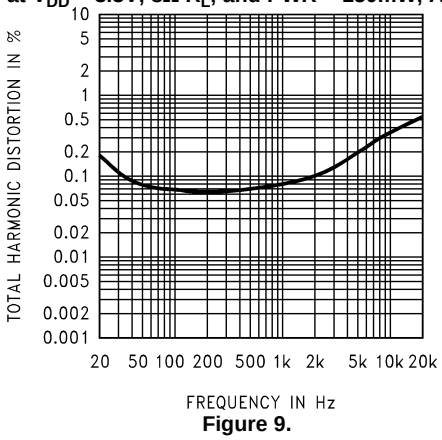


Figure 9.

THD+N vs Frequency
at V_{DD} = 3V, R_L = 8Ω, PWR = 250mW, A_V = 2

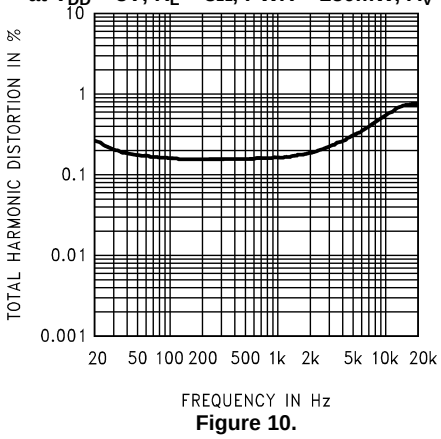


Figure 10.

THD+N vs Frequency
at V_{DD} = 2.6V, R_L = 8Ω, PWR = 100mW, A_V = 2

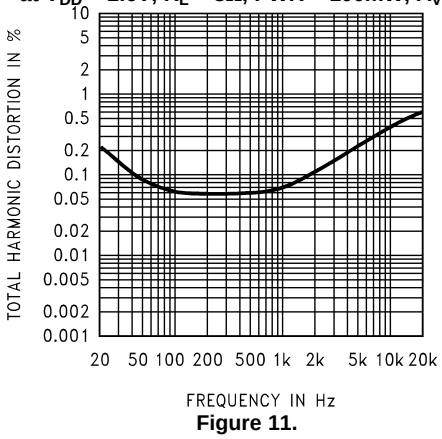


Figure 11.

THD+N vs Frequency
at V_{DD} = 2.6V, R_L = 4Ω, PWR = 100mW, A_V = 2

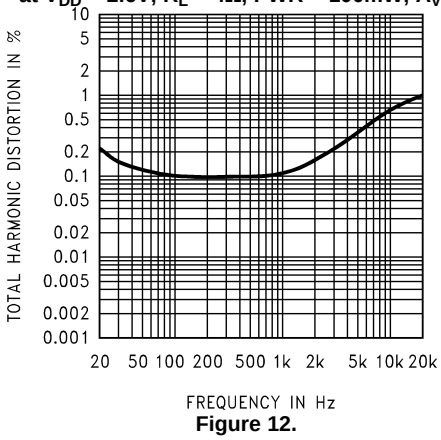


Figure 12.

THD+N vs Power Out
at V_{DD} = 5V, R_L = 8Ω, 1kHz, A_V = 2

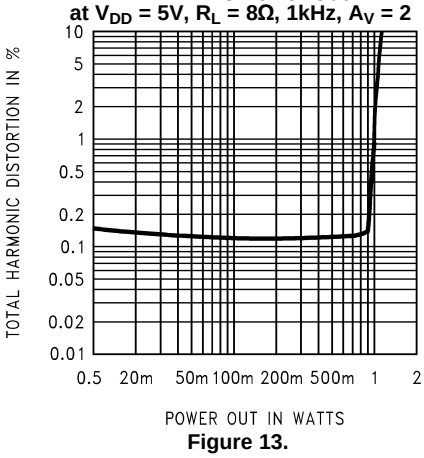


Figure 13.

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Typical Performance Characteristics (continued)

THD+N vs Power Out at V_{DD} = 3.3V, R_L = 8Ω, 1kHz, A_V = 2

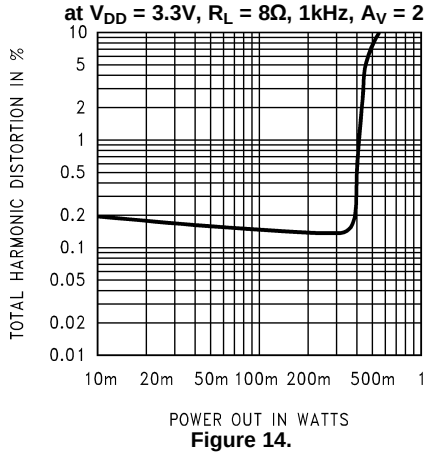


Figure 14.

THD+N vs Power Out at V_{DD} = 3V, R_L = 8Ω, 1kHz, A_V = 2

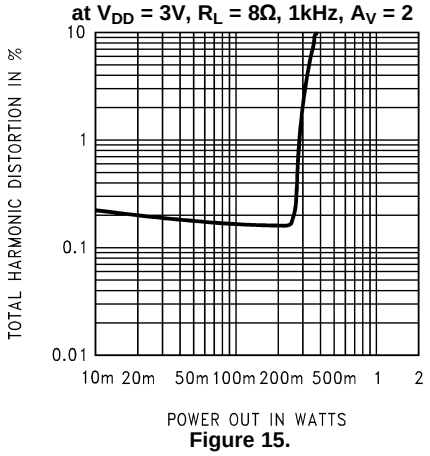


Figure 15.

THD+N vs Power Out at V_{DD} = 2.6V, R_L = 8Ω, 1kHz, A_V = 2

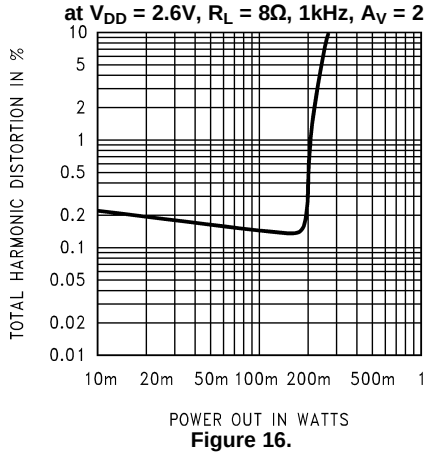


Figure 16.

THD+N vs Power Out at V_{DD} = 2.6V, R_L = 4Ω, 1kHz, A_V = 2

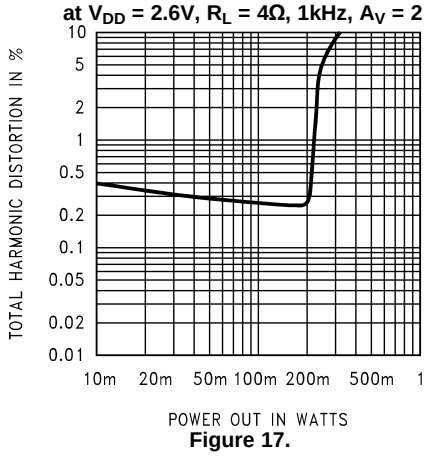


Figure 17.

Power Supply Rejection Ratio (PSRR) at A_V = 2
V_{DD} = 5V, V_{ripple} = 200mvp-p
R_L = 8Ω, R_{IN} = 10Ω

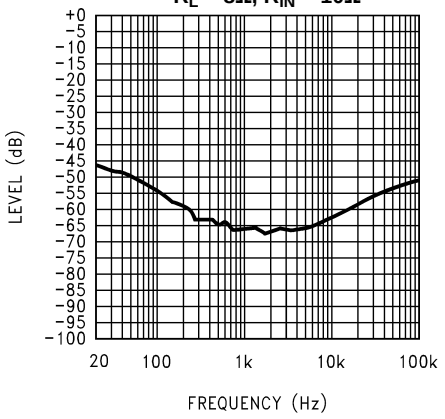


Figure 18.

Power Supply Rejection Ratio (PSRR) at A_V = 2
V_{DD} = 5V, V_{ripple} = 200mvp-p
R_L = 8Ω, R_{IN} = Float

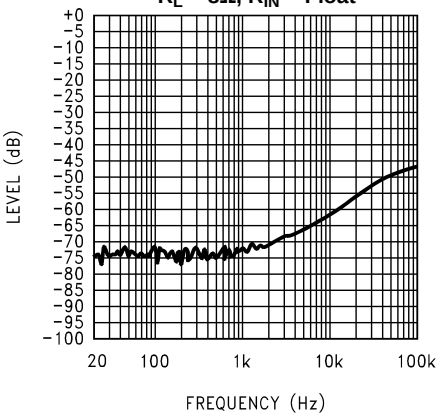


Figure 19.

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Typical Performance Characteristics (continued)

Power Supply Rejection Ratio (PSRR) at A_V = 4
V_{DD} = 5V, V_{ripple} = 200mvp-p
R_L = 8Ω, R_{IN} = 10Ω

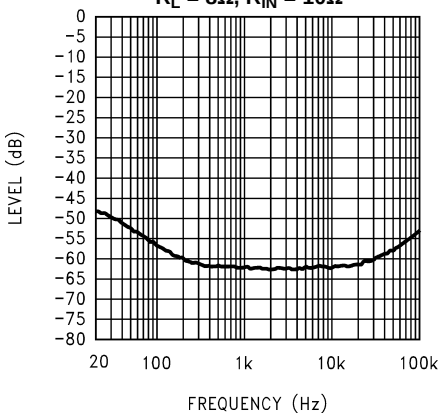


Figure 20.

Power Supply Rejection Ratio (PSRR) at A_V = 4
V_{DD} = 5V, V_{ripple} = 200mvp-p
R_L = 8Ω, R_{IN} = Float

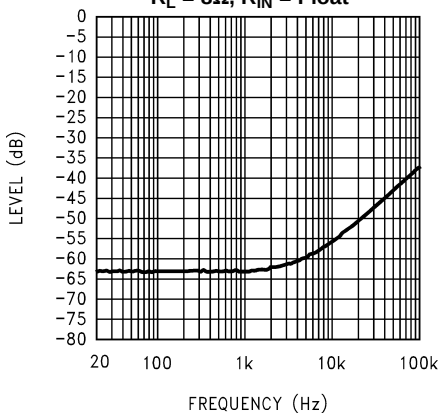


Figure 21.

Power Supply Rejection Ratio (PSRR) at A_V = 2
V_{DD} = 3V, V_{ripple} = 200mvp-p,
R_L = 8Ω, R_{IN} = 10Ω

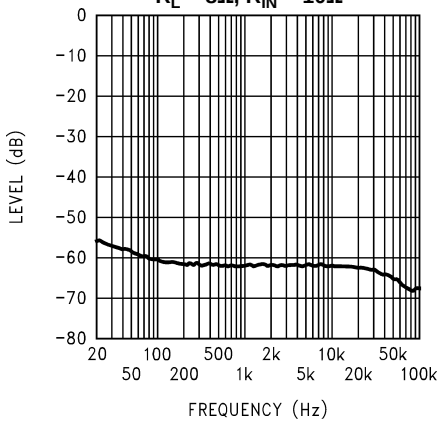


Figure 22.

Power Supply Rejection Ratio (PSRR) at A_V = 2
V_{DD} = 3V, V_{ripple} = 200mvp-p,
R_L = 8Ω, R_{IN} = Float

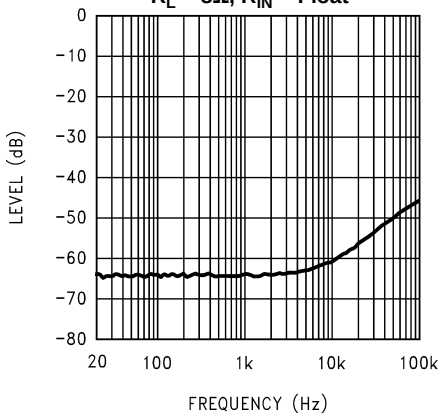


Figure 23.

Power Supply Rejection Ratio (PSRR) at A_V = 4
V_{DD} = 3V, V_{ripple} = 200mvp-p,
R_L = 8Ω, R_{IN} = 10Ω

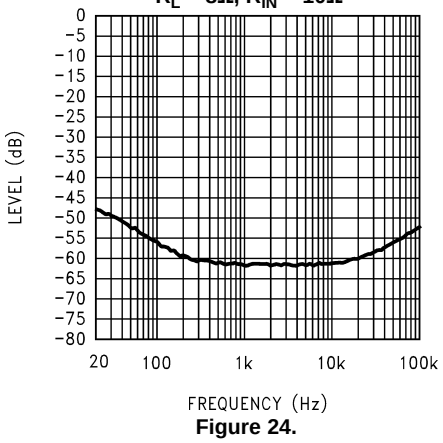


Figure 24.

Power Supply Rejection Ratio (PSRR) at A_V = 4
V_{DD} = 3V, V_{ripple} = 200mvp-p,
R_L = 8Ω, R_{IN} = Float

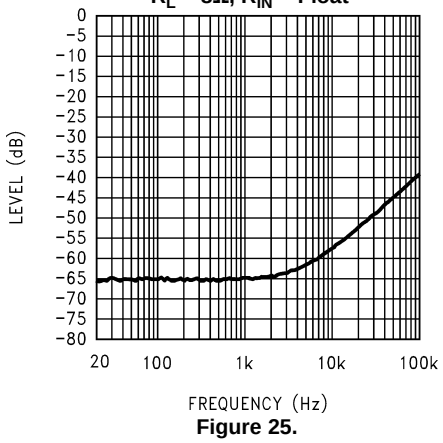


Figure 25.

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Typical Performance Characteristics (continued)

Power Supply Rejection Ratio (PSRR) at A_V = 2
V_{DD} = 3.3V, V_{ripple} = 200mvp-p,
R_L = 8Ω, R_{IN} = 10Ω

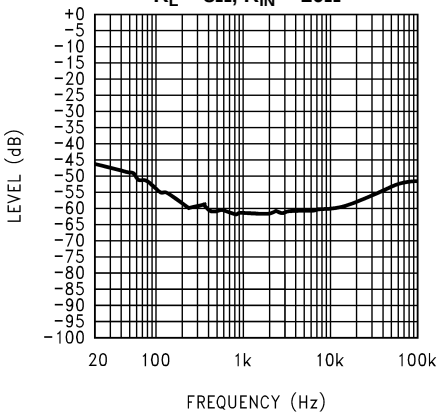


Figure 26.

Power Supply Rejection Ratio (PSRR) at A_V = 2
V_{DD} = 2.6V, V_{ripple} = 200mvp-p,
R_L = 8Ω, R_{IN} = 10Ω

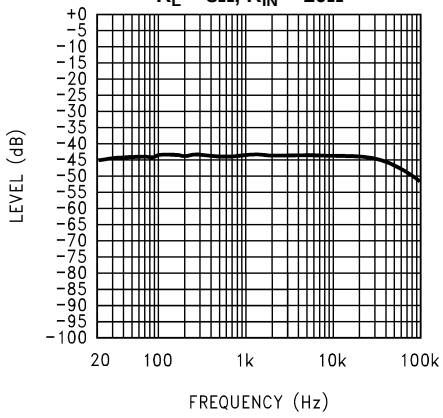


Figure 27.

PSRR vs DC Output Voltage
V_{DD} = 5V, A_V = 2

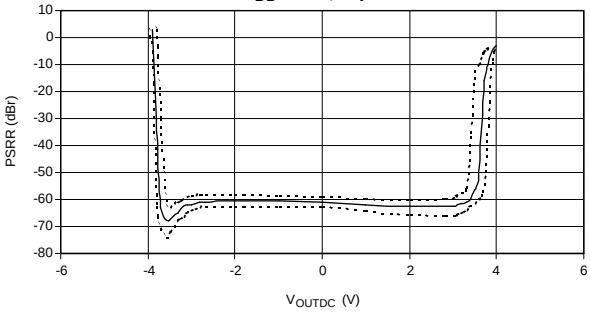


Figure 28.

PSRR vs DC Output Voltage
V_{DD} = 5V, A_V = 4

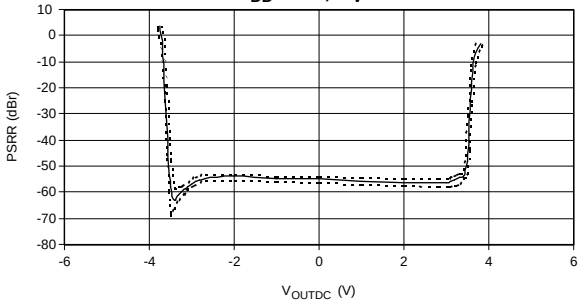


Figure 29.

PSRR vs DC Output Voltage
V_{DD} = 5V, A_V = 10

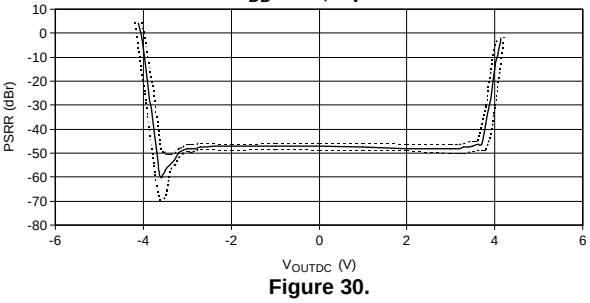


Figure 30.

PSRR vs DC Output Voltage
V_{DD} = 3V, A_V = 2

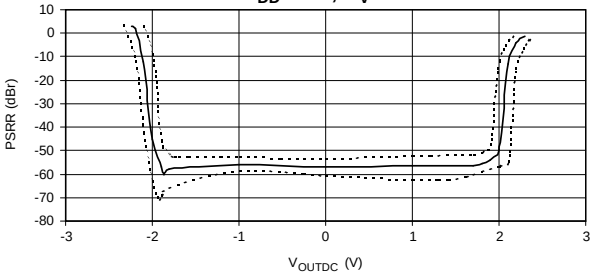


Figure 31.

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Typical Performance Characteristics (continued)

PSRR vs DC Output Voltage
V_{DD} = 3V, A_V = 4

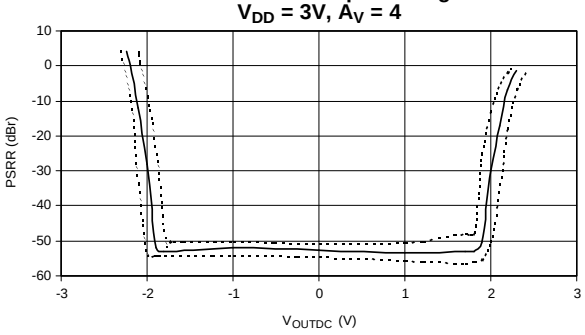


Figure 32.

PSRR vs DC Output Voltage
V_{DD} = 3V, A_V = 10

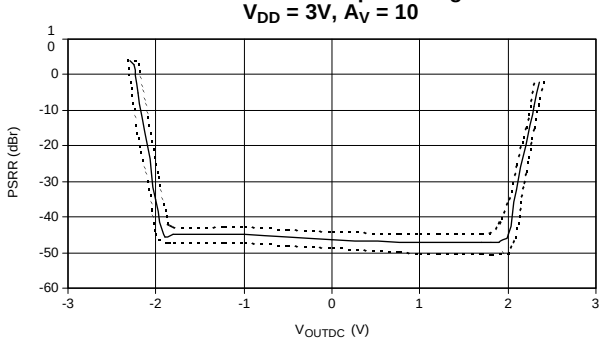


Figure 33.

PSRR Distribution V_{DD} = 5V
217Hz, 200mvp-p,
-30, +25, and +80°C

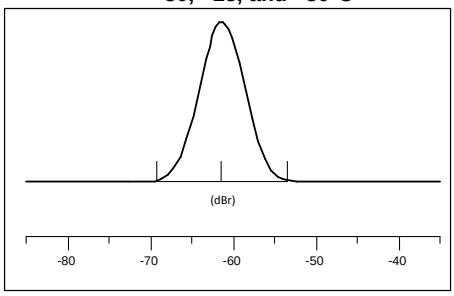


Figure 34.

PSRR Distribution V_{DD} = 3V
217Hz, 200mvp-p,
-30, +25, and +80°C

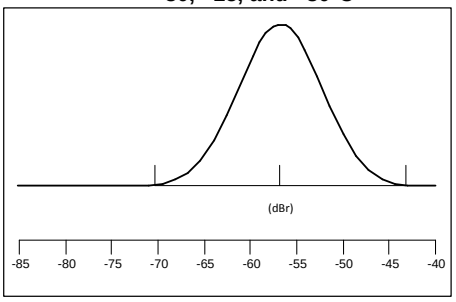


Figure 35.

Power Supply Rejection Ration vs
Bypass Capacitor Size
V_{DD} = 5V, Input Grounded = 10Ω, Output Load = 8Ω

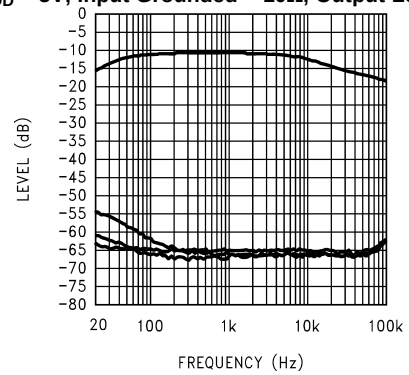


Figure 36. Top Trace = No Cap, Next Trace Down = 1µf
Next Trace Down = 2µf, Bottom Trace = 4.7µf

Power Supply Rejection Ration vs
Bypass Capacitor Size
V_{DD} = 3V, Input Grounded = 10Ω, Output Load = 8Ω

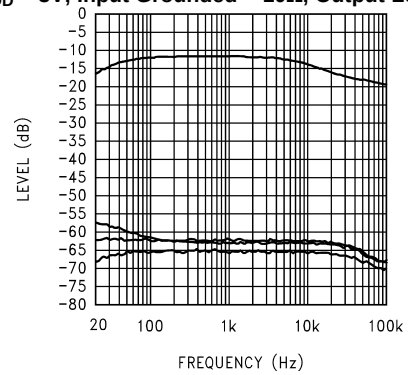


Figure 37. Top Trace = No Cap, Next Trace Down = 1µf
Next Trace Down = 2µf, Bottom Trace = 4.7µf

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Typical Performance Characteristics (continued)

LM4890 vs LM4877 Power Supply Rejection Ratio
V_{DD} = 5V, Input Grounded = 10Ω
Output Load = 8Ω, 200mV Ripple

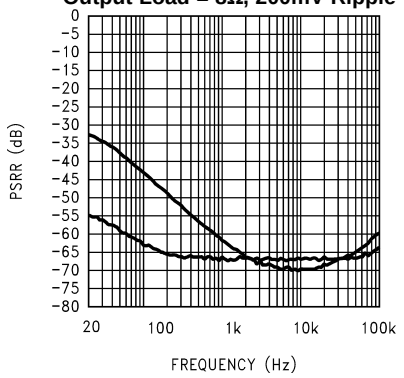


Figure 38. LM4890 = Bottom Trace
LM4877 = Top Trace

LM4890 vs LM4877 Power Supply Rejection Ratio
V_{DD} = 3V, Input Grounded = 10Ω
Output Load = 8Ω, 200mV Ripple

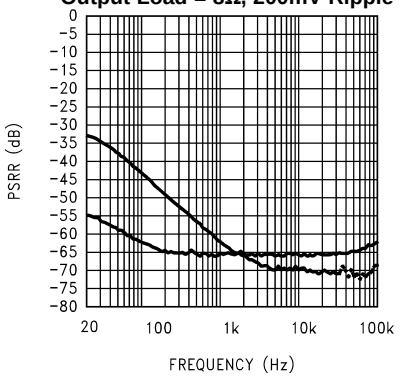
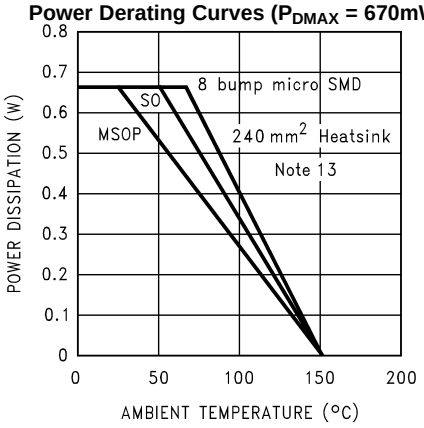


Figure 39. LM4890 = Bottom Trace
LM4877 = Top Trace

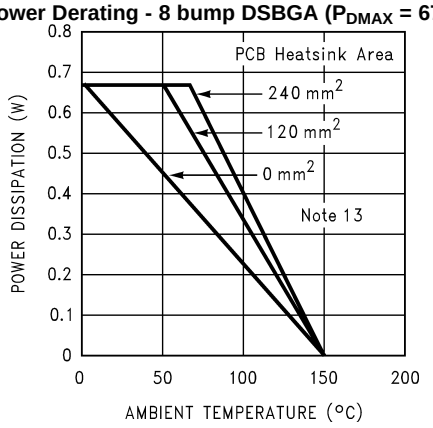
Power Derating Curves (P_{DMAX} = 670mW)



Note: (P_{DMAX} = 670mW for 5V, 8Ω)

Figure 40. Ambient Temperature in Degrees C

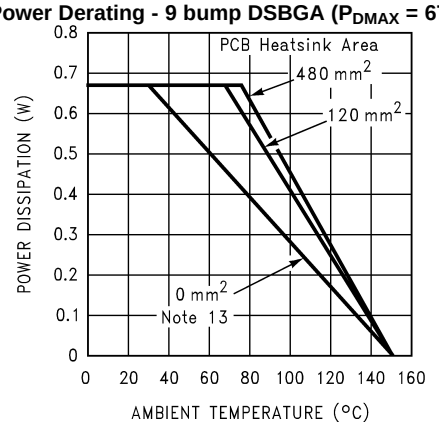
Power Derating - 8 bump DSBGA (P_{DMAX} = 670mW)



Note: (P_{DMAX} = 670mW for 5V, 8Ω)

Figure 41. Ambient Temperature in Degrees C

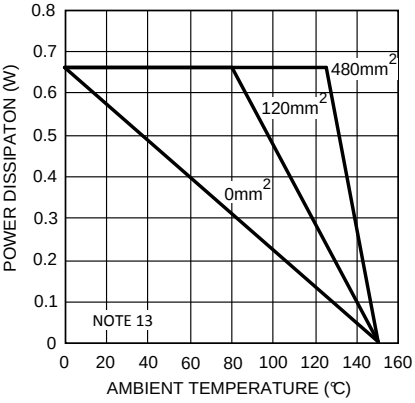
Power Derating - 9 bump DSBGA (P_{DMAX} = 670mW)



Note: (P_{DMAX} = 670mW for 5V, 8Ω)

Figure 42. Ambient Temperature in Degrees C

Power Derating - 10 Pin LD Pkg (P_{DMAX} = 670mW)



Note: (P_{DMAX} = 670mW for 5V, 8Ω)

Figure 43. Ambient Temperature in Degrees C

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Typical Performance Characteristics (continued)

Power Output vs Supply Voltage

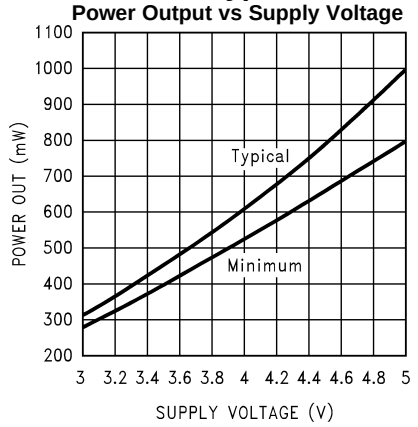


Figure 44.

Power Output vs Temperature

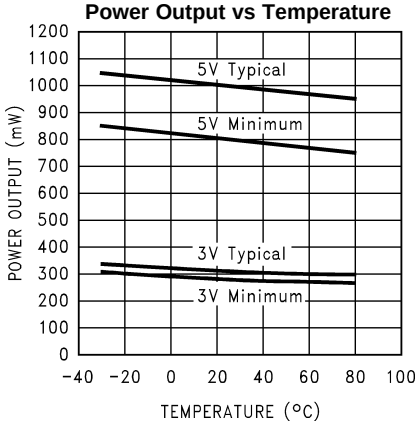


Figure 45.

Power Dissipation vs Output Power
V_{DD} = 5V, 1kHz, 8Ω, THD ≤ 1.0%

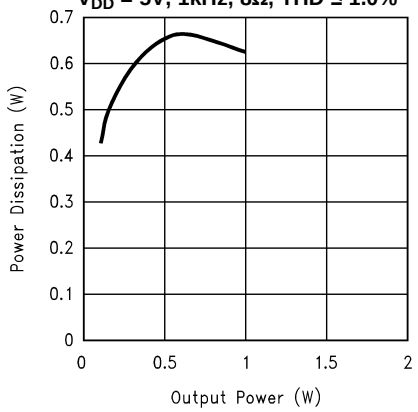


Figure 46.

Power Dissipation vs Output Power
V_{DD} = 3.3V, 1kHz, 8Ω, THD ≤ 1.0%

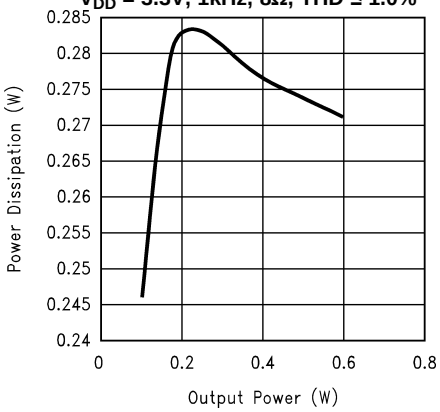


Figure 47.

Power Dissipation vs Output Power
V_{DD} = 2.6V, 1kHz

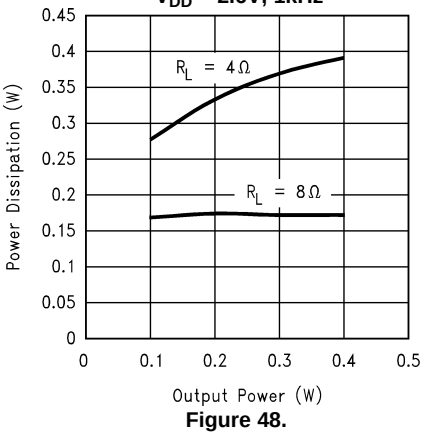


Figure 48.

Output Power
vs Load Resistance

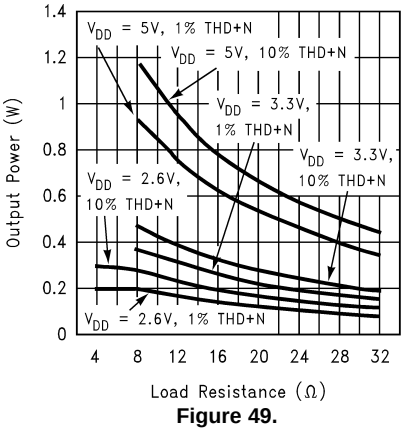


Figure 49.

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Typical Performance Characteristics (continued)

Supply Current vs Ambient Temperature

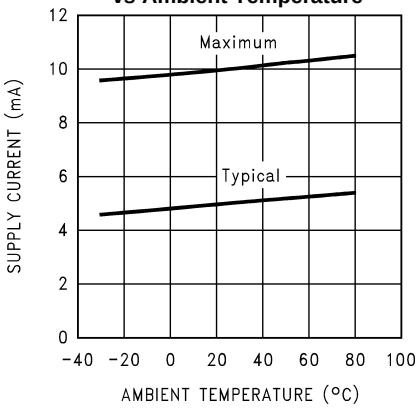


Figure 50.

Clipping (Dropout) Voltage vs Supply Voltage

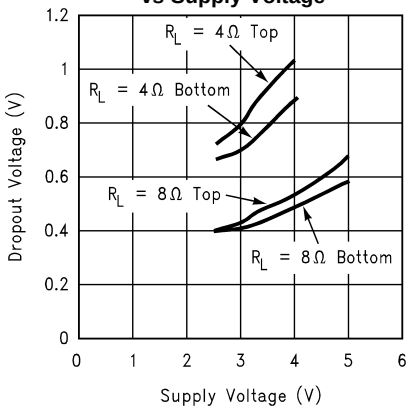


Figure 51.

Max Die Temp at P_{DMAX} (9 bump DSBGA)

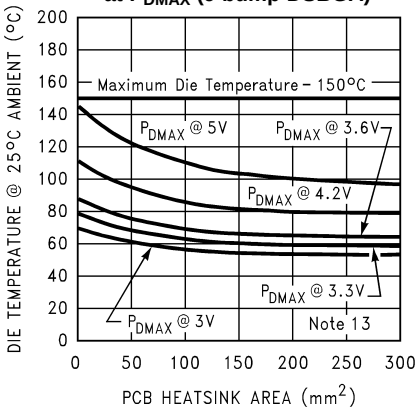


Figure 52.

Max Die Temp at P_{DMAX} (8 bump DSBGA)

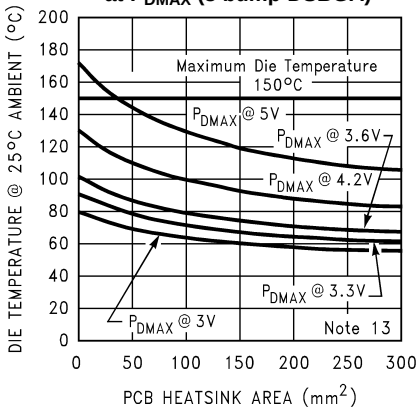


Figure 53.

Output Offset Voltage

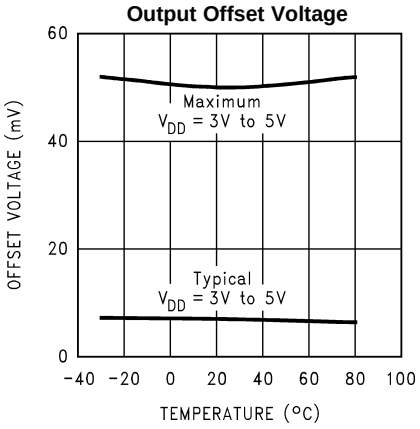


Figure 54.

Supply Current vs Shutdown Voltage

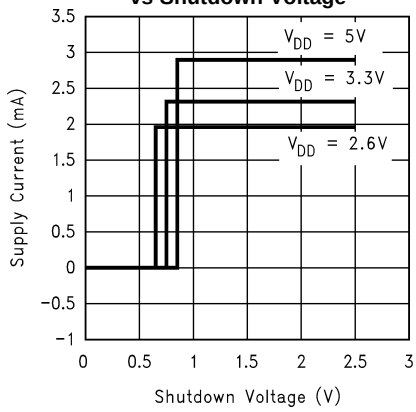


Figure 55.

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Typical Performance Characteristics (continued)

Shutdown Hysterisis Voltage
V_{DD} = 5V

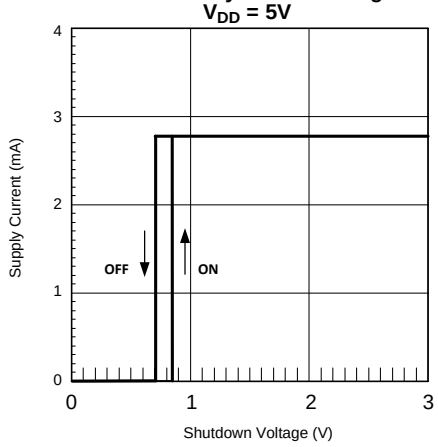


Figure 56.

Shutdown Hysterisis Voltage
V_{DD} = 3V

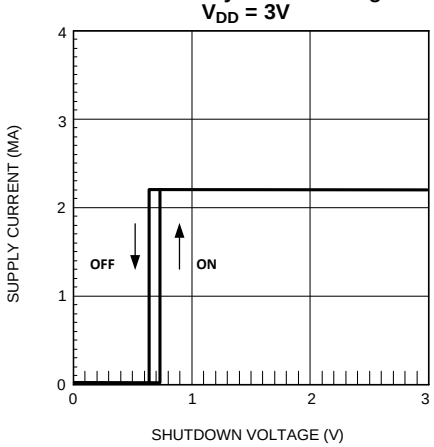


Figure 57.

Open Loop Frequency Response
V_{DD} = 5V, No Load

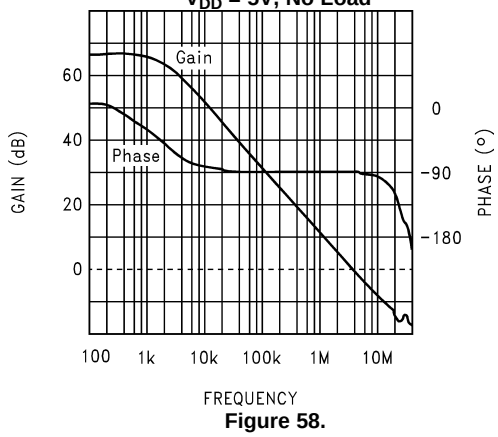


Figure 58.

Open Loop Frequency Response
V_{DD} = 3V, No Load

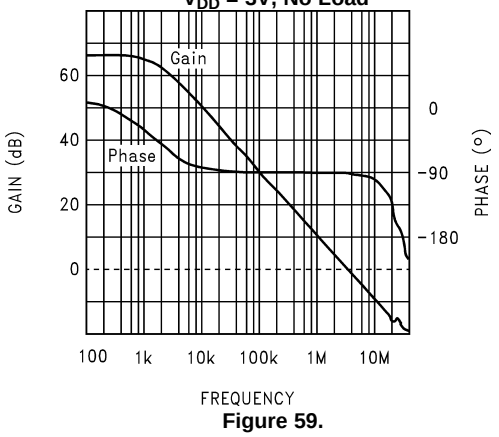


Figure 59.

Gain / Phase Response, A_V = 2
V_{DD} = 5V, 8Ω Load, C_{LOAD} = 500pF

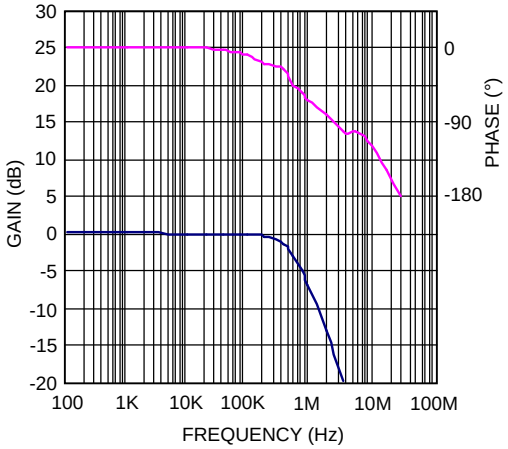


Figure 60.

Gain / Phase Response, A_V = 4
V_{DD} = 5V, 8Ω Load, C_{LOAD} = 500pF

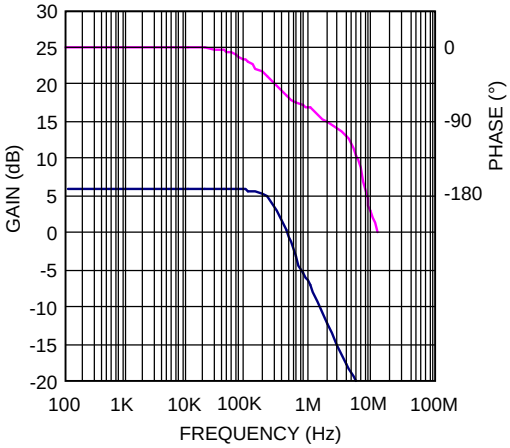


Figure 61.

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Typical Performance Characteristics (continued)

Phase Margin vs C_{LOAD}, A_V = 2
V_{DD} = 5V, 8Ω Load
Capacitance to gnd on each output

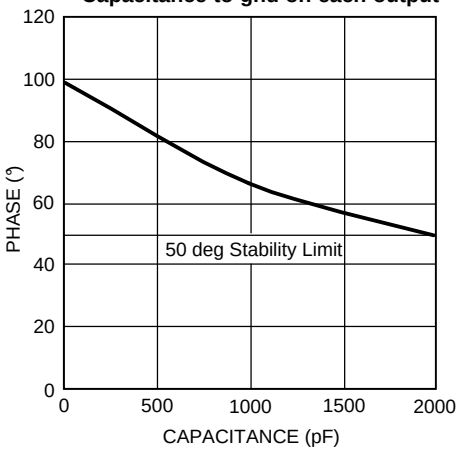


Figure 62.

Phase Margin vs C_{LOAD}, A_V = 4
V_{DD} = 5V, 8Ω Load
Capacitance to gnd on each output

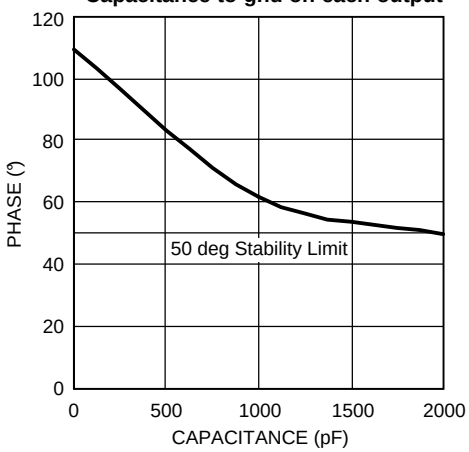


Figure 63.

Phase Margin and Limits
vs Application Variables, R_{IN} = 22KΩ

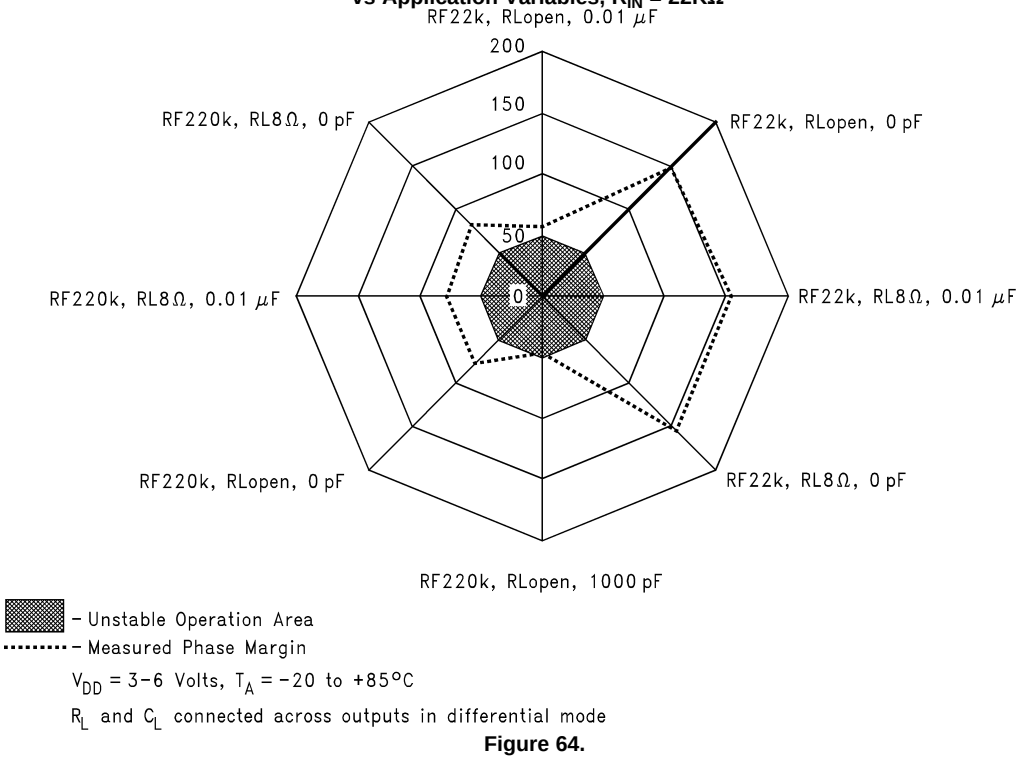


Figure 64.

Typical Performance Characteristics (continued)

Wake Up Time (T_{WU})

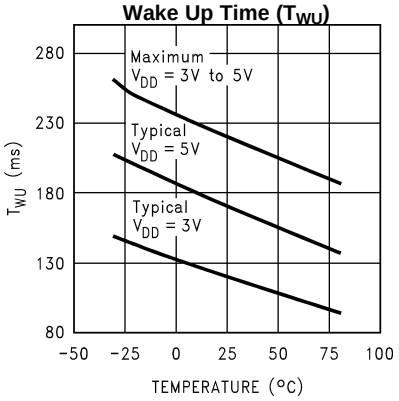


Figure 65.

Frequency Response vs Input Capacitor Size

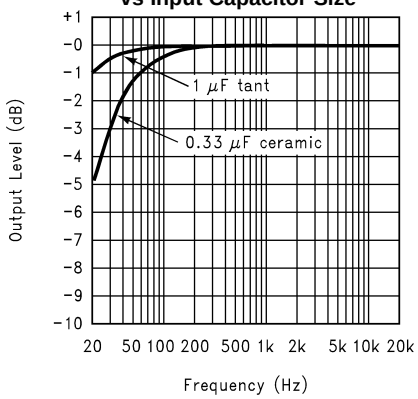


Figure 66.

Noise Floor

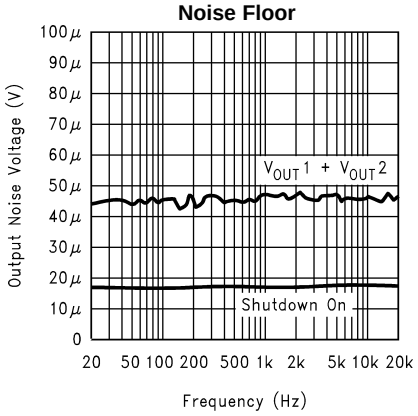


Figure 67.

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APPLICATION INFORMATION

BRIDGED CONFIGURATION EXPLANATION

As shown in Figure 7, the LM4890 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_{IN} while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 7 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_{IN})$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section.

A bridge configuration, such as the one used in the LM4890, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS FOR THE LM4890LD

The LM4890LD's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. The LM4890LD package should have its DAP soldered to the grounded copper pad (heatsink) under the LM4890LD (the NC pins, no connect, and ground pins should also be directly connected to this copper pad-heatsink area). The area of the copper pad (heatsink) can be determined from the LD Power Derating graph. If the multiple layer copper heatsink areas are used, then these inner layer or backside copper heatsink areas should be connected to each other with 4 (2 x 2) vias. The diameter for these vias should be between 0.013 inches and 0.02 inches with a 0.050inch pitch-spacing. Ensure efficient thermal conductivity by plating through and solder-filling the vias. Further detailed information concerning PCB layout, fabrication, and mounting an WSON package is available from TI's Package Engineering Group under application note AN1187.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4890 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the LM4890. Refer to the Application Information on the LM4890 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers and output loading.

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POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4890. The selection of a bypass capacitor, especially C_{BYPASS}, is dependent upon PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4890 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. By switching the shutdown pin to ground, the LM4890 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than $0.5V_{DC}$, the idle current may be greater than the typical value of 0.1µA. (Idle current is measured with the shutdown pin grounded).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and disables the amplifier. If the switch is open, then the external pull-up resistor will enable the LM4890. This scheme ensures that the shutdown pin will not float thus preventing unwanted state changes.

SHUTDOWN OUTPUT IMPEDANCE

For R_f = 20k ohms:

Z_{OUT1} (between Out1 and GND) = 10k||50k||R_f = 6kΩ

Z_{OUT2} (between Out2 and GND) = 10k||(40k+(10k||R_f)) = 8.3kΩ

Z_{OUT1-2} (between Out1 and Out2) = 40k||(10k+(10k||R_f)) = 11.7kΩ

The -3dB roll off for these measurements is 600kHz

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4890 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4890 is unity-gain stable which gives the designer maximum system flexibility. The LM4890 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, Audio Power Amplifier Design, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 7. The input coupling capacitor, C_{IN}, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

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In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_{IN}. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_{BYPASS}, is the most critical component to minimize turn-on pops since it determines how fast the LM4890 turns on. The slower the LM4890's outputs ramp to their quiescent DC voltage (nominally 1/2V_{DD}), the smaller the turn-on pop. Choosing C_{BYPASS} equal to 1.0µF along with a small value of C_{IN}, (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_{BYPASS} equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_{BYPASS} equal to 1.0µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 2 and add the output voltage. Using this method, the minimum supply voltage would be (V_{opeak} + (V_{ODTOP} + V_{ODBOT})), where V_{ODBOT} and V_{ODTOP} are extrapolated from the Dropout Voltage vs Supply Voltage curve in theTypical Performance Characteristics.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (2)$$

5V is a standard voltage which in most applications is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4890 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 3.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (3)$$

$$R_f/R_{IN} = A_{VD}/2 \quad (4)$$

From Equation 3, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance is 20 kΩ, and with an A_{VD} gain of 3, a ratio of 1.5:1 of R_f to R_{IN} results in an allocation of R_{IN} = 20 kΩ and R_f = 30 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the External Components Description section, R_{IN} in conjunction with C_{IN} create a highpass filter.

$C_{IN} \geq 1/(2\pi * 20\ k\Omega * 20Hz) = 0.397\mu F$; use 0.39µF

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The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100kHz, the resulting GBWP = 300kHz which is much smaller than the LM4890 GBWP of 2.5MHz. This calculation shows that if a designer has a need to design an amplifier with a higher differential gain, the LM4890 can still be used without running into bandwidth limitations.

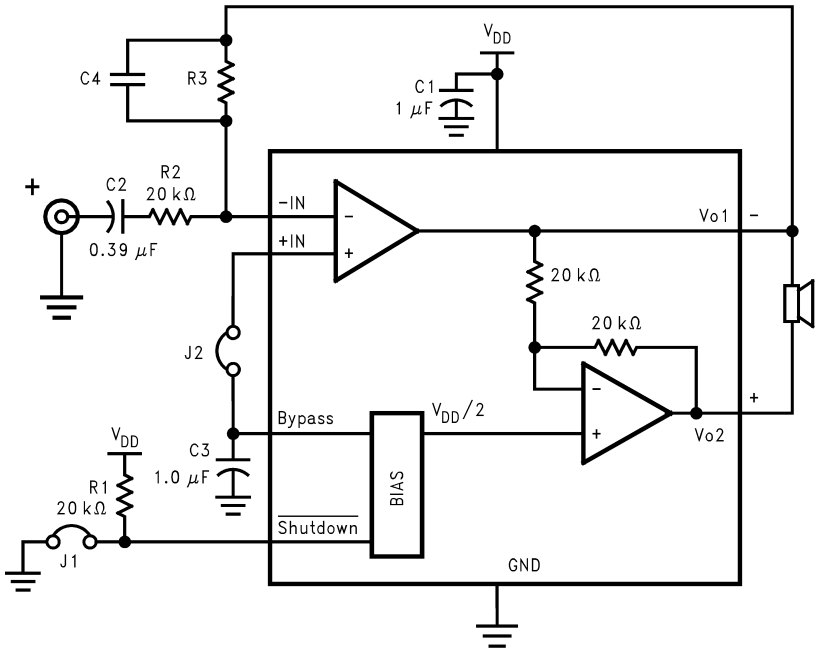


Figure 68. HIGHER GAIN AUDIO AMPLIFIER

The LM4890 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in Figure 68 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320 kHz.

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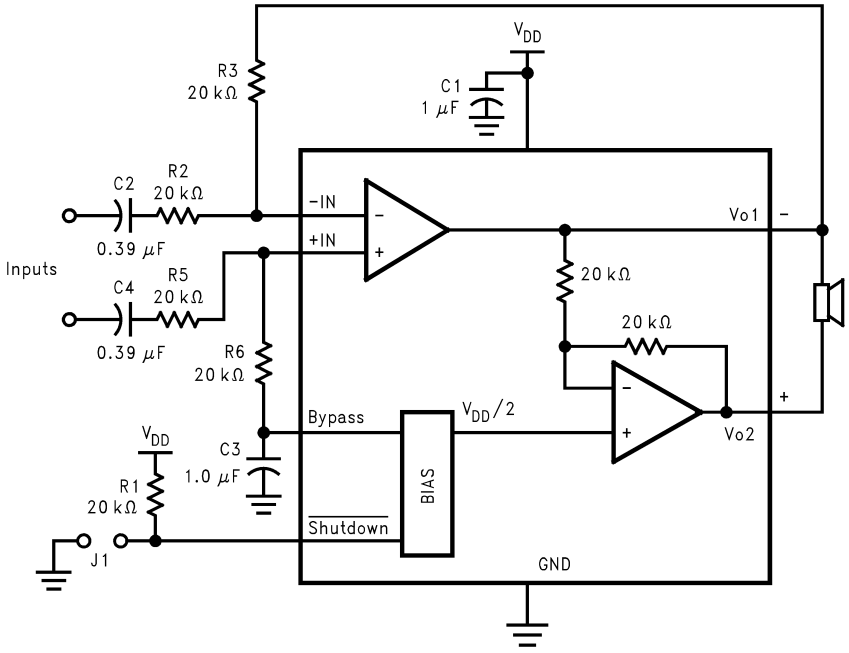


Figure 69. DIFFERENTIAL AMPLIFIER CONFIGURATION FOR LM4890

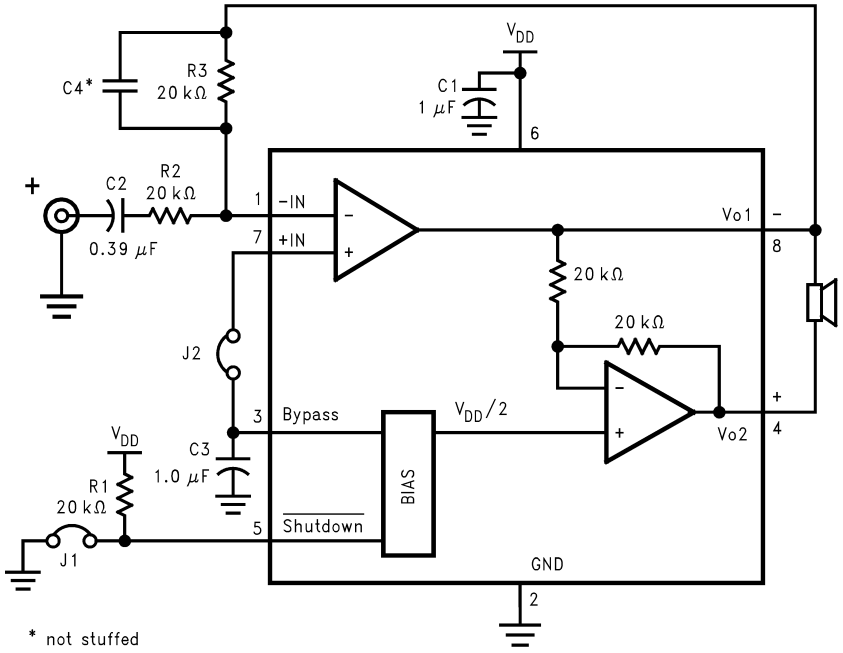
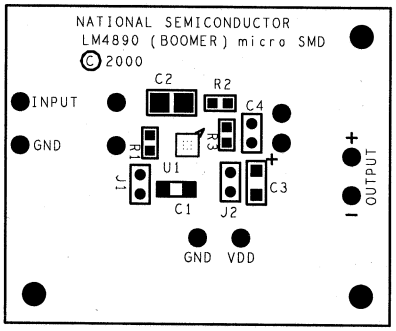


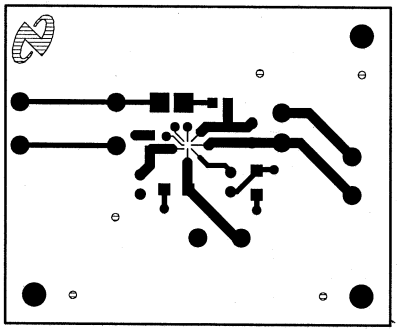
Figure 70. REFERENCE DESIGN BOARD and LAYOUT - DSBGA

LM4890 DSBGA BOARD ARTWORK

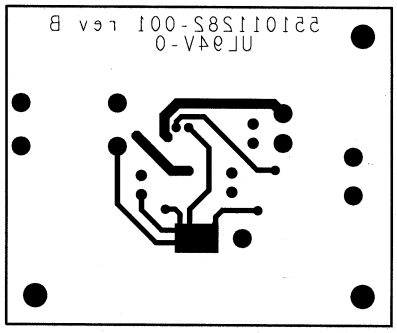
Silk Screen



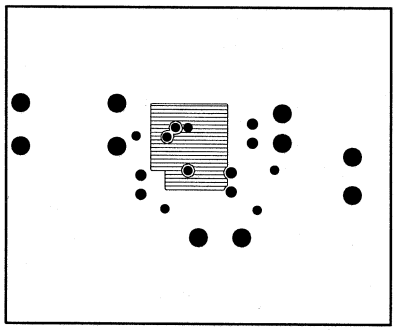
Top Layer



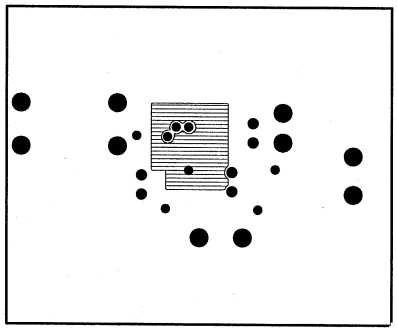
Bottom Layer



Inner Layer V_{DD}



Inner Layer Ground



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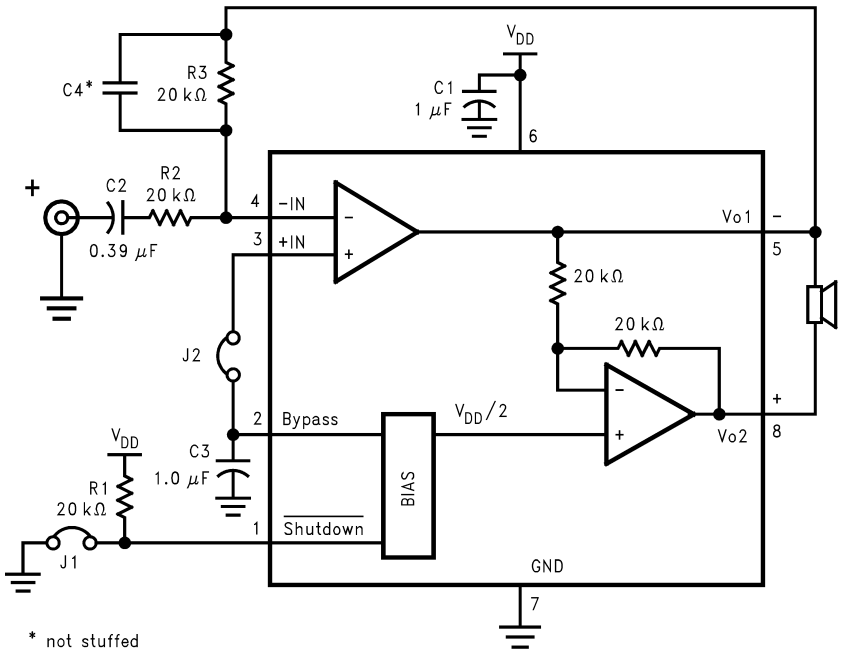


Figure 71. REFERENCE DESIGN BOARD and PCB LAYOUT GUIDELINES - VSSOP and SOIC Boards

LM4890 SOIC DEMO BOARD ARTWORK

Figure 72. Silk Screen

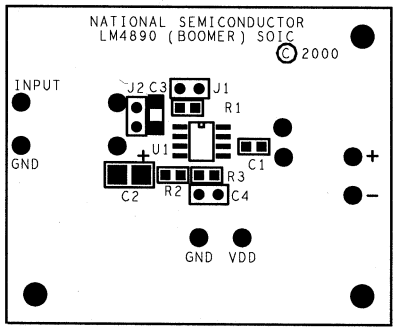


Figure 73. Top Layer

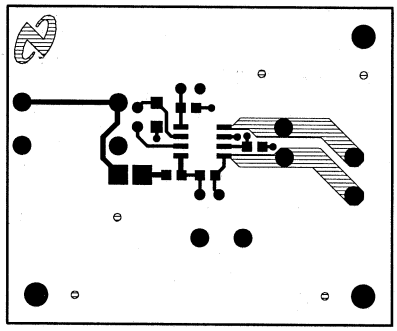
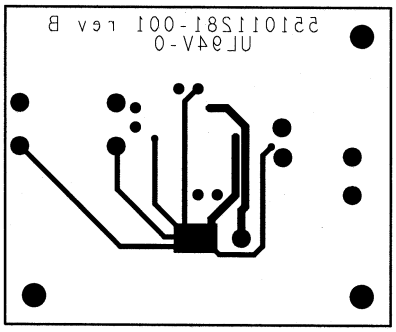


Figure 74. Bottom Layer



LM4890 VSSOP DEMO BOARD ARTWORK

Figure 75. Silk Screen

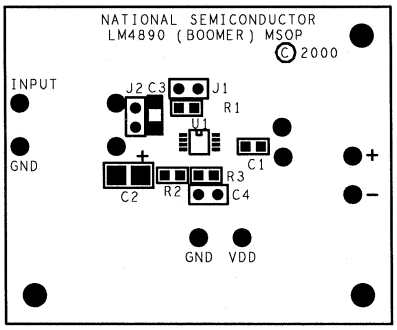


Figure 76. Top Layer

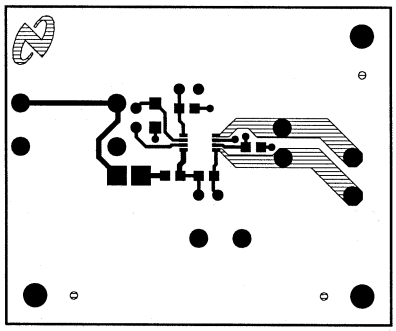


Figure 77. Bottom Layer

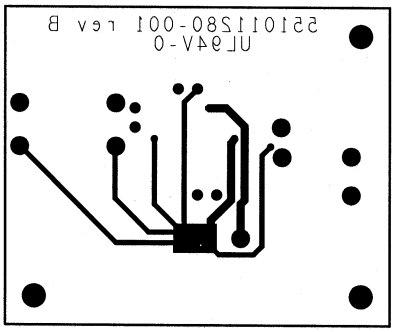


Table 1. Mono LM4890 Reference Design Boards

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Table 1. Mono LM4890 Reference Design Boards
Bill of Material for all 3 Demo Boards (continued)

Bill of Material for all 3 Demo Boards

Item	Part Number	Part Description	Qty	Ref Designator
1	551011208-001	LM4890 Mono Reference Design Board	1	
10	482911183-001	LM4890 Audio AMP	1	U1
20	151911207-001	Tant Cap 1uF 16V 10	1	C1
21	151911207-002	Cer Cap 0.39uF 50V Z5U 20% 1210	1	C2
25	152911207-001	Tant Cap 1uF 16V 10	1	C3
30	472911207-001	Res 20K Ohm 1/10W 5	3	R1, R2, R3
35	210007039-002	Jumper Header Vertical Mount 2X1 0.100	2	J1, J2

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATIONS

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

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REVISION HISTORY

Changes from Revision K (May 2013) to Revision L	Page
• Changed layout of National Data Sheet to TI format	27

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4890M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 90M
LM4890M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 90M
LM4890MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G90
LM4890MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G90
LM4890MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G90
LM4890MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G90
LM4890MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 90M
LM4890MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 90M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

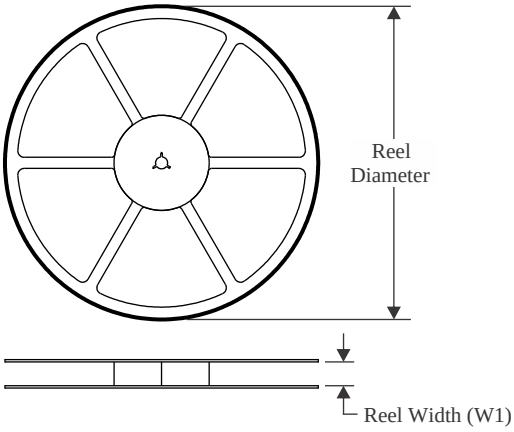
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

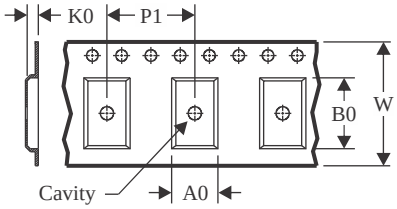
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

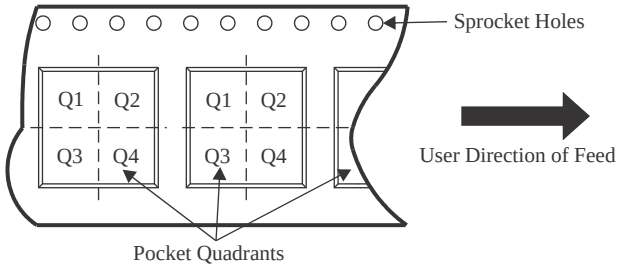


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

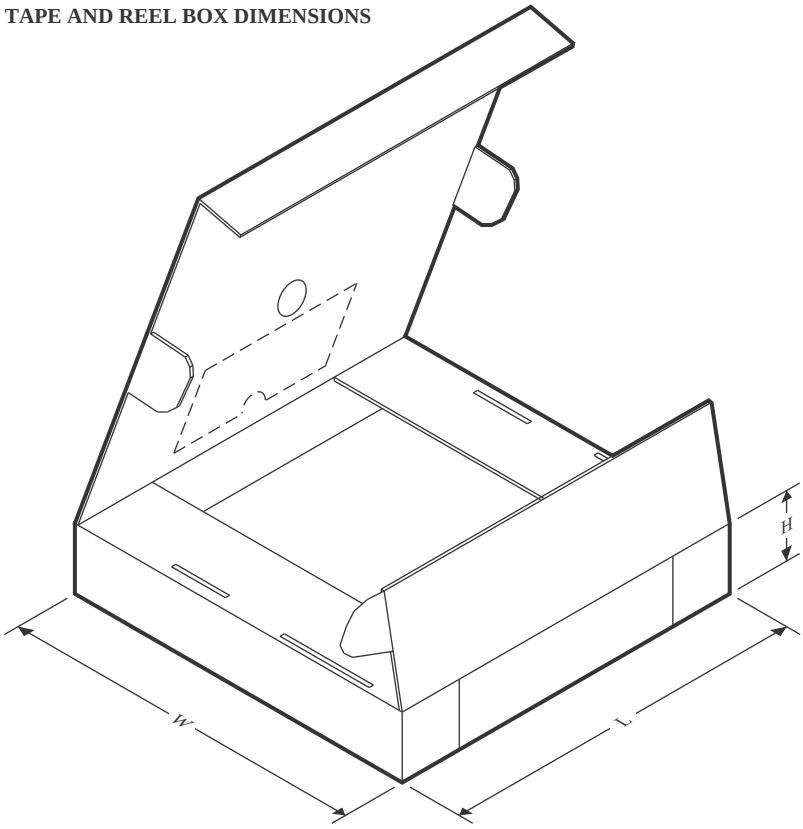
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4890MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4890MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4890MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

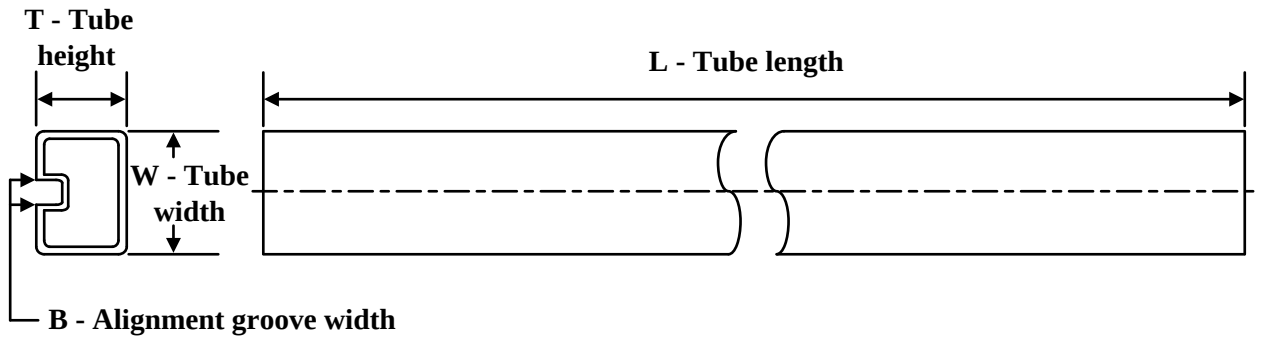
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4890MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4890MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM4890MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

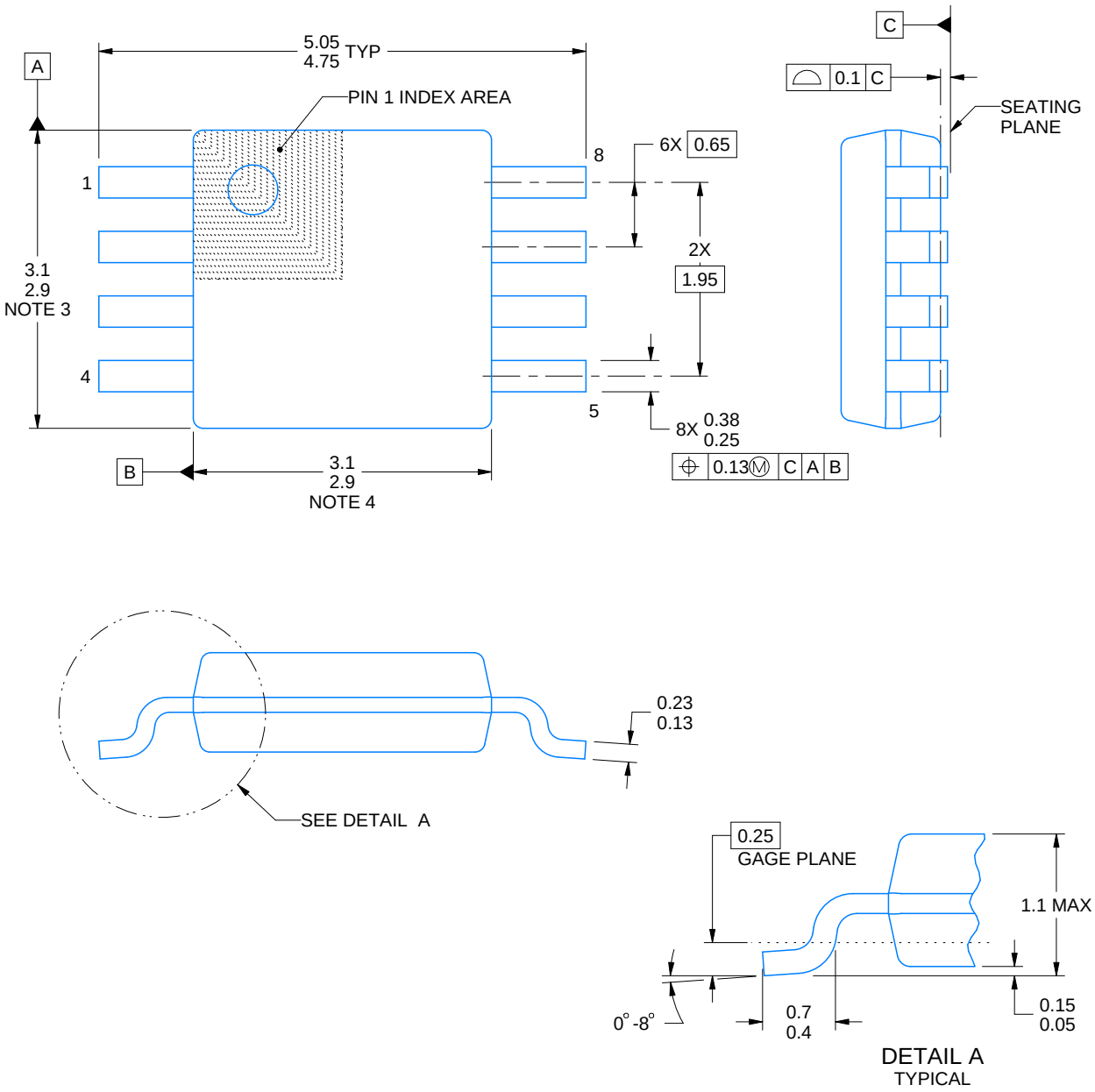
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4890M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM4890M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

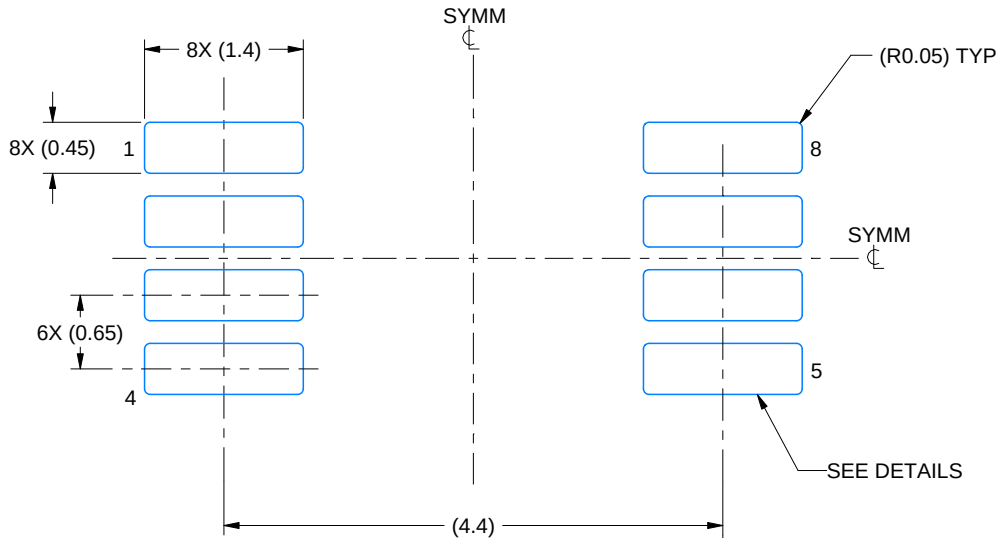
SMALL OUTLINE PACKAGE



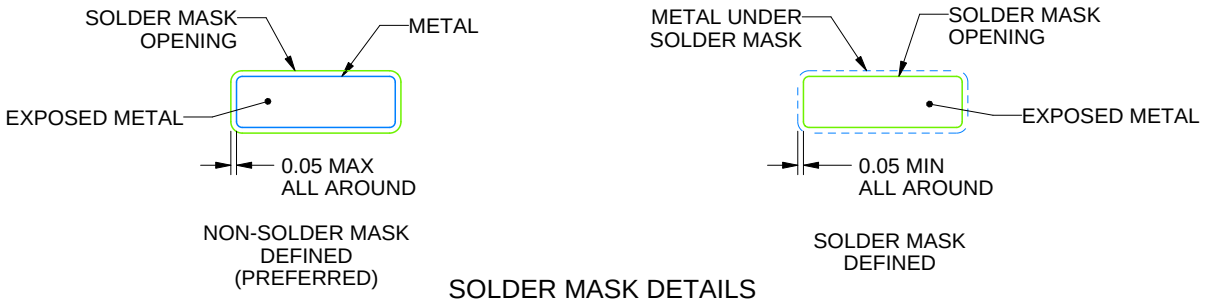
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

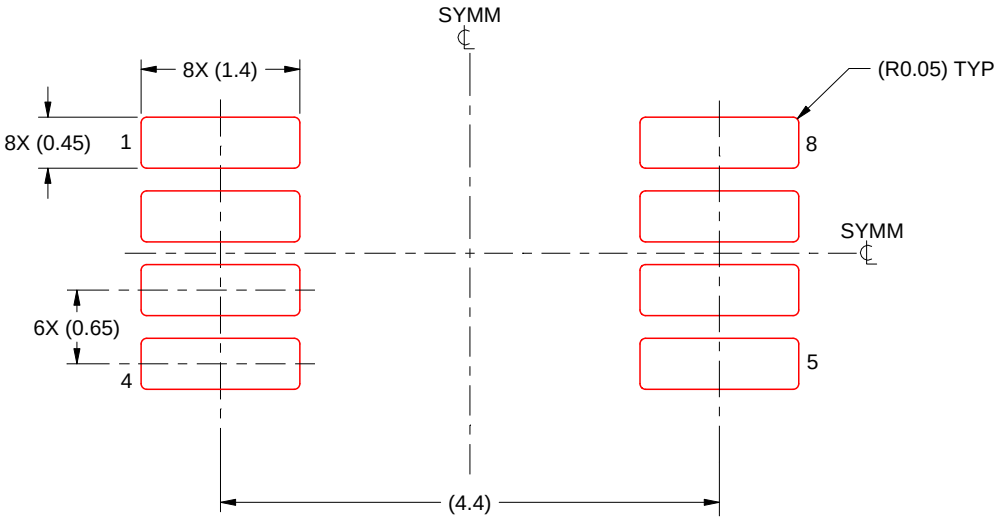


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

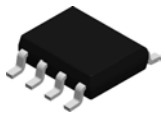


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

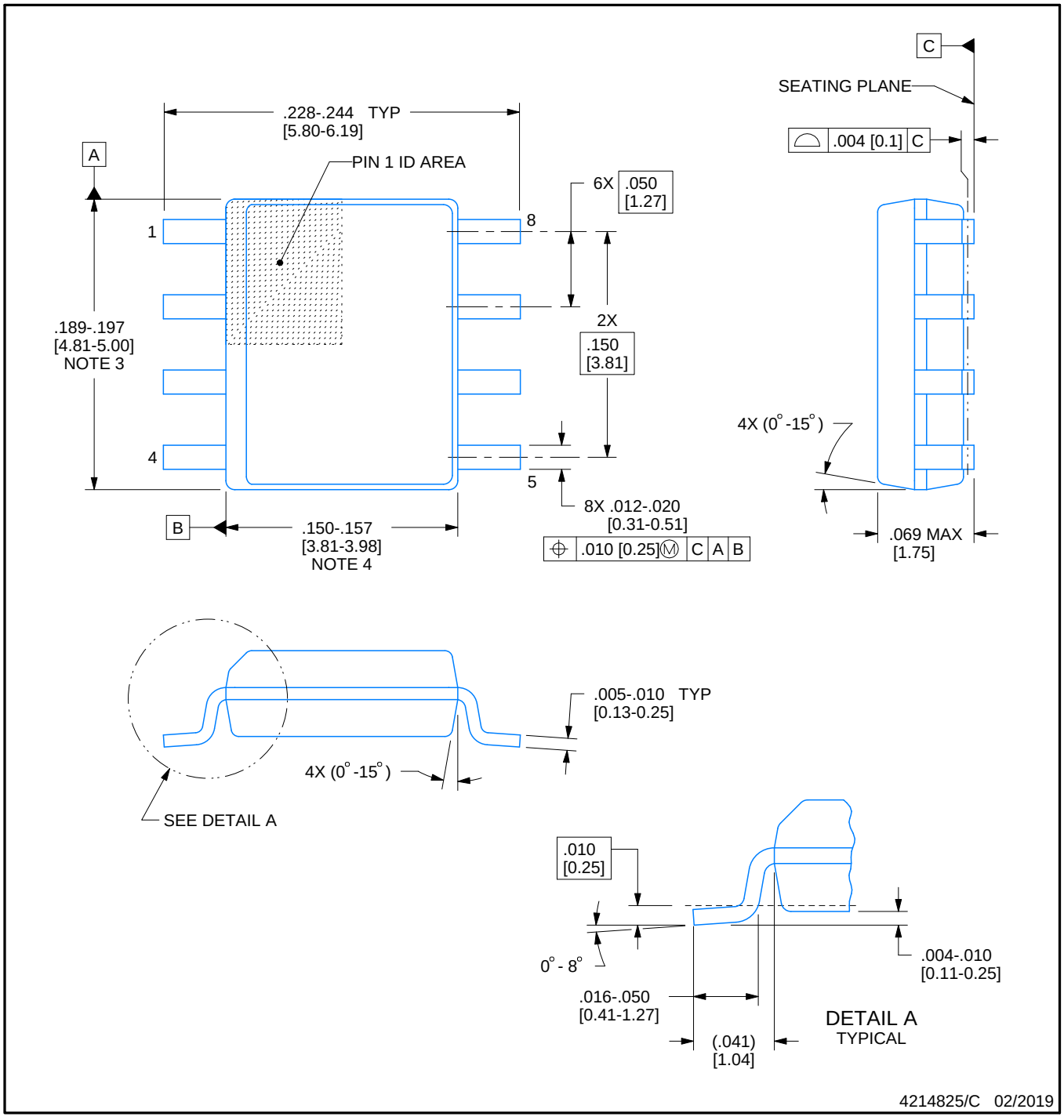


PACKAGE OUTLINE

D0008A

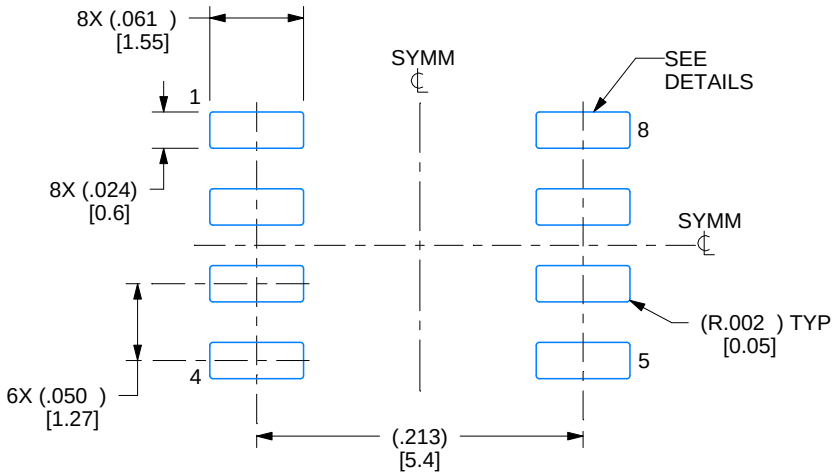
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

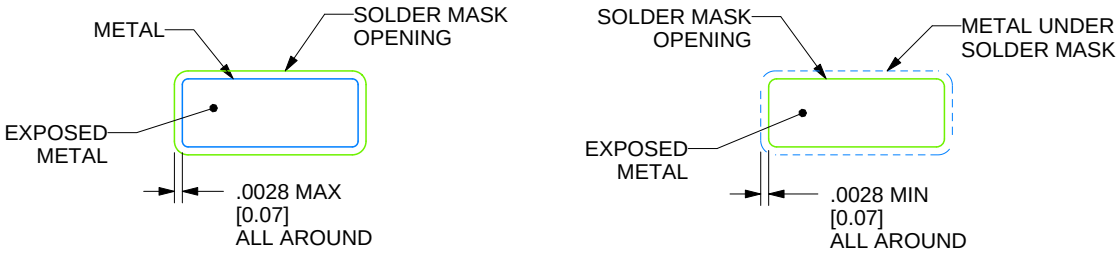


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

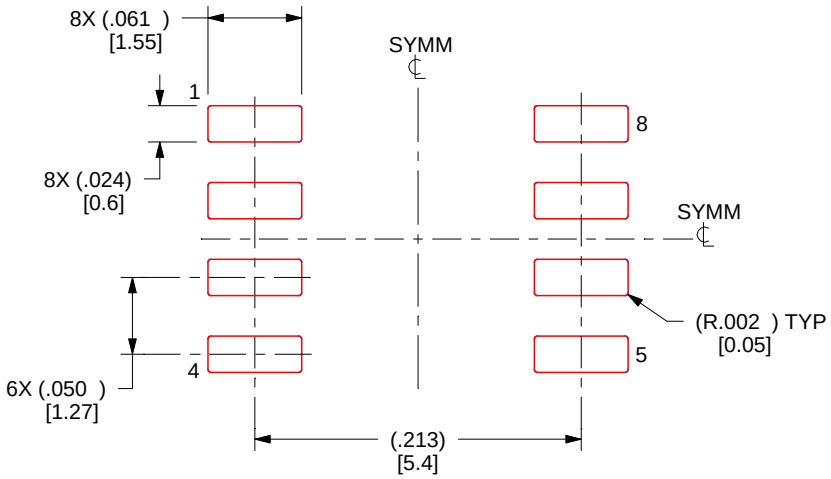
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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