LM8272 Dual RRIO, High Output Current and Unlimited Cap Load Op Amp in Miniature Package

1 Features

- GBWP: 24MHz
- Wide supply voltage range: 2.7V to 24V
- Slew rate: 35V/µs
- Supply current/channel: 1.35mA
- Cap load tolerance Unlimited
- Output short circuit current: ±125mA
- Output current (1V from rails): ±65mA
- Input common mode voltage: 0.3V beyond rails
- Input voltage noise: 12nV/ $\sqrt{\text{Hz}}$
- Input current noise: 1pA/ $\sqrt{\text{Hz}}$
- THD+N: < 0.00022%

2 Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side/low side sensing
- Headphone amplifier

3 Description

The LM8272 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, and unlimited capacitive load drive capability. LM8272 is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being designed for other low power and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 90dB of Common Mode Rejection allows high side and low side sensing among many applications without concerns for exceeding the range and with no compromise in accuracy. An exceptionally wide operating supply voltage range of 2.7V to 24V removes any concerns over functionality under extreme conditions and offers flexibility of use in multitude of applications. In addition, most device parameters are insensitive to power supply variations. This design enhancement is yet another step in simplifying the usage.

The LM8272 is offered in the 8-pin VSSOP package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM8272	DGK (VSSOP, 8)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....5
5.5 Electrical Characteristics....6
5.6 Typical Performance Characteristics....7
5.7 Old Die vs New Die....13
6 Application and Implementation....14
6.1 Driving Capacitive Loads:....14
6.2 Output Short Circuit Current and Dissipation Issues:....14
6.3 Other Application Hints:....15
6.4 LM8272 Advantages:....15
6.5 Electrical Overstress....16
7 Device and Documentation Support....18
7.1 Support Resources....18
7.2 Trademarks....18
7.3 Electrostatic Discharge Caution....18
7.4 Glossary....18
8 Revision History....18
9 Mechanical, Packaging, and Orderable Information....19

Copyright © 2026 Texas Instruments Incorporated

4 Pin Configuration and Functions

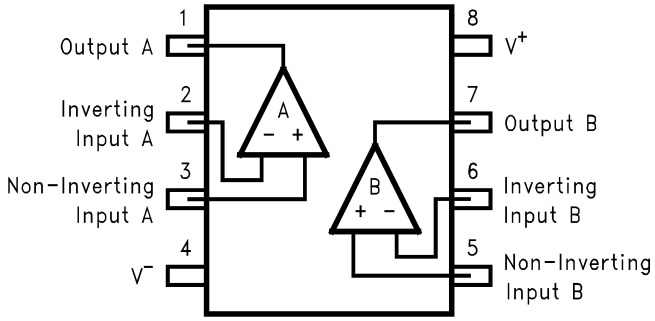


Figure 4-1. 8-Pin VSSOP Top View

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	OUT A	O	Output A
2	-IN A	I	Inverting Input A
3	+IN A	I	Non-Inverting Input A
4	V-	I	Negative Supply
5	+IN B	I	Non-Inverting Input B
6	-IN B	I	Inverting Input B
7	OUT B	O	Output B
8	V+	I	Positive Supply

Copyright © 2026 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN} Differential(5)			±10	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(5)		±10	V
	Current(3)		±10	mA
Output Short Circuit Duration			See(3)(4)	
Supply Voltage (V^+ - V^-)			27	V
Voltage at Input/Output pins			V^+ +0.3, V^- −0.3	V
Junction Temperature(2)			+150	°C
Storage temperature range, T_{stg}		−65	+150	°C
Soldering Information:	Infrared or Convection (20s)		235	°C
	Wave Soldering (10s)		260	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) The maximum power dissipation is a function of TJ(max), $R_{\theta JA}$, and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(max) - TA)/ $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) Output short circuit duration is infinite for VS ≤ 6V at room temperature and below. For VS > 6V, allowable short circuit duration is 1.5ms.
(5) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5V, limit the input current to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	
		Machine Model (MM)(3)	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) Human body model, 1.5kΩ in series with 100pF. Machine Model, 0Ω is series with 200pF.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V^+ – V^-)	2.7		24	V
Operating Temperature Range(1)	−40		+85	°C

(1) The maximum power dissipation is a function of TJ(max), $R_{\theta JA}$, and TA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(max) - TA)/ $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

Copyright © 2026 Texas Instruments Incorporated

5.4 Thermal Information

THERMAL METRIC[1]		DGK	UNIT
		8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	169.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

Copyright © 2026 Texas Instruments Incorporated

5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 24V (±1.35V to ±12V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM}= V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = V–				±5	mV
			−40°C ≤ T_A ≤ +125°C		±0.7	±7	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = V–	−40°C ≤ T_A ≤ +125°C		±2		µV/°C
I_B	Input Bias Current		−40°C ≤ T_A ≤ +125°C			±2.7	µA
		Max room temperature				±2	
I_{OS}	Input Offset Current				20	250	nA
V_{CM}	Input Common-Mode Voltage Range			(V–) – 0.1	(V+) + 0.1		V
CMRR	Common Mode Rejection Ratio	V– < V_{CM} < (V+) – 2V	−40°C ≤ T_A ≤ +125°C	80	100		dB
PSRR	Power Supply Rejection Ratio	V_{CM}= V–, V_S = 5V to 24V	−40°C ≤ T_A ≤ +125°C	74	109		dB
A_{OL}	Open Loop Voltage Gain	V_S = 24V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V	−40°C ≤ T_A ≤ +125°C	60	85		dB
V_O	Voltage Output Swing from Rail	Positive and negative rail headroom	V_S = 24V, R_L = 10kΩ		58	68	mV
			V_S = 24V, R_L = 2kΩ		117	137	
I_{SC}	Output Short Circuit Current	V_S = 24V			±125		mA
		V_S = 5V(3)			±85		
		V_S = 2.7V(3)			±60		
I_S	Supply Current (Both channels)	V_{CM} = V−, I_O = 0A			2.7	3.9	mA
			−40°C ≤ T_A ≤ +125°C			4.5	
SR	Slew Rate	V_S = 24V, V_{STEP} = 10V, G = +1, C_L = 20pF			35		V/µs
GBW	Gain-Bandwidth Product				11		MHz
Phi_m	Phase Margin	G = +1, R_L = 10kΩ, C_L = 20pF			50		°
e_n	Input Voltage Noise Density	f = 1kHz			50		nV/ $\sqrt{Hz}$
i_n	Input Current Noise Density	f = 1kHz			1		pA/ $\sqrt{Hz}$
t_s	Settling Time	To 0.1%, V_S = 24V, V_{STEP} = 10V, G = +1, C_L = 50pF			430		ns
THD+N	Total Harmonic Distortion +Noise	V_S = 24V, V_O = $3V_{RMS}$, G = 1, f = 1kHz, R_L = 10kΩ			113		dB
f_{max}	Full Power Bandwidth	Z_L = (20pF || 10kΩ) to $V^+/2$			700		kHz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are verifies by testing or statistical analysis.
(3) Specified by characterization only.

Copyright © 2026 Texas Instruments Incorporated

5.6 Typical Performance Characteristics

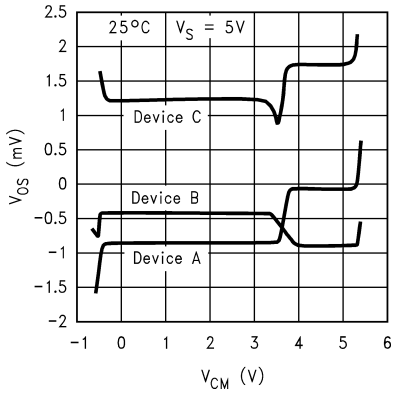


Figure 5-1. V_{OS} vs V_{CM} for Three Representative Units (Old Die)

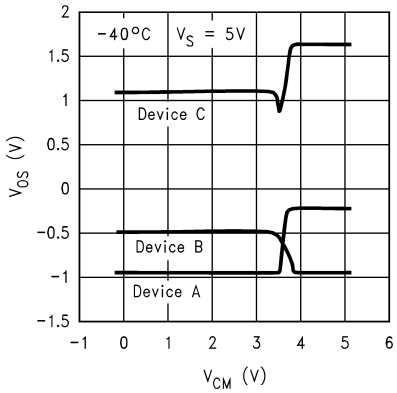


Figure 5-2. V_{OS} vs V_{CM} for Three Representative Units (Old Die)

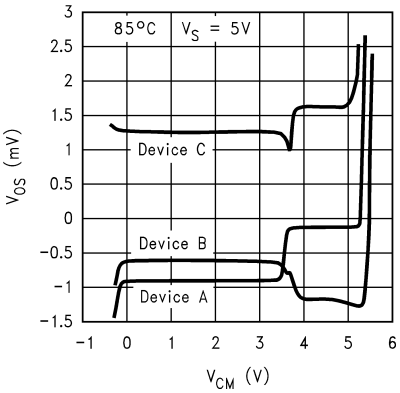


Figure 5-3. V_{OS} vs V_{CM} for Three Representative Units (Old Die)

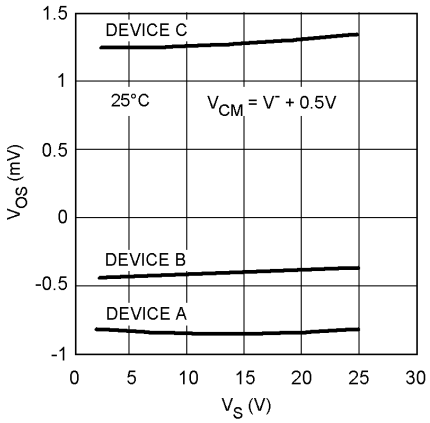


Figure 5-4. V_{OS} vs V_S for Three Representative Units (Old Die)

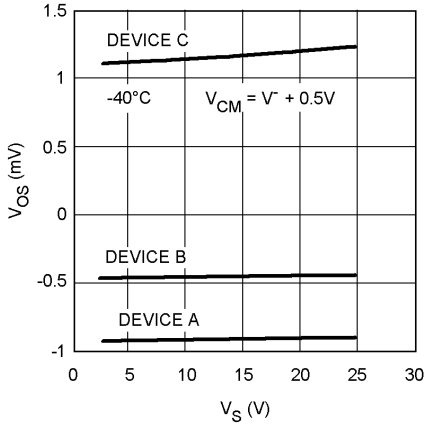


Figure 5-5. V_{OS} vs V_S for Three Representative Units (Old Die)

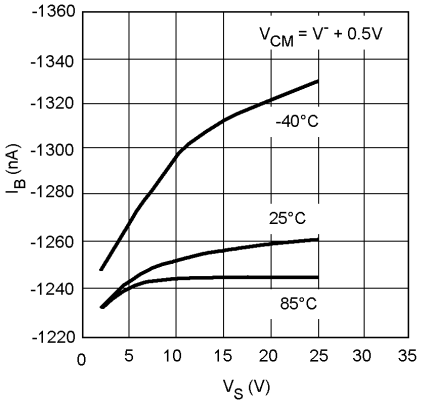


Figure 5-6. I_B vs V_S (Old Die)

Copyright © 2026 Texas Instruments Incorporated

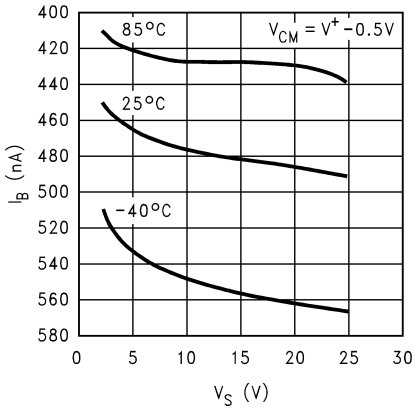


Figure 5-7. I_B vs V_S (Old Die)

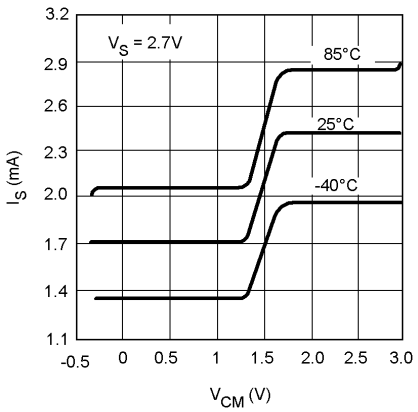


Figure 5-8. I_S vs V_{CM} (Old Die)

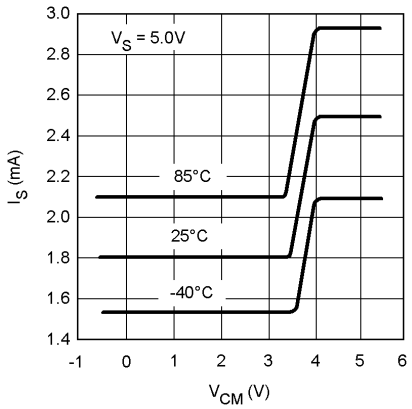


Figure 5-9. I_S vs V_{CM} (Old Die)

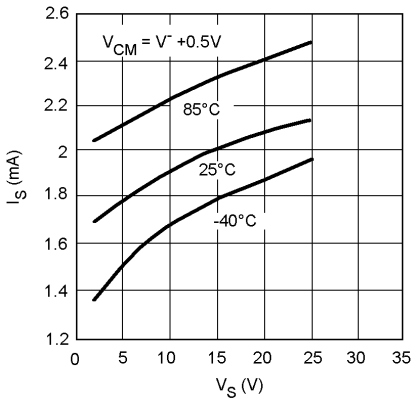


Figure 5-10. I_S vs V_S (Old Die)

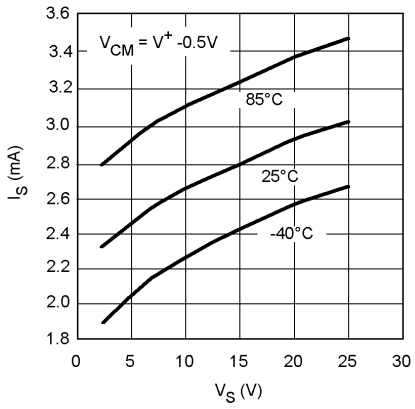


Figure 5-11. I_S vs V_S (Old Die)

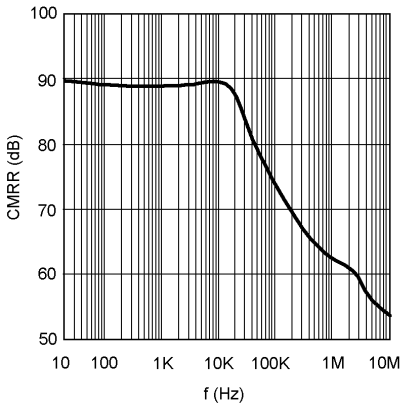


Figure 5-12. CMRR vs Frequency (Old Die)

Copyright © 2026 Texas Instruments Incorporated

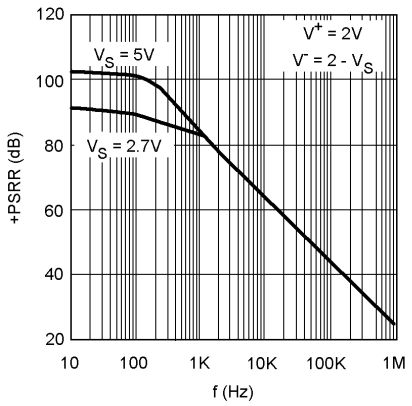


Figure 5-13. +PSRR vs Frequency (Old Die)

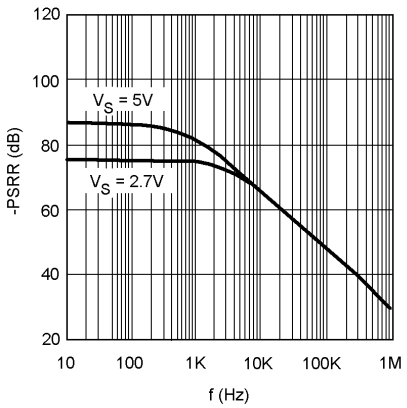


Figure 5-14. −PSRR vs Frequency (Old Die)

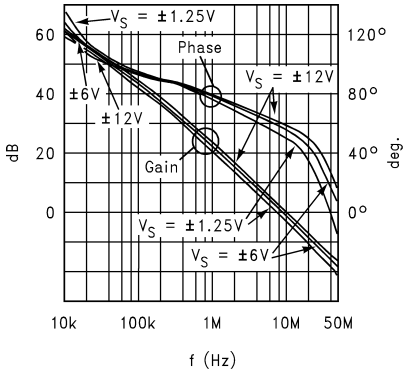


Figure 5-15. Open Loop Gain/Phase for Various Supplies (Old Die)

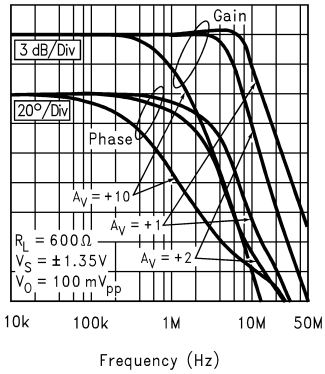


Figure 5-16. Closed Loop Frequency Response for Various Gains (Old Die)

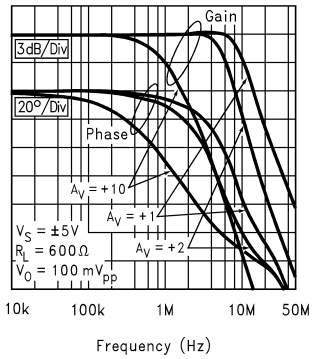


Figure 5-17. Closed Loop Frequency Response for Various Gains (Old Die)

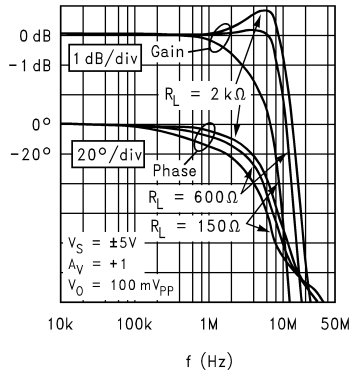


Figure 5-18. Closed Loop Frequency Response for Various R_L (Old Die)

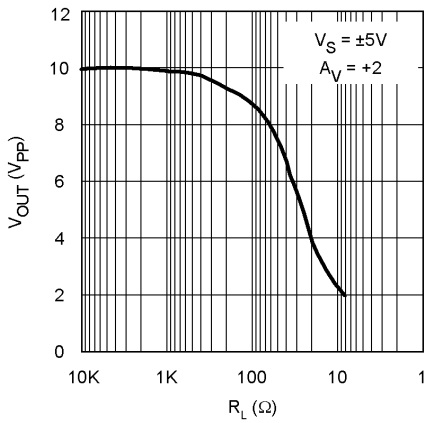


Figure 5-19. Maximum Output Swing vs Load (1% Distortion) (Old Die)

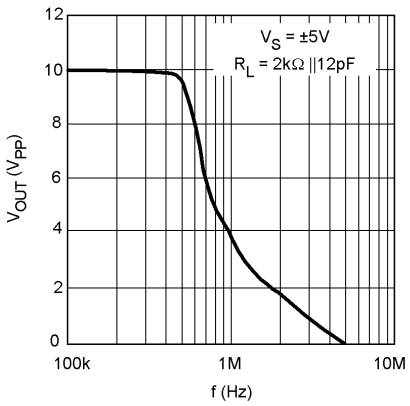


Figure 5-20. Maximum Output Swing vs Frequency (1% Distortion) (Old Die)

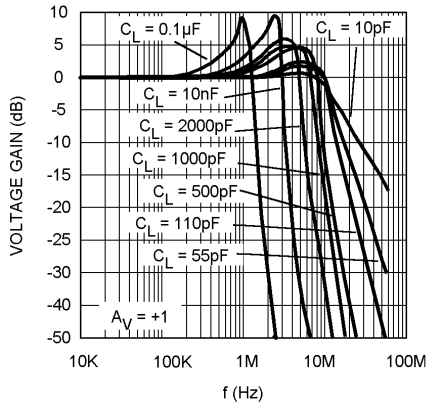


Figure 5-21. Closed Loop Small Signal Frequency Response for Various C_L (Old Die)

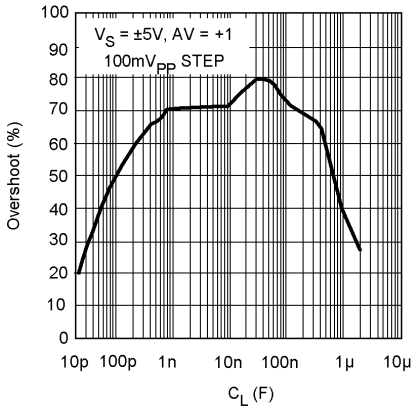


Figure 5-22. Overshoot vs Cap Load (Old Die)

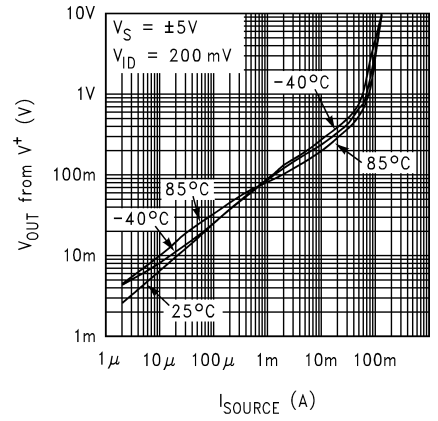


Figure 5-23. V_{OUT} from V^+ vs I_{SOURCE} (Old Die)

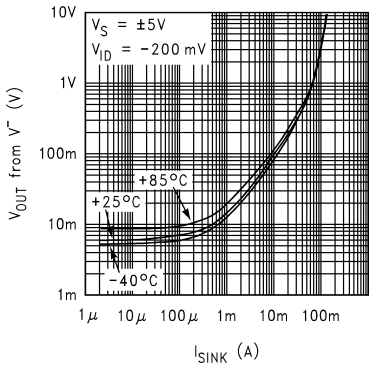


Figure 5-24. V_{OUT} from V^- vs I_{SINK} (Old Die)

Copyright © 2026 Texas Instruments Incorporated

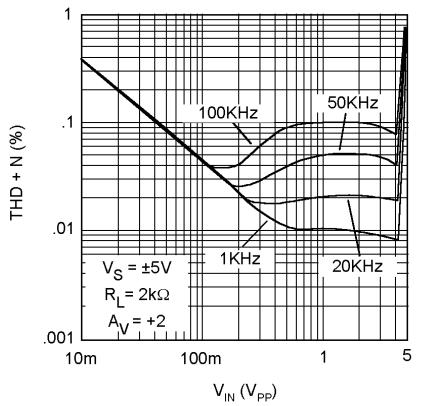


Figure 5-25. THD+N vs Input Amplitude for Various Frequency (Old Die)

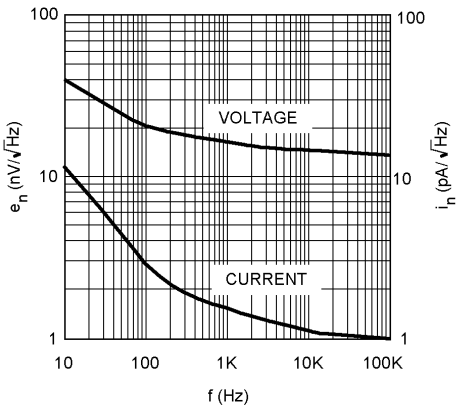


Figure 5-26. Input Referred Noise Density (Old Die)

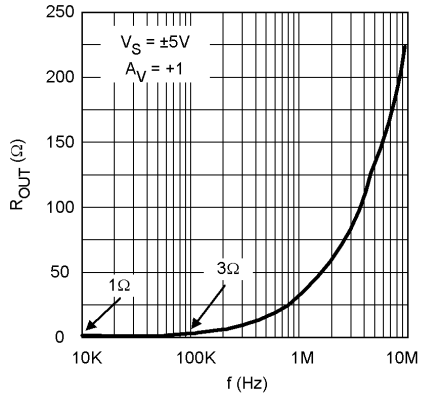
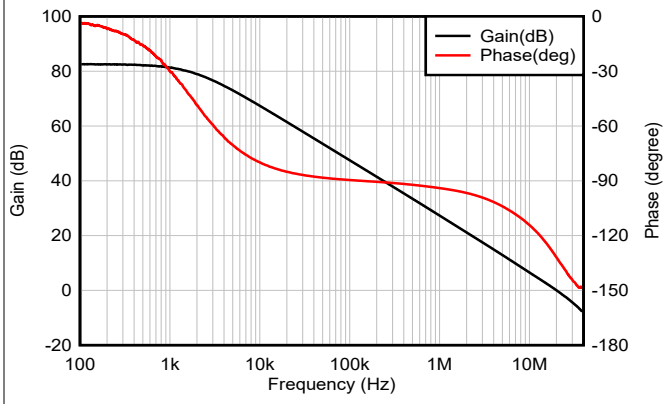


Figure 5-27. Closed Loop Output Impedance vs Frequency (Old Die)



C_L = 20 pF

Figure 5-28. Open-Loop Gain and Phase vs Frequency, New Die

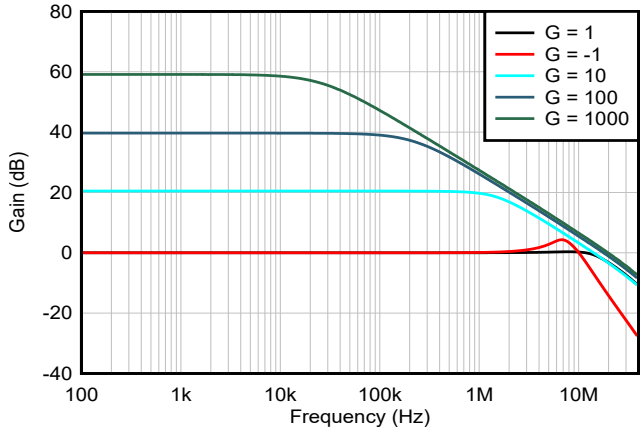


Figure 5-29. Closed-Loop Gain vs Frequency (New Die)

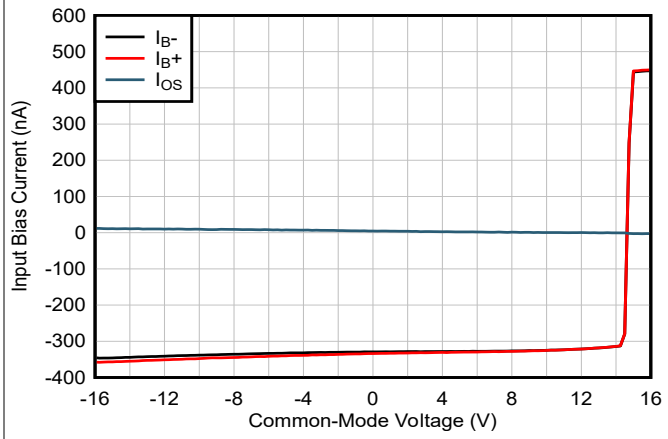


Figure 5-30. Input Bias Current and Offset Current vs Common-Mode Voltage (New Die)

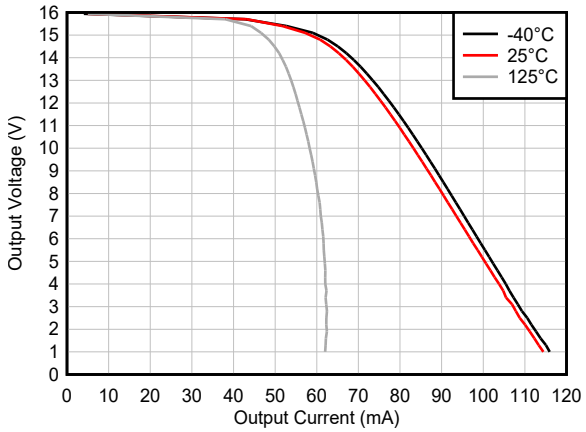


Figure 5-31. Output Voltage Swing vs Output Current (Sourcing) (New Die)

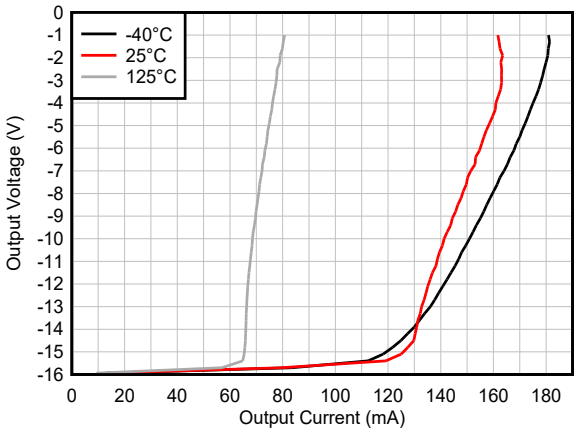


Figure 5-32. Output Voltage Swing vs Output Current (Sinking) (New Die)

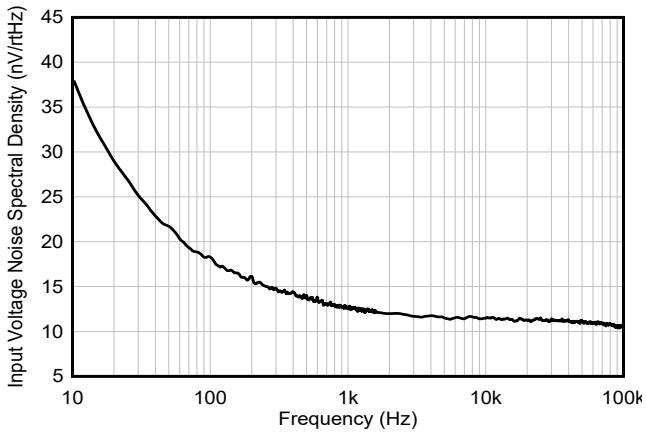


Figure 5-33. Input Voltage Noise Spectral Density vs Frequency (New Die)

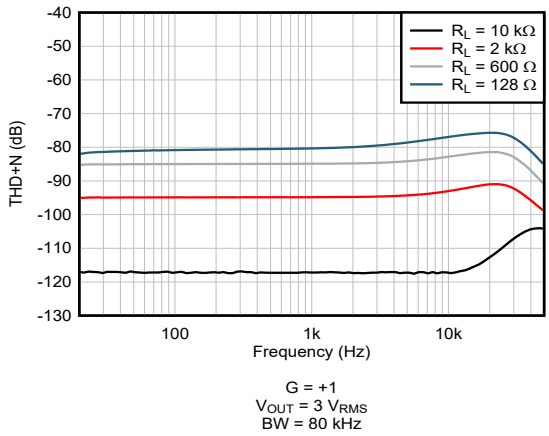


Figure 5-34. THD+N Ratio vs Frequency (New Die)

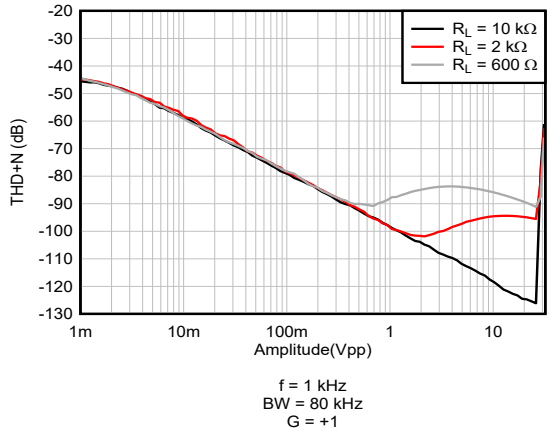


Figure 5-35. THD+N vs Output Amplitude (New Die)

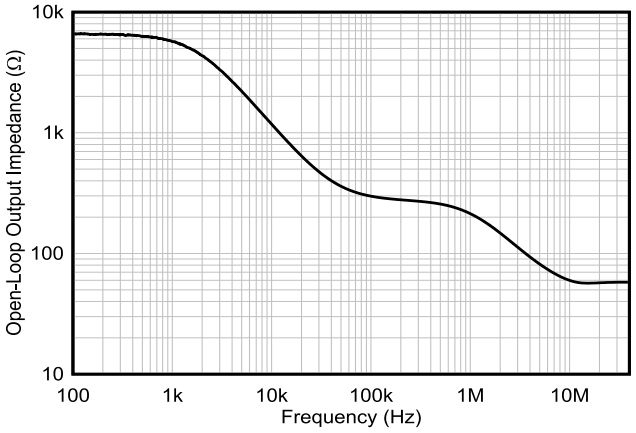


Figure 5-36. Open-Loop Output Impedance vs Frequency (New Die)

Copyright © 2026 Texas Instruments Incorporated

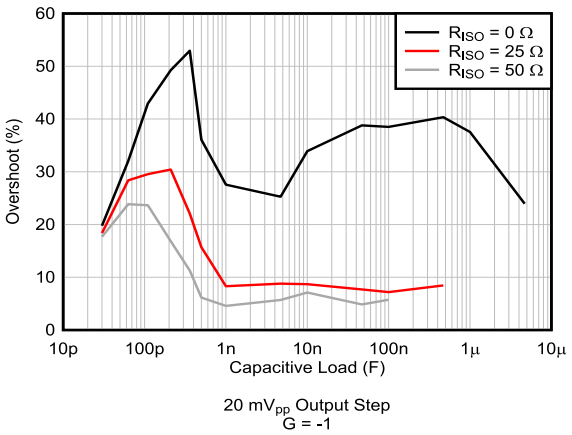


Figure 5-37. Small-Signal Overshoot vs Capacitive Load (New Die)

5.7 Old Die vs New Die

As of the publication of revision G of this datasheet, Texas Instruments has moved manufacturing of the die for LM8272 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “GF6”, for the new die the CSO is “TID”. The old die information is in the shipping information. The old die CSO is “GF6”, for the new die the CSO is “TID”. The old die information is maintained in this datasheet for comparison purposes, but all new manufacturing has moved to the new die.

Copyright © 2026 Texas Instruments Incorporated

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Driving Capacitive Loads:

The LM8272 is specifically designed to drive unlimited capacitive loads without oscillations. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features is an excellent choice for applications such as TFT flat panel buffers, A/D converter input amplifiers, and others.

However, as in most op amps, addition of a series isolation resistor between the op amp and the capacitive load improves the settling and overshoot performance.

To keep an acceptable phase margin, unlimited capacitive load drive devices lower the gain bandwidth product under larger capacitive loads. The LM8272 is specified to have a gain bandwidth product of 24MHz without significant capacitive load, but this value can begin to decrease at the point where a traditional amplifier can begin to become unstable. This tradeoff is what extends the output drive capability. LM8272 is designed with a wide gain bandwidth product to make sure there is headroom for many general-purpose applications with higher capacitive loads.

6.2 Output Short Circuit Current and Dissipation Issues:

The LM8272 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, output short circuit condition can be tolerated indefinitely.

With the op amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power can include an average value (due to a DC load current) and an AC component. DC load current flows if there is an output voltage offset, or if the output AC average current is non-zero, or if the op amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$$P_{tolal} = P_Q + P_{DC} + P_{AC} \quad (1)$$

$$P_Q = I_S \times V_S \text{ (Op Amp Quiescent Power Dissipation)} \quad (2)$$

$$P_{DC} = I_O \times [V_r - V_o] \text{(DC Load Power)} \quad (3)$$

P_{AC} = See Table 6-1 below (AC Load Power)

where:

- I_S: Supply Current
- V_S: Total Supply Voltage (V^+ - V^-)
- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current

Table 6-1 below shows the maximum AC component of the load power dissipated by the op amp for standard Sinusoidal, Triangular, and Square Waveforms:

Copyright © 2026 Texas Instruments Incorporated

Table 6-1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V^2)		
SINUSOIDAL	**TRIANGULAR**	**SQUARE**
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = \left[46.9 \times 10^{-3}\right] \times \left[\frac{24^2}{600}\right] = 45.0\text{mW} \quad (4)$$

6.3 Other Application Hints:

The use of supply decoupling is mandatory in most applications. As with most relatively high speed and high output current op amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (approximately 0.01µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor acts as the charge “bucket” for fast load current spikes at the op amp output. The combination of these capacitors provides supply decoupling and helps keep the op amp oscillation free under any load.

6.4 LM8272 Advantages:

Compared to other rail-to-rail input and output devices, the LM8272 offers several advantages such as:

- Improved cross over distortion
- Nearly constant supply current throughout the output voltage swing range and close to either rail.
- Nearly constant unity gain frequency (f_u) and Phase Margin (Phi_m) for all operating supplies and load conditions.
- No output phase reversal under input overload condition.

Copyright © 2026 Texas Instruments Incorporated

6.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Equivalent Internal ESD Circuitry Relative to a Typical Circuit, is helpful to have a good understanding of this basic ESD circuitry and relevance to an electrical overstress event. Figure 6-1 shows an illustration of the ESD circuits contained in the LM8272 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

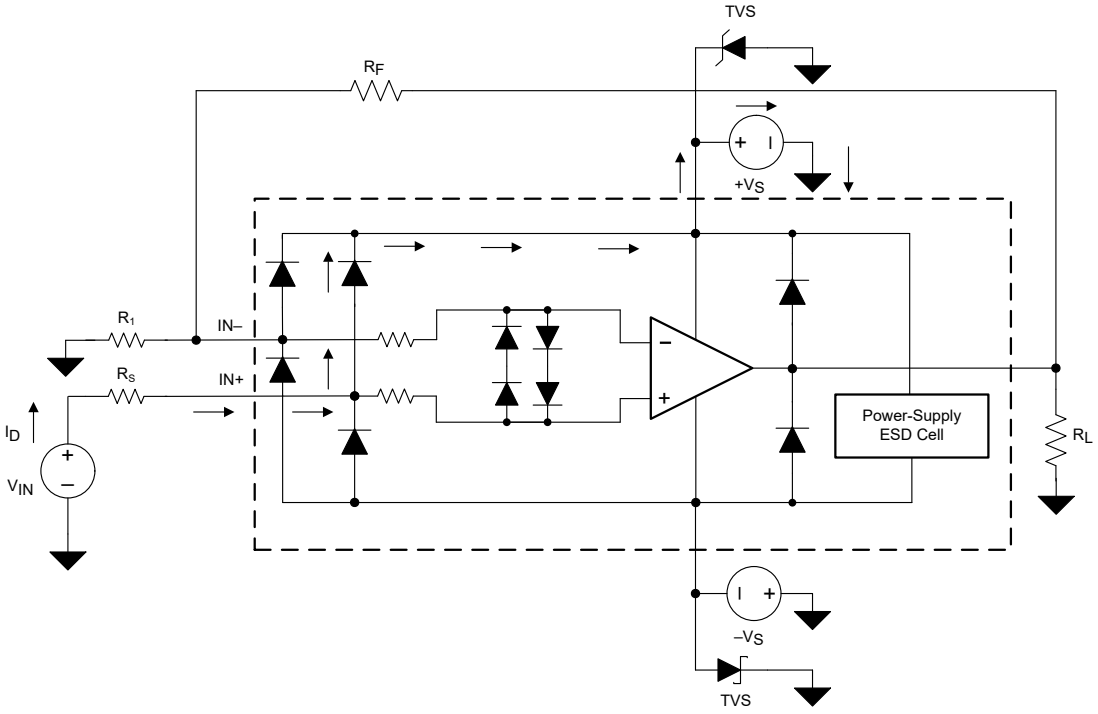


Figure 6-1. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

Copyright © 2026 Texas Instruments Incorporated

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the LM8272 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 6-1), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 6-1 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier cannot operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply terminals. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The LM8272 input terminals are protected from excessive differential voltage with back-to-back diodes; see Figure 6-1. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast - ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. These diodes can also be forward-biased in some comparator applications. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the LM8272. Figure 6-1 shows an example configuration that implements a current-limiting feedback resistor.

Copyright © 2026 Texas Instruments Incorporated

7 Device and Documentation Support

7.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2015) to Revision G (November 2026)	Page
• Added Signal Input Pins specification	4
• Updated footnotes	4
• Added the second row	4
• Changed the supply voltage minimum value from 2.5V to 2.7V	4
• Removed Input Bias Current typical value	6
• Changed Input Bias Current maximum value from ±2.8µA to ±2.7µA	6
• Added Max room temperature test condition for Input Bias Current with maximum value ±2µA	6
• Changed Input Offset Current typical value from 30nA to 20nA and maximum value from 275nA to 250nA	6
• Changed Power Supply Rejection Ratio typical value from 3.5µV/V to 109dB	6
• Added Power Supply Rejection Ratio minimum value of 74dB	6
• Added Open Loop Voltage Gain minimum value of 60dB	6
• Added New Die typical characteristics plots	7
• Added Old vs New die topic	13
• Deleted the sections titled *Block Diagram and Operational Description A) Input Stage*, *B) Output Stage:*, *C) Output Voltage Swing Close to V-*, and *Estimating the Output Voltage Swing*	14
• Updated *Driving Capacitive Loads* section	14
• Added the *Electrical Overstress* section	16

Changes from Revision E (August 2014) to Revision F (August 2015)	Page
• Changed GBWP from 15MHz to 24MHz	1
• Changed Slew rate from 15V/µs to 35V/µs	1
• Changed Supply current/channel from 0.95mA to 1.35mA	1
• Changed Output short circuit current ±130mA to ±125mA	1
• Changed Input voltage noise 15nV/√Hz to 12nV/√Hz	1
• Changed Input current noise 1.4pA/√Hz to 1pA/√Hz	1

Copyright © 2026 Texas Instruments Incorporated

- Changed operating supply voltage range from 2.5V to 2.7V....1
- Changed pin 5 From: -IN B To: +IN B Non-Inverting Input B in the *Pin Functions* table....3
- Changed pin 6 From: +IN B To: -IN B Inverting Input B in the *Pin Functions* table....3
- Moved Storage temperature range to the *Absolute Maximum Ratings*....4
- Changed *Handling Ratings* To: *Section 5.2*....4

Changes from Revision D (March 2013) to Revision E (August 2014) **Page**

- Changed datasheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Mechanical, Packaging, and Ordering Information. 1
- Deleted T_J = 25°C....6

Changes from Revision C (March 2013) to Revision D (March 2013) **Page**

- Changed layout of National Data Sheet to TI format....15

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM8272MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A60
LM8272MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A60

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

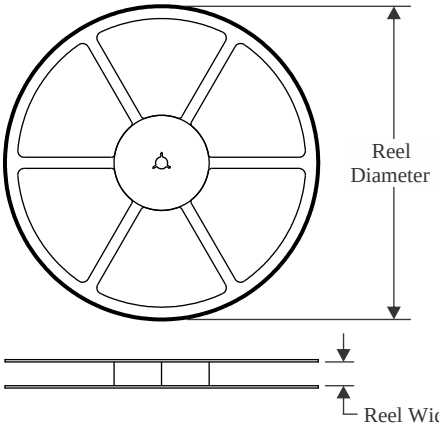
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

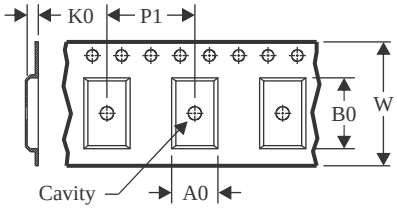
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

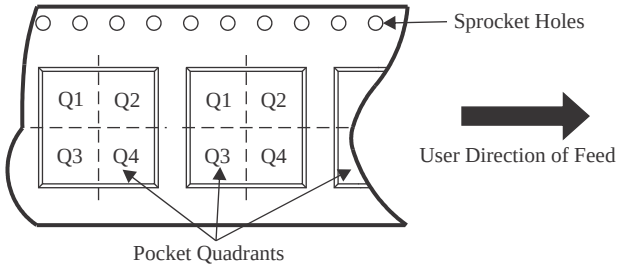


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

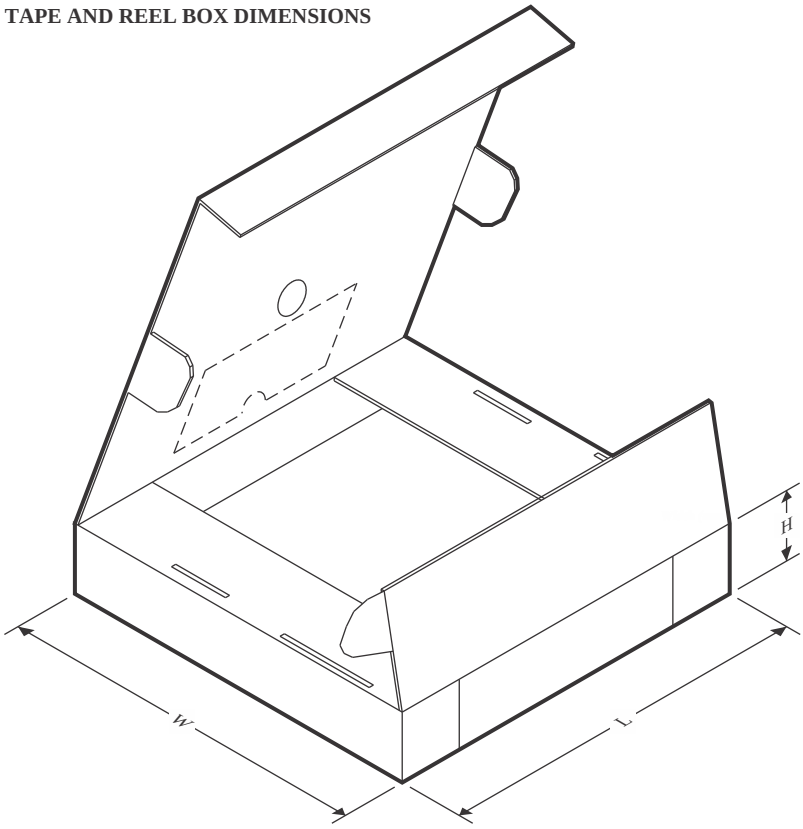
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8272MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM8272MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

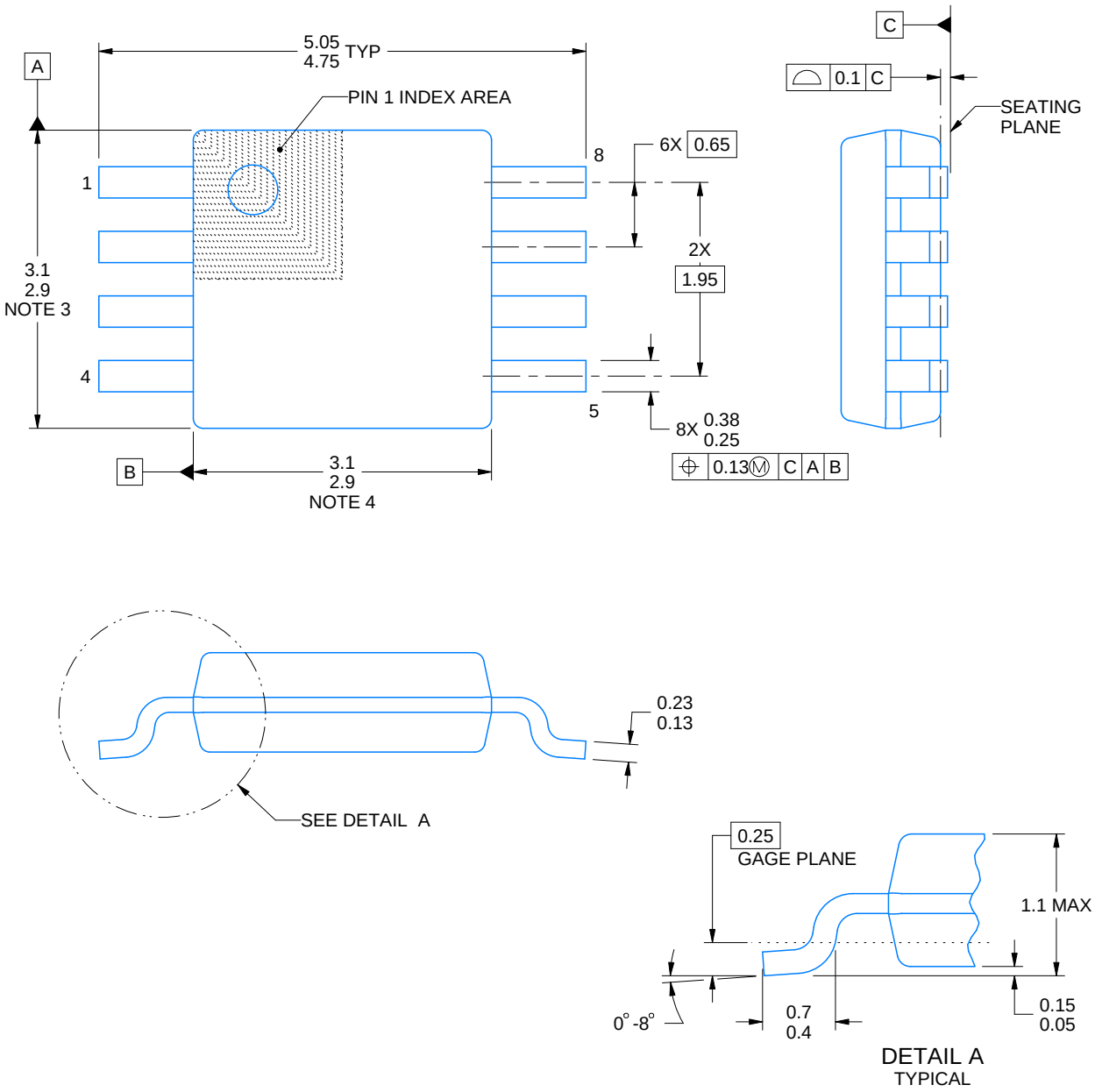
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8272MMX/NOPB	VSSOP	DGK	8	3500	366.0	364.0	50.0
LM8272MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

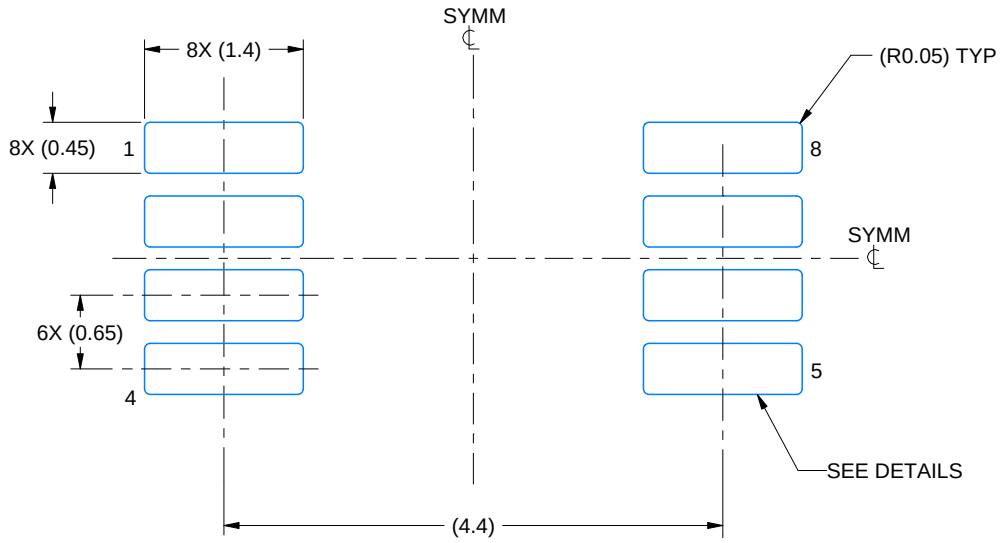
SMALL OUTLINE PACKAGE



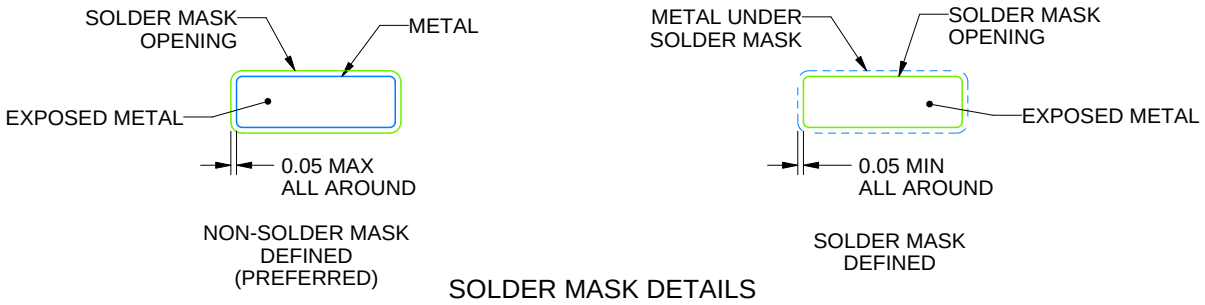
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

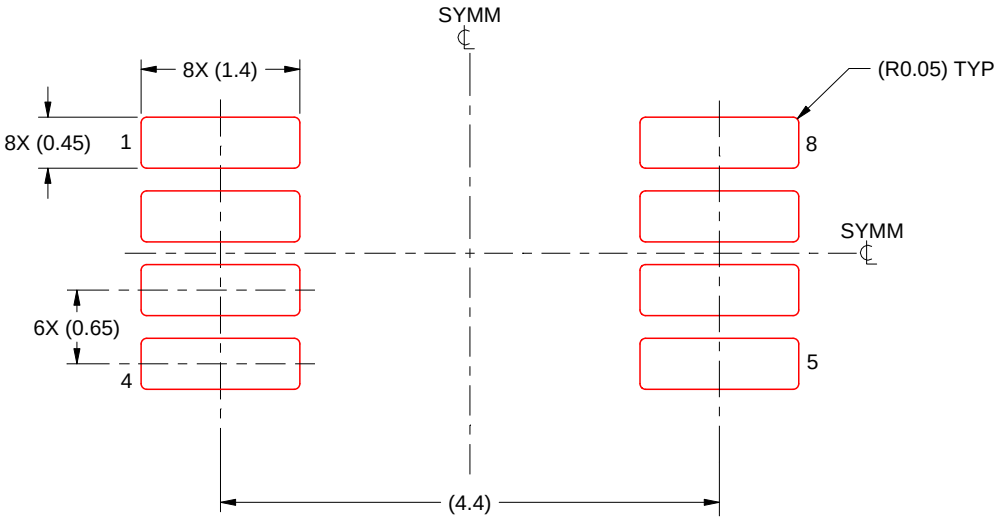


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025