参考文献

LMC603x CMOS 双通道运算放大器

1 特性

- 适用于 2kΩ 和 600Ω 负载
- 高压增益：126dB，2kΩ
- 低失调电压漂移：2.3μV/°C
- 超低输入偏置电流：40fA
- 输入共模范围包括 V–
- 可由标准 5V 和 15V 电源供电
- I_Q = 375μA/放大器；与 V+ 无关
- 低噪声：22nV/√Hz
- 压摆率：1.1V/μs
- 性能优于 TLC272

2 应用

- 高阻抗缓冲器或前置放大器
- 电流/电压转换器
- 长期积分器
- 采样保持电路
- 医疗仪器

3 说明

双通道 LMC6032 和四通道 LMC6034 (LMC603x) 是 CMOS 运算放大器，可由单电源或双电源供电。器件性能特性包括输入共模范围（包括接地）、低输入偏置电流以及为实际负载（例如 2kΩ 和 600Ω）提供的高压增益。

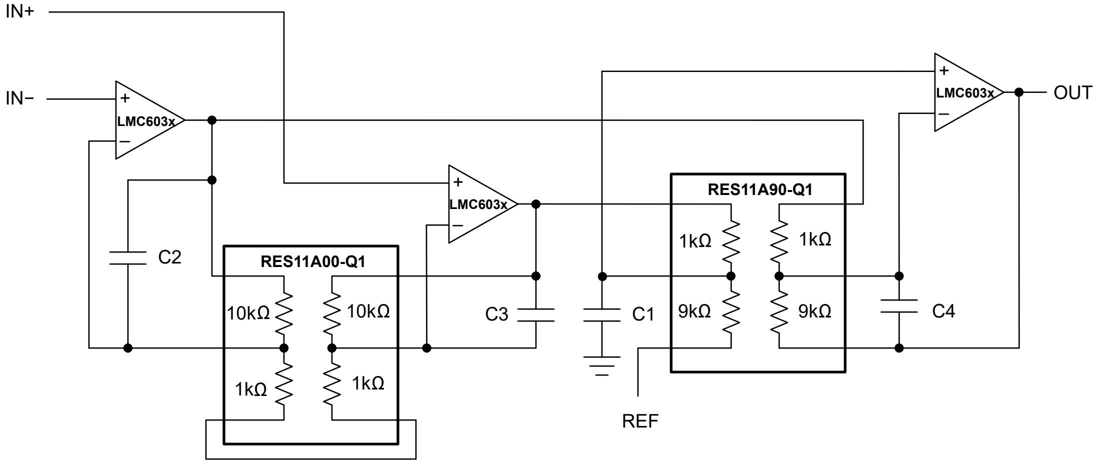
该芯片采用 TI 先进的 CMOS 工艺制造而成。

有关更高性能特性，请参阅 OPA928。

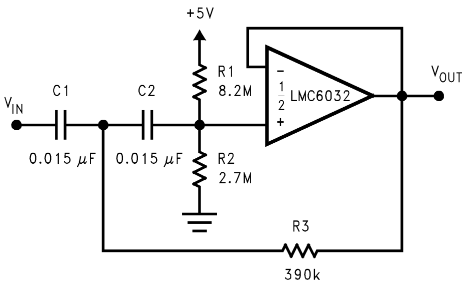
器件信息

器件型号	通道	封装[1]
LMC6032	双	D（SOIC，8）
		P（PDIP，8）
LMC6034	四通道	D（SOIC，14）
		P（PDIP，14）

(1) 如需更多信息，请参阅节 9。



典型应用：仪表放大器和 **RES11A**



典型应用：**10Hz** 高通滤波器

English Data Sheet: SNOS609

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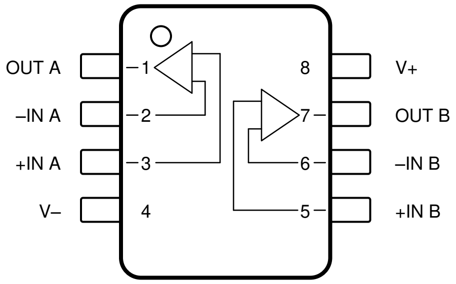
4 Pin Configuration and Functions

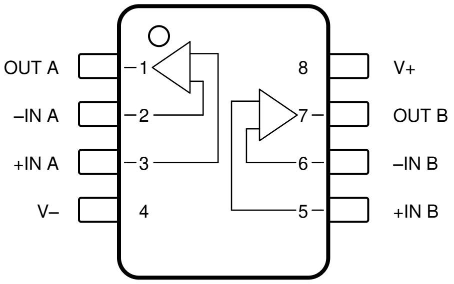


Not to scale

LMC6032 D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

表 4-1. Pin Functions: LMC6032

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
– IN A	2	Input	Inverting input, channel A
+IN B	5	Input	Noninverting input, channel B
– IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V –	4	Power	Negative (lowest) power supply



Not to scale

LMC6034 D Package, 14-Pin SOIC, and P Package, 14-Pin PDIP (Top View)

表 4-2. Pin Functions: LMC6034

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
– IN A	2	Input	Inverting input, channel A
– IN B	6	Input	Inverting input, channel B
– IN C	9	Input	Inverting input, channel C
– IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V –	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Differential input voltage			±Supply voltage	V
Supply voltage, V_S = (V+) – (V –)	Single supply	0	16	V
	Dual supply		±8	
Output short circuit	To V+		See(2)	mA
	To V –		See(3)	
Signal input pins	Voltage	(V –) – 0.3	(V+) + 0.3	V
	Current		±5	mA
Output pin current			±18	mA
Power supply pin	Current		35	mA
Power dissipation		See(4)		
Temperature	Operating, T_A	– 40	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	– 65	150	
	Lead (soldering, 10 sec.)		260	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

(3) Do not connect output to V+, when V+ is greater than 13V or reliability will be adversely affected.

(4) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V –)	Single supply	4.75		15.5	V
	Dual supply	±2.375		±7.75	
Specified temperature		– 40		85	°C
Power dissipation				See(2)	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed.

(2) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a printed circuit board.

5.4 Thermal Information LMC6032

THERMAL METRIC(1)		**LMC6032**		**UNIT**
		D (SOIC)	**P (PDIP)**	
		8 PINS	**8 PINS**	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	101	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information LMC6034

THERMAL METRIC(1)		**LMC6034**		**UNIT**
		D (SOIC)	**P(PDIP)**	
		14 PINS	**14 PINS**	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	85	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

at T_A = +25°C, V_S = 5V (V− = 0V), V_{CM} = 1.5V, V_{OUT} = V_S / 2, and R_L = 1MΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±9	mV
		T_A = −40°C to +85°C				±11	
dV_{OS}/dT	Input offset voltage drift	T_A = −40°C to +85°C			±2.3		μV/°C
PSRR	Power-supply rejection ratio	Positive, 5V ⩽ V+ ⩽ 15V		63	83		dB
			T_A = −40°C to +85°C	60			
		Negative, −5V ⩽ V+ ⩽ −10V		74	94		
			T_A = −40°C to +85°C	70			
INPUT BIAS CURRENT							
I_B	Input bias current				±40		fA
		T_A = −40°C to +85°C				±200	pA
I_{OS}	Input offset current				±10		fA
		T_A = −40°C to +85°C				±100	pA
NOISE							
e_n	Input voltage noise density	f = 1kHz			22		nV/√Hz
i_n	Input current noise density	f = 1kHz			4		fA/√Hz
THD	Total harmonic distortion	f= 10kHz, G = −10V/V, R_L = 2kΩ, V_O = 8V_{pp}, V_S = ±5V			0.2		%
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	To positive rail, 5V ⩽ V_S ⩽ 15V, CMRR > 50dB		(V+) − 2.3	(V+) − 1.9		V
			T_A = −40°C to +85°C	(V+) − 2.6			
		To negative rail, 5V ⩽ V_S ⩽ 15V, CMRR > 50dB			(V−) − 0.4	(V−) − 0.1	
			T_A = −40°C to +85°C			(V−)	
CMRR	Common-mode rejection ratio	V_S = 15V, 0V < V_{CM} < 12V		63	83		dB
			T_A = −40°C to +85°C	60			
INPUT IMPEDANCE							
R_{IN}	Input resistance				> 1		TΩ
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	Sourcing, V_S = 15V, V_{CM} = 7.5V, 7.5V < V_O < 11.5V, R_L = 2kΩ		200	2000		V/mV
			T_A = −40°C to +85°C	100			
		Sinking, V_S = 15V, V_{CM} = 7.5V, 2.5V < V_O < 7.5V, R_L = 2kΩ		90	500		
			T_A = −40°C to +85°C	40			
		Sourcing, V_S = 15V, V_{CM} = 7.5V, 7.5V < V_O < 11.5V, R_L = 600Ω		100	1000		
			T_A = −40°C to +85°C	75			
		Sinking, V_S = 15V, V_{CM} = 7.5V, 2.5V < V_O < 7.5V, R_L = 600Ω		50	250		
			T_A = −40°C to +85°C	20			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.4		MHz
SR	Slew rate(1)	V_S = 15V, 10V step		0.8	1.1		V/μs
			T_A = −40°C to +85°C	0.4			
θ_m	Phase margin				50		°
	Crosstalk	Dual and quad channel, V_S = 15V, R_L = 10kΩ to 7.5V, f = 1kHz, V_O = 13V_{pp}			130		dB

5.6 Electrical Characteristics（续）

at T_A = +25°C, V_S = 5V (V^- = 0V), V_{CM} = 1.5V, V_{OUT} = V_S / 2, and R_L = 1MΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing	Positive rail V_S = 5V, R_L = 2kΩ to mid-supply		4.20	4.87		V
			T_A = –40°C to +85°C	4.00			
		Negative rail V_S = 5V, R_L = 2kΩ to mid-supply			0.10	0.25	
			T_A = –40°C to +85°C			0.35	
		Positive rail V_S = 5V, R_L = 600Ω to mid-supply		4.00	4.61		
			T_A = –40°C to +85°C	3.80			
		Negative rail V_S = 5V, R_L = 600Ω to mid-supply			0.30	0.63	
			T_A = –40°C to +85°C			0.75	
		Positive rail V_S = 15V, R_L = 2kΩ to mid-supply		13.50	14.63		
			T_A = –40°C to +85°C	13.00			
		Negative rail V_S = 15V, R_L = 2kΩ to mid-supply			0.26	0.45	
			T_A = –40°C to +85°C			0.55	
		Positive rail V_S = 15V, R_L = 600Ω to mid-supply		12.50	13.90		
			T_A = –40°C to +85°C	12.00			
		Negative rail V_S = 15V, R_L = 600Ω to mid-supply			0.79	1.45	
			T_A = –40°C to +85°C			1.75	
I_{SC}	Short-circuit current	Sourcing V_S = 5V, V_O = 0V		13	22		mA
			T_A = –40°C to +85°C	9			
		Sinking V_S = 5V, V_O = 5V		13	21		
			T_A = –40°C to +85°C	9			
		Sourcing V_S = 15V, V_O = 0V		23	40		
			T_A = –40°C to +85°C	15			
		Sinking V_S = 15V, V_O = 13V[2]		23	39		
			T_A = –40°C to +85°C	15			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_O = 1.5V	LMC6032		375	800	μA
			LMC6032, T_A = –40°C to +85°C			950	
			LMC6034		375	675	
			LMC6034, T_A = –40°C to +85°C			750	

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(1) Specification limit established from device population bench system measurements across multiple lots. Number specified is the slower of either the positive or negative slew rates.

(2) Do not connect output to V+, when V+ is greater than 13V or reliability can be adversely affected.

Typical Characteristics

at T_A = 25°C, V_S = ±7.5V, V_{OUT} = mid-supply, and R_L > 1M Ω (unless otherwise noted)

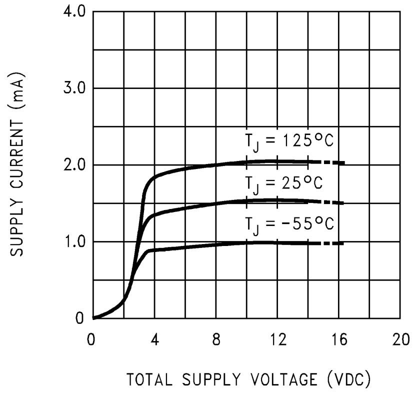


图 5-1. Supply Current vs Supply Voltage

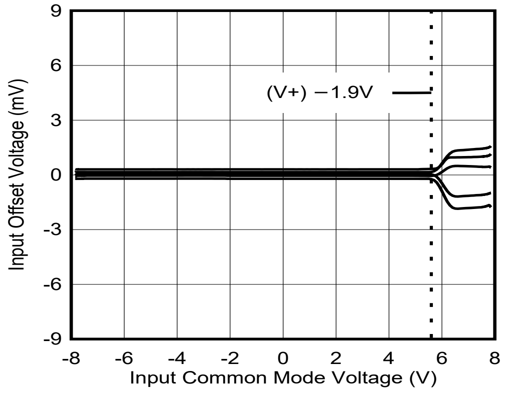


图 5-2. Offset Voltage vs Input Common-Mode Voltage

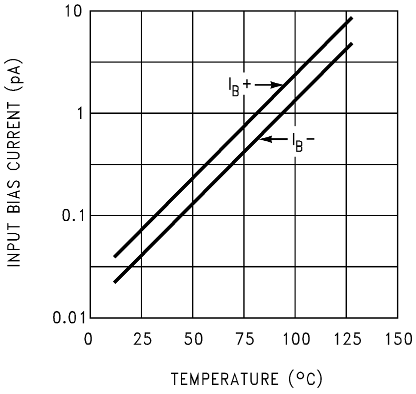


图 5-3. Input Bias Current

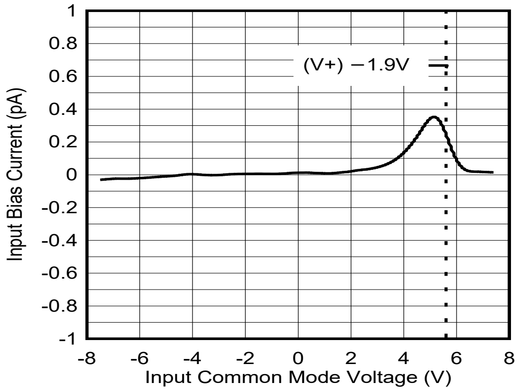
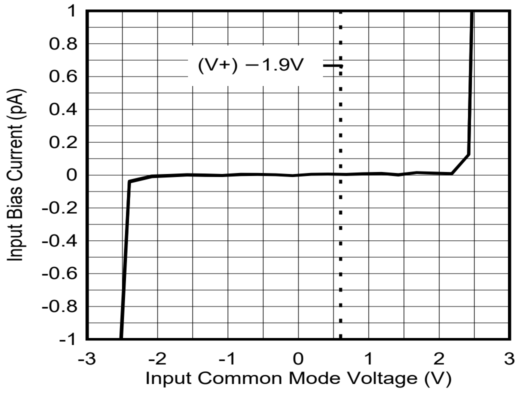


图 5-4. Input Bias Current vs Input Common-Mode Voltage



V_S = ±2.5V

图 5-5. Input Bias Current vs Input Common-Mode Voltage

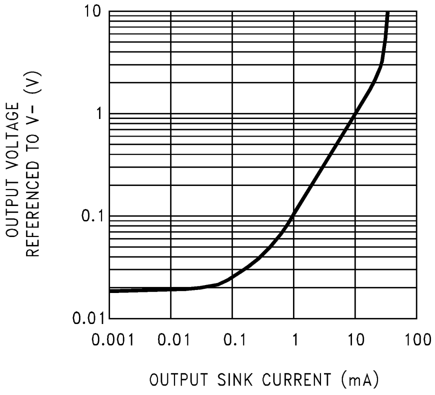


图 5-6. Output Characteristics Current Sinking

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±7.5V, V_{OUT} = mid-supply, and R_L > 1M Ω (unless otherwise noted)

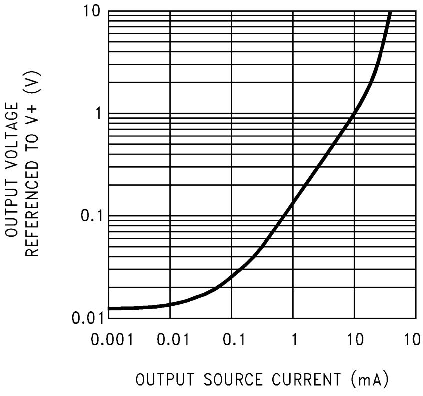


图 5-7. Output Characteristics Current Sourcing

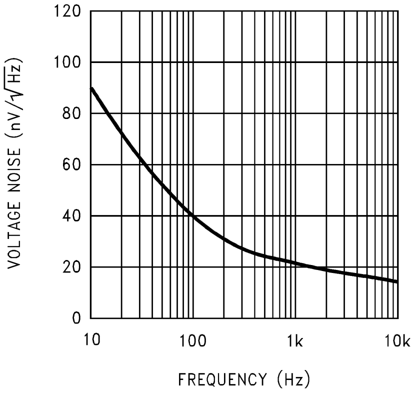


图 5-8. Input Voltage Noise vs Frequency

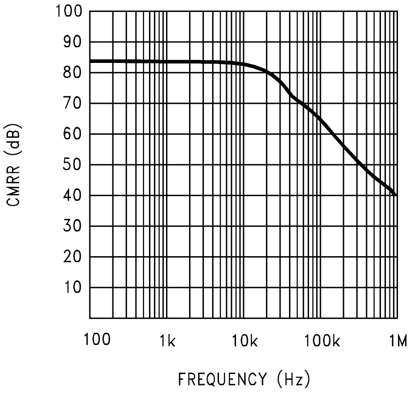


图 5-9. CMRR vs Frequency

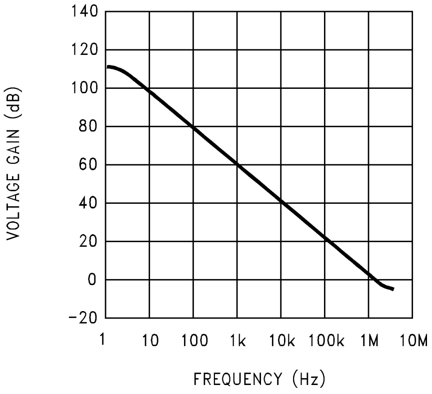


图 5-10. Open-Loop Frequency Response

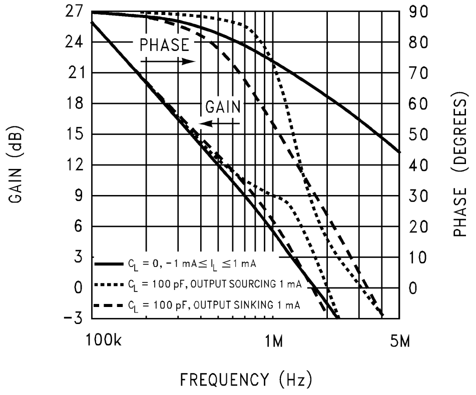


图 5-11. Frequency Response vs Capacitive Load

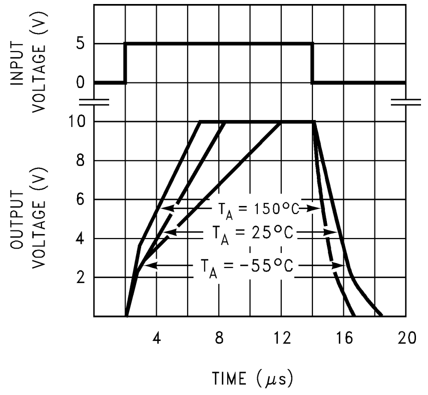


图 5-12. Noninverting Large-Signal Pulse Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±7.5V, V_{OUT} = mid-supply, and R_L > 1MΩ (unless otherwise noted)

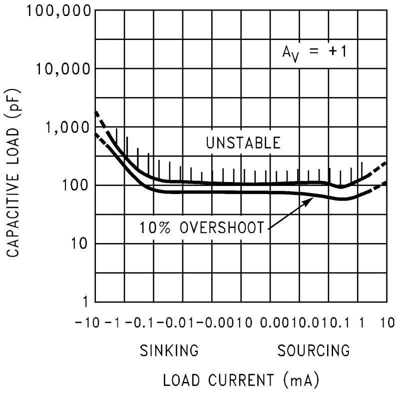


图 5-13. Stability vs Capacitive Load

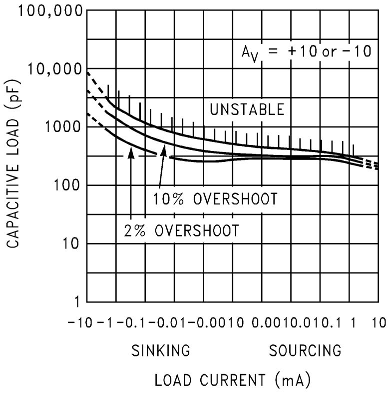


图 5-14. Stability vs Capacitive Load

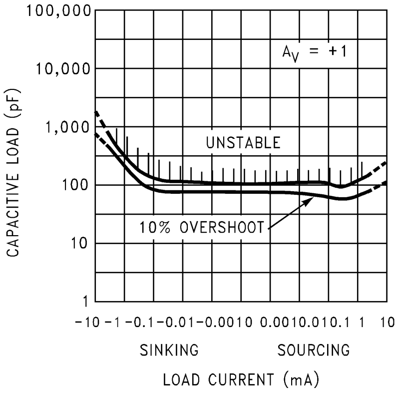
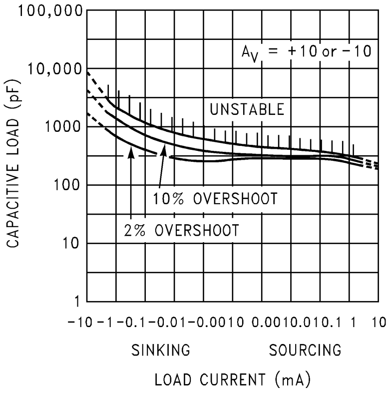


图 5-15. Stability vs Capacitive Load



Avoid resistive loads of less than 500Ω because these loads can cause instability.

图 5-16. Stability vs Capacitive Load

6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

6.1 Application Information

6.1.1 Amplifier Topology

The topology chosen for the LMC603x, shown in 图 6-1, is unconventional compared to general-purpose op amps. The LMC603x incorporates novel op-amp design that enables a wide input common-mode range and rail to rail output swing even when driving a large load. The input common-mode range includes ground, making the LMC603x an excellent choice for single-supply applications. While the LMC603x supports both a wide supply and common-mode voltage range, large input common-mode voltage can cause a degradation of input bias current performance.

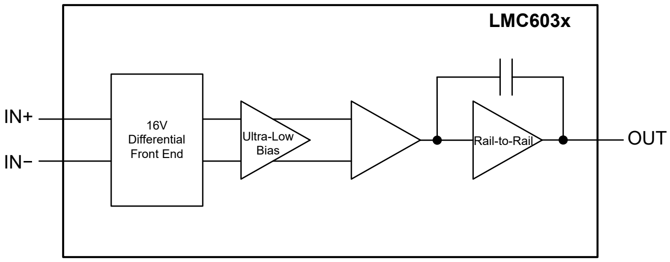


图 6-1. LMC603x Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600 Ω load. The gain while sinking is greater than most CMOS op amps as a result of the additional gain stage; however, under heavy load (600 Ω), the gain can be reduced as indicated in 节 5.6.

6.1.2 Compensating Input Capacitance

The high input resistance of the LMC603x op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit can be especially sensitive to the printed circuit board (PCB) layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and ac ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, and so on) and the feedback resistors create a pole in the feedback path. In 图 6-2, the frequency of this pole is:

$$f_P = \frac{1}{2\pi C_S R_P} \tag{1}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, and so on, and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all the following formulas, apply to inverting and noninverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ , the frequency of the feedback pole can be quite high, since C_S is generally less than 10pF. If the frequency of the feedback pole is much greater than the *ideal* closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole has a negligible effect on stability, as only a small amount of phase shift is added.

However, if the feedback pole is less than approximately 6 to 10 times the *ideal* −3dB frequency, add a feedback capacitor, C_F, between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier low-frequency noise gain: To maintain stability, a feedback capacitor is probably needed if:

$$\left(\frac{R_F}{R_{IN}}+1\right) \le \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S} \qquad (2)$$

where

- $\left(\frac{R_F}{R_{IN}}+1\right)$ is the amplifier low-frequency noise gain.
- GBW is the amplifier gain bandwidth product.

An amplifier low-frequency noise gain is represented by the following formula:

$$\left(\frac{R_F}{R_{IN}}+1\right) \qquad (3)$$

regardless of whether the amplifier is being used in an inverting or noninverting mode. A feedback capacitor is more likely to be needed when the noise gain is low, the feedback resistor is large. or both.

If the previous condition is met (indicating a feedback capacitor is probably be needed), and the noise gain is large enough that $\left(\frac{R_F}{R_{IN}}+1\right) \ge 2\sqrt{GBW \times R_F \times C_S}$, the following value of feedback capacitor is recommended:

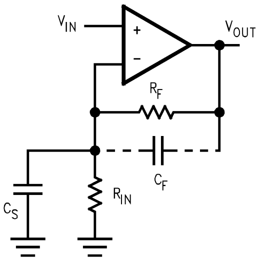
$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}}+1\right)} \qquad (4)$$

If $\left(\frac{R_F}{R_{IN}}+1\right) < 2\sqrt{GBW \times R_F \times C_S}$, the feedback capacitor is:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}} \qquad (5)$$

These capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F} \qquad (6)$$



C_S consists of the amplifier input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

图 6-2. General Operational Amplifier Circuit

Using the smaller capacitors give much higher bandwidth with little degradation of transient response. Using a somewhat larger feedback capacitor can be necessary in any of the above cases to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a PCB stray capacitance can be larger or smaller than the breadboard capacitance, so the actual preferred value for C_F can be different from the one estimated using the breadboard. In most cases, check the value of C_F on the actual circuit, starting with the computed value.

6.1.3 Capacitive Load Tolerance

Like many other op amps, the LMC603x can oscillate when applied a load that appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See also 节 Typical Characteristics.

The load capacitance interacts with the op amp output resistance to create an additional pole. If this pole frequency is sufficiently low, the op amp phase margin is degraded so that the amplifier is no longer stable at low gains. 图 6-3 shows that the addition of a small resistor (50 Ω to 100 Ω) in series with the op amp output, and a capacitor (5pF to 10pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. In all cases, the output can ring heavily when the load capacitance is near the threshold for oscillation.

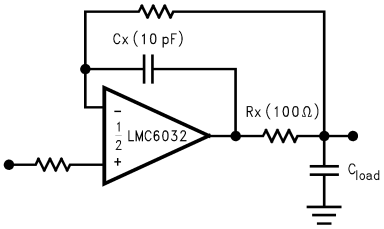


图 6-3. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pullup resistor to V^+ (图 6-4). Typically, a pullup resistor conducting 500 μA or more significantly improves capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. The open-loop gain of the amplifier can also be affected by the pullup resistor (see 节 5.6).

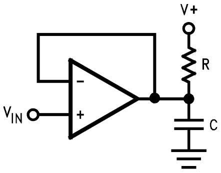


图 6-4. Compensating for Large Capacitive Loads with a Pullup Resistor

6.1.4 Bias Current Testing

The test method of 图 6-5 is appropriate for bench-testing bias current with reasonable accuracy. To understand the circuit operation, first close switch S2 momentarily. When S2 is opened, then:

$$I_{b-} = \frac{dV_{OUT}}{dt} \times C_2 \tag{7}$$

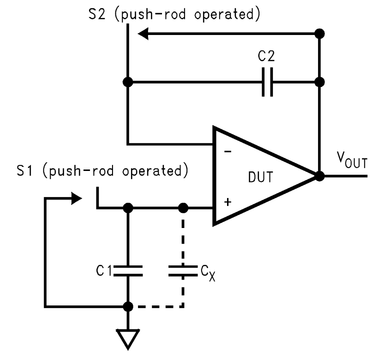


图 6-5. Simple Input Bias Current Test Circuit

A recommended capacitor for C2 is a 5pF or 10pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b-, the leakage of the capacitor and socket must be taken into account. Leave switch S2 shorted most of the time, or else the dielectric absorption of the capacitor C2 can cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted), then:

$$I_{b+} = \frac{dV_{OUT}}{dt} \times (C_1 + C_x) \tag{8}$$

where C_x is the stray capacitance at the + input.

6.2 Typical Applications

Typical Single-Supply Applications

Additional single-supply applications ideas are found in the LM358 data sheet. The LMC603x is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features can improve the performance of many existing single-supply applications. Be aware, however, the supply voltage range of the LMC603x is smaller than that of the LM358.

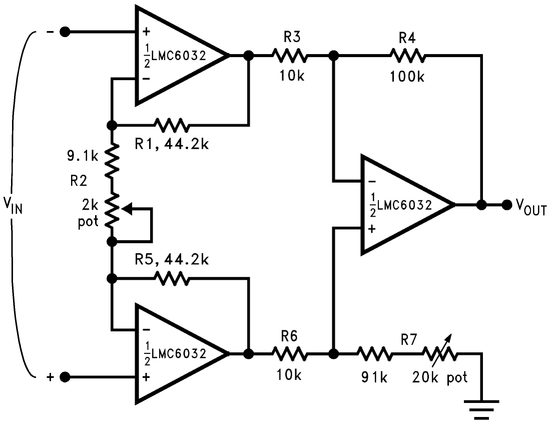


图 6-6. Instrumentation Amplifier

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

If R1 = R5, R3 = R6, and R4 = R7, then A_V = 100 for circuit shown.

Use low-drift resistors for good CMRR performance over temperature. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain is adjusted through R2. CMRR is adjusted through R7. An improved circuit can be designed using the RES11A-Q1, low-drift, precision, matched resistor pairs. 图 6-7 shows how a precise gain of 99 is easily implemented. The capacitors are optional and are be used to improve noise performance, if needed.

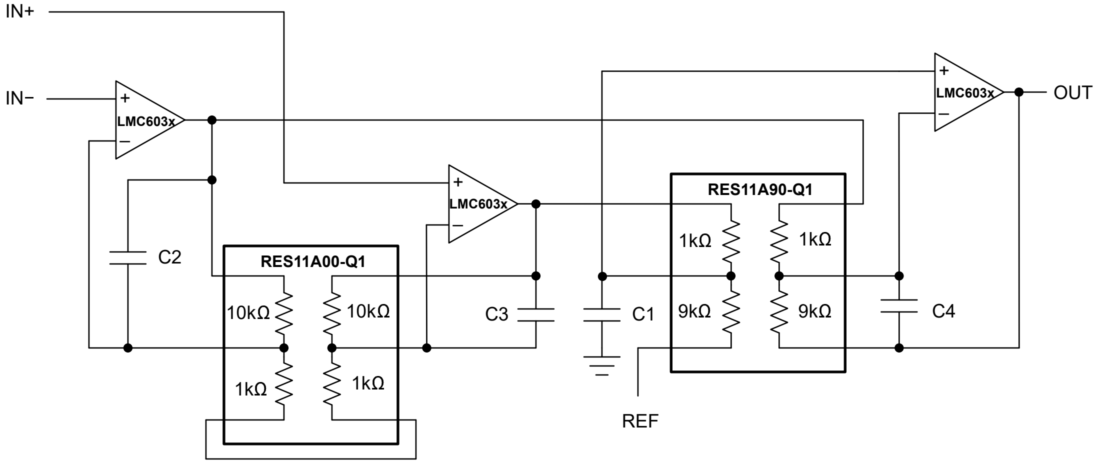
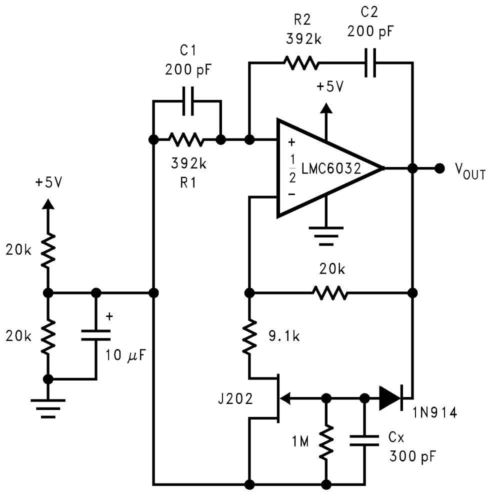


图 6-7. Improved Instrumentation Amplifier With RES11A



Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{OSC} = 1/2 \pi RC$

where R = R1 = R2 and C = C1 = C2.

图 6-8. Sine-Wave Oscillator

This circuit, as shown, oscillates at 2.0kHz with a peak-to-peak output swing of 4.0V.

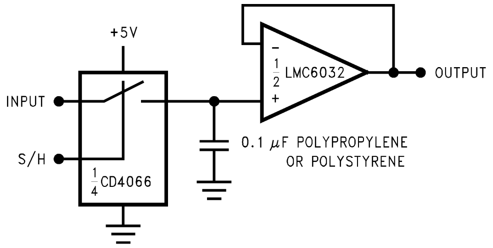


图 6-9. Low-Leakage Sample-and-Hold

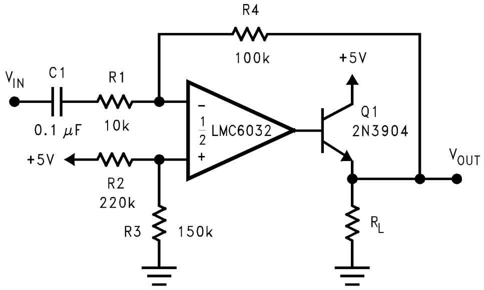


图 6-11. Power Amplifier

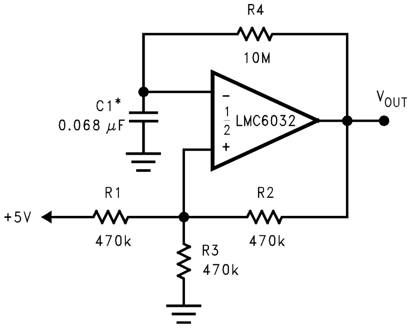
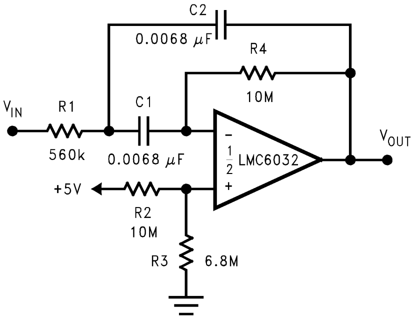


图 6-10. 1Hz Square-Wave Oscillator



$f_O = 10Hz, Q = 2.1, gain = -8.8$

图 6-12. 10Hz Bandpass Filter

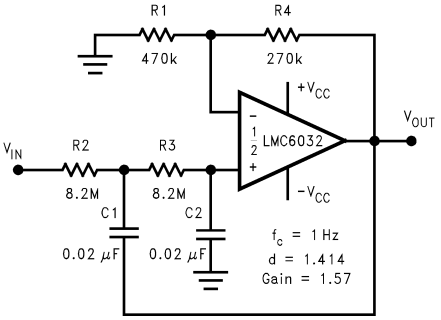
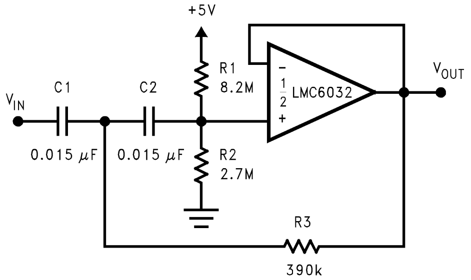
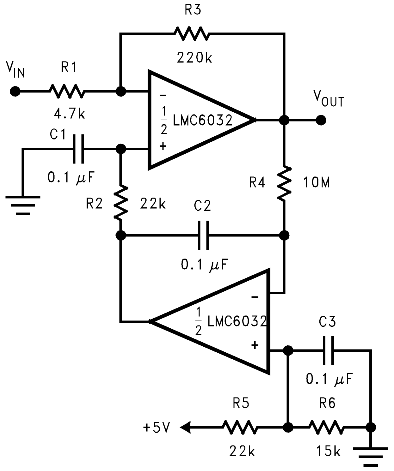


图 6-13. 1Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



f_c = 10Hz, d = 0.895, gain = 1, 2dB pass-band ripple

图 6-14. 10Hz High-Pass Filter



Gain = −46.8 Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1mV).

图 6-15. High-Gain Amplifier With Offset Voltage Reduction

6.3 Layout

6.3.1 Layout Guidelines

6.3.1.1 Printed Circuit Board Layout for High-Impedance Work

Generally, any circuit that operates with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low bias current of the LMC603x, typically less than 40fA, an excellent layout is essential. Fortunately, the techniques for obtaining low leakages are quite simple. Foremost, do not ignore the surface leakage of the PCB, even though the leakage can sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC603x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so on, connected to the op amp inputs. See 图 6-16. To have a significant effect, place guard rings on both the top and bottom of the PCB. This PCB foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, can leak 5pA if the trace were a 5V bus adjacent to the pad of an input. This causes a 100 times degradation from the LMC603x actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ causes only 50fA of leakage current, or perhaps a minor (2:1) degradation of the amplifier performance. See 图 6-17, 图 6-18, 图 6-19 for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see 图 6-20.

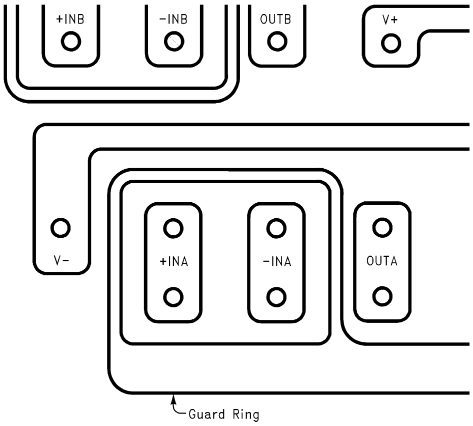


图 6-16. Example of Guard Ring in PCB Layout

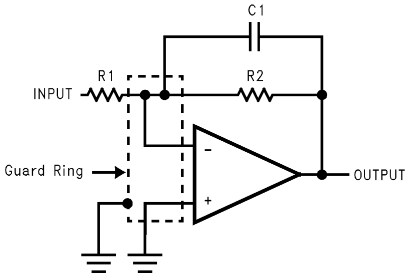


图 6-17. Inverting Amplifier Guard-Ring Connections

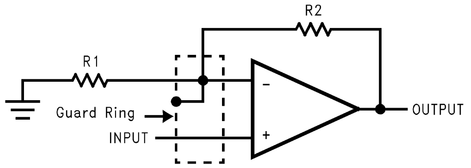


图 6-18. Noninverting Amplifier Guard-Ring Connections

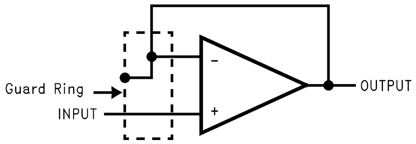


图 6-19. Follower Guard-Ring Connections

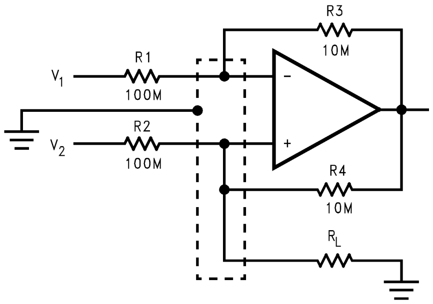
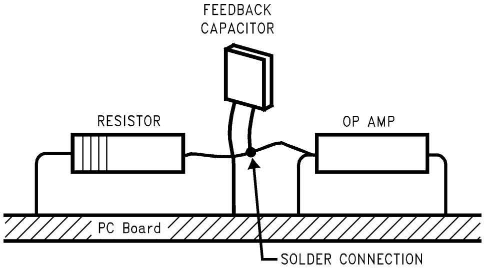


图 6-20. Howland Current-Pump Guard-Ring Connections

Be aware that when laying out a PCB for the sake of just a few circuits is inappropriate, there is another technique which is even better than a guard ring on a PCB. Do not insert the amplifier input pin into the board at all, but bend the pin up in the air and use only air as an insulator. Air is an excellent insulator. In this case you forgo some of the advantages of PCB construction, but the advantages of air are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See 图 6-21.



Input pins are lifted out of PCB and soldered directly to components. All other pins connected to the PCB.

图 6-21. Air Wiring

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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7.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.4 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (March 2013) to Revision D (February 2024)	Page
• 添加了 LMC6034 和相关信息	1
• 将 I_Q 从 400 μ A 更改为 375 μ A，以与*特性* 中的*电气 特性 匹配*	1
• 将*特性* 中的高压增益从 12dB 更改为 126dB（拼写错误）	1
• 向*特性* 中添加了低噪声并删除了低失真	1
• 向*说明* 中添加了 OPA928 高性能基准	1
• Added *Pin Configuration and Functions*	2
• Added *Thermal Information*	5
• Changed parameter names to conform with new standards in *Electrical Characteristics*	6
• Changed input current noise specification from 0.0002pA/ $\sqrt{\text{Hz}}$ to 4fA/ $\sqrt{\text{Hz}}$ in *Electrical Characteristics*	6
• Changed total harmonic distortion specification from 0.01% to 0.2% in *Electrical Characteristics*	6
• Updated conditions in the header of *Typical Characteristics*	8
• Added input offset voltage vs common mode voltage and input bias current vs common mode voltage	8
• Updated description and circuit topology diagram in *Amplifier Topology*	11
• Added new instrumentation amplifier circuit using the RES11A to *Typical Applications*	15

Changes from Revision B (March 2013) to Revision C (March 2013)	Page
• Changed layout of National Data Sheet to TI format	15

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6032IM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC60 32IM
LMC6032IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMC60 32IM
LMC6032IMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC60 32IM
LMC6032IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC60 32IM
LMC6032IN/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC 6032IN
LMC6032IN/NOPB.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC 6032IN
LMC6032IN/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC 6032IN
LMC6034IM/NOPB	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6034IM
LMC6034IMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC6034IM
LMC6034IMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC6034IM
LMC6034IMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMC6034IM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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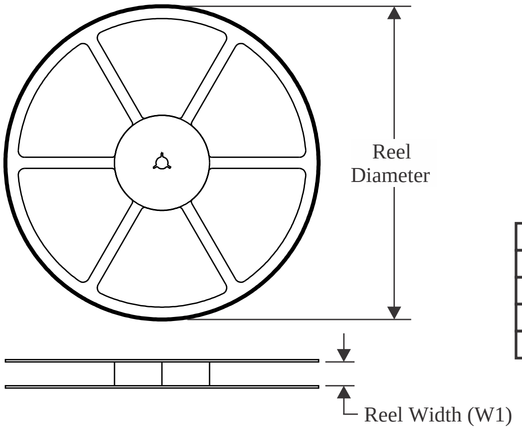
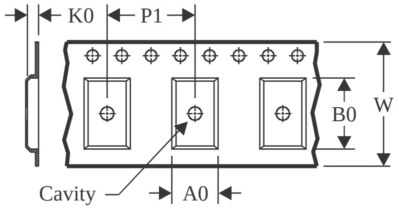
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

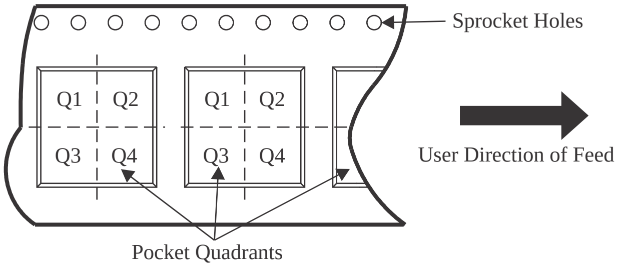


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

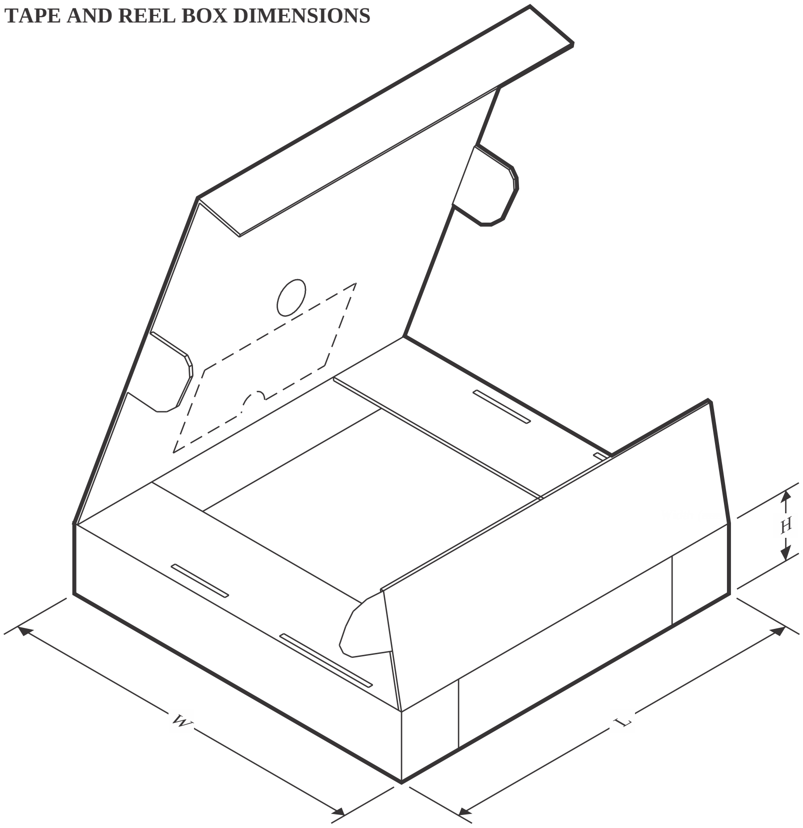
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6032IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMC6032IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6034IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

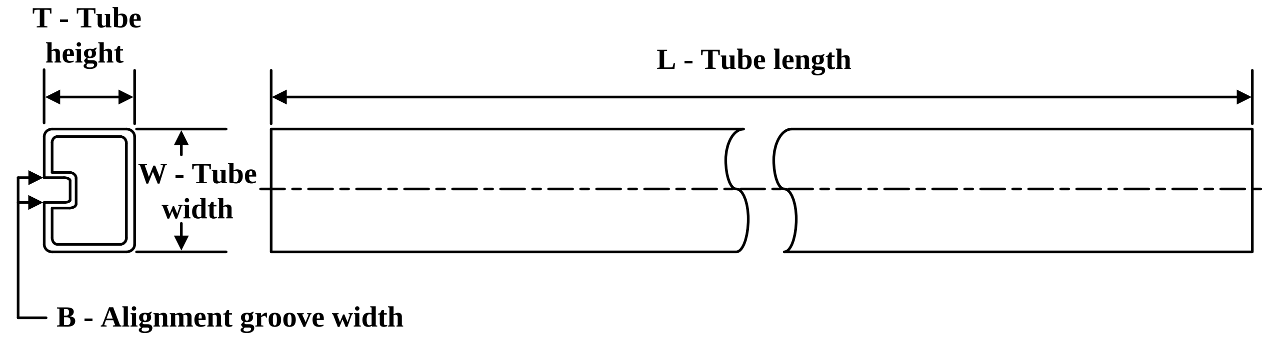
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

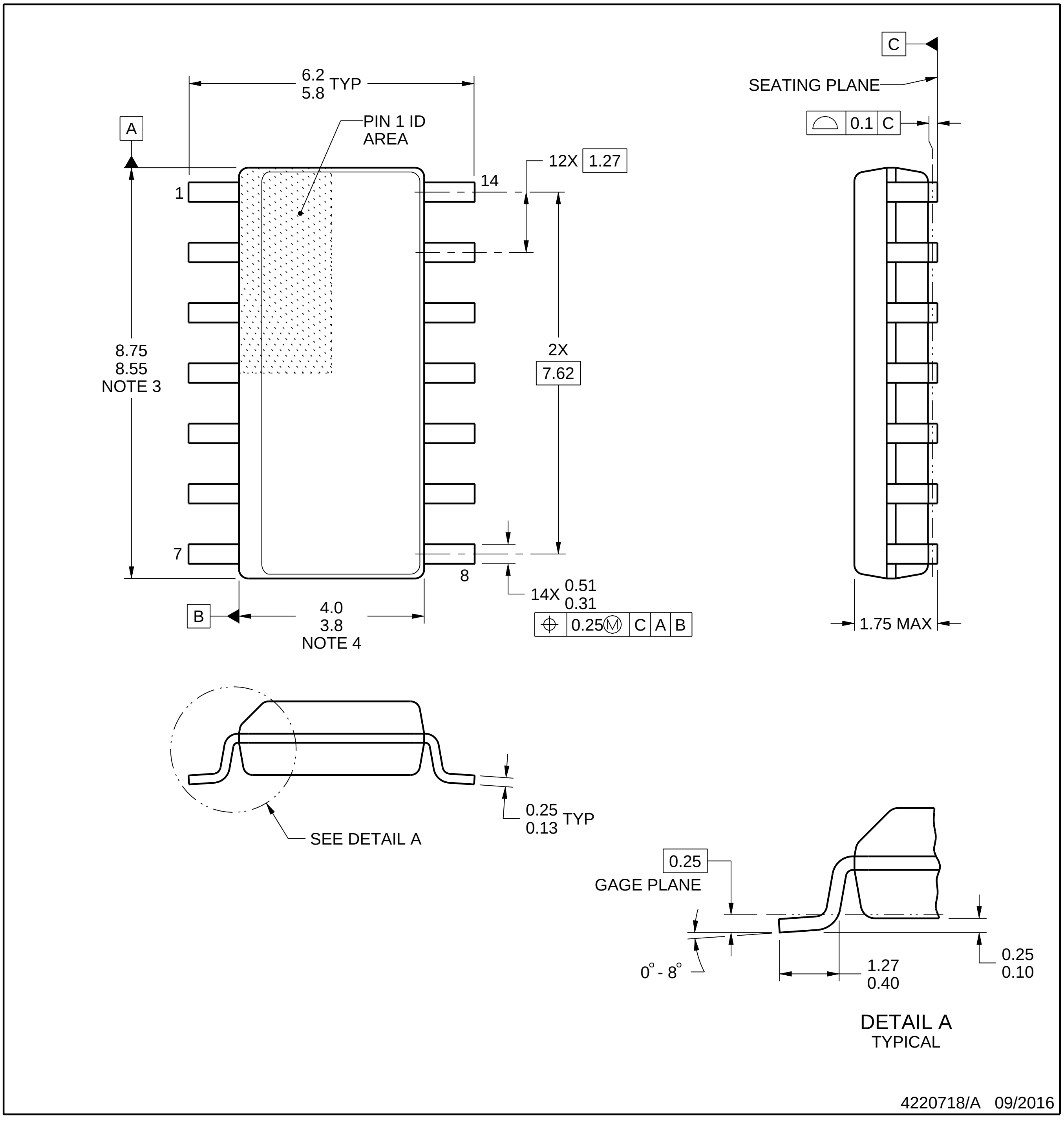
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6032IMX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LMC6032IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6034IMX/NOPB	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



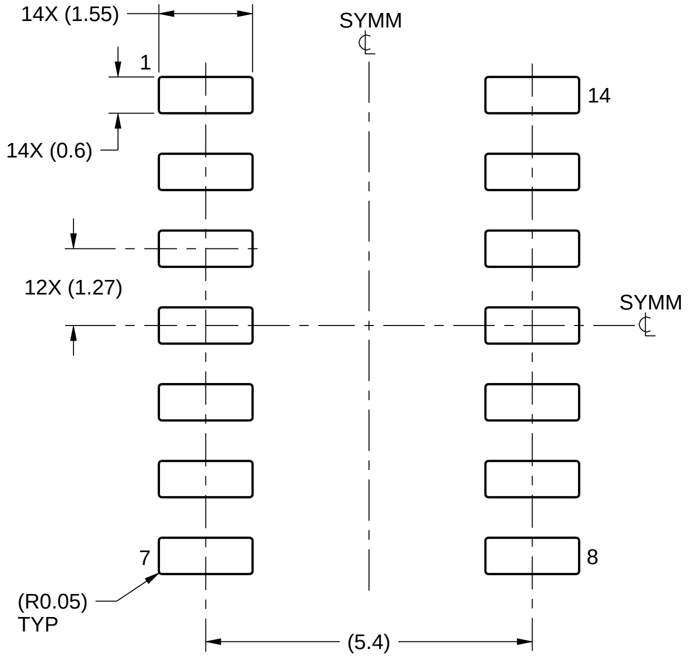
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6032IN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC6032IN/NOPB	P	PDIP	8	40	506	13.97	11230	4.32
LMC6032IN/NOPB.A	P	PDIP	8	40	502	14	11938	4.32
LMC6032IN/NOPB.A	P	PDIP	8	40	506	13.97	11230	4.32
LMC6032IN/NOPB.B	P	PDIP	8	40	502	14	11938	4.32
LMC6032IN/NOPB.B	P	PDIP	8	40	506	13.97	11230	4.32

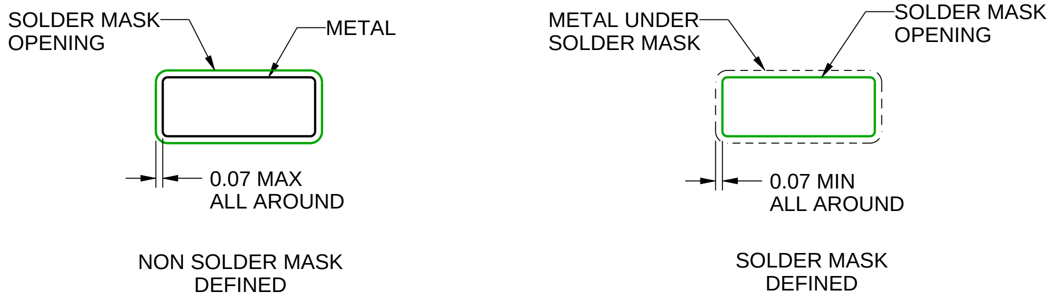


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

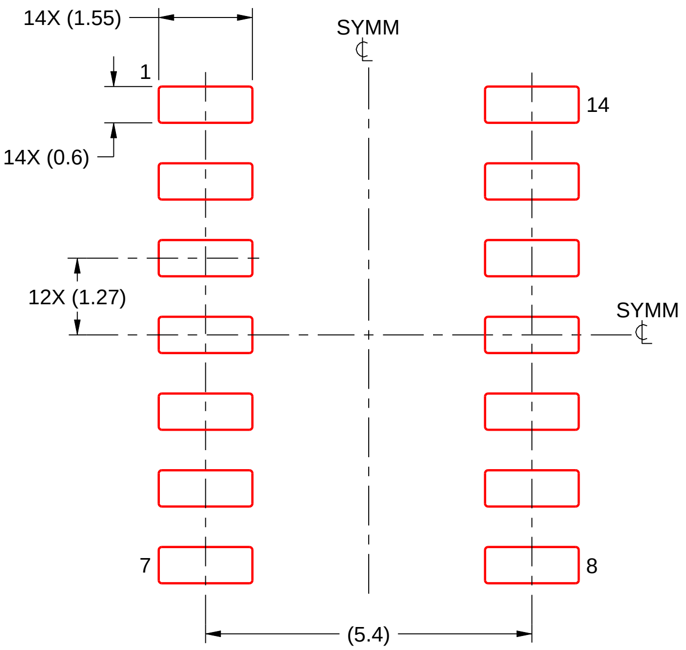


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

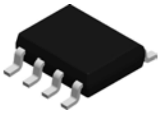


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

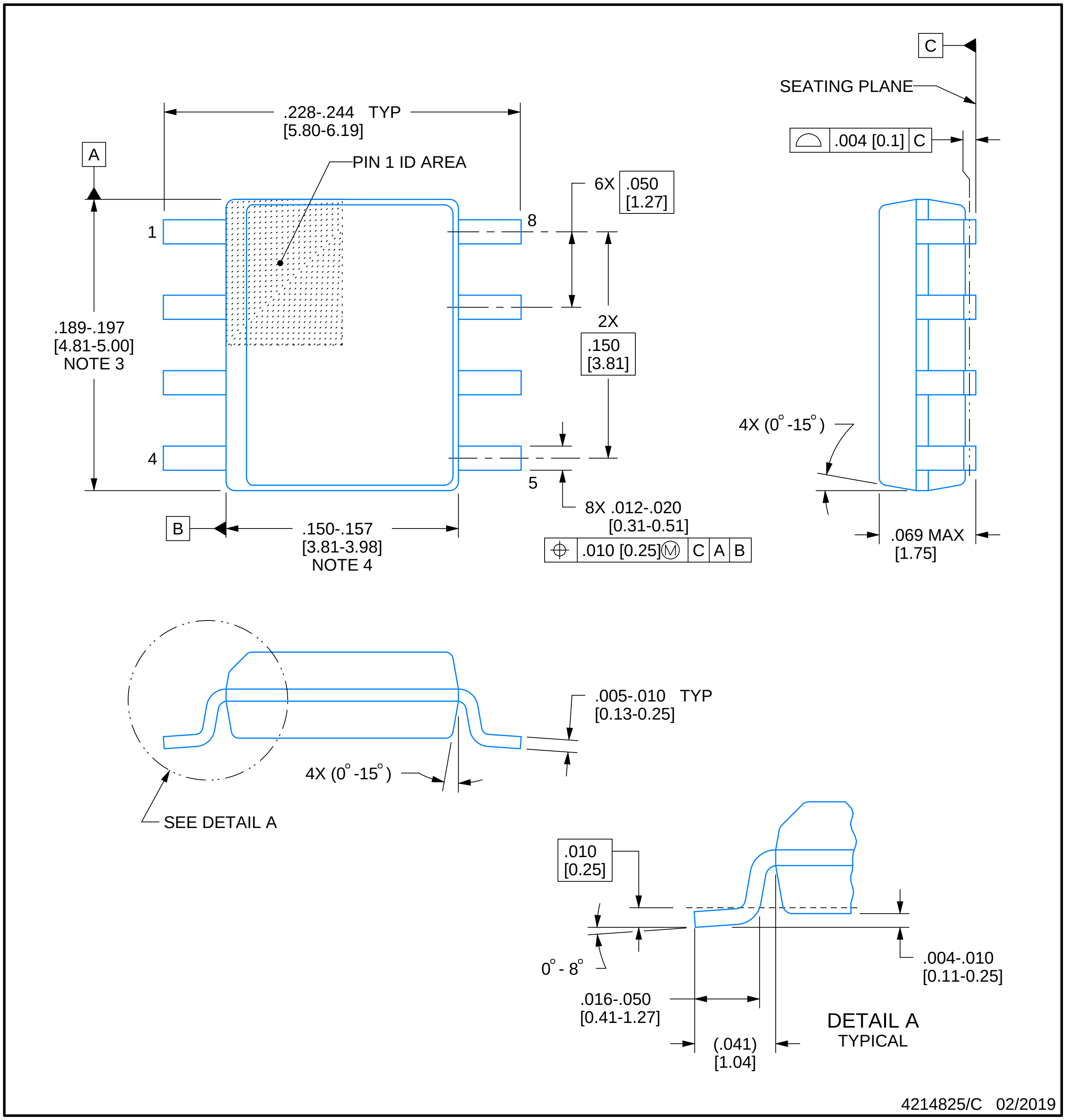


PACKAGE OUTLINE

D0008A

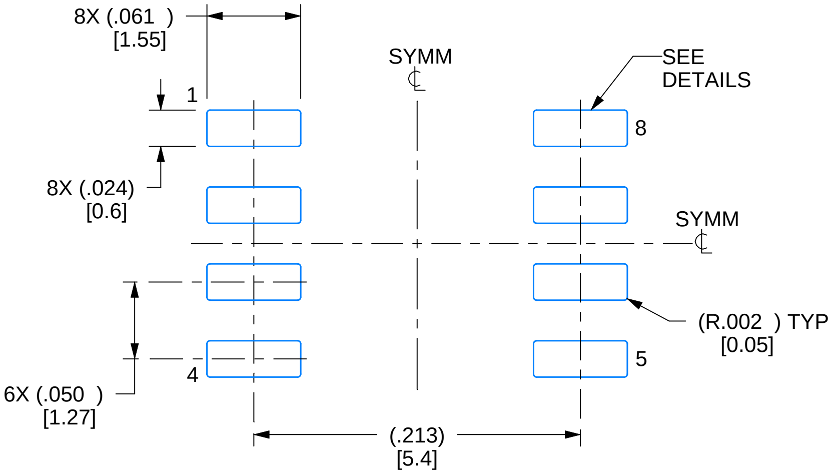
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

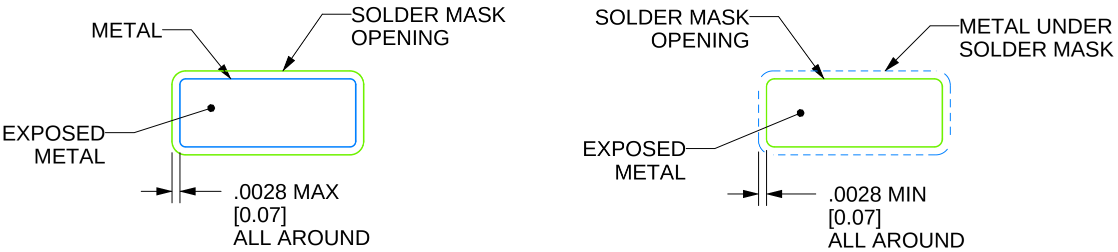


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

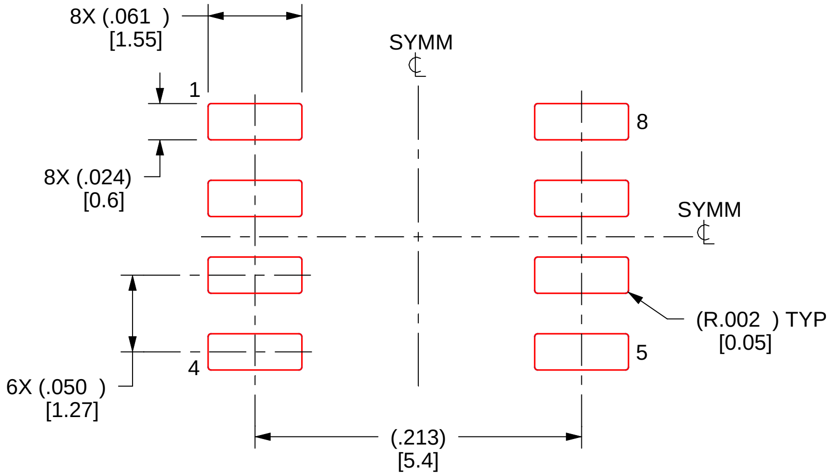
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

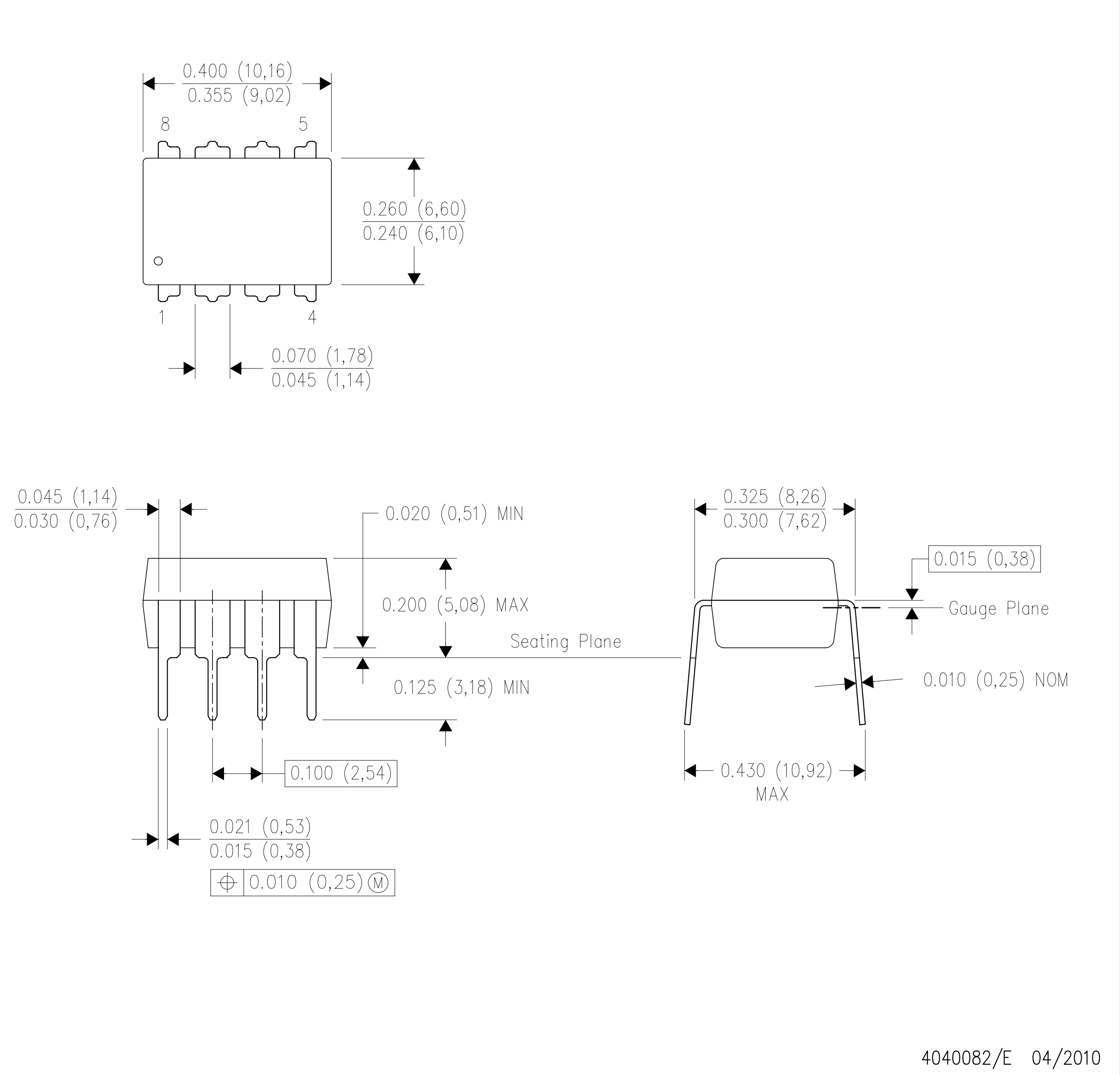


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

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