LMH6572 三通道 2:1 高速视频多路复用器

1 特性

- 350MHz、250mV、−3dB 带宽
- 290MHz、$2V_{PP}$、−3dB 带宽
- 10ns 通道开关时间
- 90dB 通道到通道隔离（在 5MHz 条件下）
- 0.02% 差分增益，0.02° 差分相位
- 0.1dB 增益平坦度：140MHz
- 1400V/µs 压摆率
- 宽电源电压范围：
  6V (±3V) 至 12V (±6V)
- 10MHz 时为 −78dB HD2
- 10MHz 时为 −75dB HD3

2 应用

- RGB 视频路由器
- 多输入视频监控器
- 容错数据开关

3 说明

LMH6572 是一款经过优化的高性能模拟多路复用器，适用于专业级视频应用和其他高保真度、高带宽模拟应用。LMH6572 可在 $2V_{PP}$ 输出信号电平提供 290MHz 带宽。140MHz 的 0.1dB 带宽和 1500V/µs 的压摆率使得该部件适用于高清电视 (HDTV) 和高分辨率多媒体视频 应用。

LMH6572 针对 NTSC 和 PAL 视频信号的差分增益误差和差分相位误差分别为 0.02% 和 0.02°，支持复合视频 应用 ，同时可驱动后部端接的单个 75Ω 负载。LM6572 可提供 80mA 线性输出电流来驱动多个视频负载 应用。

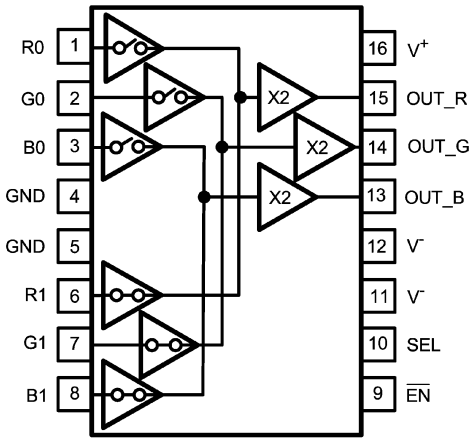
LMH6572 具有 2V/V (+6dBv) 的内部增益，能够以 1V/V (0dBv) 的净增益驱动后部端接传输线。

LMH6572 可提供 SSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMH6572	SSOP (16)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (May 2013) to Revision G **Page**

- 已删除 预览水印 ... 1
- 已添加 *器件信息* 表、*引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- Deleted bolding from Electrical Characteristics specifications, added temperature range to test conditions for clarification 5
- Changed *Overview* title from *General Information* ... 11
- Changed *Layout Considerations* title to *Layout Guidelines* ... 16

Changes from Revision E (April 2013) to Revision F **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 16

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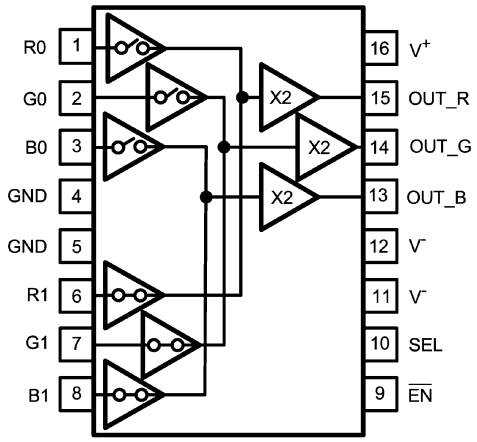
5 Pin Configuration and Functions

DBQ Package
16-Pin SSOP
Top View



Truth Table

SEL	$\overline{EN}$	OUT
0	0	CH 1
1	0	CH 0
X	1	Disable

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6 Specifications

6.1 Absolute Maximum Ratings

see (1)(2)

	MIN	MAX	UNIT
Supply Voltage ($V^+ - V^-$)		13.2	V
I_{OUT}(3)		130	mA
Input Voltage Range		±(V_S)	V
Maximum Junction Temperature(4)		+150	°C
Storage temperature, T_{stg}	–65	+150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations. See the *Power Dissipation* section for more details. A short circuit condition should be limited to 5 seconds or less.
(4) Human Body Model, 1.5 kΩ in series with 100 pF. Machine Model 0 Ω in series with 200 pF.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (1)

		MIN	NOM	MAX	UNIT
	Operating Temperature	–40		85	°C
	Supply Voltage Range	6		12	V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

6.4 Thermal Information

THERMAL METRIC(1)		LMH6572 DBQ (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 ±5V Electrical Characteristics

V_S = ±5 V and R_L = 100 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	–3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		350		MHz
LSBW	–3 dB Bandwidth(2)	V_{OUT} = 2 V_{PP}	250	290		MHz
.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		140		MHz
DG	Differential Gain	R_L = 150 Ω, f = 4.43 MHz		0.02%		
DP	Differential Phase	R_L = 150 Ω, f = 4.43 MHz		0.02		deg
TIME DOMAIN RESPONSE						
TRS	Channel to Channel Switching Time	Logic Transition to 90% Output		10		ns
	Enable and Disable Times	Logic Transition to 90% or 10% Output		11		ns
TRL	Rise and Fall Time	2-V Step		1.5		ns
TSS	Settling Time to 0.05%	2-V Step		17		ns
OS	Overshoot	4-V Step		5%		
SR	Slew Rate(2)	4-V Step	1200	1400		V/µs
DISTORTION						
HD2	2nd Harmonic Distortion	2 V_{PP} , 10 MHz		−78		dBc
HD3	3rd Harmonic Distortion	2 V_{PP} , 10 MHz		−75		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two tones 2 V_{PP} at Output		−80		dBc
EQUIVALENT INPUT NOISE						
VN	Voltage	>1 MHz, Input Referred		5		nV/√Hz
ICN	Current	>1 MHz, Input Referred		5		pA/√Hz
STATIC, DC PERFORMANCE						
GAIN	Voltage Gain			2.0		V/V
	Gain Error(3)	No load, with respect to nominal gain of 2.00 V/V		±0.3%	±0.5%	
		No load, with respect to nominal gain of 2.00 V/V, T_A = –40°C to +85°C		±0.3%	±0.7%	
	Gain Error	R_L = 50 Ω, with respect to nominal gain of 2.00 V/V		0.3%		
VIO	Output Offset Voltage(3)	V_{IN} = 0 V		1	±14	mV
		V_{IN} = 0 V, T_A = –40°C to +85°C		1	±17.5	
DVIO	Average Drift			27		µV/°C
IBN	Input Bias Current(3)(4)	V_{IN} = 0 V		−1.4	±5.0	µA
		V_{IN} = 0 V, T_A = –40°C to +85°C		−1.4	±5.6	
DIBN	Average Drift			7		nA/°C
PSRR	Power Supply Rejection Ratio(3)	DC, Input referred	50	54		dB
		DC, Input referred, T_A = –40°C to +85°C	48	54		
ICC	Supply Current(3)	No load	20	23	25	mA
		No load, T_A = –40°C to +85°C	20	23	28.5	
	Supply Current Disabled(3)	No load		2.0	2.2	mA
		No load, T_A = –40°C to +85°C		2.0	2.3	
VIH	Logic High Threshold(3)	Select and Enable Pins	2.0			V

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See the *Power Dissipation* section for information on temperature de-rating of this device. Minimum and maximum ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
(2) Parameters ensured by design.
(3) Parameters ensured by electrical testing at 25° C.
(4) Positive Value is current into device.

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±5V Electrical Characteristics (continued)

V_S = ±5 V and R_L = 100 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
VIL	Logic Low Threshold(3)	Select and Enable Pins			0.8	V
IiL	Logic Pin Input Current Low(4)	Logic Input = 0 V		−1	±5.0	µA
		Logic Input = 0 V, T_A = –40°C to +85°C		−1	±15	
IiH	Logic Pin Input Current High(4)	Logic Input = 2.0 V	112	150	200	µA
		Logic Input = 2.0 V, T_A = –40°C to +85°C	100	150	210	
MISCELLANEOUS PERFORMANCE						
RF	Internal Feedback and Gain Set Resistor Values		650	800	940	Ω
		T_A = –40°C to +85°C	620	800	1010	
RODIS	Disabled Output Resistance	Internal Feedback and Gain Set Resistors in Series to Ground	1.3	1.6	1.88	kΩ
RIN+	Input Resistance			100		kΩ
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.26		Ω
VO	Output Voltage Range	No Load	±3.83	±3.9		V
		No Load, T_A = –40°C to +85°C	±3.80	±3.9		
VOL		R_L = 100 Ω	±3.52	±3.53		V
		R_L = 100 Ω, T_A = –40°C to +85°C	±3.5	±3.53		
CMIR	Input Voltage Range		±2	±2.5		V
IO	Linear Output Current(3)(4)	V_{IN} = 0 V	+70	±80		mA
		V_{IN} = 0 V, T_A = –40°C to +85°C	40	±80		
ISC	Short Circuit Current(5)	V_{IN} = ±2 V, Output Shorted to Ground		±230		mA
XTLK	Channel to Channel Crosstalk	V_{IN} = 2 V_{PP} at 5 MHz		-90		dBc
XTLK	Channel to Channel Crosstalk	V_{IN} = 2 V_{PP} at 100 MHz		-54		dBc
XTLK	All Hostile Crosstalk	In A, C, Out B, V_{IN} = 2 V_{PP} at 5 MHz		-95		dBc

(5) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations. See the *Power Dissipation* section for more details. A short circuit condition should be limited to 5 seconds or less.

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6.6 ±3.3V Electrical Characteristics

V_S = ±3.3 V, R_L = 100 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		360		MHz
LSBW	−3 dB Bandwidth	V_{OUT} = 2.0 V_{PP}		270		MHz
0.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		80		MHz
GFP	Peaking	DC to 200 MHz		0.3		dB
DG	Differential Gain	R_L = 150 Ω, f = 4.43 MHz		0.02%		
DP	Differential Phase	R_L = 150 Ω, f = 4.43 MHz		0.03		deg
TIME DOMAIN RESPONSE						
TRL	Rise and Fall Time	2-V Step		2.0		ns
TSS	Settling Time to 0.05%	2-V Step		15		ns
OS	Overshoot	2-V Step		5%		
SR	Slew Rate	2-V Step		1000		V/µs
DISTORTION						
HD2	2nd Harmonic Distortion	2 V_{PP}, 10 MHz		−70		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 10 MHz		−74		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two tones 2 V_{PP} at Output		-79		dBc
STATIC, DC PERFORMANCE						
GAIN	Voltage Gain			2.0		V/V
VIO	Output Offset Voltage	V_{IN} = 0 V		1		mV
DVIO	Average Drift			36		µV/°C
IBN	Input Bias Current(2)	V_{IN} = 0 V		2		µA
DIBN	Average Drift			24		nA/°C
PSRR	Power Supply Rejection Ratio	DC, Input Referred		54		dB
ICC	Supply Current	R_L = ∞		20		mA
VIH	Logic High Threshold	Select and Enable Pins			1.3	V
VIL	Logic Low Threshold	Select and Enable Pins	0.4			V
MISCELLANEOUS PERFORMANCE						
RIN+	Input Resistance			100		kΩ
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.27		Ω
VO	Output Voltage Range	No Load		±2.5		V
VOL		R_L = 100 Ω		±2.2		V
CMIR	Input Voltage Range			±1.2		V
IO	Linear Output Current	V_{IN} = 0V		±60		mA
ISC	Short Circuit Current	V_{IN} = ±1V, Output Shorted to Ground		±150		mA
XTLK	Channel to Channel Crosstalk	5 MHz		-90		dBc

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See the *Power Dissipation* section for information on temperature de-rating of this device. Minimum and maximum ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Positive Value is current into device.

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6.7 Typical Characteristics

V_S = ±5 V and R_L = 100 Ω (unless otherwise noted)

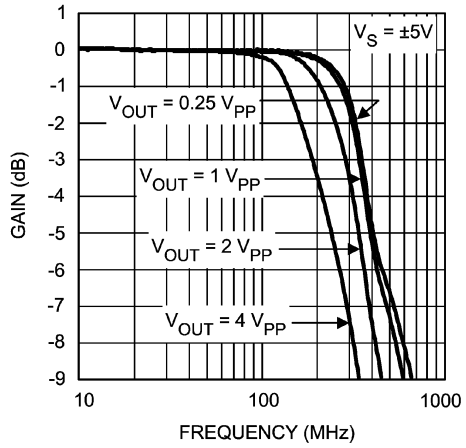

Figure 1. Frequency Response vs V_{OUT}

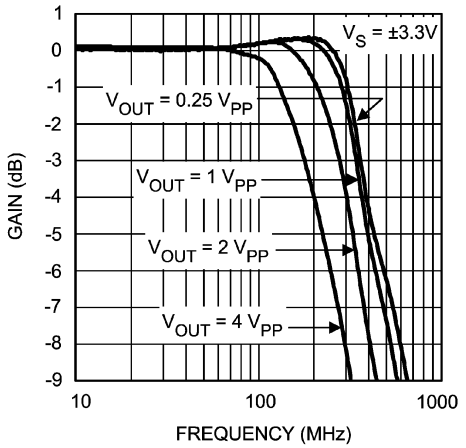

Figure 2. Frequency Response vs V_{OUT}

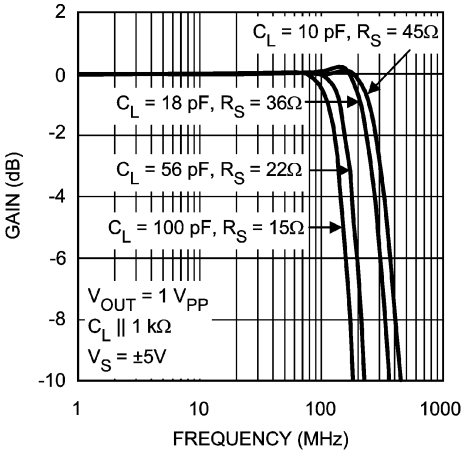

Figure 3. Frequency Response vs Capacitive Load

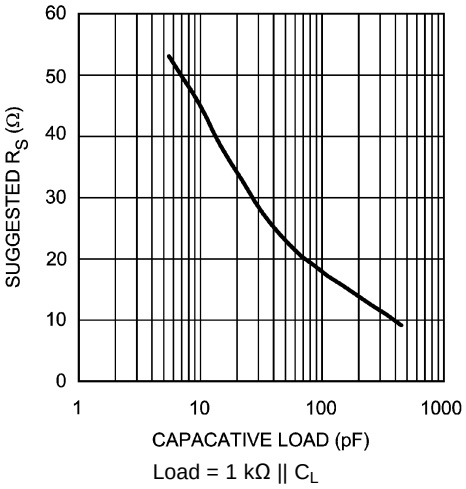

Figure 4. Suggested R_S vs Capacitive Load

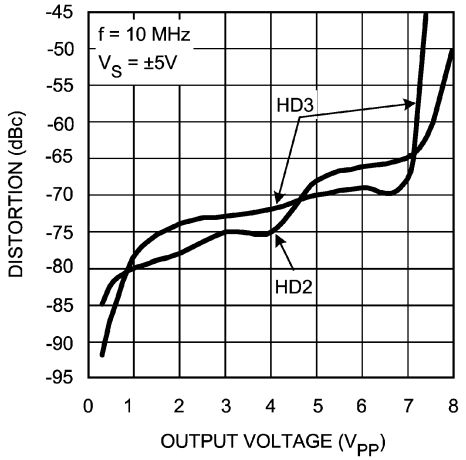

Figure 5. Harmonic Distortion vs Output Voltage

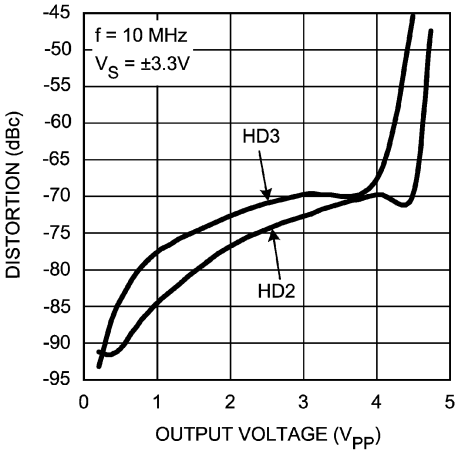

Figure 6. Harmonic Distortion vs Output Voltage

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Typical Characteristics (continued)

V_S = ±5 V and R_L = 100 Ω (unless otherwise noted)

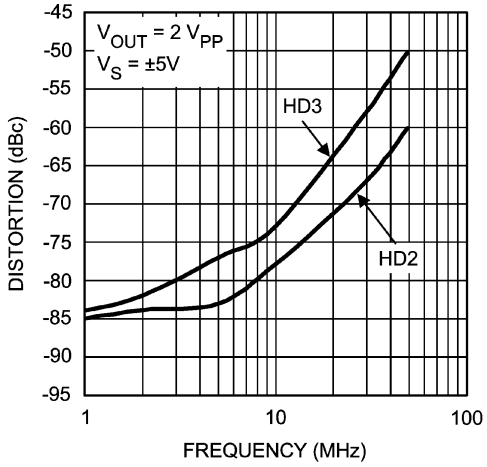

Figure 7. Harmonic Distortion vs Frequency

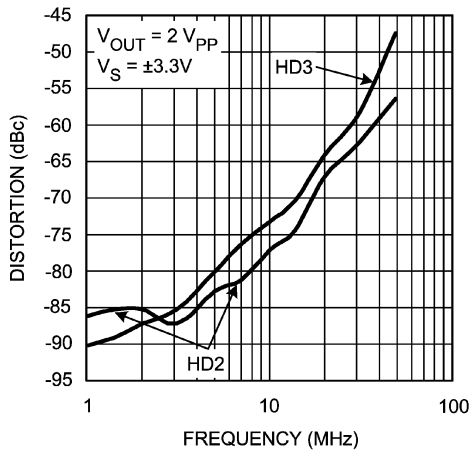

Figure 8. Harmonic Distortion vs Frequency

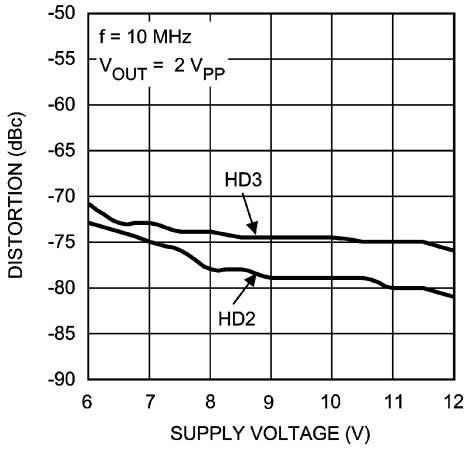

Figure 9. Harmonic Distortion vs Supply Voltage

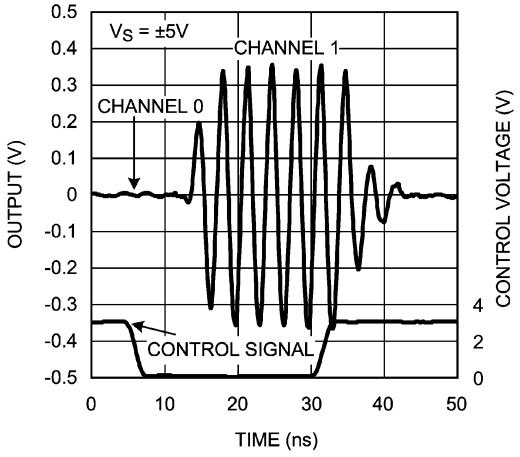

Figure 10. Channel Switching Time

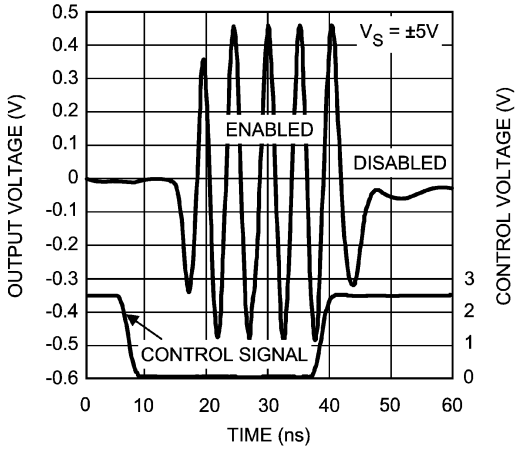

Figure 11. Disable Time

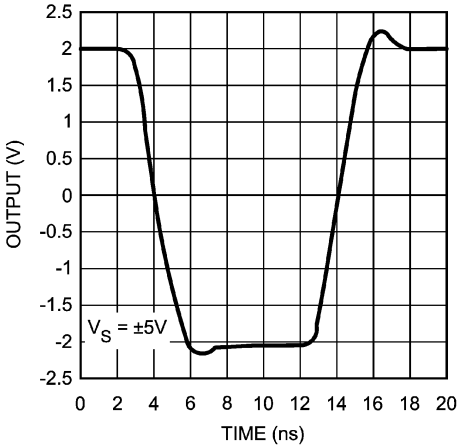

Figure 12. Pulse Response

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Typical Characteristics (continued)

V_S = ±5 V and R_L = 100 Ω (unless otherwise noted)

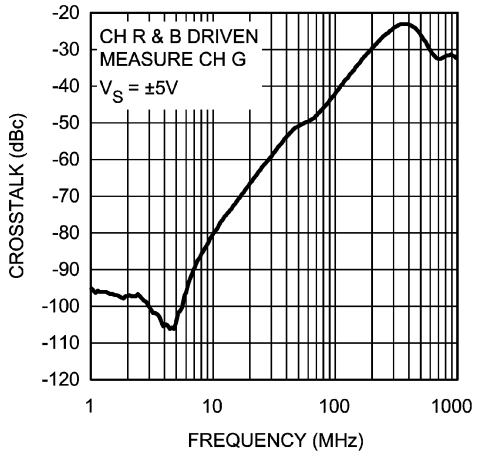

Figure 13. Crosstalk

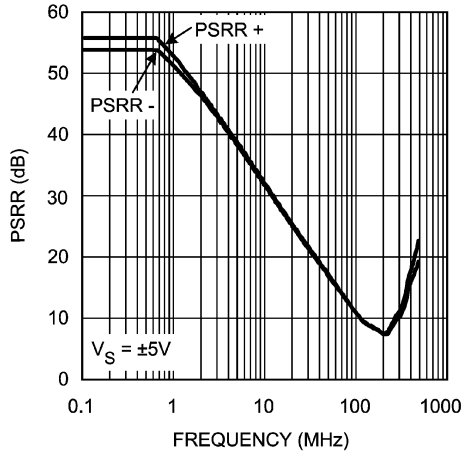

Figure 14. PSRR

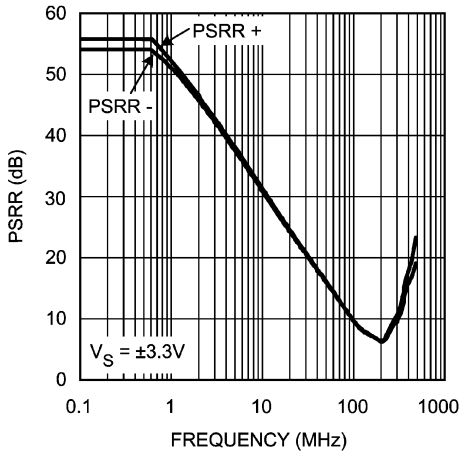

Figure 15. PSRR

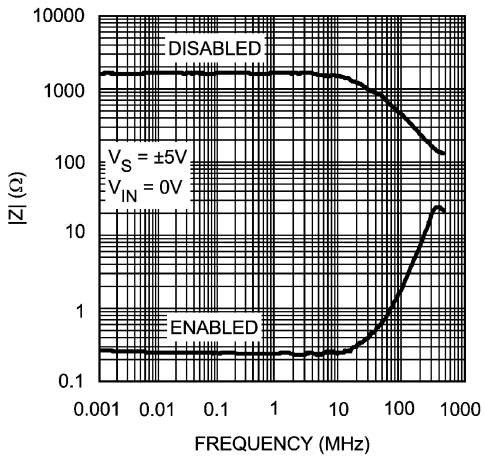

Figure 16. Closed-Loop Output Impedance

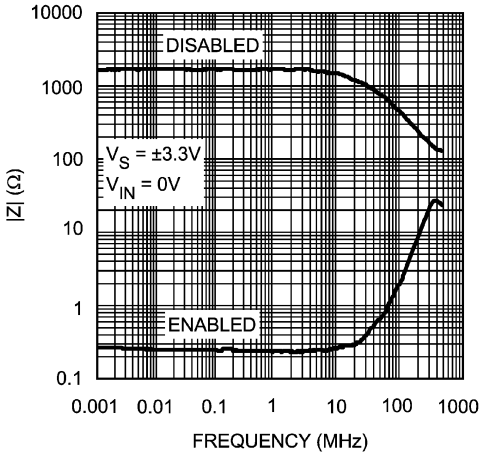

Figure 17. Closed-Loop Output Impedance

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7 Detailed Description

7.1 Overview

The LMH6572 is a high-speed triple 2:1 analog multiplexer, optimized for very high speed and low distortion. With a fixed gain of 2 and excellent AC performance, the LMH6572 is ideally suited for switching high resolution, presentation grade video signals. The LMH6572 has no internal ground reference. Single or split supply configurations are both possible. The LMH6572 features very high speed channel switching and disable times. When disabled the LMH6572 output is high impedance, making multiplexer expansion possible by combining multiple devices.

7.2 Feature Description

7.2.1 Single Supply Operation

The LMH6572 uses mid-supply referenced circuits for the select and disable pins. In order to use the LMH6572 in single supply configuration, it is necessary to use a circuit similar to Figure 19. In this configuration the logical inputs are compatible with high breakdown open collector TTL, or open drain CMOS logic. In addition, the default logic state is reversed since there is a pull-up resistor on those pins. Single supply operation also requires the input to be biased to within the common mode input range of roughly ±2V from the mid-supply point.

7.2.2 Video Performance

The LMH6572 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 18 shows a typical configuration for driving a 75-Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

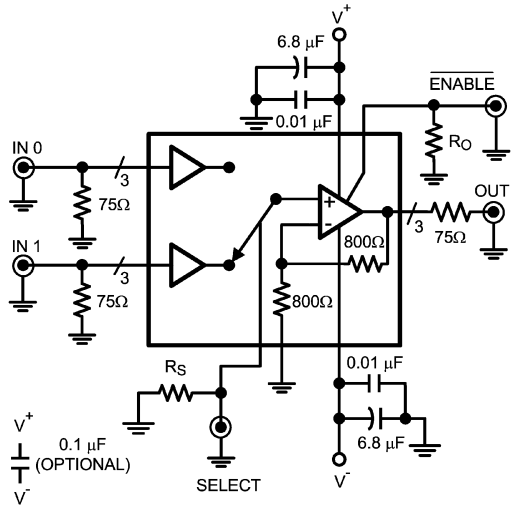

Figure 18. Typical Application

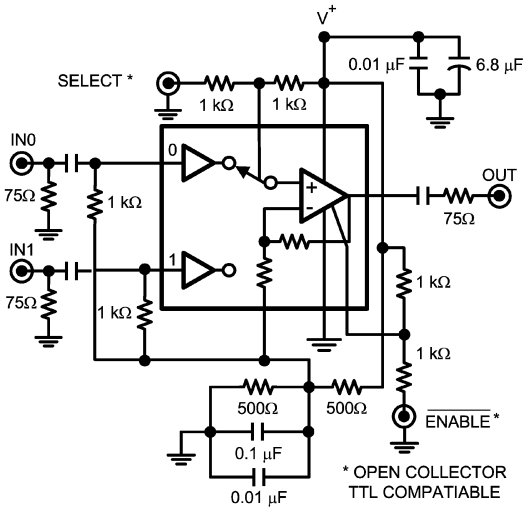

Figure 19. Single Supply Application

7.2.3 Gain Accuracy

The gain accuracy of the LMH6572 is accurate to ±0.5% (0.3% typical) and stable over temperature. The internal gain setting resistors, RF and RG, match very well; however, over process and temperature their absolute value will change.

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Feature Description (continued)

7.2.4 Expanding the Multiplexer

It is possible to build higher density multiplexers by paralleling several LMH6572s. Figure 20 shows a 4:1 RGB MUX using two LMH6572s:

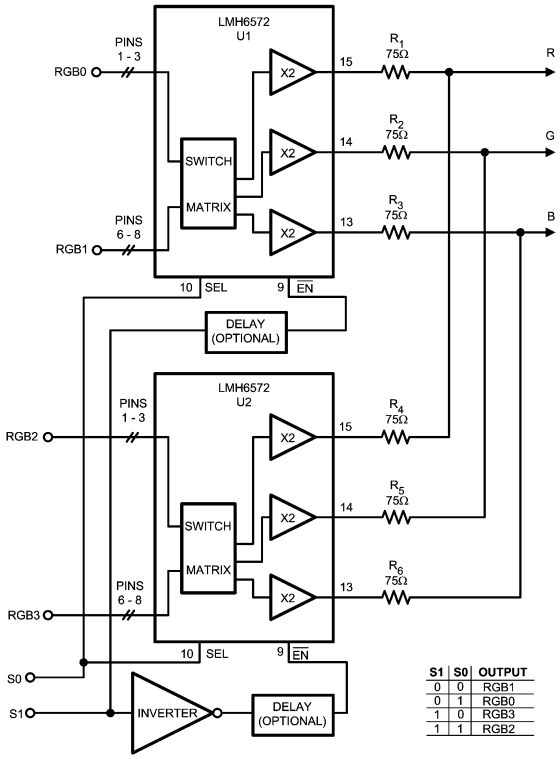

Figure 20. RGB MUX Using Two LMH6572's

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added prior to the $\overline{\text{ENABLE}}$(EN) pin of each device, as shown. Figure 21 shows one possible approach to this delay circuit. The delay circuit shown will delay $\overline{\text{ENABLE}}$'s H to L transitions (R_1 and C_1 decay) but will not delay its L to H transition.

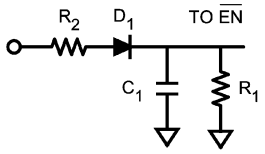

Figure 21. Delay Circuit Implementation

R_2 should be kept small compared to R_1 in order to not reduce the $\overline{\text{ENABLE}}$ voltage and to produce little or no delay to the $\overline{\text{ENABLE}}$ L to H transition.

With the $\overline{\text{ENABLE}}$ pin putting the output stage into a high impedance state, several LMH6572's can be tied together to form a larger input MUX. However, there is a slight loading effect on the active output caused by the off-channel feedback and gain set resistors, as shown in Figure 21. Figure 22 is assuming there are four LMH6572 devices tied together to form a triple 8:1 MUX. With the internal resistors valued at approximately 800Ω, the gain error is about -0.57 dB, or about −6%.

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Feature Description (continued)

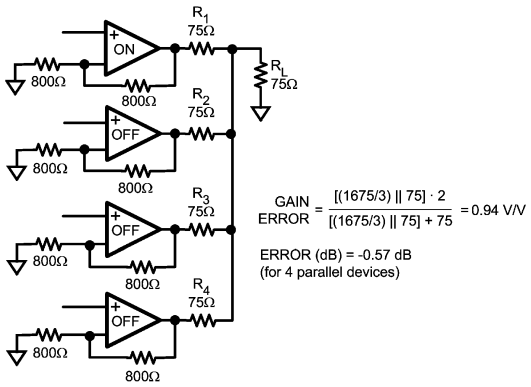

Figure 22. Multiplexer Input Expansion by Combining Outputs

An alternate approach would be to tie the outputs directly together and let all devices share a common back termination resistor in order to alleviate the gain error issue above.

The drawback in this case is the increased capacitive load presented to the output of each LMH6572 due to the offstate capacitance of the LMH6572.

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Feature Description (continued)

7.2.5 Other Applications

The LMH6572 may be utilized in systems that involve a single RGB channel as well whenever there is a need to switch between different “flavors” of a single RGB input.

Here are some examples:

1. RGB positive polarity, negative polarity switch
2. RGB full resolution, high-pass filter switch

In each of these applications, the same RGB input occupies one set of inputs to the LMH6572 and the other “flavor” would be tied to the other input set.

7.2.5.1 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor. Figure 23 shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 24 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

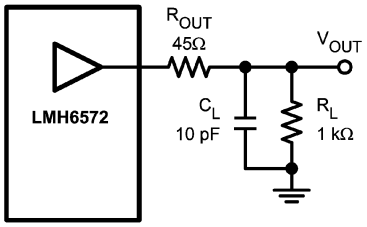

Figure 23. Decoupling Capacitive Loads

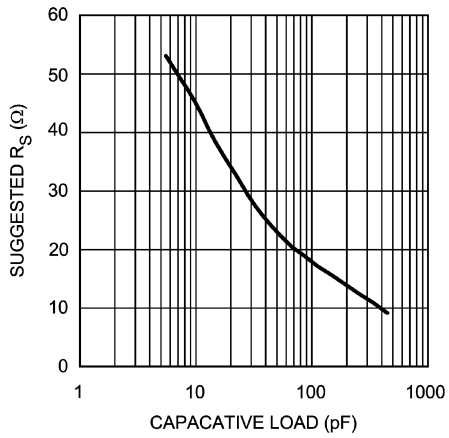

Figure 24. Recommended R_{OUT} vs Capacitive Load

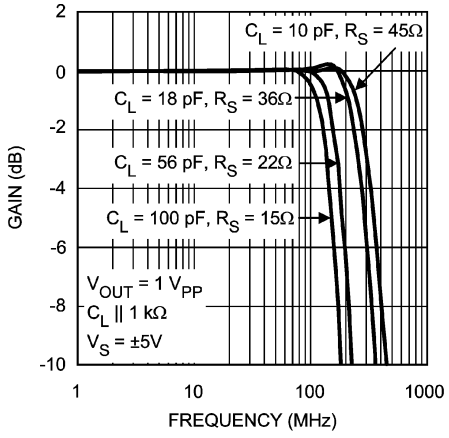

Figure 25. Frequency Response vs Capacitive Load

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8 Power Supply Recommendations

8.1 Power Dissipation

The LMH6572 is optimized for maximum speed and performance in the small form factor of the standard SSOP package. To achieve its high level of performance, the LMH6572 consumes 23 mA of quiescent current, which cannot be neglected when considering the total package power dissipation limit. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6572:

1. Calculate the quiescent (no-load) power:

$$P_{AMP} = I_{CC} * (V_S)$$

where

- $V_S = V^+ - V^-$ (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D \text{ (rms)} = \text{rms } [(V_S - V_{OUT}) * I_{OUT}]$$

where

- V_{OUT} and I_{OUT} are the voltage across and the current through the external load
- V_S is the total supply voltage (2)

3. Calculate the total RMS power:

$$P_T = P_{AMP} + P_D \quad (3)$$

The maximum power that the LMH6572 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150°C - T_{AMB}) / \theta_{JA}$$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SSOP package θ_{JA} is 125 °C/W (4)

8.2 ESD Protection

The LMH6572 is protected against electrostatic discharge (ESD) on all pins. The LMH6572 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6572 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

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9 Layout

9.1 Layout Guidelines

Whenever questions about layout arise, use the LMH730151 evaluation board as a guide. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device; however, the smaller ceramic capacitors should be placed as close to the device as possible. In Figure 18 and Figure 19, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 μF and 0.1 μF ceramic capacitors for each supply bypass.

9.1.1 Evaluation Boards

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LMH6572	SSOP	LMH730151

An evaluation board can be shipped when a device sample request is placed with Texas Instruments.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6572MQ/NOPB	Active	Production	SSOP (DBQ) | 16	95 | TUBE	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ
LMH6572MQ/NOPB.A	Active	Production	SSOP (DBQ) | 16	95 | TUBE	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ
LMH6572MQX/NOPB	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ
LMH6572MQX/NOPB.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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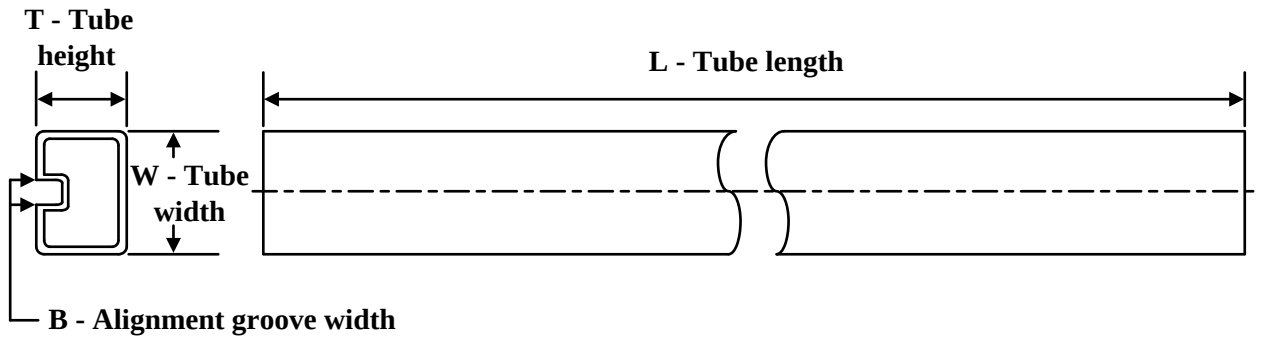
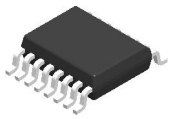


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6572MQ/NOPB	DBQ	SSOP	16	95	495	8	4064	3.05
LMH6572MQ/NOPB.A	DBQ	SSOP	16	95	495	8	4064	3.05

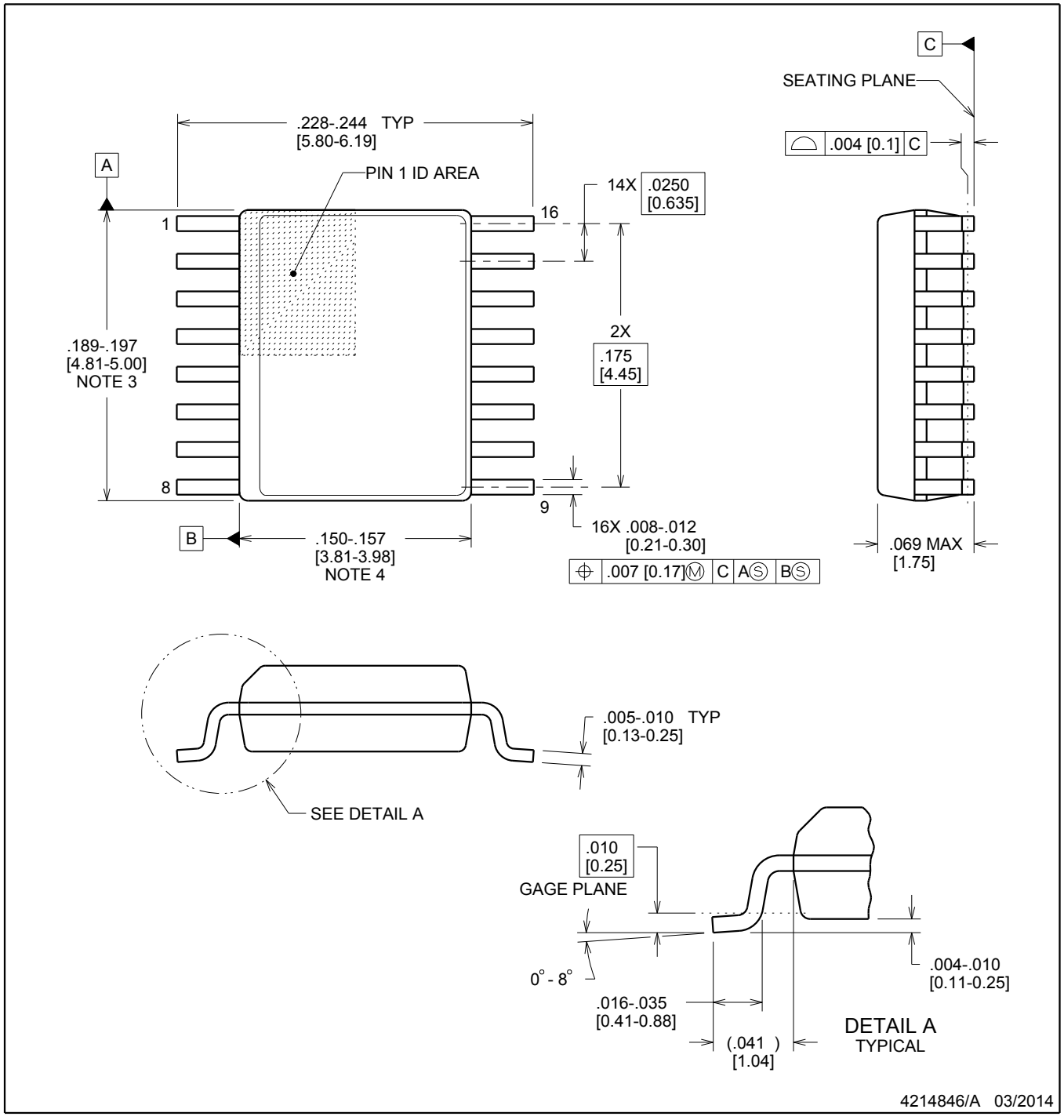


PACKAGE OUTLINE

DBQ0016A

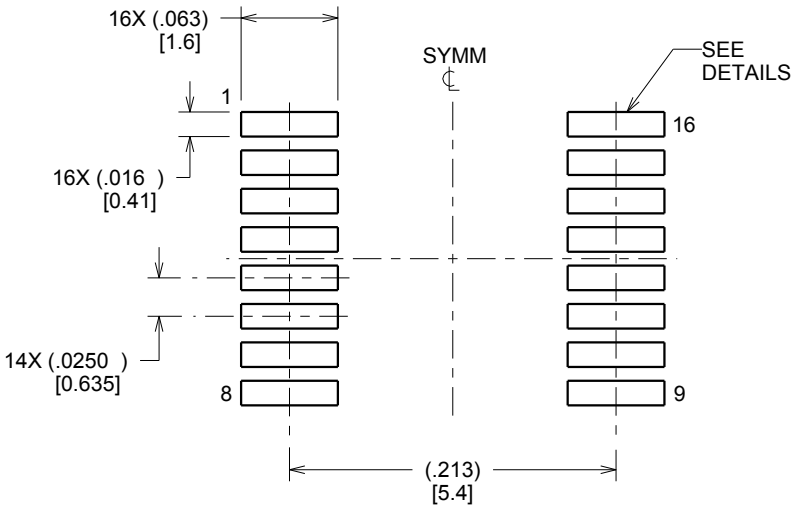
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

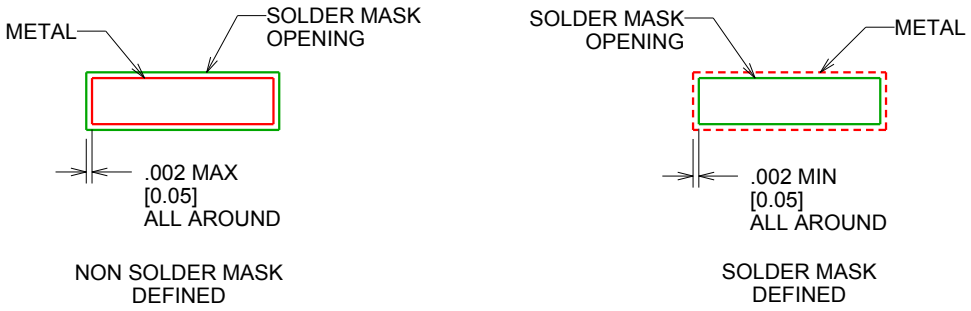


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

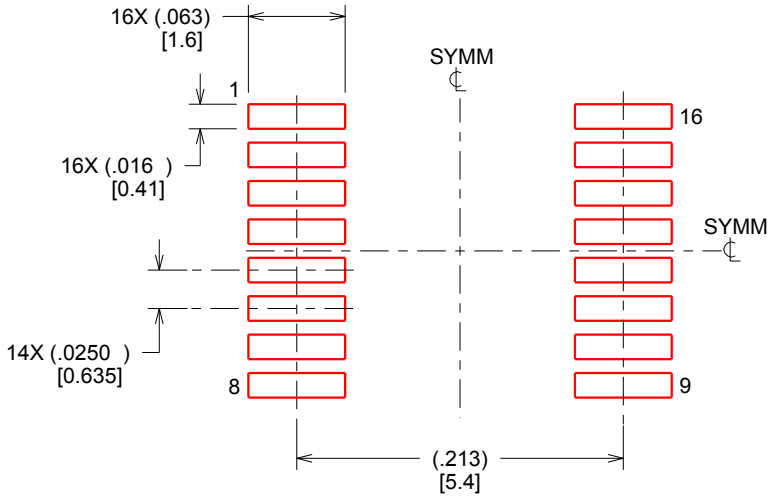
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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