

# 具有通用输入的 LMK00101 超低抖动 LVCMOS 扇出缓冲器/电平转换器

查询样品: [LMK00101](#)

## 特性

- 10 个低电压互补金属氧化物半导体/低压晶体管-晶体管逻辑 (LVCMOS/LVTTL) 输出, DC 达到 **200MHz**
- 通用输入
  - 低电压正射极耦合逻辑 (LVPECL)
  - 低压差分信令 (LVDS)
  - 主机时钟信号电平 (HCSL)
  - 短截线串联端接逻辑 (SSTL)
  - **LVCMOS/LVTTL**
- 晶体振荡器接口
  - 晶振输入频率: **10 至 40MHz**
- 输出偏斜: **6ps**
- 附加相位抖动
  - **156.25MHz (12kHz 至 20MHz)** 时为 **30fs**
- 低传播延迟
- 内核运行电源电压 **3.3V 或 2.5V**
- 可调输出电压
  - 每组 **1.5V, 1.8V, 2.5V 和 3.3V**
- **32 引脚超薄四方扁平无引线封装 (WQFN) 5.0 x 5.0 x 0.8mm**

## 目标应用

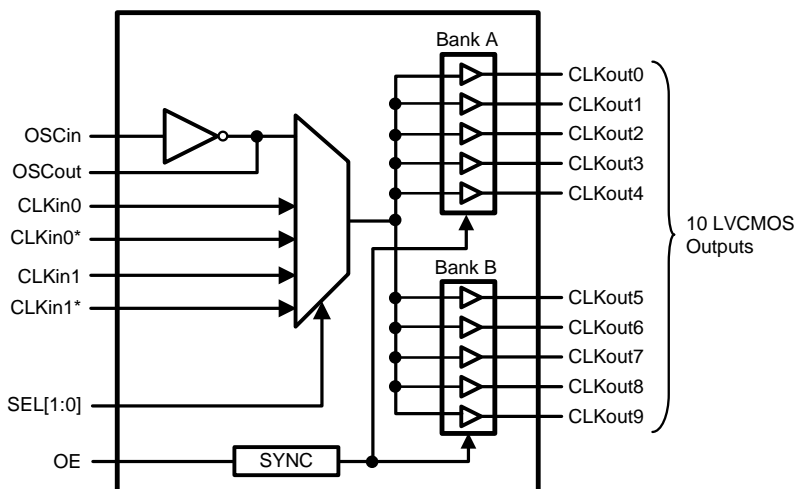
- 针对射频拉远单元 (RRU) 应用的 **LO** 基准分布
- 同步光网络 (SONET), 以太网, 光纤信道线路接口卡
- 光传输网络
- 千兆无源光网络 (GPON) 光线路终端 (OLT) / 光网络单元 (ONU)
- 服务器和存储局域网络互连
- 医疗成像
- 便携式测试和测量
- 高端 A/V

## 说明

LMK00101 是一款高新能、低噪声 LVCMOS 扇出缓冲器, 此缓冲器能够从一个差分、单端或晶振输入中分配 10 个超低抖动时钟。LMK00101 支持针对无毛刺脉冲运行的同步输出使能。超低偏斜、低抖动和高电源抑制比 (PSRR) 使得这个缓冲器非常适合于多种网络互连, 电信, 服务器和存储局域网络互连, RRU LO 基准分布, 医疗和测试设备应用。

内核电压可被设定为 2.5V 或者 3.3V, 而输出电压可被设定为 1.5V, 1.8V, 2.5V 或者 3.3V。可通过引脚编程轻松地对 LMK00101 进行配置。

## Functional Block Diagram



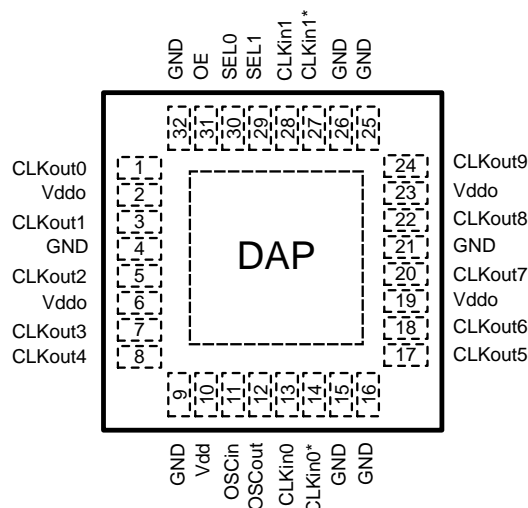
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012–2013, Texas Instruments Incorporated  
English Data Sheet: [SNAS572](#)

## Connection Diagram



**Figure 1. 32-Pin WQFN Package  
(Top down view through device)**

### PIN DESCRIPTIONS

Pin #	Pin Name	Type	Description
DAP	DAP	-	The DAP should be grounded
1	CLKout0	Output	LVC MOS Output
2, 6	Vddo	Power	Power Supply for Bank A (CLKout0 to CLKout4) CLKout pins.
19,23	Vddo	Power	Power Supply for Bank B (CLKout5 to CLKout9) CLKout pins.
3	CLKout1	Output	LVC MOS Output
4,9,15,16, 21,25,26,32	GND	GND	Ground
5	CLKout2	Output	LVC MOS Output
7	CLKout3	Output	LVC MOS Output
8	CLKout4	Output	LVC MOS Output
10	Vdd	Power	Supply for operating core and input buffer
11	OSCin	Input	Input for Crystal
12	OSCout	Output	Output for Crystal
13	CLKin0	Input	Input Pin
14	CLKin0*	Input	Complementary input pin
17	CLKout5	Output	LVC MOS Output
18	CLKout6	Output	LVC MOS Output
20	CLKout7	Output	LVC MOS Output
22	CLKout8	Output	LVC MOS Output
24	CLKout9	Output	LVC MOS Output
27	CLKin1*	Input	Complementary Input Pin
28	CLKin1	Input	Input Pin
29	SEL1	Input	MSB for Input Clock Selection. This pin has an internal pull-down resistor. <sup>(1)</sup>
30	SEL0	Input	LSB for Input Clock Selection. This pin has an internal pull-down resistor. <sup>(1)</sup>
31	OE	Input	Output Enable. This pin has an internal pull-down resistor. <sup>(1)</sup>

(1) CMOS control input with internal pull-down resistor.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)(3)</sup>

Parameter	Symbol	Ratings	Units
Core Supply Voltage	V <sub>dd</sub>	-0.3 to 3.6	V
Output Supply Voltage	V <sub>ddo</sub>	-0.3 to 3.6	V
Input Voltage	V <sub>IN</sub>	-0.3 to V <sub>dd</sub> + 0.3	V
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C
Lead Temperature (solder 4 s)	T <sub>L</sub>	+260	°C
Junction Temperature	T <sub>J</sub>	+125	°C

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) This device is a high performance integrated circuit with ESD handling precautions. Handling of this device should only be done at ESD protected work stations. The device is rated to a HBM-ESD of > 2.5 kV, a MM-ESD of > 250 V, and a CDM-ESD of > 1 kV.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature	T <sub>A</sub>	-40	25	85	°C
Core Supply Voltage	V <sub>dd</sub>	2.375	3.3	3.45	V
Output Supply Voltage <sup>(1)</sup>	V <sub>ddo</sub>	1.425	3.3	V <sub>dd</sub>	V

- (1) V<sub>ddo</sub> should be less than or equal to V<sub>dd</sub> (V<sub>ddo</sub> ≤ V<sub>dd</sub>)

## PACKAGE THERMAL RESISTANCE

### 32-Lead WQFN

Package	Symbols	Ratings	Units
Thermal resistance from junction to ambient on 4-layer JEDEC board <sup>(1)</sup>	θ <sub>JA</sub>	50	°C/W
Thermal resistance from junction to case <sup>(2)</sup>	θ <sub>JC</sub> (DAP)	20	°C/W

- (1) Specification assumes 5 thermal vias connect to die attach pad to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the QFN. For best thermal dissipation it is recommended that the maximum number of vias be used on the board layout.
- (2) Case is defined as the DAP (die attach pad).

## ELECTRICAL CHARACTERISTICS

( $2.375\text{ V} \leq V_{dd} \leq 3.45\text{ V}$ ,  $1.425 \leq V_{ddo} \leq V_{dd}$ ,  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , Differential inputs. Typical values represent most likely parametric norms at  $V_{dd} = V_{ddo} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ , at the Recommended Operation Conditions at the time of product characterization and are not ensured). Test conditions are:  $F_{\text{test}} = 100\text{ MHz}$ , Load =  $5\text{ pF}$  in parallel with  $50\text{ }\Omega$  unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Total Device Characteristics						
Vdd	Core Supply Voltage		2.375	2.5 or 3.3	3.45	V
Vddo	Output Supply Voltage		1.425	1.5, 1.8, 2.5, or 3.3	Vdd	V
I <sub>Vdd</sub>	Core Current	No CLKin		16	25	mA
		V <sub>ddo</sub> = 3.3 V, F <sub>test</sub> = 100 MHz		24		
		V <sub>ddo</sub> = 2.5 V, F <sub>test</sub> = 100 MHz		20		
I <sub>Vddo[n]</sub>	Current for Each Output	V <sub>ddo</sub> = 2.5 V, OE = High, F <sub>test</sub> = 100 MHz		5		mA
		V <sub>ddo</sub> = 3.3 V, OE = High, F <sub>test</sub> = 100 MHz		7		
		OE = Low		0.1		
I <sub>Vdd</sub> + I <sub>Vddo</sub>	Total Device Current with Loads on all outputs	OE = High @ 100 MHz		95		mA
		OE = Low		16		
Power Supply Ripple Rejection (PSRR)						
PSRR	Ripple Induced Phase Spur Level	100 kHz, 100 mVpp Ripple Injected on V <sub>dd</sub> , V <sub>ddo</sub> = 2.5 V		-44		dBc
Outputs <sup>(1)</sup>						
Skew	Output Skew <sup>(2)</sup>	Measured between outputs, referenced to CLKout0		6	25	ps
t <sub>PD</sub>	Propagation Delay CLKin to CLKout <sup>(2)</sup>	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω V <sub>dd</sub> = 3.3 V; V <sub>ddo</sub> = 3.3 V	0.85	1.4	2.2	ns
		C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω V <sub>dd</sub> = 2.5 V; V <sub>ddo</sub> = 1.5 V	1.1	1.8	2.8	ns
t <sub>PD, PP</sub>	Part-to-part Skew <sup>(2) (3)</sup>	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω V <sub>dd</sub> = 3.3 V; V <sub>ddo</sub> = 3.3 V			0.35	ns
		C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω V <sub>dd</sub> = 2.5 V; V <sub>ddo</sub> = 1.5 V			0.6	ns
f <sub>CLKout</sub>	Output Frequency <sup>(4)</sup>		DC		200	MHz
t <sub>Rise</sub>	Rise/Fall Time	V <sub>dd</sub> = 3.3 V, V <sub>ddo</sub> = 1.8 V, C <sub>L</sub> = 10 pF		250		ps
		V <sub>dd</sub> = 2.5 V, V <sub>ddo</sub> = 2.5 V, C <sub>L</sub> = 10 pF		275		
		V <sub>dd</sub> = 3.3 V, V <sub>ddo</sub> = 3.3 V, C <sub>L</sub> = 10 pF		315		
V <sub>CLKoutLow</sub>	Output Low Voltage				0.1	V
V <sub>CLKoutHigh</sub>	Output High Voltage		Vddo-0.1			
R <sub>CLKout</sub>	Output Resistance			50		ohm
t <sub>j</sub>	RMS Additive Jitter	f <sub>CLKout</sub> = 156.25 MHz, CMOS input slew rate ≥ 2 V/ns C <sub>L</sub> = 5 pF, BW = 12 kHz to 20 MHz		30		fs

(1) AC Parameters for CMOS are dependent upon output capacitive loading

(2) Parameter is specified by design, not tested in production.

(3) Part-to-part skew is calculated as the difference between the fastest and slowest  $t_{PD}$  across multiple devices.

(4) Specified by characterization.

## ELECTRICAL CHARACTERISTICS (continued)

( $2.375\text{ V} \leq V_{DD} \leq 3.45\text{ V}$ ,  $1.425 \leq V_{DDO} \leq V_{DD}$ ,  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , Differential inputs. Typical values represent most likely parametric norms at  $V_{DD} = V_{DDO} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ , at the Recommended Operation Conditions at the time of product characterization and are not ensured). Test conditions are:  $F_{\text{test}} = 100\text{ MHz}$ , Load =  $5\text{ pF}$  in parallel with  $50\text{ }\Omega$  unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Digital Inputs (OE, SEL0, SEL1)						
V <sub>Low</sub>	Input Low Voltage	V <sub>dd</sub> = 2.5 V			0.4	V
V <sub>High</sub>	Input High Voltage	V <sub>dd</sub> = 2.5 V	1.3			
		V <sub>dd</sub> = 3.3 V	1.6			
I <sub>IH</sub>	High Level Input Current				50	uA
I <sub>IL</sub>	Low Level Input Current		-5		5	
CLKin0/0* and CLKin1/1* Input Clock Specifications, <sup>(5)</sup> <sup>(6)</sup>						
I <sub>IH</sub>	High Level Input Current	V <sub>CLKin</sub> = V <sub>dd</sub>			20	uA
I <sub>IL</sub>	Low Level Input Current	V <sub>CLKin</sub> = 0 V	-20			uA
V <sub>IH</sub>	Input High Voltage				V <sub>dd</sub>	V
V <sub>IL</sub>	Input Low Voltage		GND			
V <sub>CM</sub>	Differential Input Common Mode Input Voltage <sup>(7)</sup>	V <sub>ID</sub> = 150 mV	0.5		V <sub>dd</sub> -1.2	V
		V <sub>ID</sub> = 350 mV	0.5		V <sub>dd</sub> -1.1	
		V <sub>ID</sub> = 800 mV	0.5		V <sub>dd</sub> -0.9	
V <sub>I_SE</sub>	Single-Ended Input Voltage Swing <sup>(8)</sup>	CLKinX driven single-ended (AC or DC coupled), CLKinX* AC coupled to GND or externally biased within V <sub>CM</sub> range	0.3		2	V <sub>pp</sub>
V <sub>ID</sub>	Differential Input Voltage Swing	CLKin driven differentially	0.15		1.5	V
OSCin/OSCout Pins						
f <sub>OSCin</sub>	Input Frequency <sup>(9)</sup>	Single-Ended Input, OSCout floating	DC		200	MHz
f <sub>XTAL</sub>	Crystal Frequency Input Range	Fundamental Mode Crystal ESR < 200 Ω ( f <sub>Xtal</sub> ≤ 30 MHz ) ESR < 120 Ω ( f <sub>Xtal</sub> > 30 MHz ) <sup>(10)</sup> <sup>(9)</sup>	10		40	MHz
C <sub>OSCin</sub>	Shunt Capacitance			1		pF
V <sub>IH</sub>	Input High Voltage	Single-Ended Input, OSCout floating			2.5	V

(5) See [Differential Voltage Measurement Terminology](#) for definition of  $V_{\text{ID}}$  and  $V_{\text{OD}}$ .

(6) Refer to application note *AN-912 Common Data Transmission Parameters and their Definitions* (literature number [SNLA036](#)) for more information.

(7) When using differential signals with  $V_{\text{CM}}$  outside of the acceptable range for the specified  $V_{\text{ID}}$ , the clock must be AC coupled.

(8) Parameter is specified by design, not tested in production.

(9) Specified by characterization.

(10) The ESR requirements stated are what is necessary in order to ensure that the Oscillator circuitry has no start up issues. However, lower ESR values for the crystal might be necessary in order to stay below the maximum power dissipation requirements for that crystal.

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified:  $V_{dd} = V_{ddo} = 3.3\text{ V}$ ,  $T_A = 20\text{ }^{\circ}\text{C}$ ,  $C_L = 5\text{ pF}$ , CLKIn driven differentially, input slew rate  $\geq 2\text{ V/ns}$ .

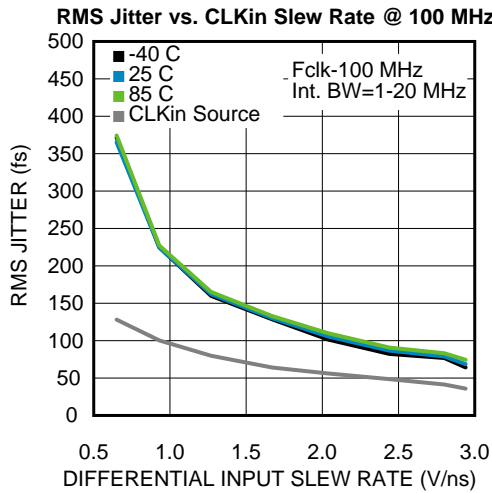


Figure 2.

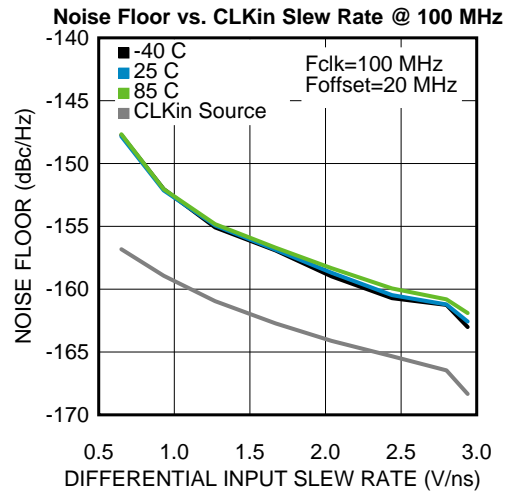
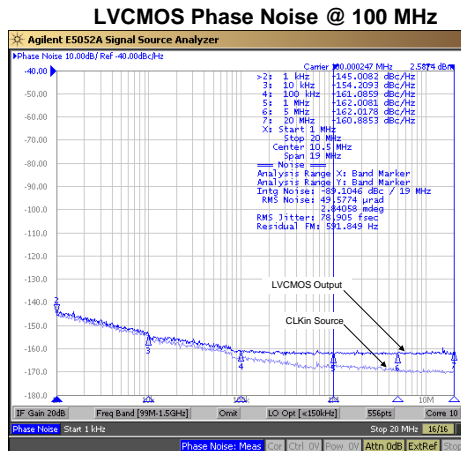


Figure 3.



Test conditions: LVC MOS Input, slew rate  $\geq 2\text{ V/ns}$ ,  $C_L = 5\text{ pF}$  in parallel with  $50\text{ }\Omega$ , BW = 1 MHz to 20 MHz

Figure 4.

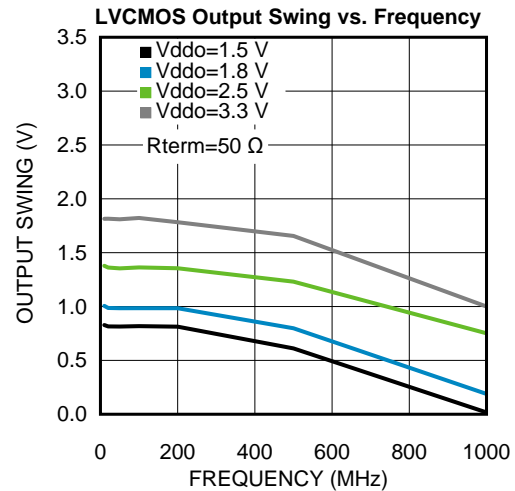


Figure 5.

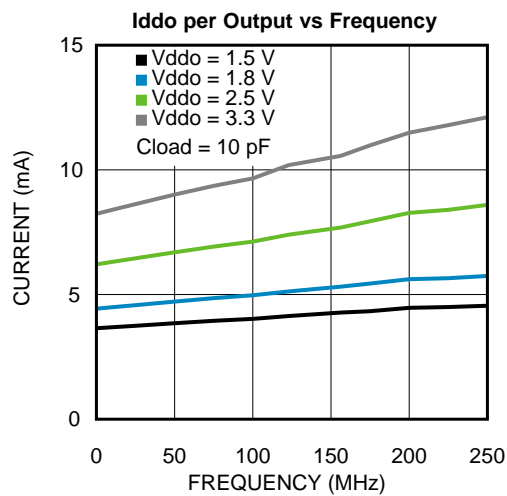


Figure 6.

## MEASUREMENT DEFINITIONS

### Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically  $V_{ID}$  or  $V_{OD}$  depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is  $V_{SS}$  and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair.  $V_{SS}$  can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of  $V_{OD}$  as described in the first section

Figure 7 illustrates the two different definitions side-by-side for inputs and Figure 8 illustrates the two different definitions side-by-side for outputs. The  $V_{ID}$  and  $V_{OD}$  definitions show  $V_A$  and  $V_B$  DC levels that the non-inverting and inverting signals toggle between with respect to ground.  $V_{SS}$  input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

$V_{ID}$  and  $V_{OD}$  are often defined in volts (V) and  $V_{SS}$  is often defined as volts peak-to-peak ( $V_{PP}$ ).

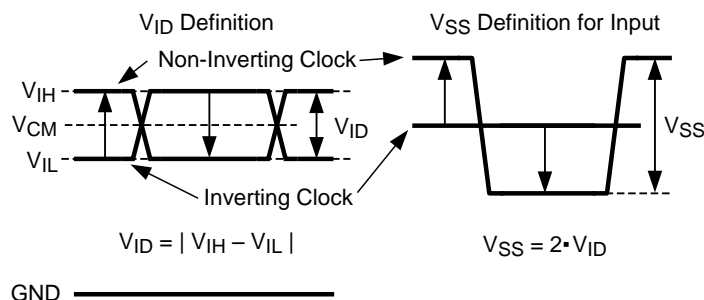


Figure 7. Two Different Definitions for Differential Input Signals

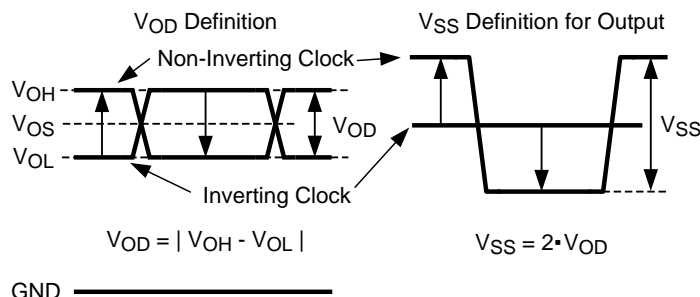


Figure 8. Two Different Definitions for Differential Output Signals

## FUNCTIONAL DESCRIPTION

The LMK00101 is a 10 output LVCMOS clock fanout buffer with low additive jitter that can operate up to 200 MHz. It features a 3:1 input multiplexer with a crystal oscillator input, single supply or dual supply (lower power) operation, and pin-programmable device configuration. The device is offered in a 32-pin WQFN package.

### $V_{dd}$ and $V_{ddo}$ Power Supplies

Separate core and output supplies allow the output buffers to operate at the same supply as the  $V_{dd}$  core supply (3.3 V or 2.5 V) or from a lower supply voltage (3.3 V, 2.5 V, 1.8 V, or 1.5 V). Compared to single-supply operation, dual supply operation enables lower power consumption and output-level compatibility.

Bank A (CLKout0 to CLKout4) and Bank B (CLKout5 to CLKout9) may also be operated at different  $V_{ddo}$  voltages, provided neither  $V_{ddo}$  voltage exceeds  $V_{dd}$ .

#### NOTE

Care should be taken to ensure the  $V_{ddo}$  voltage does not exceed the  $V_{dd}$  voltage to prevent turning-on the internal ESD protection circuitry.

**DO NOT DISCONNECT OR GROUND ANY OF THE  $V_{ddo}$  PINS** as the  $V_{ddo}$  pins are internally connected within an output bank.

## CLOCK INPUTS

The LMK00101 has three different inputs, CLKin0/CLKin0\*, CLKin1/CLKin1\*, and OSCin that can be driven in different manners that are described in the following sections.

### SELECTION OF CLOCK INPUT

Clock input selection is controlled using the SEL0 and SEL1 pins as shown in [Table 1](#). Refer to [Driving the Clock Inputs](#) for clock input requirements. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator will start-up and its clock will be distributed to all outputs. Refer to [Crystal Interface](#) for more information. Alternatively, OSCin may be driven by a single ended clock, up to 200 MHz, instead of a crystal.

**Table 1. Input Selection**

SEL1	SEL0	Input
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin (Crystal Mode)

### CLKin/CLKin\* Pins

The LMK00101 has two differential inputs (CLKin0/CLKin0\* and CLKin1/CLKin1\*) that can be driven single-ended or differentially. They can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, or other differential and singled ended signals that meet the input requirements under the “CLKin0/0\* and CLKin1/1\* Input Clock Specifications” portion of the [ELECTRICAL CHARACTERISTICS](#) and <sup>(1)</sup>. Refer to [Driving the Clock Inputs](#) for more details on driving the LMK00101 inputs.

In the event that a Crystal mode is not selected and the CLKin pins do not have an AC signal applied to them, [Table 2](#) following will be the state of the outputs.

(1) When using differential signals with  $V_{CM}$  outside of the acceptable range for the specified  $V_{ID}$ , the clock must be AC coupled.



**Table 2. CLKInX Input vs. Output States**

CLKInX	CLKInX*	Output State
Open	Open	Logic Low
Logic Low	Logic Low	Logic Low
Logic High	Logic Low	Logic High
Logic Low	Logic High	Logic Low

### OSCIn/OSCOut Pins

The LMK00101 has a crystal oscillator which will be powered up when OSCIn is selected. Alternatively, OSCIn may be driven by a single ended clock, up to 200 MHz, instead of a crystal. Refer to [Crystal Interface](#) for more information.

If Crystal mode is selected and the pins do not have an AC signal applied to them, [Table 3](#) will be the state of the outputs. If Crystal mode is selected an open state is not allowed on OSCIn, as the outputs may oscillate due to the crystal oscillator circuitry.

**Table 3. OSCIn Input vs. Output States**

OSCIn	Output State
Open	Not Allowed
Logic Low	Logic High
Logic High	Logic Low

## CLOCK OUTPUTS

The LMK00101 has 10 LVCMOS outputs.

### Output Enable Pin

When the output enable pin is held High, the outputs are enabled. When it is held Low, the outputs are held in a Low state as shown in [Table 4](#).

**Table 4. Output Enable Pin States**

OE	Outputs
Low	Disabled (Hi-Z)
High	Enabled

The OE pin is synchronized to the input clock to ensure that there are no runt pulses. When OE is changed from Low to High, the outputs will initially have an impedance of about 400  $\Omega$  to ground until the second falling edge of the input clock. Starting with the second falling edge of the input clock, the outputs will buffer the input. If the OE pin is taken from Low to High when there is no input clock present, the outputs will either go High or Low and stay at that state; they will not oscillate. When the OE pin is taken from High to Low the outputs will become Low after the second falling edge of the clock input and then will go to a Disabled (Hi-Z) state starting after the next rising edge.

### Using Less than Ten Outputs

Although the LMK00101 has 10 outputs, not all applications will require all of these. In this case, the unused outputs should be left floating with a minimum copper length to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

#### NOTE

For best soldering practices, the minimum trace length should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

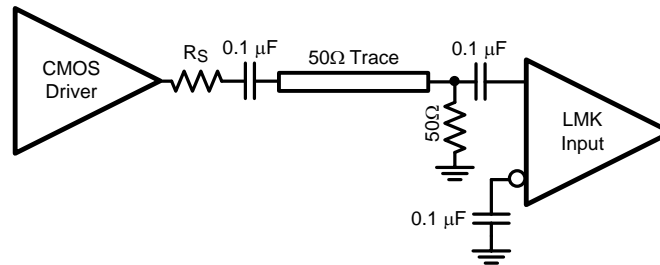
## APPLICATION INFORMATION

### Driving the Clock Inputs

The LMK00101 has two differential inputs (CLKin0/CLKin0\* and CLKin1/CLKin1\*) that can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, and other differential and single ended signals that meet the input requirements specified in [ELECTRICAL CHARACTERISTICS](#). The device can accept a wide range of signals due to its wide input common mode voltage range ( $V_{CM}$ ) and input voltage swing ( $V_{ID}$ )/dynamic range. AC coupling may also be employed to shift the input signal to within the  $V_{CM}$  range.

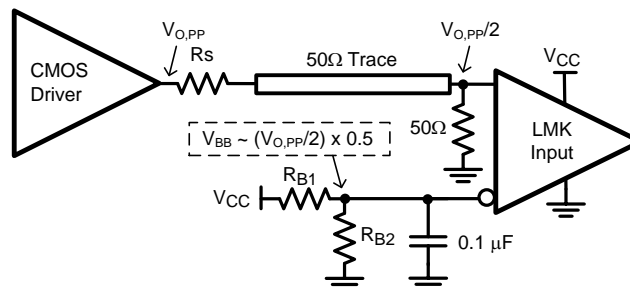
To achieve the best possible phase noise and jitter performance, it is recommended that the input have a high slew rate of 2 V/ns(differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential input signal is recommended over single-ended because it typically provides higher slew rate and common-mode noise rejection.

While it is recommended to drive the CLKin/CLKin\* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the [Electrical Characteristics](#). For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, a 50  $\Omega$  load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in [Figure 9](#). The output impedance of the LVCMOS driver plus  $R_S$  should be close to 50  $\Omega$  to match the characteristic impedance of the transmission line and load termination.



**Figure 9. Preferred Configuration: Single-Ended LVCMOS Input, AC Coupling, Near and Far End Termination**

A single-ended clock may also be DC coupled to CLKinX as shown in [Figure 10](#). A 50- $\Omega$  load resistor should be placed near the CLKinX input for signal attenuation and line termination. Because half of the single-ended swing of the driver ( $V_{O,PP} / 2$ ) drives CLKinX, CLKinX\* should be externally biased to the midpoint voltage of the attenuated input swing ( $(V_{O,PP} / 2) \times 0.5$ ). The external bias voltage should be within the specified input common voltage ( $V_{CM}$ ) range. This can be achieved using external biasing resistors in the k $\Omega$  range ( $R_{B1}$  and  $R_{B2}$ ) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.



**Figure 10. Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing**

If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with a single-ended external clock as shown in Figure 11. The input clock should be AC coupled to the OSCin pin, which has an internally generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either differential input (CLKinX) since it offers higher operating frequency, better common mode, improved power supply noise rejection, and greater performance over supply voltage and temperature variations.

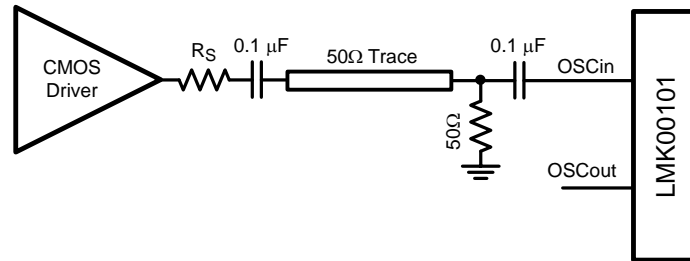


Figure 11. Driving OSCin with a Single-Ended External Clock

## Crystal Interface

The LMK00101 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in Figure 12.

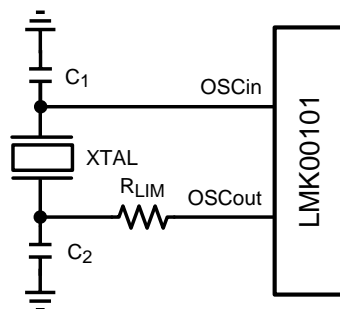


Figure 12. Crystal Interface

The load capacitance ( $C_L$ ) is specific to the crystal, but usually on the order of 18 to 20 pF. While  $C_L$  is specified for the crystal, the OSCin input capacitance ( $C_{IN} = 1$  pF typical) of the device and PCB stray capacitance ( $C_{STRAY} \sim 1$  to 3 pF) can affect the discrete load capacitor values,  $C_1$  and  $C_2$ . For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically,  $C_1 = C_2$  for optimum symmetry, so Equation 1 can be rewritten in terms of  $C_1$  only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for  $C_1$ :

$$C_1 = (C_L - C_{IN} - C_{STRAY}) * 2 \quad (3)$$

**ELECTRICAL CHARACTERISTICS** provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal,  $P_{XTAL}$ , can be computed by:

$$P_{XTAL} = I_{RMS}^2 * R_{ESR} * (1 + C_0 / C_L)^2$$

Where:

- $I_{RMS}$  is the RMS current through the crystal.
- $R_{ESR}$  is the maximum equivalent series resistance specified for the crystal.
- $C_L$  is the load capacitance specified for the crystal.
- $C_0$  is the minimum shunt capacitance specified for the crystal.

(4)

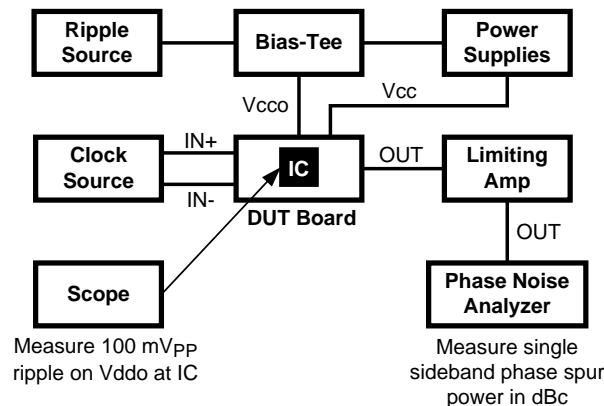
$I_{RMS}$  can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in Figure 12, an external resistor,  $R_{LIM}$ , can be used to limit the crystal drive level if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with  $R_{LIM}$  shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with  $R_{LIM}$  shorted, then a zero value for  $R_{LIM}$  can be used. As a starting point, a suggested value for  $R_{LIM}$  is 1.5 k $\Omega$ .

## Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, etc. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00101, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the singleside band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00101, power supply ripple rejection (PSRR), was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the  $V_{ddo}$  supply. The PSRR test setup is shown in Figure 13.



**Figure 13. PSRR Test Setup**

A signal generator was used to inject a sinusoidal signal onto the  $V_{ddo}$  supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the  $V_{ddo}$  pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 100 MHz under the following power supply ripple conditions:

- Ripple amplitude: 100 mVpp on  $V_{ddo} = 2.5$  V
- Ripple frequency: 100 kHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$DJ \text{ (ps pk-pk)} = [(2 * 10^{(PSRR/20)}) / (\pi * f_{clk})] * 10^{12} \quad (5)$$

## Power Supply Bypassing

The  $V_{dd}$  and  $V_{ddo}$  power supplies should have a high frequency bypass capacitor, such as 100 pF, placed very close to each supply pin. Placing the bypass capacitors on the same layer as the LMK00101 improves input sensitivity and performance. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

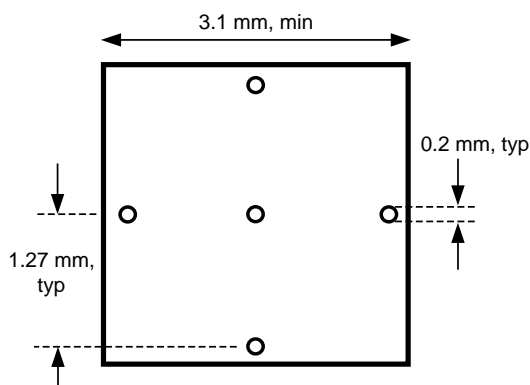
## Thermal Management

For reliability and performance reasons the die temperature should be limited to a maximum of 125 °C. That is, as an estimate,  $T_A$  (ambient temperature) plus device power consumption times  $\theta_{JA}$  should not exceed 125 °C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in Figure 14. More information on soldering WQFN (formerly referred to as LLP) packages and gerber footprints can be obtained: <http://www.ti.com/packaging>

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in Figure 14 should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.



**Figure 14. Recommended Land and Via Pattern**

## REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Deleted optional from CLKIn1* pin description. Changed complimentary to complementary. ....	2
• Added <i>not tested in production</i> to <i>specified by design</i> table note. ....	4
• Added max limit to Output Skew parameter and added tablenote to parameter in Electrical Characteristics Table. ....	4
• Changed typical value for both conditions of Propagation Delay in the Electrical Characteristics Table ....	4
• Added Min/Max limits to both conditions of Propagation Delay parameter in Electrical Characteristics Table. ....	4
• Changed both Max values of each Part-to-part Skew condition in Electrical Characteristics Table. ....	4
• Changed unit value for the first condition of Part-to-part Skew from ps to ns in the Electrical Characteristics Table. ....	4
• Changed the Typ value of each Rise/Fall Time condition in the Electrical Characteristics Table ....	4
• Added <i>not tested in production</i> to <i>specified by design</i> table note. ....	5
• Deleted VIL table note. ....	5
• Added $V_{LSE}$ parameter and spec limits with corresponding table note to Electrical Characteristics Table. ....	5
• Changed third paragraph in Driving the Clock Inputs section to include CLKIn* and LVCMOS text. Removed extra references to other figures. Revised to better correspond with information in Electrical Characteristics Table. ....	10
• Deleted Figure 10 ( <i>Near End termination</i> ) and Figure 11 ( <i>Far End termination</i> ) from <i>Driving the Clock Inputs</i> section ...	10
• Changed bypass cap text with signal attenuation text in fourth paragraph of <i>Driving the Clock Inputs</i> . ....	10
• Changed <i>Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing</i> image with revised graphic. ....	10
• Deleted two sentences in reference to two deleted images. ....	11

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMK00101SQ/NOPB</a>	Active	Production	WQFN (RTV)   32	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00101
LMK00101SQ/NOPB.A	Active	Production	WQFN (RTV)   32	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00101
<a href="#">LMK00101SQE/NOPB</a>	Active	Production	WQFN (RTV)   32	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00101
LMK00101SQE/NOPB.A	Active	Production	WQFN (RTV)   32	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00101
<a href="#">LMK00101SQX/NOPB</a>	Active	Production	WQFN (RTV)   32	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00101
LMK00101SQX/NOPB.A	Active	Production	WQFN (RTV)   32	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00101

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00101SQ/NOPB	WQFN	RTV	32	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMK00101SQE/NOPB	WQFN	RTV	32	250	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMK00101SQX/NOPB	WQFN	RTV	32	2500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

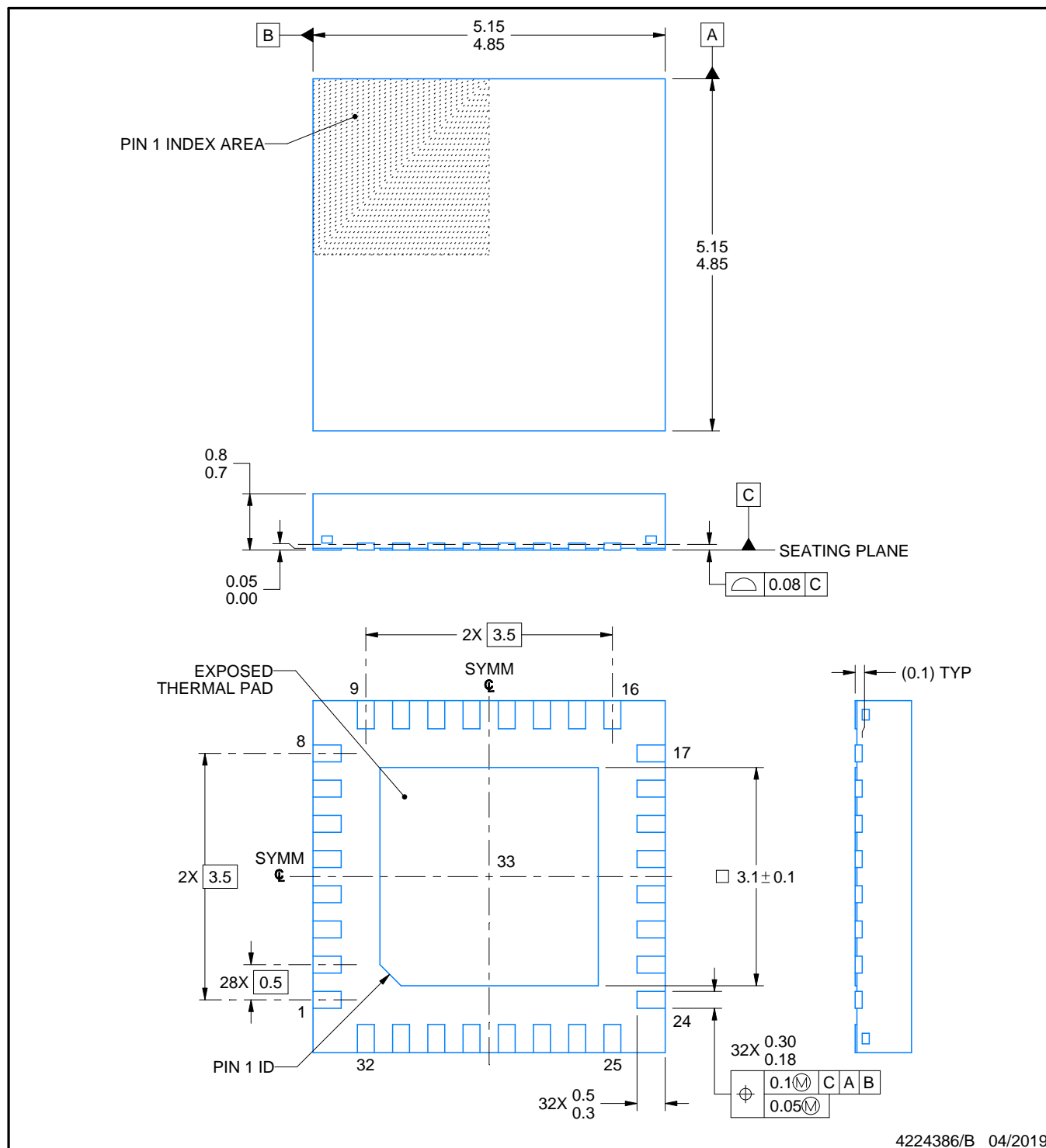
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00101SQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
LMK00101SQE/NOPB	WQFN	RTV	32	250	208.0	191.0	35.0
LMK00101SQX/NOPB	WQFN	RTV	32	2500	356.0	356.0	35.0



## PACKAGE OUTLINE

### WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

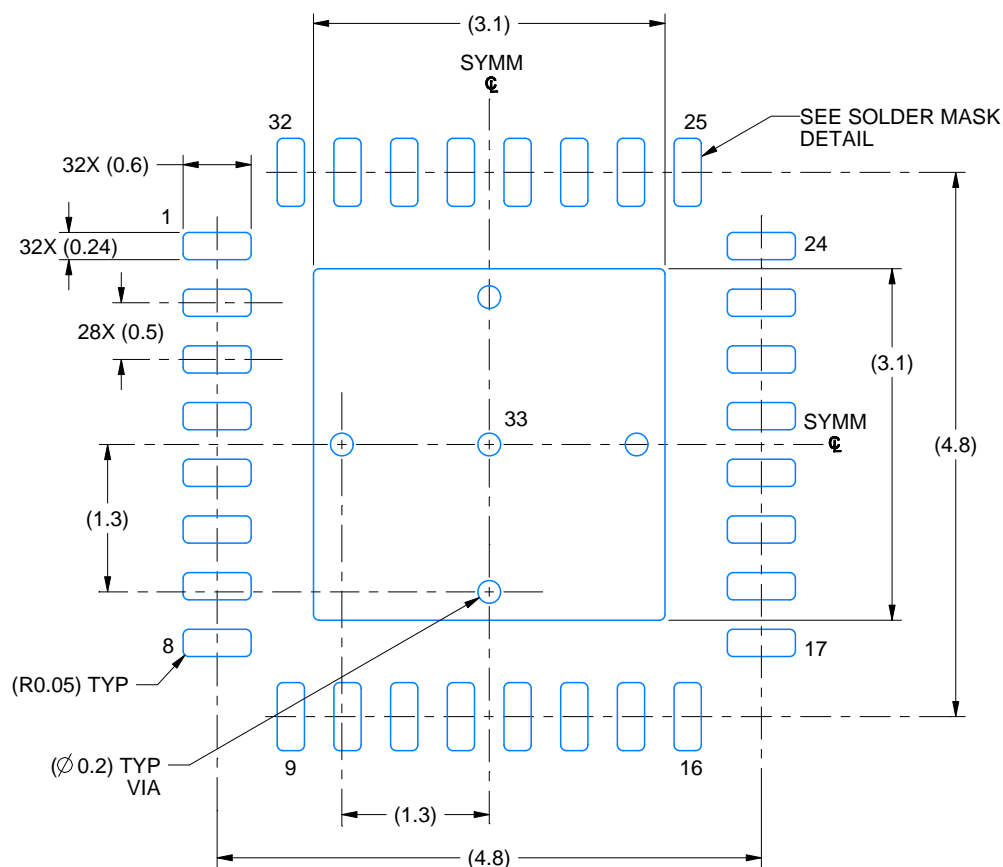
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

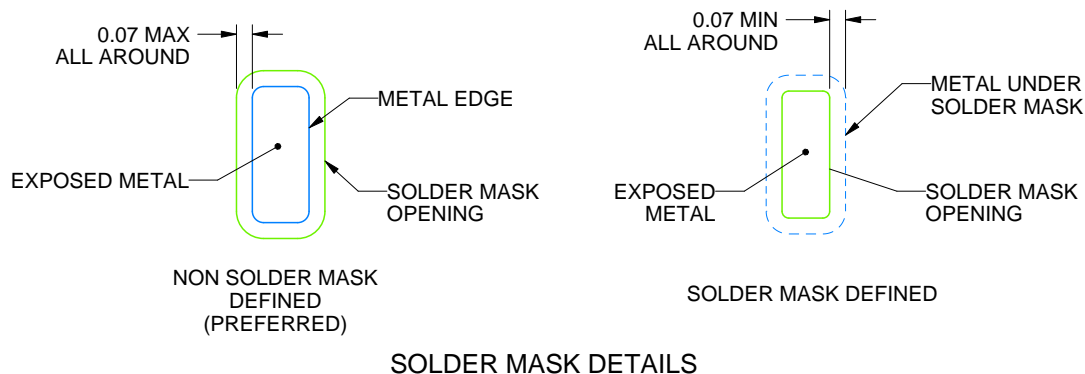
RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4224386/B 04/2019

NOTES: (continued)

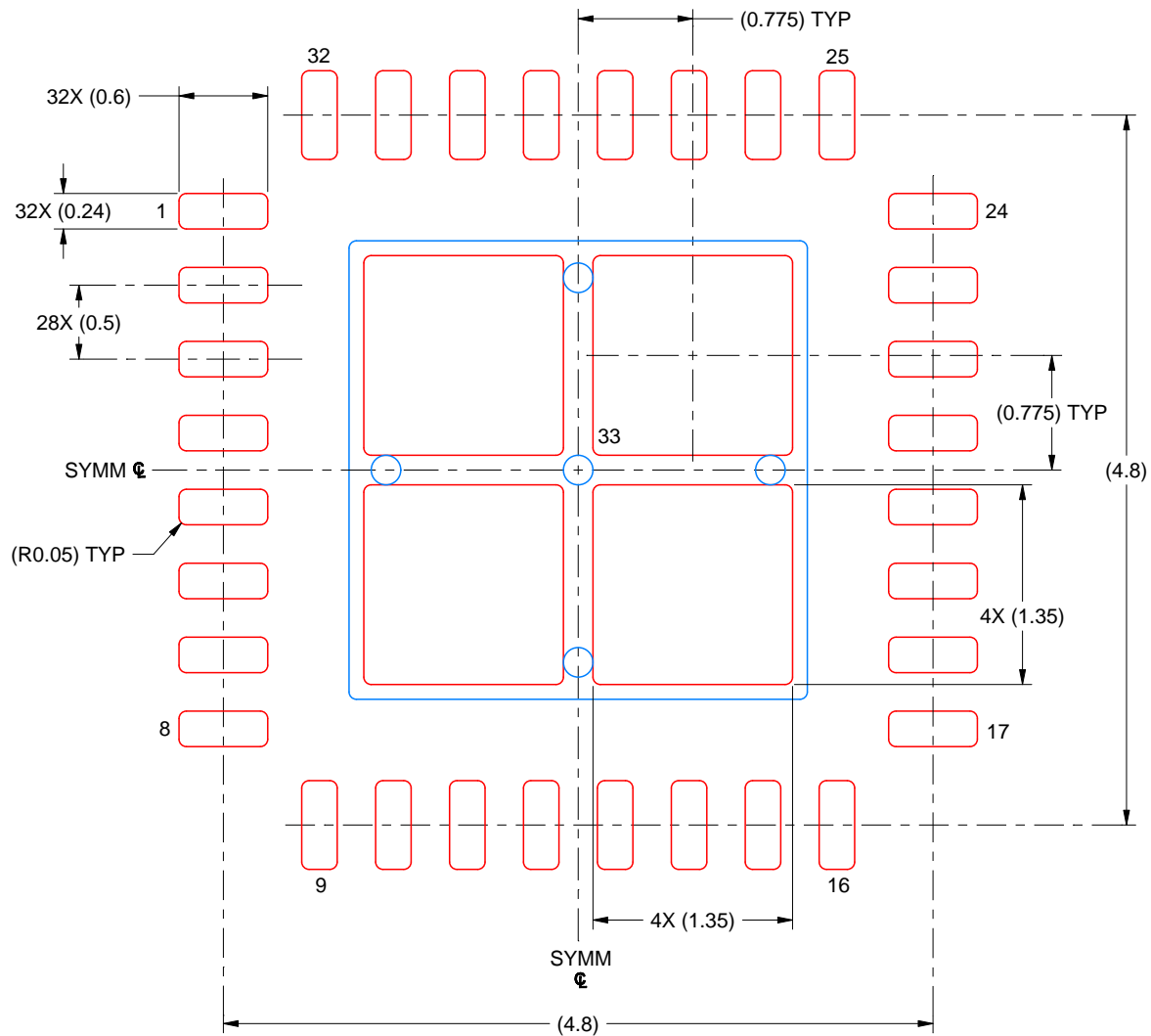
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 33  
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224386/B 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月