LMP2014MT Quad High Precision, Rail-to-Rail Output Operational Amplifier

Check for Samples: LMP2014MT

FEATURES

- **(For V_S = 5V, Typical Unless Otherwise Noted)**
- **Low Specified V_{OS} Over Temperature 60 µV**
- **Low Noise with No 1/f 35nV/√Hz**
- **High CMRR 130 dB**
- **High PSRR 120 dB**
- **High A_{VOL} 130 dB**
- **Wide Gain-Bandwidth Product 3 MHz**
- **High Slew Rate 4 V/µs**
- **Low Supply Current 3.7 mA**
- **Rail-to-Rail Output 30 mV**
- **No External Capacitors Required**

APPLICATIONS

- **Precision Instrumentation Amplifiers**
- **Thermocouple Amplifiers**
- **Strain Gauge Bridge Amplifier**

DESCRIPTION

The LMP2014MT is a member of Texas Instruments' new LMP™ precision amplifier family. The LMP2014MT offers unprecedented accuracy and stability while also being offered at an affordable price. This device utilizes patented techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra stable over time and temperature. It has excellent CMRR and PSRR ratings, and does not exhibit the familiar 1/f voltage and current noise increase that plagues traditional amplifiers. The combination of the LMP2014 characteristics makes it a good choice for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, and any other 2.7V-5V application requiring precision and long term stability.

Other useful benefits of the LMP2014 are rail-to-rail output, a low supply current of 3.7 mA, and wide gain-bandwidth product of 3 MHz. These extremely versatile features found in the LMP2014 provide high performance and ease of use.

Connection Diagram

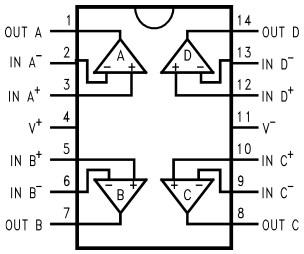


Figure 1. 14-Pin TSSOP – Top View
See Package Number PW

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance	Human Body Model	2000V
	Machine Model	200V
Supply Voltage		5.8V
Common-Mode Input Voltage		$-0.3 \le V_{CM} \le V_{CC}$ +0.3V
Lead Temperature (soldering 10 sec.)		+300°C
Differential Input Voltage		±Supply Voltage
Current at Input Pin		30 mA
Current at Output Pin		30 mA
Current at Power Supply Pin		50 mA

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Operating Ratings(1)

Supply Voltage		2.7V to 5.25V
Storage Temperature Range		−65°C to 150°C
Operating Temperature Range	LMP2014MT, LMP2014MTX	0°C to 70°C

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage			0.8	30 **60**	µV
	Offset Calibration Time			0.5	10 **12**	ms
TCV_{OS}	Input Offset Voltage			0.015		µV/°C
	Long-Term Offset Drift			0.006		µV/month
	Lifetime V_{OS} Drift			2.5		µV
I_{IN}	Input Current			-3		pA
I_{OS}	Input Offset Current			6		pA
R_{IND}	Input Differential Resistance			9		MΩ
CMRR	Common Mode Rejection Ratio	$-0.3 \le V_{CM} \le 0.9V$ $0 \le V_{CM} \le 0.9V$	95 **90**	130		dB
PSRR	Power Supply Rejection Ratio		95 **90**	120		dB
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ	95 **90**	130		dB
		R_L = 2 kΩ	90 **85**	124		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

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2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
V_O	Output Swing	R_L = 10 kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.63 **2.655**	2.68		V
				0.033	0.070 **0.075**	
		R_L = 2 kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.615 **2.615**	2.65		V
				0.061	0.085 **0.105**	
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	5 **3**	12		mA
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V	5 **3**	18		
I_S	Supply Current per Channel			0.919	1.20 **1.50**	mA

2.7V AC Electrical Characteristics

T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max (1)	Units
GBW	Gain-Bandwidth Product			3		MHz
SR	Slew Rate			4		V/µs
θ_m	Phase Margin			60		Deg
G_m	Gain Margin			−14		dB
e_n	Input-Referred Voltage Noise			35		nV/√Hz
i_n	Input-Referred Current Noise					pA/√Hz
e_np-p	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10 Hz		850		nV_{pp}
t_{rec}	Input Overload Recovery Time			50		ms

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

5V DC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage			0.12	30 **60**	µV
	Offset Calibration Time			0.5	10 **12**	ms
TCV_{OS}	Input Offset Voltage			0.015		µV/°C
	Long-Term Offset Drift			0.006		µV/month
	Lifetime V_{OS} Drift			2.5		µV
I_{IN}	Input Current			-3		pA
I_{OS}	Input Offset Current			6		pA
R_{IND}	Input Differential Resistance			9		MΩ
CMRR	Common Mode Rejection Ratio	−0.3 ≤ V_{CM} ≤ 3.2 0 ≤ V_{CM} ≤ 3.2	100 **90**	130		dB

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

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5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
PSRR	Power Supply Rejection Ratio		95 **90**	120		dB
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ	105 **100**	130		dB
		R_L = 2 kΩ	95 **90**	132		
V_O	Output Swing	R_L = 10 kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.92 **4.95**	4.978		V
				0.040	0.080 **0.085**	
		R_L = 2 kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.875 **4.875**	4.919		V
				0.091	0.125 **0.140**	
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	8 **6**	15		mA
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V	8 **6**	17		
I_S	Supply Current per Channel			0.930	1.20 **1.50**	mA

5V AC Electrical Characteristics

T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
GBW	Gain-Bandwidth Product			3		MHz
SR	Slew Rate			4		V/µs
θ_m	Phase Margin			60		deg
G_m	Gain Margin			−15		dB
e_n	Input-Referred Voltage Noise			35		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise					$pA/\sqrt{Hz}$
e_np-p	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10 Hz		850		nV_{PP}
t_{rec}	Input Overload Recovery Time			50		ms

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

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Typical Performance Characteristics

T_A=25C, V_S= 5V unless otherwise specified.

Supply Current vs. Supply Voltage

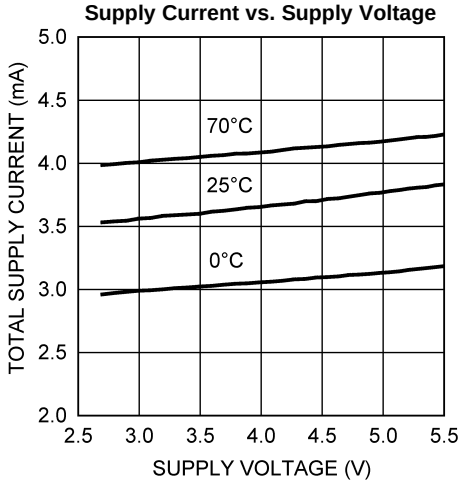


Figure 2.

Offset Voltage vs. Supply Voltage

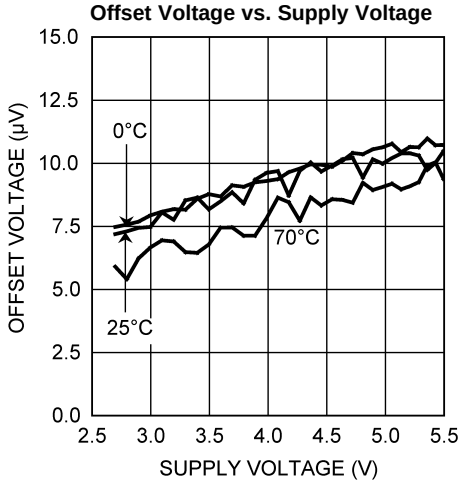


Figure 3.

Offset Voltage vs. Common Mode

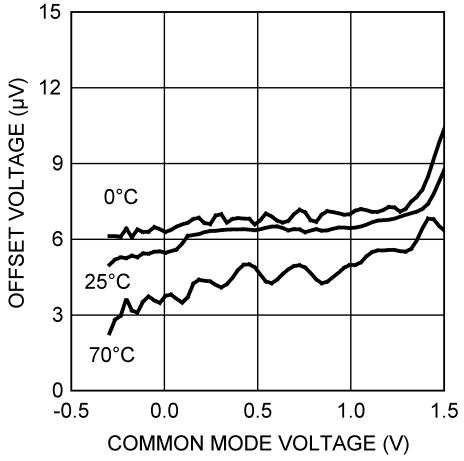


Figure 4.

Offset Voltage vs. Common Mode

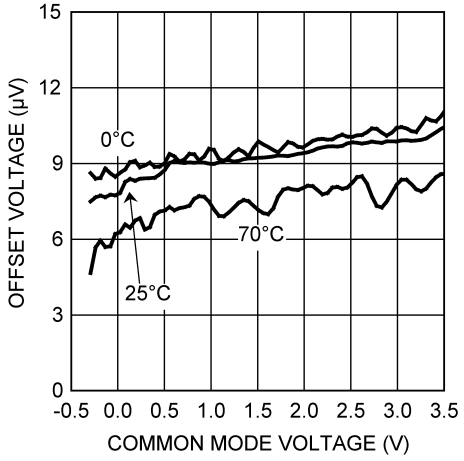


Figure 5.

Voltage Noise vs. Frequency

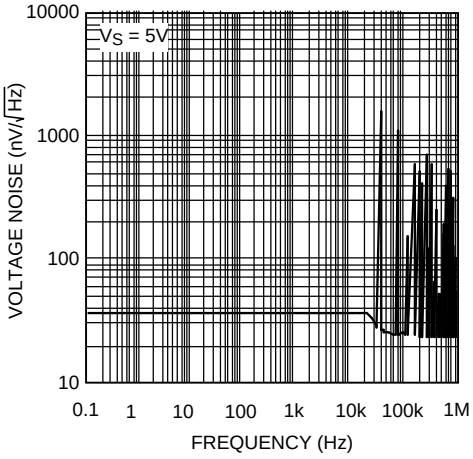


Figure 6.

Input Bias Current vs. Common Mode

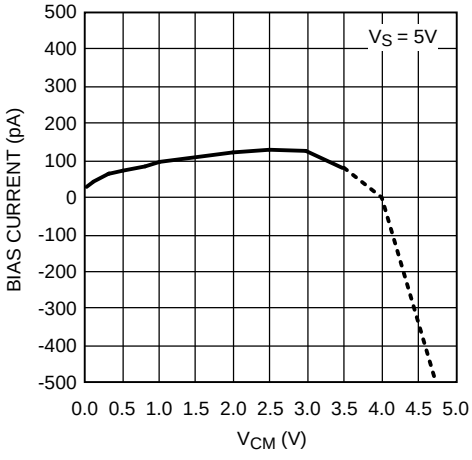


Figure 7.

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Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

PSRR vs. Frequency

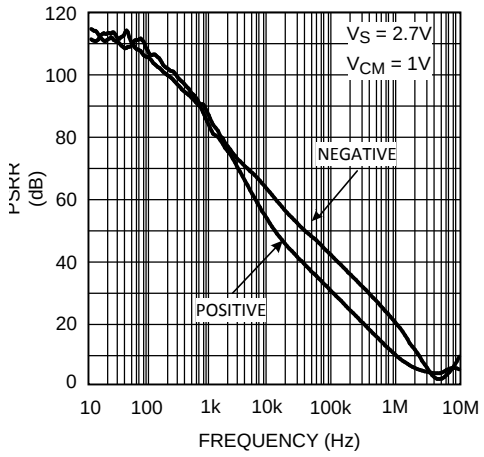


Figure 8.

PSRR vs. Frequency

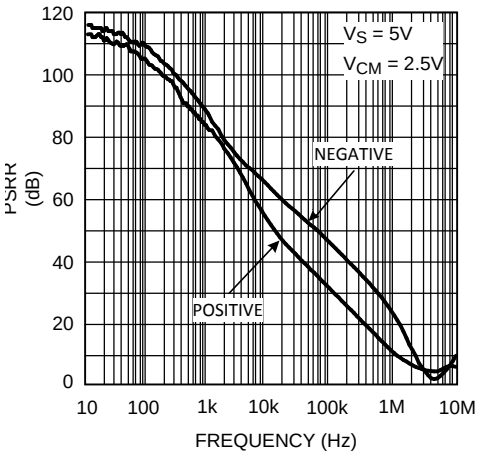


Figure 9.

Output Sourcing @ 2.7V

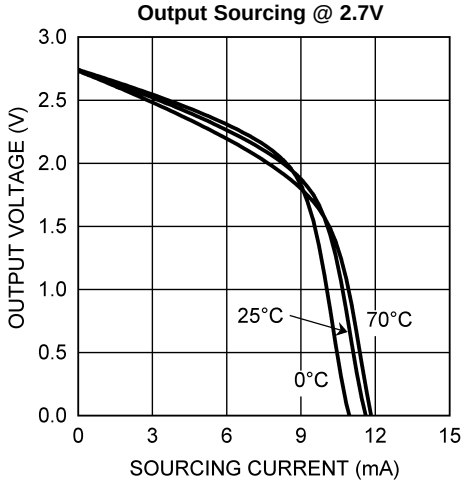


Figure 10.

Output Sourcing @ 5V

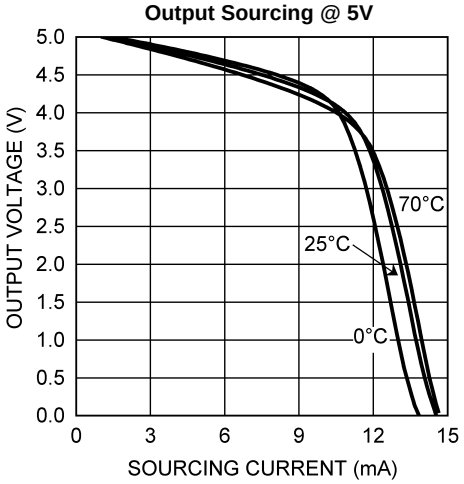


Figure 11.

Output Sinking @ 2.7V

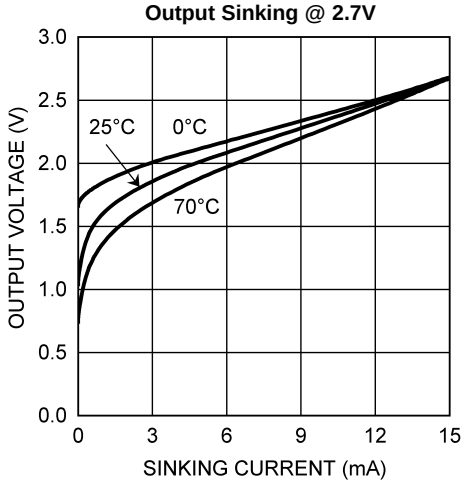


Figure 12.

Output Sinking @ 5V

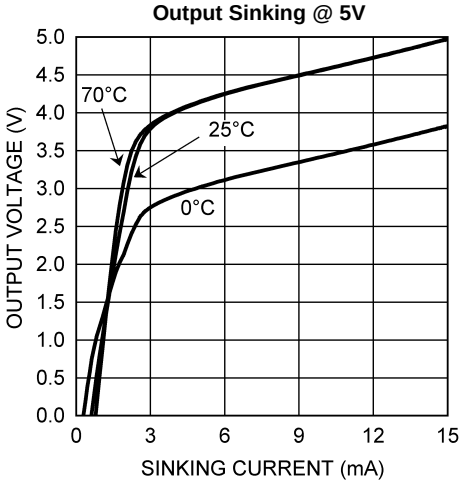


Figure 13.

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Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

Max Output Swing vs. Supply Voltage

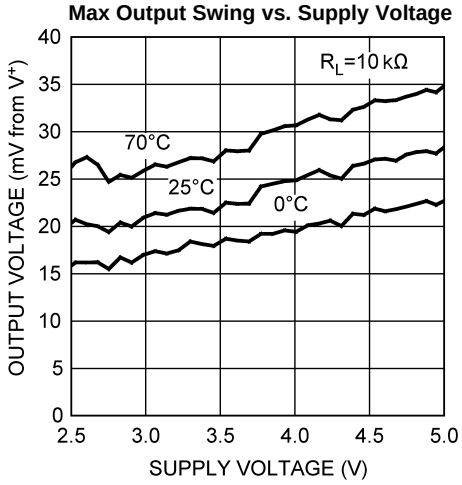


Figure 14.

Max Output Swing vs. Supply Voltage

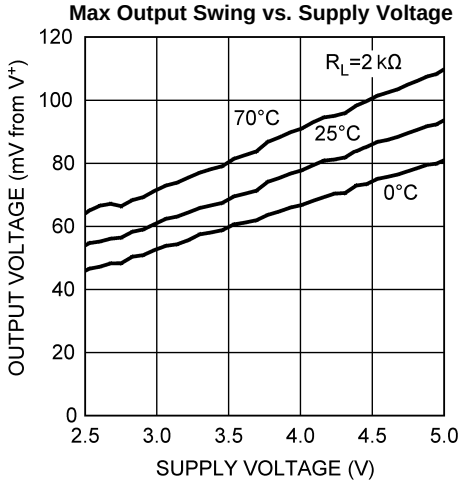


Figure 15.

Min Output Swing vs. Supply Voltage

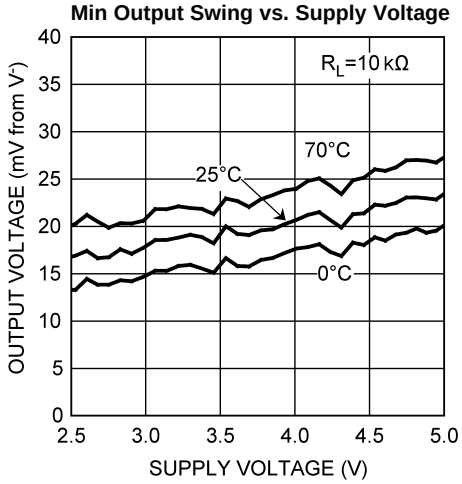


Figure 16.

Min Output Swing vs. Supply Voltage

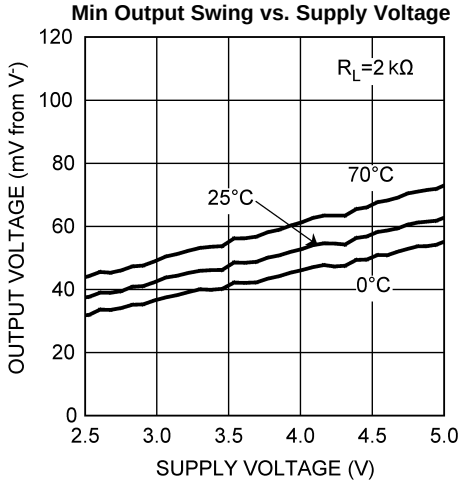


Figure 17.

CMRR vs. Frequency

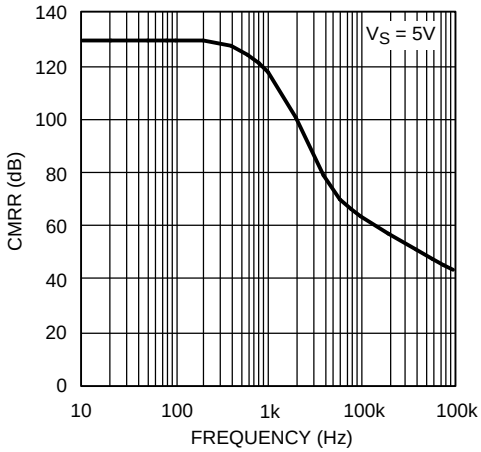


Figure 18.

Open Loop Gain and Phase vs. Supply Voltage

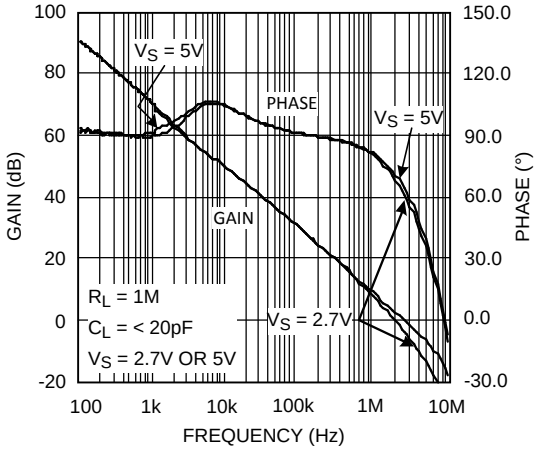


Figure 19.

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Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

Open Loop Gain and Phase vs. R_L @ 2.7V

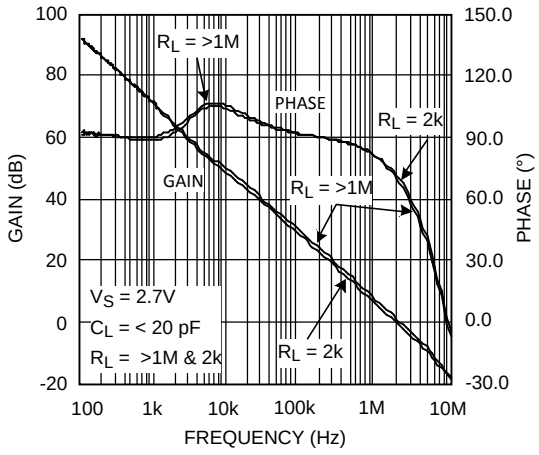


Figure 20.

Open Loop Gain and Phase vs. R_L @ 5V

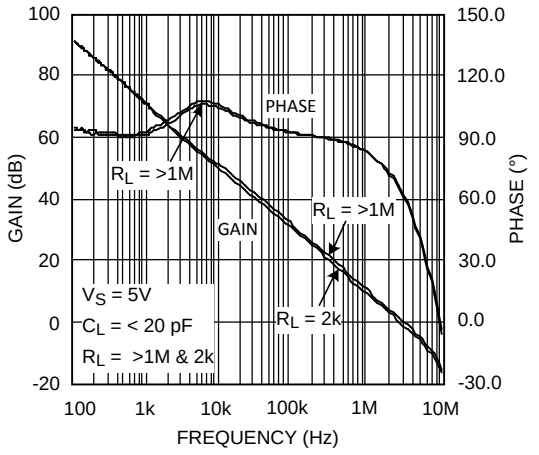


Figure 21.

Open Loop Gain and Phase vs. C_L @ 2.7V

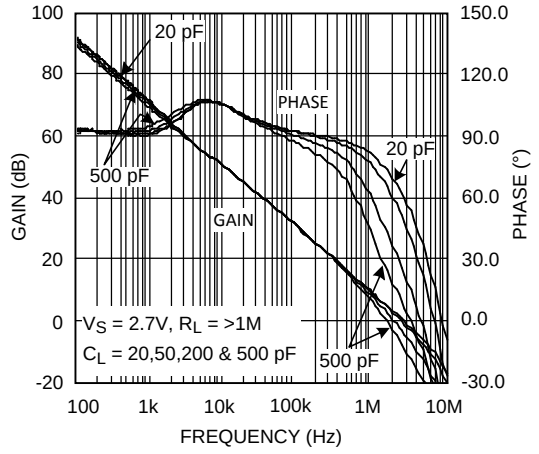


Figure 22.

Open Loop Gain and Phase vs. C_L @ 5V

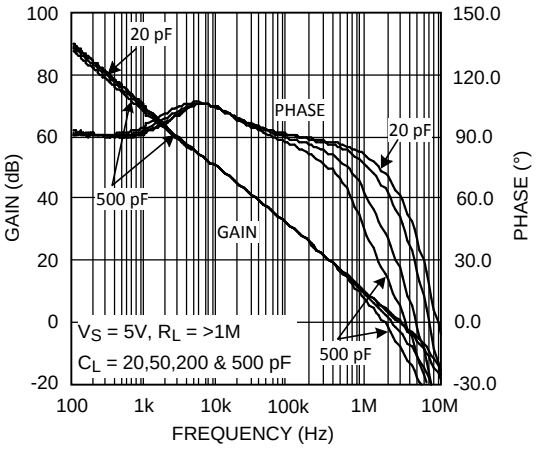


Figure 23.

Open Loop Gain and Phase vs. Temperature @ 2.7V

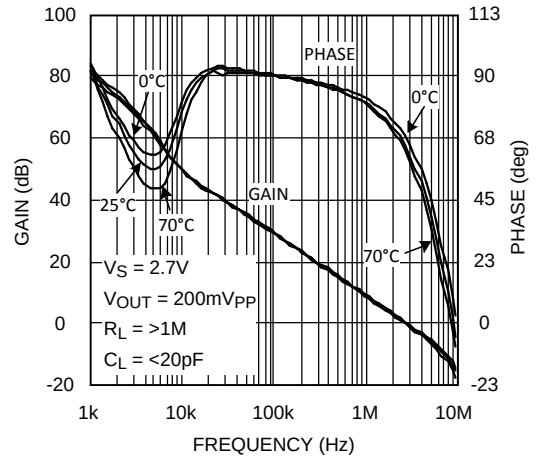


Figure 24.

Open Loop Gain and Phase vs. Temperature @ 5V

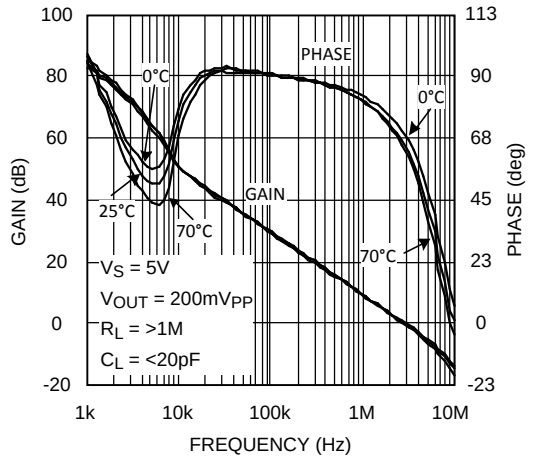


Figure 25.

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Typical Performance Characteristics (continued)

T_A=25C, V_S= 5V unless otherwise specified.

THD+N vs. AMPL

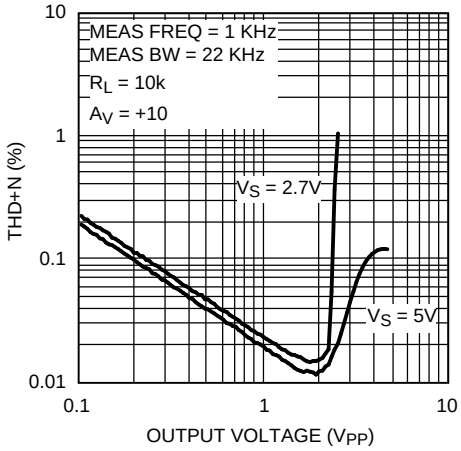


Figure 26.

THD+N vs. Frequency

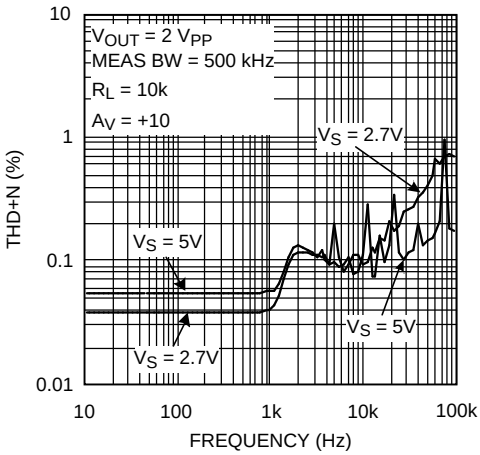


Figure 27.

0.1 Hz − 10 Hz Noise vs. Time

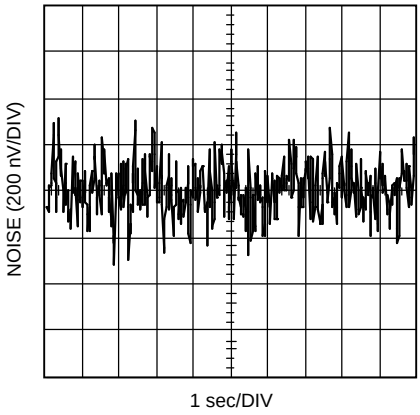


Figure 28.

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APPLICATION INFORMATION

THE BENEFITS OF LMP2014 NO 1/f NOISE

Using patented methods, the LMP2014 eliminates the 1/f noise present in other amplifiers. That noise, which increases as frequency decreases, is a major source of measurement error in all DC-coupled measurements. Low-frequency noise appears as a constantly-changing signal in series with any measurement being made. As a result, even when the measurement is made rapidly, this constantly-changing noise signal will corrupt the result. The value of this noise signal can be surprisingly large. For example: If a conventional amplifier has a flat-band noise level of 10nV/√Hz and a noise corner of 10 Hz, the RMS noise at 0.001 Hz is 1µV/√Hz. This is equivalent to a 0.50 µV peak-to-peak error, in the frequency range 0.001 Hz to 1.0 Hz. In a circuit with a gain of 1000, this produces a 0.50 mV peak-to-peak output error. This number of 0.001 Hz might appear unreasonably low, but when a data acquisition system is operating for 17 minutes, it has been on long enough to include this error. In this same time, the LMP2014 will only have a 0.21 mV output error. This is smaller by 2.4 x. Keep in mind that this 1/f error gets even larger at lower frequencies. At the extreme, many people try to reduce this error by integrating or taking several samples of the same signal. This is also doomed to failure because the 1/f nature of this noise means that taking longer samples just moves the measurement into lower frequencies where the noise level is even higher.

The LMP2014 eliminates this source of error. The noise level is constant with frequency so that reducing the bandwidth reduces the errors caused by noise.

Another source of error that is rarely mentioned is the error voltage caused by the inadvertent thermocouples created when the common "Kovar type" IC package lead materials are soldered to a copper printed circuit board. These steel-based leadframe materials can produce over 35 µV/°C when soldered onto a copper trace. This can result in thermocouple noise that is equal to the LMP2014 noise when there is a temperature difference of only 0.0014°C between the lead and the board!

For this reason, the lead-frame of the LMP2014 is made of copper. This results in equal and opposite junctions which cancel this effect.

OVERLOAD RECOVERY

The LMP2014 recovers from input overload much faster than most chopper-stabilized op amps. Recovery from driving the amplifier to 2X the full scale output, only requires about 40 ms. Many chopper-stabilized amplifiers will take from 250 ms to several seconds to recover from this same overload. This is because large capacitors are used to store the unadjusted offset voltage.

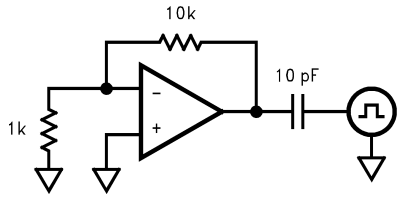


Figure 29.

The wide bandwidth of the LMP2014 enhances performance when it is used as an amplifier to drive loads that inject transients back into the output. ADCs (Analog-to-Digital Converters) and multiplexers are examples of this type of load. To simulate this type of load, a pulse generator producing a 1V peak square wave was connected to the output through a 10 pF capacitor. (Figure 29) The typical time for the output to recover to 1% of the applied pulse is 80 ns. To recover to 0.1% requires 860ns. This rapid recovery is due to the wide bandwidth of the output stage and large total GBW.

NO EXTERNAL CAPACITORS REQUIRED

The LMP2014 does not need external capacitors. This eliminates the problems caused by capacitor leakage and dielectric absorption, which can cause delays of several seconds from turn-on until the amplifier's error has settled.

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MORE BENEFITS

The LMP2014 offers the benefits mentioned above and more. It has a rail-to-rail output and consumes only 950 µA of supply current while providing excellent DC and AC electrical performance. In DC performance, the LMP2014 achieves 130 dB of CMRR, 120 dB of PSRR and 130 dB of open loop gain. In AC performance, the LMP2014 provides 3 MHz of gain-bandwidth product and 4 V/µs of slew rate.

HOW THE LMP2014 WORKS

The LMP2014 uses new, patented techniques to achieve the high DC accuracy traditionally associated with chopper-stabilized amplifiers without the major drawbacks produced by chopping. The LMP2014 continuously monitors the input offset and corrects this error. The conventional chopping process produces many mixing products, both sums and differences, between the chopping frequency and the incoming signal frequency. This mixing causes large amounts of distortion, particularly when the signal frequency approaches the chopping frequency. Even without an incoming signal, the chopper harmonics mix with each other to produce even more trash. If this sounds unlikely or difficult to understand, look at the plot (Figure 30), of the output of a typical (MAX432) chopper-stabilized op amp. This is the output when there is no incoming signal, just the amplifier in a gain of -10 with the input grounded. The chopper is operating at about 150 Hz; the rest is mixing products. Add an input signal and the noise gets much worse. Compare this plot with Figure 31 of the LMP2014. This data was taken under the exact same conditions. The auto-zero action is visible at about 30 kHz but note the absence of mixing products at other frequencies. As a result, the LMP2014 has very low distortion of 0.02% and very low mixing products.

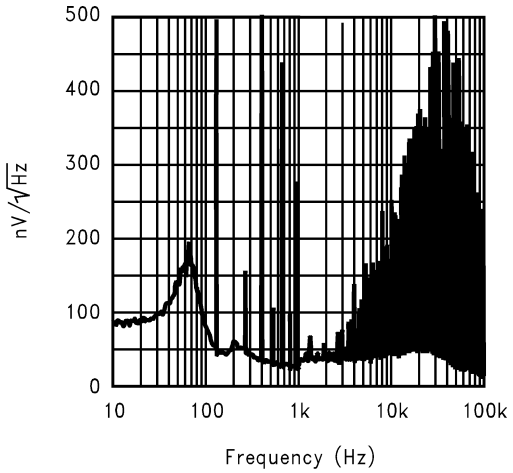


Figure 30.

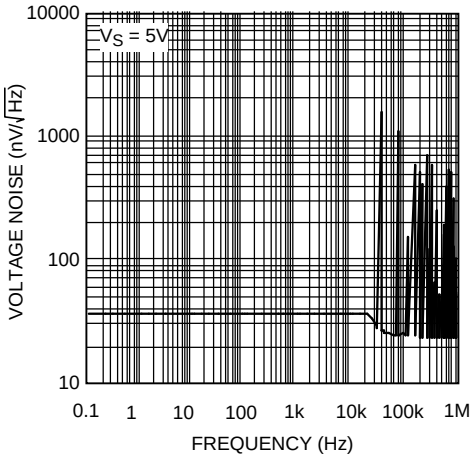


Figure 31.

INPUT CURRENTS

The LMP2014's input currents are different than standard bipolar or CMOS input currents in that it appears as a current flowing in one input and out the other. Under most operating conditions, these currents are in the picoamp level and will have little or no effect in most circuits. These currents tend to increase slightly when the common-mode voltage is near the minus supply. (See the typical curves.) At high temperatures such as 70°C, the input currents become larger, 0.5 nA typical, and are both positive except when the V_{CM} is near V^-. If operation is expected at low common-mode voltages and high temperature, do not add resistance in series with the inputs to balance the impedances. Doing this can cause an increase in offset voltage. A small resistance such as 1 kΩ can provide some protection against very large transients or overloads, and will not increase the offset significantly.

PRECISION STRAIN-GAUGE AMPLIFIER

This Strain-Gauge amplifier (Figure 32) provides high gain (1006 or ~60 dB) with very low offset and drift. Using the resistors' tolerances as shown, the worst case CMRR will be greater than 108 dB. The CMRR is directly related to the resistor mismatch. The rejection of common-mode error, at the output, is independent of the differential gain, which is set by R3. The CMRR is further improved, if the resistor ratio matching is improved, by specifying tighter-tolerance resistors, or by trimming.

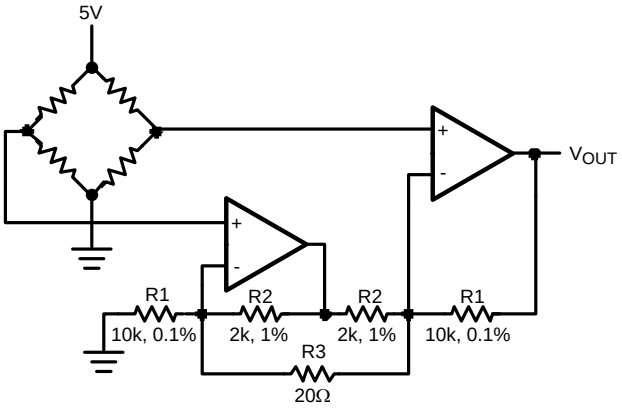


Figure 32.

Extending Supply Voltages and Output Swing by Using a Composite Amplifier Configuration:

In cases where substantially higher output swing is required with higher supply voltages, arrangements like the ones shown in Figure 33 and Figure 34 could be used. These configurations utilize the excellent DC performance of the LMP2014 while at the same time allow the superior voltage and frequency capabilities of the LM6171 to set the dynamic performance of the overall amplifier. For example, it is possible to achieve ±12V output swing with 300 MHz of overall GBW (A_V = 100) while keeping the worst case output shift due to V_{OS} less than 4 mV. The LMP2014 output voltage is kept at about mid-point of its overall supply voltage, and its input common mode voltage range allows the V- terminal to be grounded in one case (Figure 33, inverting operation) and tied to a small non-critical negative bias in another (Figure 34, non-inverting operation). Higher closed-loop gains are also possible with a corresponding reduction in realizable bandwidth. Table 1 shows some other closed loop gain possibilities along with the measured performance in each case.

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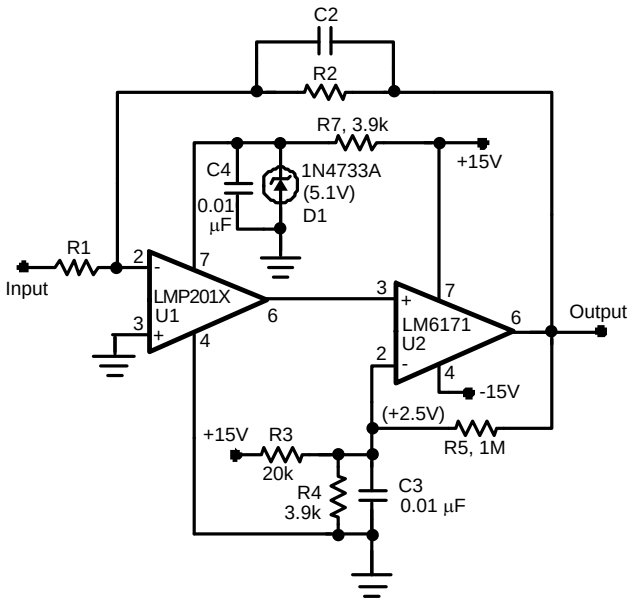


Figure 33.

Table 1. Composite Amplifier Measured Performance

AV	R1 Ω	R2 Ω	C2 pF	BW MHz	SR (V/µs)	en p-p (mV_{PP})
50	200	10k	8	3.3	178	37
100	100	10k	10	2.5	174	70
100	1k	100k	0.67	3.1	170	70
500	200	100k	1.75	1.4	96	250
1000	100	100k	2.2	0.98	64	400

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In terms of the measured output peak-to-peak noise, the following relationship holds between output noise voltage, e_n p-p, for different closed-loop gain, A_V, settings, where −3 dB Bandwidth is BW:

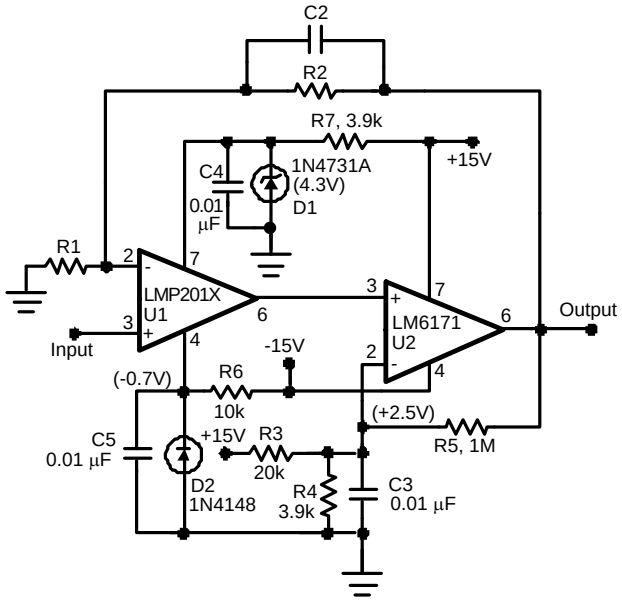


Figure 34.

It should be kept in mind that in order to minimize the output noise voltage for a given closed-loop gain setting, one could minimize the overall bandwidth. As can be seen from Equation 1 above, the output noise has a square-root relationship to the Bandwidth.

In the case of the inverting configuration, it is also possible to increase the input impedance of the overall amplifier, by raising the value of R1, without having to increase the feed-back resistor, R2, to impractical values, by utilizing a "Tee" network as feedback. See the LMC6442 Data Sheet (Application Notes section) for more details on this.

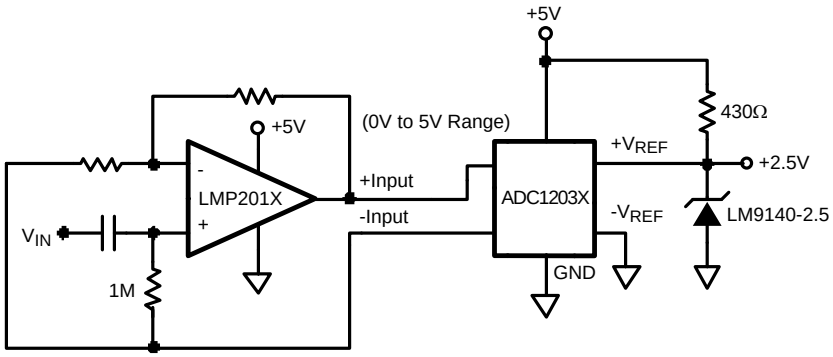


Figure 35.

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LMP2014 AS ADC INPUT AMPLIFIER

The LMP2014 is a great choice for an amplifier stage immediately before the input of an ADC (Analog-to-Digital Converter), whether AC or DC coupled. See Figure 35 and Figure 36. This is because of the following important characteristics:

a. Very low offset voltage and offset voltage drift over time and temperature allow a high closed-loop gain setting without introducing any short-term or long-term errors. For example, when set to a closed-loop gain of 100 as the analog input amplifier for a 12-bit A/D converter, the overall conversion error over full operation temperature and 30 years life of the part (operating at 50°C) would be less than 5 LSBs.

b. Fast large-signal settling time to 0.01% of final value (1.4 µs) allows 12 bit accuracy at 100 KH_Z or more sampling rate.

c. No flicker (1/f) noise means unsurpassed data accuracy over any measurement period of time, no matter how long. Consider the following op amp performance, based on a typical low-noise, high-performance commercially-available device, for comparison:

   Op amp flatband noise = $8nV/\sqrt{Hz}$

   1/f corner frequency = 100 Hz

   A_V = 2000

   Measurement time = 100 sec

   Bandwidth = 2 Hz

   This example will result in about 2.2 mV_{PP} (1.9 LSB) of output noise contribution due to the op amp alone, compared to about 594 μV_{PP} (less than 0.5 LSB) when that op amp is replaced with the LMP2014 which has no 1/f contribution. If the measurement time is increased from 100 seconds to 1 hour, the improvement realized by using the LMP2014 would be a factor of about 4.8 times (2.86 mV_{PP} compared to 596 µV when LMP2014 is used) mainly because the LMP2014 accuracy is not compromised by increasing the observation time.

d. Copper leadframe construction minimizes any thermocouple effects which would degrade low level/high gain data conversion application accuracy (see discussion under " The Benefits of the LMP2014" section above).

e. Rail-to-Rail output swing maximizes the ADC dynamic range in 5-Volt single-supply converter applications. Below are some typical block diagrams showing the LMP2014 used as an ADC amplifier.

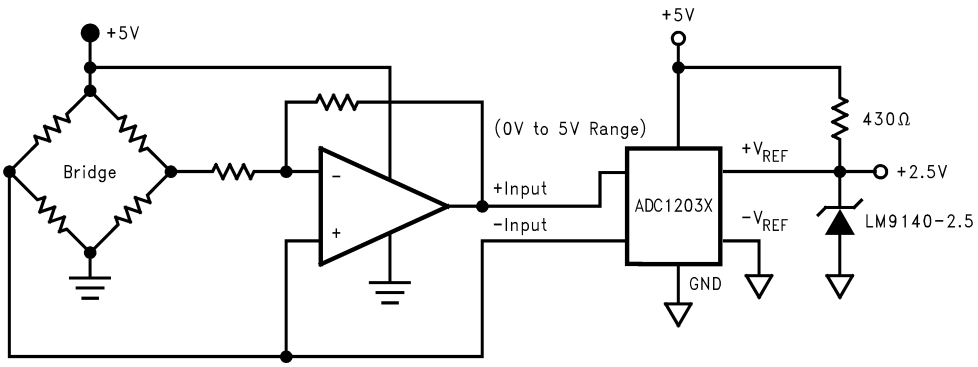


Figure 36.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	15

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP2014MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LMP20 14MT
LMP2014MT/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LMP20 14MT
LMP2014MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LMP20 14MT
LMP2014MTX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LMP20 14MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

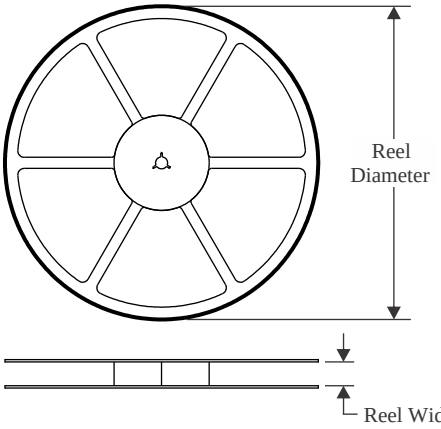
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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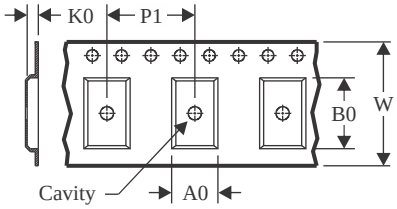
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

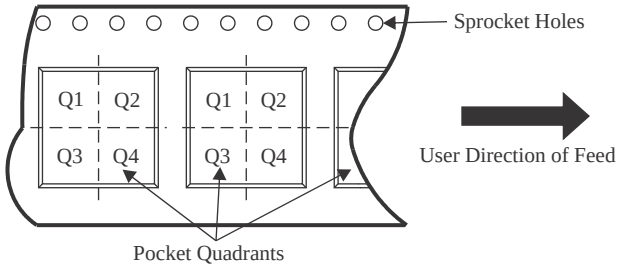


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

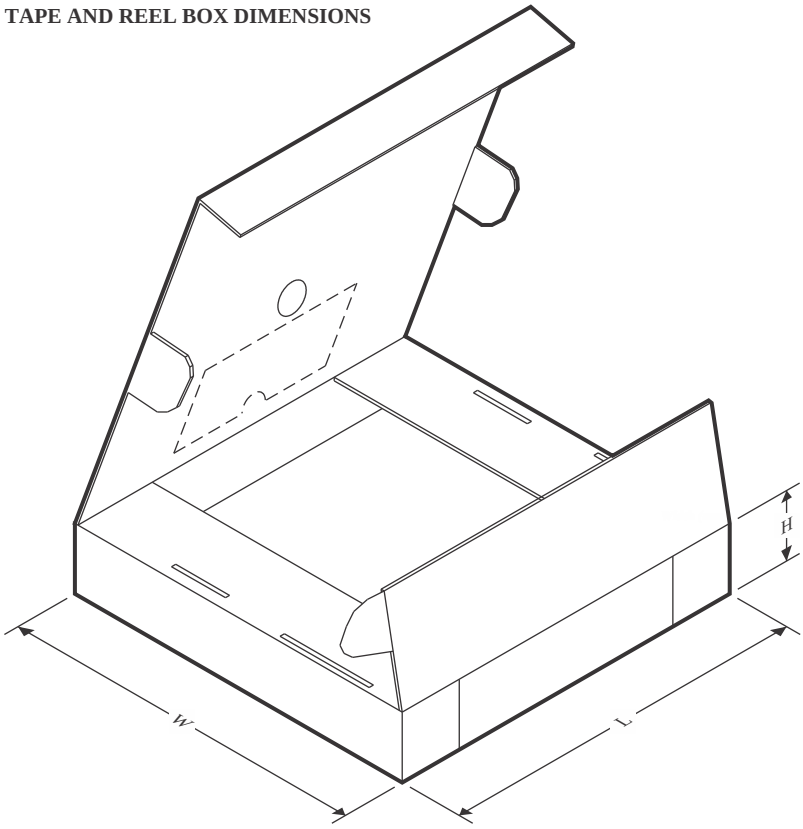
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP2014MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

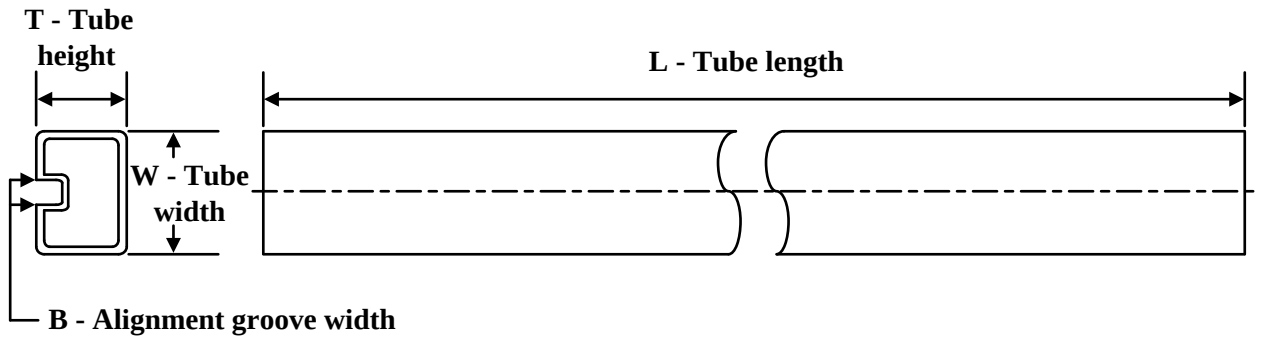
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP2014MTX/NOPB	TSSOP	PW	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

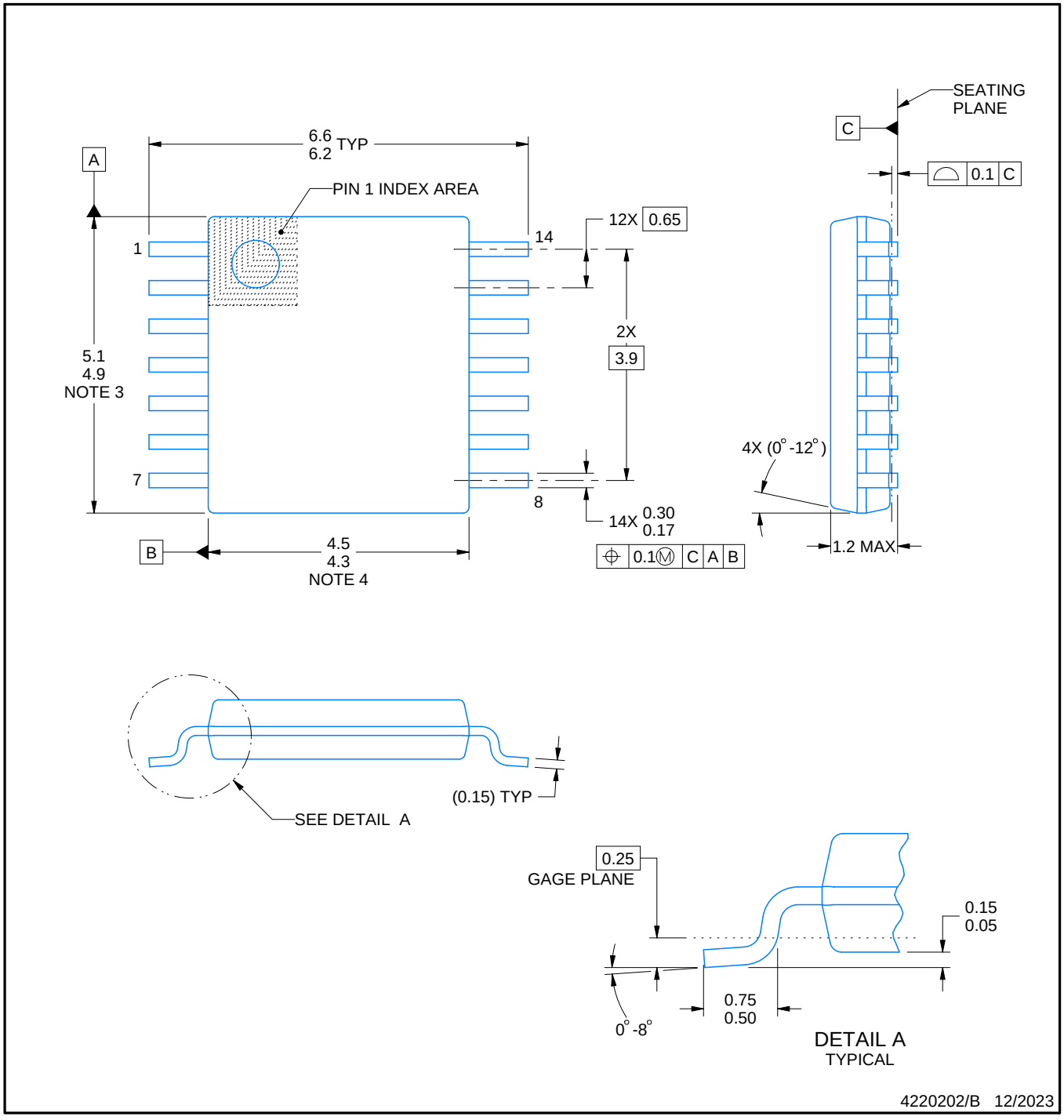
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP2014MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMP2014MT/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0014A

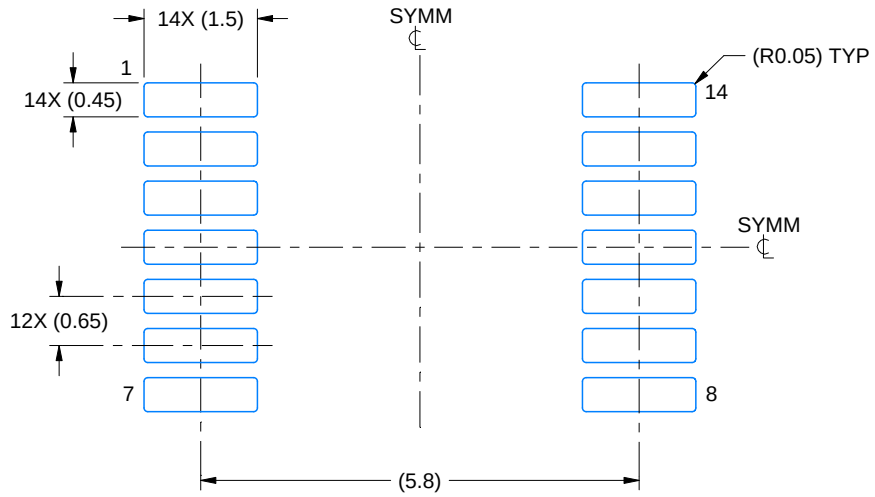
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

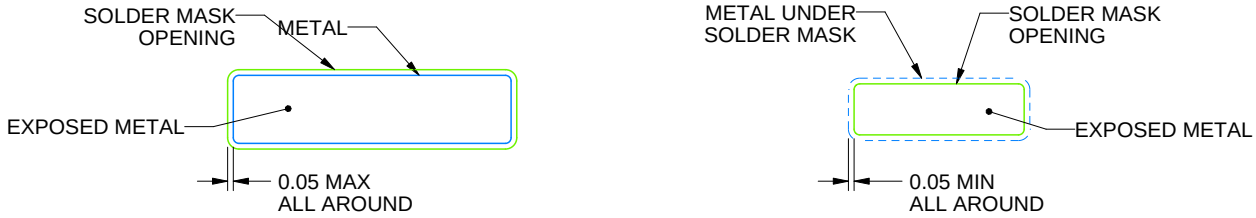


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

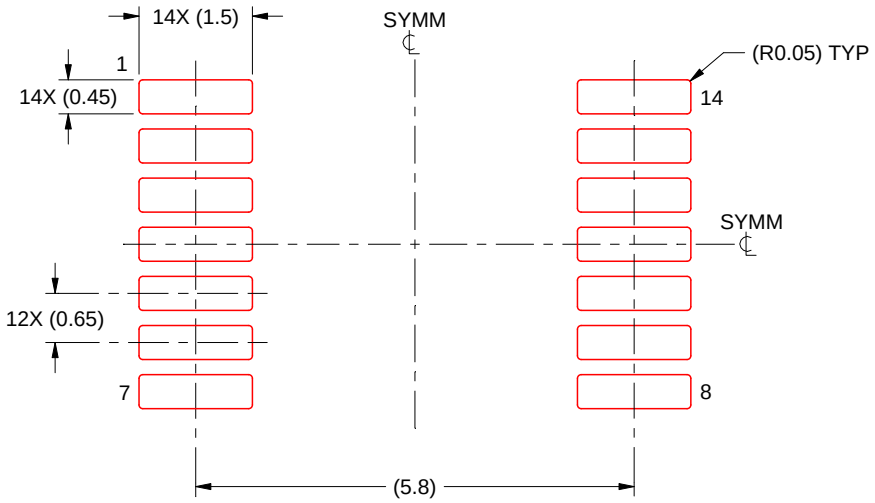


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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