LMP8350 Ultra-Low Distortion Fully-Differential Precision ADC Driver With Selectable Power Modes

1 Features

- Differential Input and Output
- Tri-Level Power Settings with Shutdown
- Ultra Low HD2/HD3 and THD+N Distortion
- Adjustable Output Common-Mode Level
- Fully-Balanced Differential Architecture
- Single- or Dual-Supply Operation
- Operating Voltage Range 4.5 V to 12 V
- Supply Current 3 mA to 13 mA
- Total THD+N at 1 KHz 0.000097%
- HD2 / HD3 Distortion at 1 KHz < –124 dBc
- Bandwidth 118 mHz
- Settling to 0.1% 20 ns
- Low Offset Drift 0.4 µV/°C
- Offset Voltage 80 µV
- Voltage Noise 4.6 nV/Hz
- Operating Temperature Range −40°C to +85°C

2 Applications

- High-Resolution Differential ADC Drivers
- Portable Instrumentation
- Precision Line Drivers

3 Description

The LMP8350 device is an ultra low distortion fully-differential amplifier designed for driving high-performance precision analog-to-digital converters (ADC). As part of the PowerWise™ family, a unique mode enable pin allows the user to choose from three different operating modes, trading power consumption for dynamic performance.

The high power mode is optimized for highest AC performance. The low noise, wide bandwidth, and fast slew rate make the LMP8350 ideal for driving 24-bit ADCs with input sampling rates of 10 MHz or less. The medium power mode is optimized for precision DC performance, and can be used to drive 24-bit ADCs with input sampling rates of 6 MHz or less. The low power mode is a trade-off between AC performance and quiescent current for power-sensitive applications. The disable mode fully shuts down the amplifier for further standby power savings.

The fully differential architecture of this device allows for easy implementation of a single-ended to fully-differential output conversion. Driving a 3-Vpp, 1-kHz output sine wave with the amplifier powered by ±3.3-V rails in high power mode yields 0.000098% THD+N.

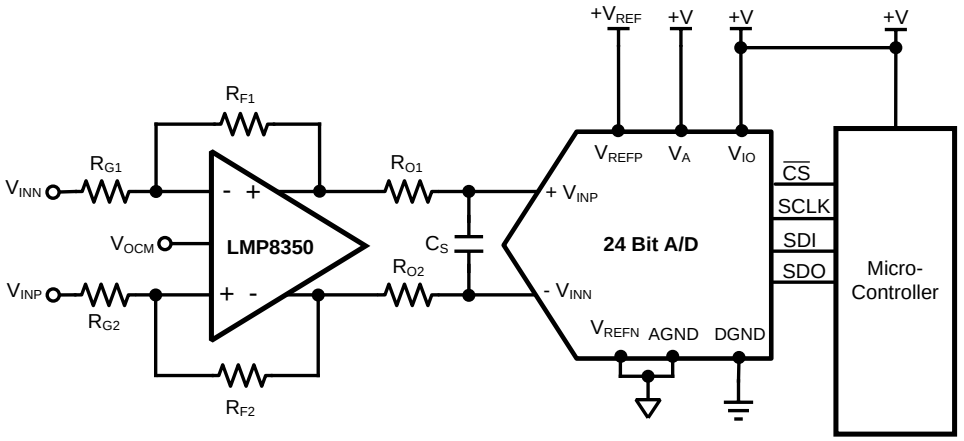
The LMP8350 is part of the LMP™ precision amplifier family, and is offered in the 8-pin SOIC package, with an operating temperature range of −40°C to +85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP8350	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C — **Page**

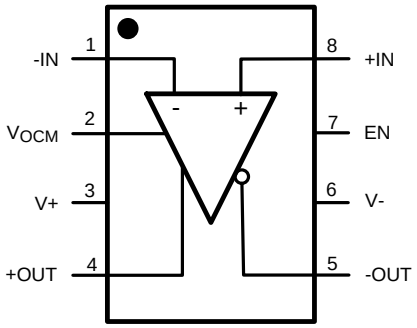
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision A (March 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 29

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	–IN	I	Inverting Input
2	V_{OCM}	I	Output common-mode voltage set input. Sets output common mode voltage equal to the applied V_{OCM} pin voltage.
3	V+	I	Positive power supply voltage
4	+OUT	O	Noninverting output
5	–OUT	O	Inverting output
6	V–	I	Negative power supply voltage
7	EN	I	Enable and power select input. Applied voltage sets power level or shutdown mode.
8	+IN	I	Noninverting Input

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)(3)

	MIN	MAX	UNIT
Output short circuit duration	See (4)		
V+ relative to V–	–0.3	12.9	V
IN+, IN–, OUT, EN and V_{OCM} pins	(V+) + 0.3	(V–) – 0.3	V
Input current		1	mA
Junction temperature (5)		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications: SNOA549
(4) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (–) is sinking.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±1250	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

	MIN	MAX	UNIT
Temperature range (T_A)	–40	85	°C
Supply voltage ($V_S = V^+ – V^–$)	4.5	12	V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.

6.4 Thermal Information

THERMAL METRIC (1)		LMP8350 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	150	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.5 10-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F = R_G = 1 kΩ, Fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS(2)		MIN(3)	TYP(4)	MAX(3)	UNIT
10-V DC CHARACTERISTICS							
V_{OS}	Input offset voltage (RTI)	High power	T_A = 25°C		±0.6	±4	mV
			At the temperature extremes			±4.05	
		Mid power	T_A = 25°C		±0.08	±2	
			At the temperature extremes			±2.03	
		Low power	T_A = 25°C		±0.1	±2.5	
			At the temperature extremes			±2.52	
TCV_{OS}	Input offset voltage vs.temperature(5)	High power			±0.8		µV/°C
		Mid power			±0.5		
		Low power			±0.4		
I_B	Input bias current	High power	T_A = 25°C			2	µA
			At the temperature extremes			2.1	
		Mid power	T_A = 25°C			2.7	
			At the temperature extremes			3.2	
		Low power	T_A = 25°C			3.5	
			At the temperature extremes			3.7	
A_{VOL}	Open-loop gain	High power		65	90		dB
		Mid power		72	130		
		Low power		74	114		
CMVR	Common-mode voltage range(6)	HP at CMRR ≥ 73 dB		1.2		8.8	V
		MP at CMRR ≥ 83 dB		1.2		8.8	
		LP at CMRR ≥ 77 dB		1.2		8.8	
CMRR	Common-mode rejection ratio	DC, V_{OCM} = 0,VID = 0, ΔVcm = ±0.2 V, High power		75	90		dB
		Medium power		84	130		
		Low power		79	114		
Z_{IND}	Differential input resistance	V_{CM} = mid-supply			0.48		MΩ
C_{IND}	Differential input capacitance	V_{CM} = mid-supply			1		pF
V_O	Output swing (single-ended)	High power	Low Swing	0.86	0.75	9.14	V
			High Swing	0.86	9.25	9.14	
		Mid power	Low Swing	0.85	0.74	9.15	
			High Swing	0.85	9.26	9.15	
		Low power	Low Swing	0.86	0.81	9.14	
			High Swing	0.86	9.19	9.14	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A

(2) For annotation brevity, “HP”=High Power, “MP”=Medium Power, “LP” =Low Power, “DIS”=Disabled or shut down, “SE”=Single Ended Mode, “DM”=Differential Mode. See Table 1 in Applications section for power setting details. It is also assumed R_G = R_{G1} = R_{G2}

(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(5) Drift Determined by dividing the change in parameter at temperature extremes by the total temperature change. Value is the worst case of Ta_{MIN} to 25°C and 25°C to Ta_{MAX}.

(6) At amplifier inputs.

10-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F = R_G = 1 kΩ, Fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS(2)		MIN(3)	TYP(4)	MAX(3)	UNIT
I_{SHORT}	Short-circuit current	Output shorted to mid-supply(7) High power	Low Swing	–36	-65		mA
			High Swing	75	108		
		Medium power	Low Swing	-26	-48		
			High Swing	60	85		
		Low power	Low Swing	-6	-20		
			High Swing	15	36		
PSRR	Power supply rejection ratio V_S ±10%	High power			107		dB
		Mid power			118		
		Low power			124		
I_S	Supply current	V_{EN} = 8.75(8)	T_A = 25°C		15	18	mA
			At the temperature extremes			20	
		V_{EN} = 6.25(8)	T_A = 25°C		8	10	
			At the temperature extremes			11	
		V_{EN} = 3.75(8)	T_A = 25°C		3	4	
			At the temperature extremes			5	
PD	Power-down mode	Disable voltage threshold(8)			< 1.65		V
		Shutdown current	T_A = 25°C		0.75	0.9	mA
			At the temperature extremes			0.95	
		Enable pin current			100		µA
t_{en}	Enable time	High power			15		ns
		Mid power			20		
		Low power			40		
10-V AC CHARACTERISTICS							
SSBW	Small signal bandwidth 200 mVp-p differential	High power			118		MHz
		Mid power			87		
		Low power			31		
SR	Slew rate 2 Vp-p differential(9)	High power			507		V/µs
		Mid power			393		
		Low power			178		
t_{rise}	Rise time 2 Vp-p differential	High power			3		ns
		Mid power			3.9		
		Low power			9.7		
t_{fall}	Fall time 2 Vp-p differential	High power			2.8		ns
		Mid power			3.8		
		Low power			9.6		
t_s	0.1% settling time 2 Vp-p	2-V step, C_L = 20 pF High power			20		ns
		Mid power			25		
		Low power			38		
e_n	Input referred voltage noise at 10 KHz	High power			4.6		nV/√Hz
		Mid power			4.8		
		Low power			8		

(7) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (–) is sinking.
(8) Enable voltage is referred to V– (negative supply voltage).
(9) Slew Rate is the average of the rising and falling edges.

10-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F = R_G = 1 kΩ, Fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS(2)		MIN(3)	TYP(4)	MAX(3)	UNIT
I_n	Input referred current noise at 10 KHz	f = 10 kHz High power			1.7		pA/√Hz
		Mid power			1.1		
		Low power			0.6		
THD+N	Total harmonic distortion + noise 3 Vp-p at 1 KHz	High power			0.000097%		
		Mid power			0.000109%		
		Low power			0.000185%		
HD2	2nd harmonic distortion 3 Vp-p, 1 KHz	High power			–124.7	–116	dBc
		Mid power			–122.8		
		Low power			–117.2		
	2nd harmonic distortion 6 Vp-p, 1 KHz	High power			–118.9		dBc
		Mid power			–117.6		
		Low power			–114.7		
HD3	3rd harmonic distortion 3 Vp-p, 1 KHz	High power			–139.9	–126	dBc
		Mid power			–141.9		
		Low power			–133.3		
	3rd harmonic distortion 6 Vp-p, 1 KHz	High power			–129.5		dBc
		Mid power			–132.4		
		Low power			–129.4		
10-V V_{OCM} INPUT CHARACTERISTICS							
	V_{OCM} small signal bandwidth 200 mVp-p	High power			4.8		MHz
		Mid power			2.4		
		Low power			0.64		
	V_{OCM} gain				1		V/V
	V_{OCM} offset voltage	High power			±1.62		mV
		Mid power			±0.23		
		Low power			±0.43		
	V_{OCM} voltage range	All power levels	Low Swing		1.8		V
			High Swing		8.2		
	V_{OCM} input resistance	All power levels	Low Swing		30		KΩ
			High Swing		mid-supply		

6.6 6.6-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F = R_G = 1 kΩ, Fully differential input, V_S = +6.6 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS(2)		MIN(3)	TYP(4)	MAX(3)	UNIT
6.6-V DC CHARACTERISTICS							
V_{OS}	Input offset voltage (RTI)	High power	T_A = 25°C		±0.3	±3.5	mV
			At the temperature extremes			±3.54	
		Mid power	T_A = 25°C		±0.1	±2.8	
			At the temperature extremes			±2.83	
		Low power	T_A = 25°C		±0.1	±2.5	
			At the temperature extremes			±2.52	
TCV_{OS}	Input offset voltage vs.temperature(5)	High power			±0.7		µV/°C
		Mid power			±0.5		
		Low power			±0.4		
I_B	Input bias current	High power	T_A = 25°C			1.4	µA
			At the temperature extremes			2.4	
		Mid power	T_A = 25°C			2.5	
			At the temperature extremes			3.0	
		Low power	T_A = 25°C			3.5	
			At the temperature extremes			3.7	
A_{VOL}	Open-loop gain	High power		65	70		dB
		Mid power		73	76		
		Low power		72	75		
CMVR	Common-mode voltage range(6)	HP at CMRR ≥ 68 dB		1.2		5.4	V
		MP at CMRR ≥ 63 dB		1.2		5.4	
		LP at CMRR ≥ 79 dB		1.2		5.4	
CMRR	Common-mode rejection ratio	DC, V_{OCM} = 0,VID = 0, ΔVcm = ±0.2 V High power		70	85		dB
		Mid power		86	117		
		Low power		81	113		
Z_{IND}	Differential input resistance	V_{CM} = mid-supply			0.48		MΩ
C_{IND}	Differential input capacitance	V_{CM} = mid-supply			1		pF
V_O	Output swing (single-ended)	High power	Low Swing	0.84	0.77	5.76	V
			High Swing	0.84	5.83	5.76	
		Mid power	Low Swing	0.82	0.75	5.78	
			High Swing	0.82	5.83	5.78	
		Low power	Low Swing	0.83	0.77	5.77	
			High Swing	0.83	5.83	5.77	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A
(2) For annotation brevity, “HP”=High Power, “MP”=Medium Power, “LP” =Low Power, “DIS”=Disabled or shut down, “SE”=Single Ended Mode, “DM”=Differential Mode. See Table 1 in Applications section for power setting details. It is also assumed R_G = R_{G1} = R_{G2}
(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(5) Drift Determined by dividing the change in parameter at temperature extremes by the total temperature change. Value is the worst case of Ta_{MIN} to 25°C and 25°C to Ta_{MAX}.
(6) At amplifier inputs.

6.6-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F = R_G = 1 kΩ, Fully differential input, V_S = +6.6 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS(2)		MIN(3)	TYP(4)	MAX(3)	UNIT
I_{SHORT}	Short-circuit current	Output shorted to mid-supply(7) High power	Low Swing	–30	–49		mA
			High Swing	54	83		
		Mid power	Low Swing	–19	–35		
			High Swing	40	64		
		Low power	Low Swing	–6	–15		
			High Swing	15	27		
PSRR	Power supply rejection ratio V_S ±10%	High power			111		dB
		Mid power			117		
		Low power			127		
I_S	Supply current	V_{EN} = 5.775(8)	T_A = 25°C		14	16	mA
			At the temperature extremes			18	
		V_{EN} = 4.125(8)	T_A = 25°C		7	9	
			At the temperature extremes			10	
		V_{EN} = 2.475(8)	T_A = 25°C		2	3	
			At the temperature extremes			4	
PD	Power-down mode	Disable voltage threshold(8)			<1.225		V
		Shutdown current	T_A = 25°C		0.55	0.65	mA
			At the temperature extremes			0.7	
		Enable pin current			40		µA
t_{en}	Enable time	High power			18		ns
		Mid power			22		
		Low power			43		
6.6-V AC CHARACTERISTICS							
SSBW	Small signal bandwidth 200 mVp-p differential	High power			116		MHz
		Mid power			85		
		Low power			29		
SR	Slew rate 2 Vp-p differential(9)	High power			488		V/µs
		Mid power			376		
		Low power			166		
t_{rise}	Rise time 2 Vp-p differential	High power			3.1		ns
		Mid power			4.2		
		Low power			10.4		
t_{fall}	Fall time 2 Vp-p differential	High power			3.0		ns
		Mid power			4.0		
		Low power			10.3		
t_s	0.1% settling time 2 Vp-p	2-V step, C_L = 20 pF High power			19		ns
		Mid power			25		
		Low power			43		

(7) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (–) is sinking.
(8) Enable voltage is referred to V- (negative supply voltage).
(9) Slew Rate is the average of the rising and falling edges.

6.6-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F = R_G = 1 kΩ, Fully differential input, V_S = +6.6 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS(2)		MIN(3)	TYP(4)	MAX(3)	UNIT
e_n	Input referred voltage noise at 10KHz	High power			4.5		nV/√Hz
		Mid power			4.8		
		Low power			8		
I_n	Input referred current noise at 10KHz	High power			1.7		pA/√Hz
		Mid power			1.2		
		Low power			0.6		
THD+N	Total harmonic distortion + noise 3 Vp-p at 1 KHz	High power			0.000098 %		
		Mid power			0.00011%		
		Low power			0.000089 %		
HD2	2nd harmonic distortion 3 Vp-p, 1 KHz	High power			–124.7		dBc
		Mid power			–122.8		
		Low power			–117.2		
	2nd harmonic distortion 6 Vp-p, 1 KHz	High power			–118.9		dBc
		Mid power			–117.6		
		Low power			–114.7		
HD3	3rd harmonic distortion 3 Vp-p, 1 KHz	High power			–139.9		dBc
		Mid power			-141.9		
		Low power			–133.3		
	3rd harmonic distortion 6Vp-p, 1KHz	High power			–121.4		dBc
		Mid power			–125.3		
		Low power			–124.5		
6.6-V V_{OCM} INPUT CHARACTERISTICS							
	V_{OCM} small signal bandwidth 200mVp-p	High power			4.5		MHz
		Mid power			2.2		
		Low power			0.6		
	V_{OCM} gain				1		V/V
	V_{OCM} offset voltage	High power			±0.97		mV
		Mid power			±0.43		
		Low power			±0.89		
	V_{OCM} voltage range	All power levels	Low Swing		1.2		V
			High Swing		5.4		
	V_{OCM} input resistance	All power levels	Low Swing		30		KΩ
			High Swing		mid-supply		

6.7 5-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F= R_G = 1 kΩ, Fully differential input, V_S = +5 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
5-V DC CHARACTERISTICS							
V_{OS}	Input offset voltage (RTI)	High power	T_A = 25°C		±0.2	±3.2	mV
			At the temperature extremes			±3.6	
		Mid power	T_A = 25°C		±0.1	±2.0	
			At the temperature extremes			±2.3	
		Low power	T_A = 25°C		±0.1	±2.0	
			At the temperature extremes			±2.3	
TCV_{OS}	Input offset voltage vs.temperature(4)	High power			±0.7		µV/°C
		Mid power			±0.5		
		Low power			±0.4		
I_B	Input bias current	High power	T_A = 25°C			1.5	µA
			At the temperature extremes			1.6	
		Mid power	T_A = 25°C			2.5	
			At the temperature extremes			3.0	
		Low power	T_A = 25°C			3.5	
			At the temperature extremes			3.7	
A_{VOL}	Open-loop gain	High power		63	68		dB
		Mid power		71	75		
		Low power		68	75		
CMVR	Common-mode voltage range(5)	HP at CMRR ≥ 60 dB		1.15		3.85	V
		MP at CMRR ≥ 86 dB		1.15		3.85	
		LP at CMRR ≥ 80 dB		1.15		3.85	
CMRR	Common-mode rejection ratio	DC, V_{OCM} = 0,VID = 0, ΔVcm = ±0.2 V High power		63	79		dB
		Mid power		87	114		
		Low power		82	114		
Z_{IND}	Differential input resistance	V_{CM} = mid-supply			0.48		MΩ
C_{IND}	Differential input capacitance	V_{CM} = mid-supply			1		pF
V_O	Output swing (single-ended)	High power	Low Swing	0.82	0.77	4.18	V
			High Swing	0.82	4.23	4.18	
		Mid power	Low Swing	0.82	0.75	4.18	
			High Swing	0.82	4.25	4.18	
		Low power	Low Swing	0.83	0.77	4.17	
			High Swing	0.83	4.23	4.17	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(4) Drift Determined by dividing the change in parameter at temperature extremes by the total temperature change. Value is the worst case of Ta_{MIN} to 25°C and 25°C to Ta_{MAX}.

(5) At amplifier inputs.

5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F= R_G = 1 kΩ, Fully differential input, V_S = +5 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
I_{SHORT}	Short-circuit current	Output shorted to mid-supply(6) High power	Low Swing	–25	–42		mA
			High Swing	44	72		
		Mid power	Low Swing	–16	–31		
			High Swing	34	57		
		Low power	Low Swing	–5	–13		
			High Swing	12	23		
PSRR	Power supply rejection ratio V_S ±10%	High power			117		dB
		Mid power			120		
		Low power			111		
I_S	Supply current	V_{EN} = 4.375(7)	T_A = 25°C		13	15	mA
			At the temperature extremes			17	
		V_{EN} = 3.125(7)	T_A = 25°C		7	9	
			At the temperature extremes			10	
		V_{EN} = 1.875(7)	T_A = 25°C		2	3	
			At the temperature extremes			4	
PD	Power-down mode	Disable voltage threshold(7)			<1.025		V
		Shutdown current	T_A = 25°C		0.50	0.85	mA
			At the temperature extremes			0.90	
		Enable pin current			15		µA
t_{en}	Enable time	High power			20		ns
		Mid power			22		
		Low power			50		
5-V AC CHARACTERISTICS							
SSBW	Small signal bandwidth 200 mVp-p differential	High power			114.5		MHz
		Mid power			84		
		Low power			28		
SR	Slew rate 2 Vp-p differential(8)	High power			476		V/µs
		Mid power			366		
		Low power			160		
t_{rise}	Rise time 2 Vp-p differential	High power			3.2		ns
		Mid power			4.3		
		Low power			10.8		
t_{fall}	Fall time 2 Vp-p differential	High power			3.1		ns
		Mid power			4.1		
		Low power			10.7		
t_s	0.1% settling time 2 Vp-p	2-V step, C_L = 20 pF High power			19		ns
		Mid power			24		
		Low power			48		

(6) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (–) is sinking.
(7) Enable voltage is referred to V- (negative supply voltage).
(8) Slew Rate is the average of the rising and falling edges.

5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, Avcl = +1, R_F= R_G = 1 kΩ, Fully differential input, V_S = +5 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
e_n	Input referred voltage noise	f = 10 kHz High power			4.5		nV/√Hz
		Mid power			4.8		
		Low power			8		
I_n	Input referred current noise	f = 10 kHz High power			1.8		pA/√Hz
		Mid power			1.2		
		Low power			0.6		
THD+N	Total harmonic distortion + noise 3 Vp-p at 1 KHz	High power			0.000107 %		
		Mid power			0.000114 %		
		Low power			0.000192 %		
HD2	2nd harmonic distortion 3 Vp-p, 1 KHz	High power			–125.3		dBc
		Mid power			–122.6		
		Low power			–117.0		
HD3	3rd harmonic distortion 3 Vp-p, 1 KHz	High power			–125.5		dBc
		Mid power			–130.0		
		Low power			–128.7		
5-V V_{OCM} INPUT CHARACTERISTICS							
	V_{OCM} small signal bandwidth 200 mVp-p	High power			4.4		MHz
		Mid power			2.2		
		Low power			0.56		
	V_{OCM} gain				1		V/V
	V_{OCM} offset voltage	High power			±0.46		mV
		Mid power			±0.53		
		Low power			±0.11		
	V_{OCM} voltage range	All power levels	Low Swing		1.15		V
			High Swing		3.85		
	V_{OCM} input resistance	All power levels	Low Swing		30		KΩ
			High Swing		mid-supply		

6.8 Typical Characteristics

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1 kΩ, fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.

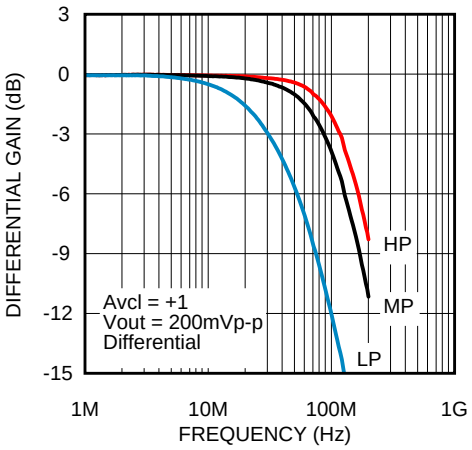


Figure 1. Frequency Response at 10 V

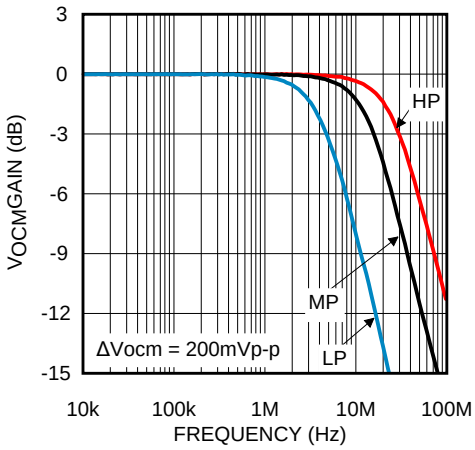


Figure 2. V_{OCM} Frequency Response at 10 V

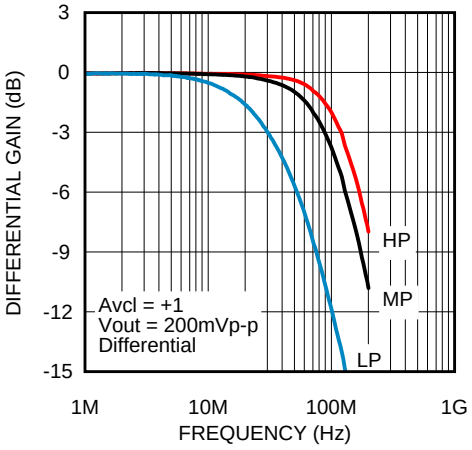


Figure 3. Frequency Response at 6.6 V

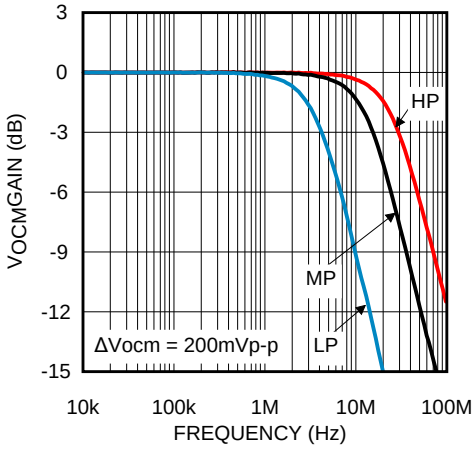


Figure 4. V_{OCM} Frequency Response at 6.6 V

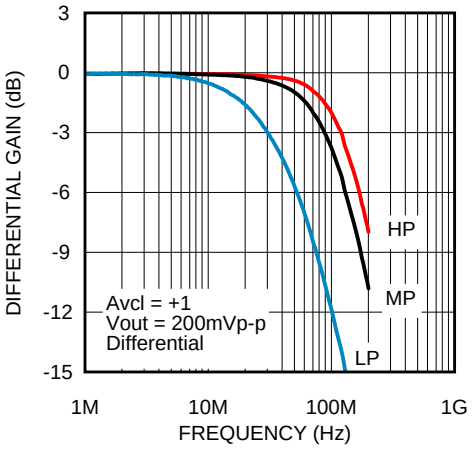


Figure 5. Frequency Response at 5 V

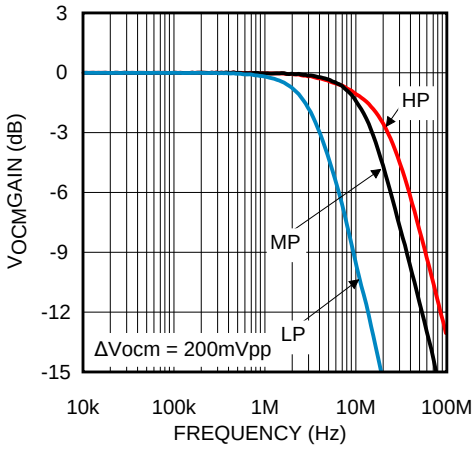


Figure 6. V_{OCM} Frequency Response at 5 V

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1 kΩ, fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.

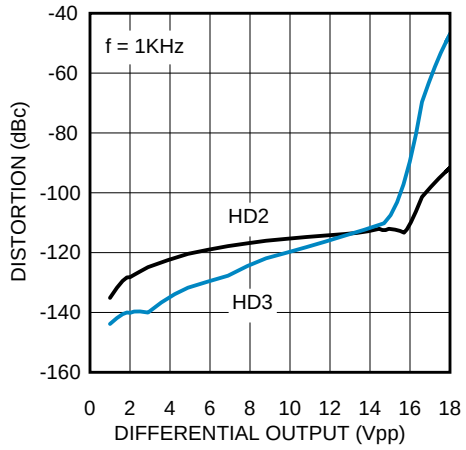


Figure 7. Distortion at 10 V, High Power

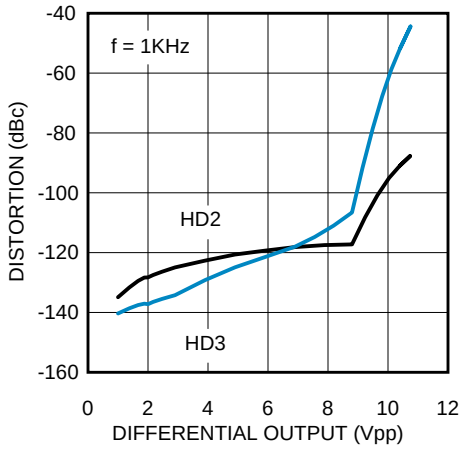


Figure 8. Distortion at 6.6 V, High Power

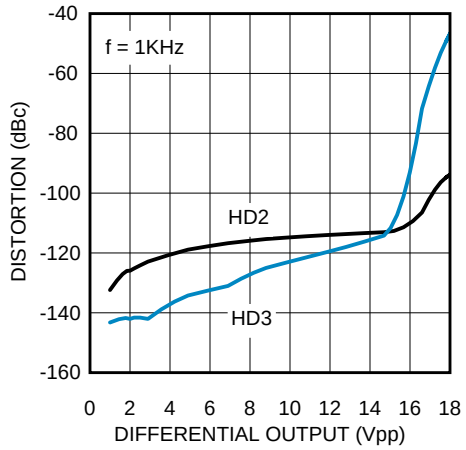


Figure 9. Distortion at 10 V, Mid Power

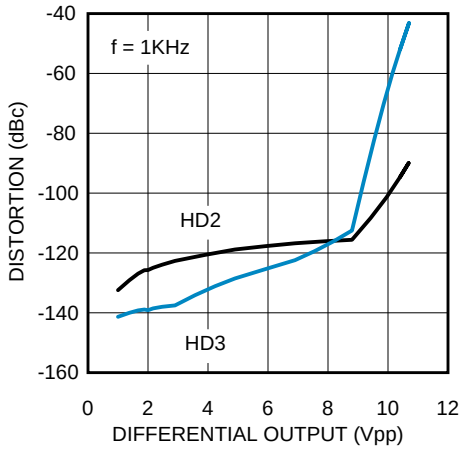


Figure 10. Distortion at 6.6 V, Mid Power

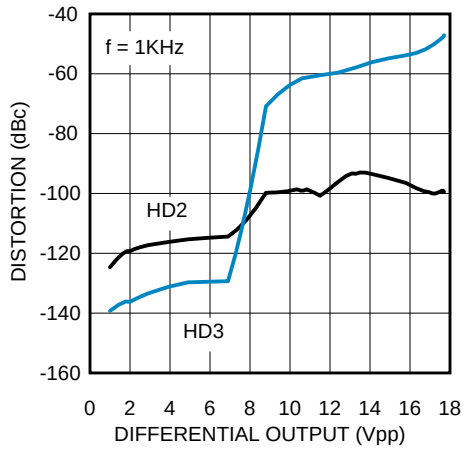


Figure 11. Distortion at 10 V, Low Power

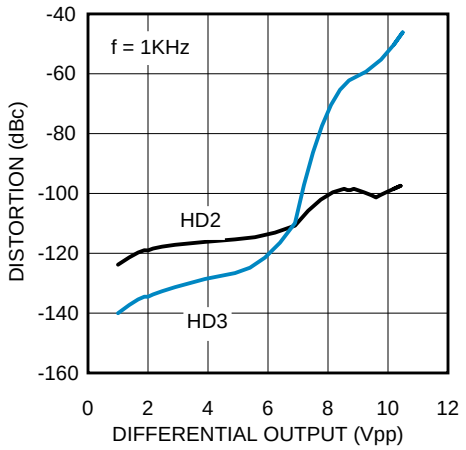


Figure 12. Distortion at 6.6 V, Low Power

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1 kΩ, fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.

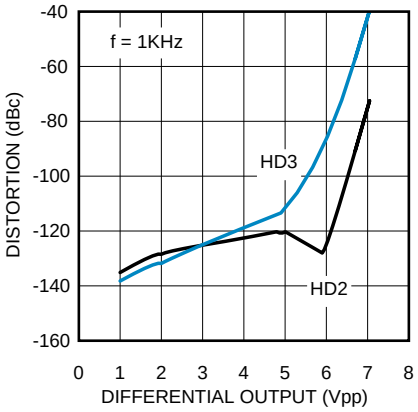


Figure 13. Distortion at 5 V, High Power

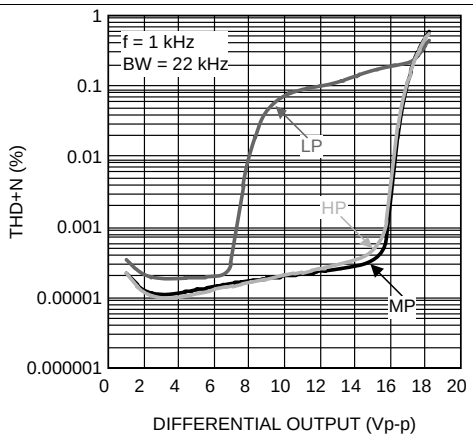


Figure 14. THD+N at 10 V

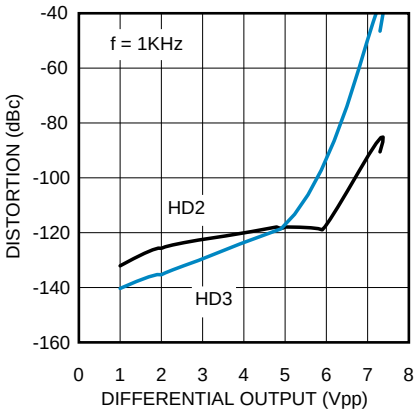


Figure 15. Distortion at 5 V, Mid Power

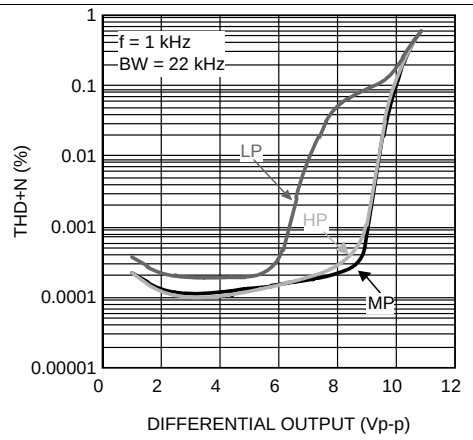


Figure 16. THD+N at 6.6 V

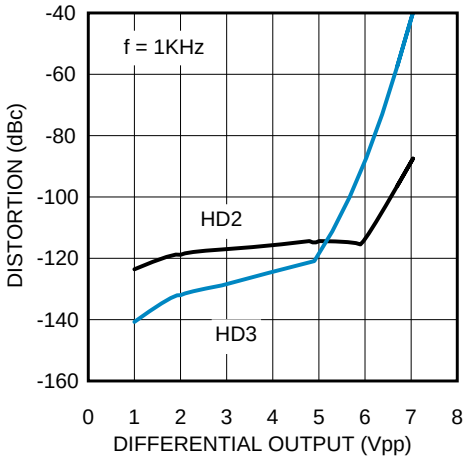


Figure 17. Distortion at 5 V, Low Power

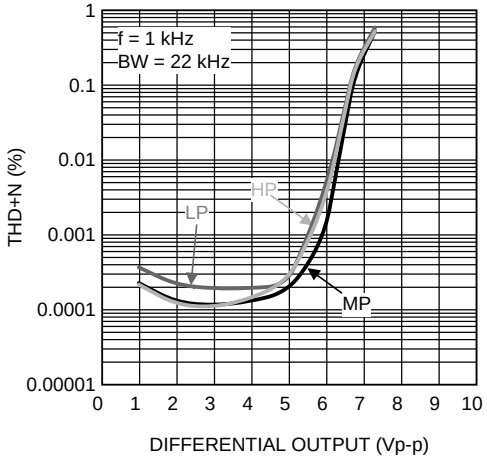


Figure 18. THD+N at 5 V

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1 kΩ, fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.

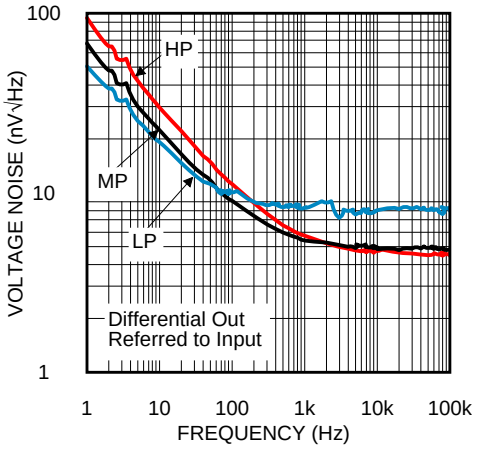


Figure 19. Voltage Noise at 10 V

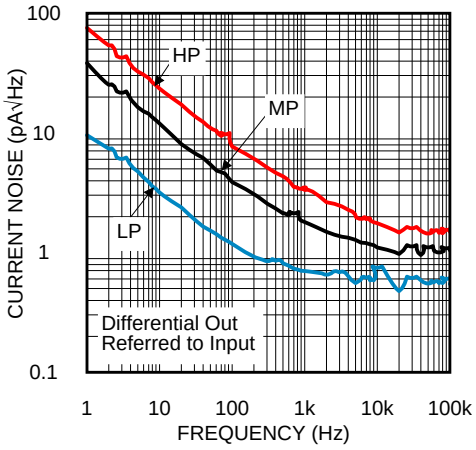


Figure 20. Current Noise at 10 V

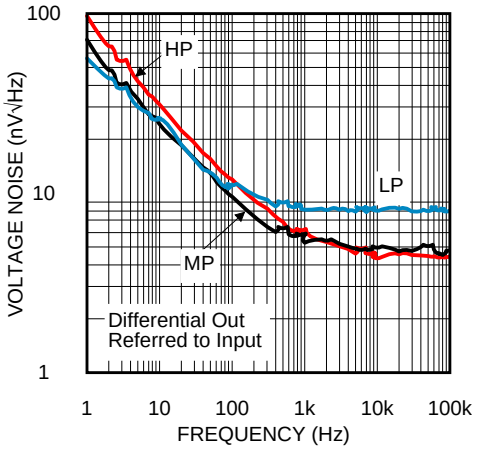


Figure 21. Voltage Noise at 6.6 V

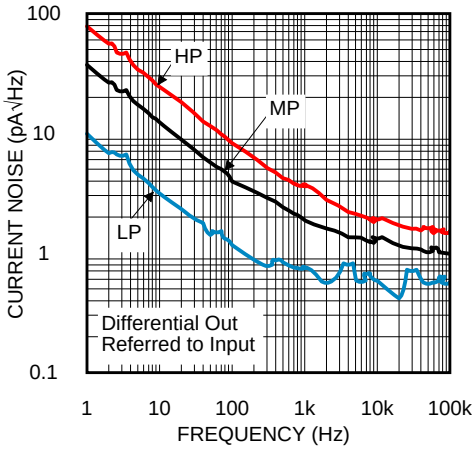


Figure 22. Current Noise at 6.6 V

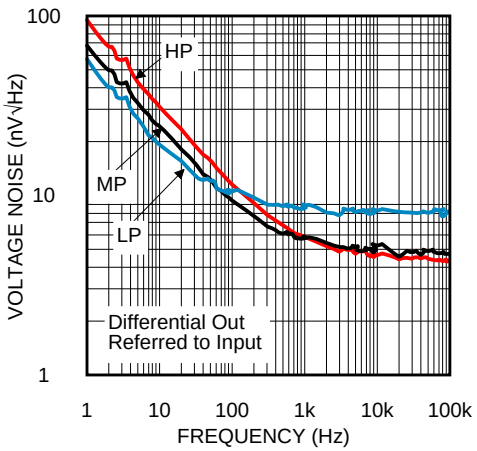


Figure 23. Voltage Noise at 5 V

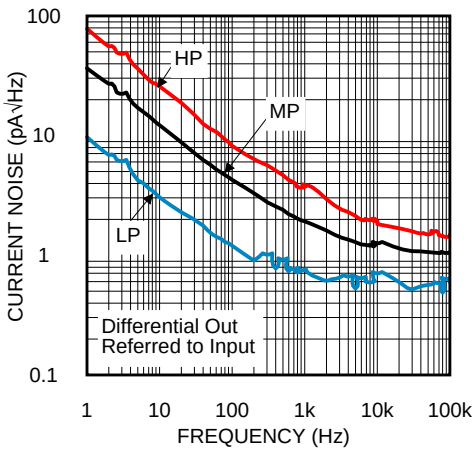


Figure 24. Current Noise at 5 V

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1 kΩ, fully differential input, V_S = +10 V, R_L = 2 kΩ//20 pF differentially, Input CMR and V_{OCM} = mid-supply and HP mode unless otherwise noted.

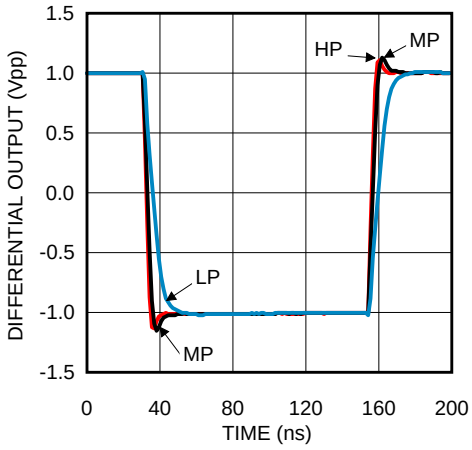


Figure 25. Pulse Response at 10 V

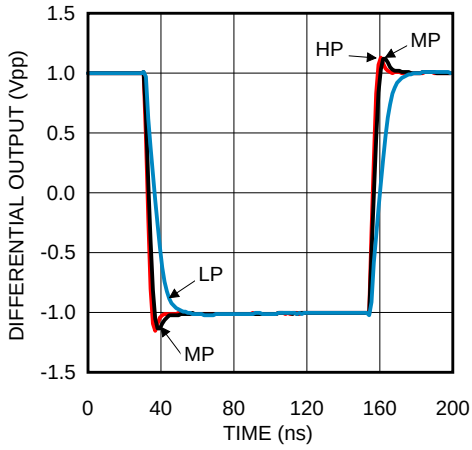


Figure 26. Pulse Response at 6.6 V

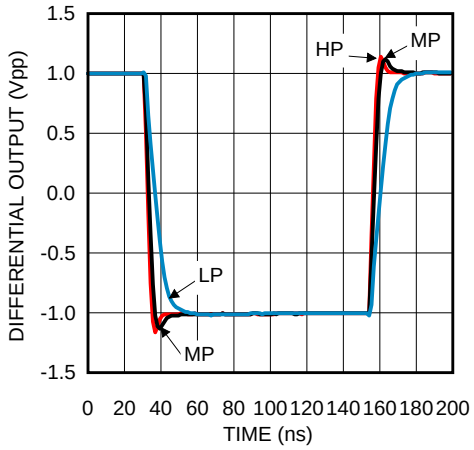


Figure 27. Pulse Response at 5 V

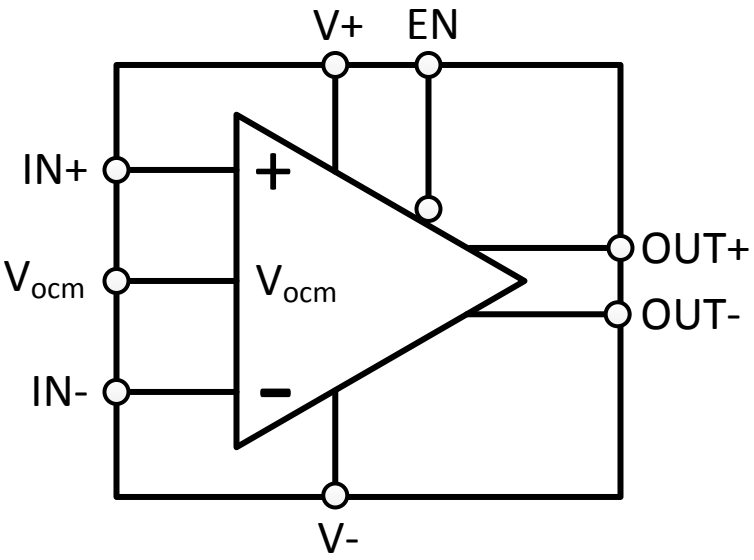
7 Detailed Description

7.1 Overview

The LMP8350 is a fully-differential voltage feedback amplifier designed to drive precision differential ADC converters. The LMP8350, though fully integrated for ultimate balance and distortion performance, functionally provides three channels. Two of these channels are the V^+ and V^- signal path channels, which function similarly to inverting mode operational amplifiers and are the primary signal paths.

The third *channel* is the common-mode (V_{OCM}) feedback circuit. This is the circuit that sets the output common mode as well as driving the V^+ and V^- outputs to be equal magnitude and opposite phase, even when only one of the two input channels is driven. The common-mode feedback circuit allows for single-ended to differential operation. The output common-mode voltage is set by applying the appropriate voltage to the V_{OCM} pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Full Bandwidth Limitations

Although the LMP8350 has a unity gain bandwidth of over 200 MHz, it is primarily intended for lower sample rate, high-precision ADCs with baseband analog input signal bandwidths in the DC to <1 MHz range (not to be confused with sampling rate). The high open-loop bandwidth of the LMP8350 is used to provide ultra low distortion and fast settling times. Maximum power bandwidth is limited by the internal output common-mode feedback path, which is limited to 1 MHz to 5 MHz. Operation with input signals above 1 MHz with near full output swings can cause random shifts in the output common mode and possible AC instabilities. For this reason, the LMP8350 is not intended to be used wide bandwidth (> 1 MHz) signal paths. Single-ended inputs rely on the common-mode signal path and will have a bandwidth limited to that of the internal common-mode buffer.

7.3.2 ESD Protection

The LMP8350 is protected against electrostatic discharge (ESD) on all pins. The LMP8350 will survive 2000-V human body model and 200-V machine model events. Under normal operation, the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMP8350 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

7.4 Device Functional Modes

7.4.1 Enable Pin and Power Mode Selection

The LMP8350 is equipped with a four-level enable (EN) pin to select one of three power modes or shutdown. These modes are selected by applying the appropriate voltage to the EN pin.

Each power level has a corresponding performance level. The high power mode will have the best overall BW and distortion performance, but at the cost of higher supply current and some DC accuracy. The low power mode has the lowest supply current, but with a noticeable loss of AC performance and output drive capabilities. The mid-power mode provides the best balance of AC and precision DC specifications. In disable mode, the amplifier is shutdown and the output stage goes into a high impedance state. Table 1 summarizes these performance trade-offs.

Table 1. Performance vs. Power Mode Summary

MODE	V_S	–3dB BW (MHz)	HD2 (dBc)	NOISE (nV/Hz)	SR (V/µS)	TYP VOS (mV)
High	10	118	–124.7	4.6	507	0.6
	6.6	116	–124.7	4.5	488	0.3
	5	114	–125.5	4.5	476	0.2
Med	10	87	–122.8	4.8	393	0.08
	6.6	85	–122.8	4.8	376	0.1
	5	84	–122.6	4.8	366	0.1
Low	10	31	–117.2	8	178	0.1
	6.6	29	–117.2	8	166	0.1
	5	28	–117	8	160	0.1

To set the mode, internally the voltage at the EN pin is compared against the total supply voltage (V_S) and sets the current consumption as shown in the table below. The EN pin voltage is referenced to the V- pin.

Table 2. Enable Pin Mode Selection

V_{EN} (V_S = V+ - V-)	POWER MODE	V_{EN} AT 10 V	V_{EN} AT 6.6 V	V_{EN} AT 5 V	I_S mA
7/8 × V_S	High	8.75	5.775	4.375	13 to 15
5/8 × V_S	Med	6.25	4.125	3.125	7 to 9
3/8 × V_S	Low	3.75	2.475	1.875	2 to 3
1/8 × V_S	Disable	1.25	0.825	0.625	< 1

The enable pin should not be allowed to float. If the enable pin is not used it can be tied to V+ to select the high power mode or set with two resistors.

Each power setting has a ±400-mV tolerance at each level, though TI recommends to keep the set voltage within the center of the range as performance may vary near the transition zones.

During shutdown, both outputs are in a high impedance state, so the feedback and gain set resistors will then set the input and output impedance of the circuit. For this reason input to output isolation will be poor in the disabled state.

The voltage at the EN pin can be generated with a resistive voltage divider or a buffer connected to a voltage source or a DAC. Figure 34 shows how to generate EN voltage with a resistive voltage divider.

Values of R_A and R_B can be calculated to achieve the voltages in Table 2, however their sum should be below 50 kΩ to keep the voltage at the enable pin stable. Recommended values for R_A and R_B are given in Table 3.

Table 3. Recommended R_A and R_B for Mode Selection

MODE	10 V	6.6 V	5 V	V_{EN}
High Power	R_A = 0 R_B = inf	R_A = 0 R_B = inf	R_A = 0 R_B = inf	> 7/8 V_S
Mid Power	R_A = 18 K R_B = 30 K	R_A = 18 K R_B = 30 K	R_A = 18 K R_B = 30 K	5/8 V_S
Low Power	R_A = 33 K R_B = 18 K	R_A = 33 K R_B = 18 K	R_A = 33 K R_B = 18 K	3/8 V_S
Shutdown	R_A = Inf R_B = 0	R_A = Inf R_B = 0	R_A = Inf R_B = 0	< 1/8 V_S

7.4.2 V_{OCM} Pin and Output Common-Mode Setting

Output common-mode voltage is set by the V_{OCM} pin. Both outputs will be offset in the same direction (phase) by an amount equal to the applied V_{OCM} voltage.

The V_{OCM} pin, if left unconnected, will self-bias to mid-supply. Two internal 60-kΩ resistors set this midpoint. These resistors are shown in Figure 28.

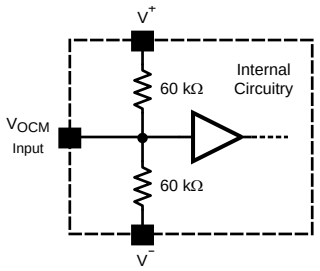


Figure 28. V_{OCM} Internal Bias Circuit

The equivalent resistance looking into the V_{OCM} pin will look like 30 kΩ to mid-supply, plus about ±700 nA for internal base currents (which scales with power mode and supply current). If left floating, the V_{OCM} input should be bypassed to ground with a 0.1-µF ceramic capacitor.

If a different output common-mode voltage is desired, the V_{OCM} pin should be driven by a clean, low impedance source to override the internal divider resistors. The V_{OCM} pin should be bypassed to ground with a 0.1-µF ceramic capacitor. It should be noted that any signal or noise-coupling into the V_{OCM} will be passed as common-mode noise and may result in the loss of dynamic range, degraded CMRR, degraded balance and higher distortion. The V_{OCM} pin is primarily intended as a DC bias path and is not intended for use as a signal path.

For applications that can tolerate slight shifts in the V_{OCM}voltage over temperature, it is also possible to use a single resistor to program the V_{OCM} voltage by paralleling one of the internal resistors to change the ratio.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Fully-Differential Operation

The LMP8350 will perform best when used with split supplies and in a fully-differential configuration. See Figure 29 for recommend circuits.

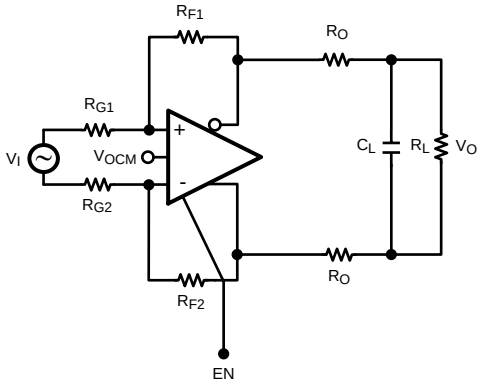


Figure 29. Typical Fully-Differential Application

The circuit shown in Figure 29 is a typical fully-differential application as might be used to drive a Sigma Delta ADC. In this circuit, closed-loop gain is calculated by Equation 1:

$$(A_V) = V_{OUT}/ V_{IN} = R_F/R_G$$

where

- $R_F=R_{F1}=R_{F2}$ and $R_G=R_{G1}=R_{G2}$ (1)

For all the applications in this data sheet , V_{IN} is presumed to be the voltage presented to the circuit by the signal source. For differential signals this will be the difference of the signals on each input (which will be double the magnitude of each individual signal), while in single-ended inputs it will just be the driven input signal.

When fed with a differential signal, the LMP8350 provides excellent distortion, balance and common-mode rejection, provided the resistors R_F, R_G and any input termination resistors (R_T) are well-matched and strict symmetry is observed in board layout. With a DC CMRR of over 80 dB, the DC and low frequency CMRR of most circuits will be dominated by the external resistor matching and board trace resistance. At low distortion levels, board layout symmetry and supply bypassing become a factor as well. It is assumed throughout this document that $R_{F1} = R_{F2}$ and $R_{G1} = R_{G2}$ for maximum channel symmetry

Precision resistors of at least 0.1% accuracy or better are recommended and careful board layout will also be required for optimum performance.

Operation with R_F feedback resistors as low as 300 Ω is possible in the high and medium power modes. This will slightly improve the noise and bandwidth results. However, feedback resistors with R_F values of less than 1 KΩ should be avoided in the low power mode due to the reduced output drive current capabilities. If low value resistors (< 300 Ω) must be used in the low power mode, the maximum output swing will need to be limited.

The resistors R_O help keep the amplifier stable when presented with a load C_L, as is common when driving an analog to digital converter (ADC).

Application Information (continued)

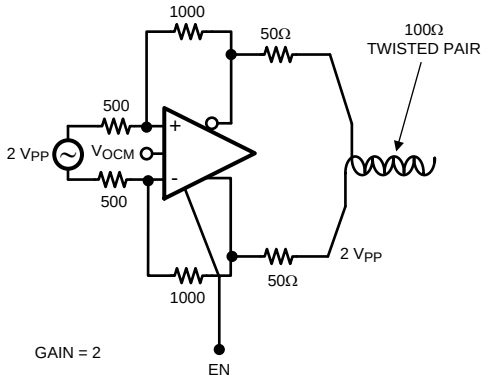


Figure 30. Fully-Differential Cable Driver

With up to 15 V_{PP} differential output voltage swing and 80 mA of linear drive current, the LMP8350 makes an excellent precision cable driver as shown in Figure 30. The LMP8350 is also suitable for driving differential cables from a single-ended source.

8.1.2 Single Supply Operation

As shown in Figure 31, the input common-mode voltage is less than the output common voltage. It is set by current flowing through the feedback network from the device output. The input common-mode voltage range places constraints on gain settings. The input common-mode voltage is calculated in Equation 2. Possible solutions to this limitation include AC coupling the input signal, using split power supplies and limiting stage gain. AC coupling with single-supply is shown in Figure 32.

V_{ICM}= Input common-mode voltage = $(V^+_{IN} + V^-_{IN})/2$. (2)

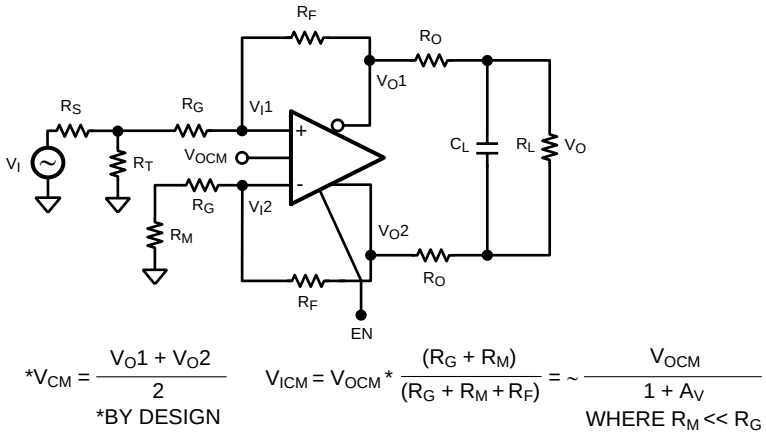


Figure 31. Relating A_V to Input/Output Common-Mode Voltages

In Figure 31 the differential closed loop gain is = A_V= R_F/R_G.

NOTE

In single-ended to differential operation V_{IN} is measured single ended while V_{OUT} is measured differentially. This means that gain is really one-half, or 6 dB, less when measured on either of the output pins separately.

Application Information (continued)

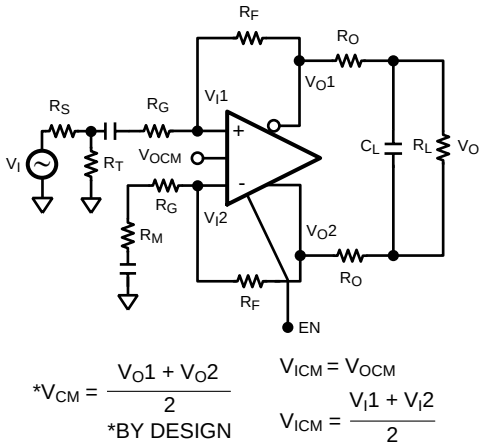


Figure 32. AC Coupled for Single-Supply Operation

8.1.3 Driving Analog to Digital Converters

Analog to digital converters (ADC) present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. Figure 33 shows a typical circuit for driving an ADC. The two resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors form part of a lowpass filter which helps to provide anti alias and noise reduction functions. The C_S capacitor helps to smooth the current spikes associated with the internal switching circuits of the ADC and also are a key component in the lowpass filtering of the ADC input. The capacitor should be a low distortion capacitor, such as an NPO, to avoid causing significant distortion terms. In the circuit of Figure 33, the cutoff frequency of the filter is calculated by Equation 3. This should be slightly less than the sampling frequency.

$$1 / (2 \times \pi \times (R_{ISO1} + R_{ISO2}) \times (C_S + C_{CONVERTER})) \quad (3)$$

NOTE

The ADC input capacitance must be factored into the frequency response of the input filter. Also as shown in Figure 33, the input capacitance to many ADCs is variable based on the clock cycle. For lower-speed, precision ADC's, the external cap is generally sized to ten times the internal sampling capacitor value. See the data sheet for your particular ADC for details.

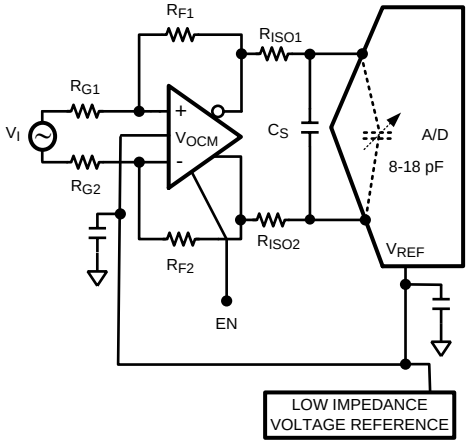


Figure 33. Driving an ADC

Application Information (continued)

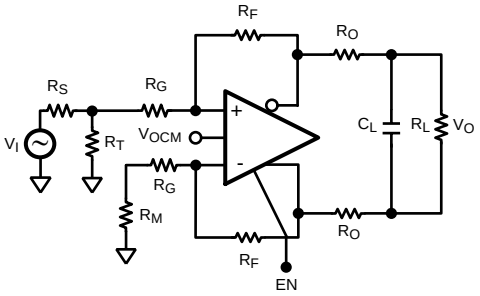
The amplifier and ADC muist be located as close together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces, and the ADC is sensitive to high-frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the Nyquist range (DC to Fs/2). See AN-236 (SNAA079) for more details on the subsampling process and the requirements this imposes on the filtering necessary in your system.

8.1.4 Capacitive Drive

As noted in the *Driving Analog to Digital Converters* section, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500 Ω or higher. A typical ADC has capacitive components of around 8 to 18 pF, and the resistive component could be 1000 Ω or higher. If driving a transmission line, such as a twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance.

8.2 Typical Application

Figure 34 shows a typical application where an LMP8350 is used to produce a differential signal from a single-ended source.



$$\text{SET } R_M = R_T \| R_S$$

$$\text{SET } R_T = \frac{1}{\left(\frac{1}{R_S} - \frac{1}{R_{IN}}\right)} \qquad R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2 * (R_F + R_G)}\right)}$$

Figure 34. Single-Ended in Differential Out

8.2.1 Design Requirements

Compared to a differential input, using a single-ended input will reduce gain by 1/2, so that the closed-loop gain will be calculated by Equation 4:

$$\text{Gain} = A_v = 0.5 \times R_F / R_G \tag{4}$$

In single-ended input operation the output common-mode voltage is set by the V_{OCM} pin. Also, In this mode the common-mode feedback circuit must recreate the signal that is not present on the unused differential input pin. The common-mode feedback circuit is responsible for ensuring balanced output with a single-ended input.

Balance error is defined as the amount of input signal that couples into the output common mode. It is measured as the undesired output common-mode swing divided by the signal on the input. Balance error can be caused by either a channel to channel gain error, or phase error. Either condition will produce a common-mode shift. The overall bandwidth is limited due to the V_{OCM} buffer bandwidth limitations in this configuration.

Supply and V_{OCM} pin bypassing are also critical in this mode of operation.

8.2.2 Detailed Design Procedure

For a single-ended input differential output configuration Figure 34, component value selection is dictated by the gain and input resistance desired. Figure 35 shows the OUT+ and OUT– relative to the single ended voltage signal input +. Depending on the feedback resistor values, the amplitude gain of the OUT+ and OUT– will vary.

Typical Application (continued)

8.2.3 Application Curve

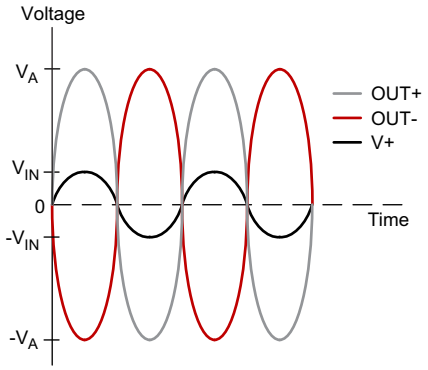


Figure 35. Single-Ended In Differential Out Amplitude vs Time Waveform

9 Power Supply Recommendations

9.1 Power Supply and V_{OCM} Bypassing

The LMP8350 requires supply bypassing capacitors as shown in Figure 36 and Figure 37 for fastest settling time and overall stability.

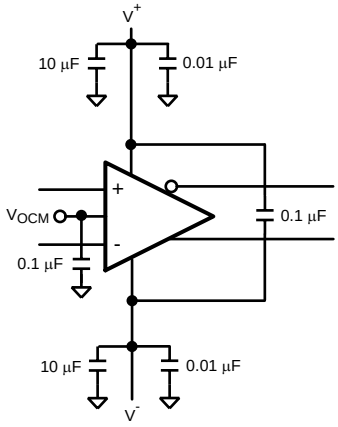


Figure 36. Split-Supply Bypassing Capacitors

The 0.01-µF and 0.1-µF capacitors should be leadless surface mount (SMT) ceramic capacitors and should be no more than 3 mm from the supply pins. The SMT capacitors should be connected directly to a ground plane. Thin traces or small vias will reduce the effectiveness of bypass capacitors.

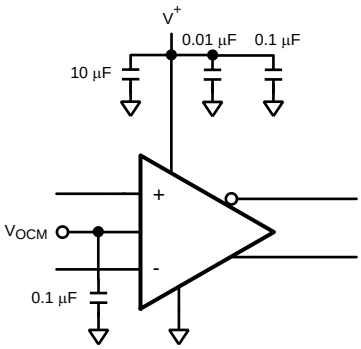


Figure 37. Single-Supply Bypassing Capacitors

Also shown in Figure 36 and Figure 37 is a capacitor from the V_{OCM} pin to ground. The V_{OCM} pin sets the output common-mode voltage. Any noise on this input is transferred directly to the output. The V_{OCM} pin should be bypassed even if the pin in not used. There is an internal resistive divider on chip to set the output common-mode voltage to the midpoint of the supply pins. The impedance looking into this pin is approximately 30 kΩ. If a different output common-mode voltage is desired drive this pin with a clean, accurate voltage reference.

10 Layout

10.1 Layout Guidelines

While the main signal path frequencies may be fairly low, the ultra low distortion and settling time specifications rely on wide internal bandwidths. Precautions usually taken for high-speed amplifiers should be followed to maintain the best settling times and lowest distortion specifications. In order to get maximum benefit from the differential circuit architecture, board layout and component selection is very critical. The circuit board should have low a inductance ground plane and well bypassed broad supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3-4 mm of the amplifier as should the supply bypass capacitors.

The LMP8350 is sensitive to parasitic capacitances on the outputs. Ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G.

With any differential signal path symmetry is very important. Even small amounts of asymmetry will contribute to distortion and balance errors. Special attention should be paid to where the bypass capacitors are grounded, as this also affects settling and distortion performance.

The LMH730154 evaluation board is an example of good layout techniques. Evaluation boards are available for purchase through the product folder on TI's website.

10.2 Layout Example

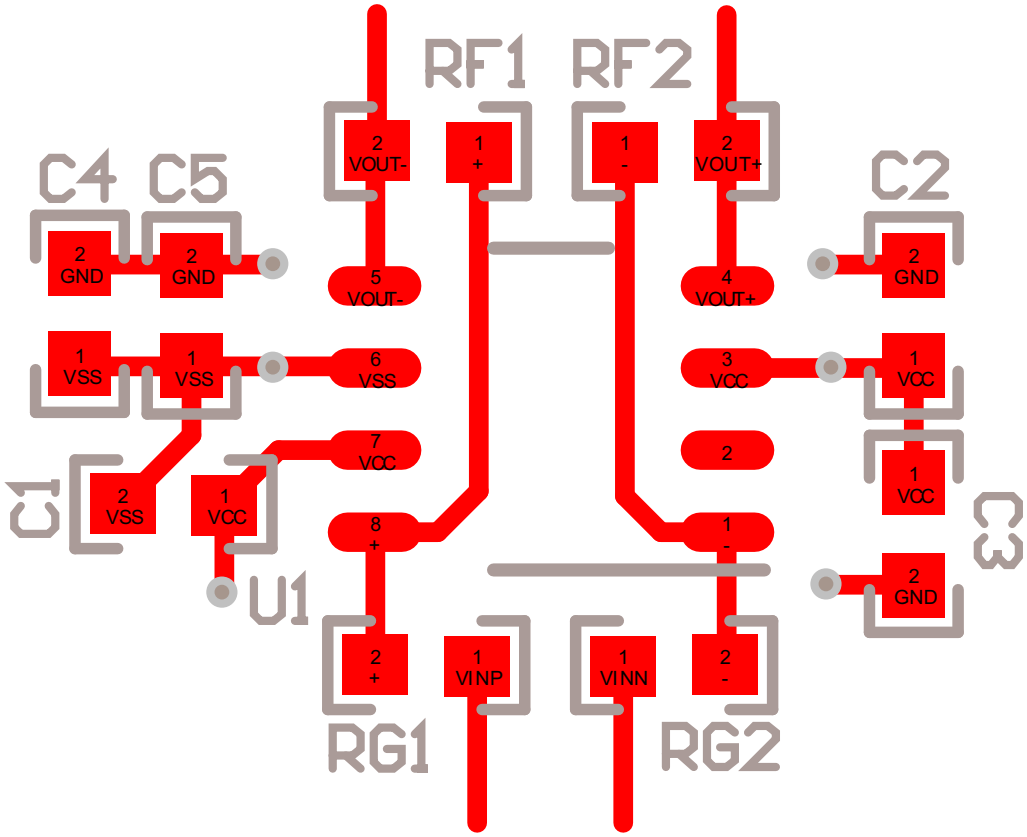


Figure 38. Layout Example

10.3 Power Dissipation

The LMP8350 is optimized for maximum performance in the small form factor of the standard SOIC package, and is essentially a dual-channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} of 150°C is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMP8350:

1. Calculate the quiescent (no-load) power using Equation 5 (Be sure to include any current through the feedback network if V_{OCM} is not mid-rail.):

   $$P_{AMP} = I_{CC} \times (V_S) \quad (5)$$

   where

   - $V_S = V^+ - V^-$.

2. Calculate the RMS power dissipated in each of the output stages using Equation 6:

   $$P_D\,(rms) = rms\,((V_S - V^+_{OUT}) \times I^+_{OUT}) + rms\,((V_S - V^-_{OUT}) \times I^-_{OUT}) \quad (6)$$

   where

   - V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage.

3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMP8350 package can dissipate at a given temperature can be derived from Equation 7:

$$P_{MAX} = (150° - T_{AMB})/\,\theta_{JA} \quad (7)$$

where

- T_{AMB} = Ambient temperature (°C)
- and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package θ_{JA} is 150°C/W.

NOTE

If V_{OCM} is not 0 V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

10.4 Evaluation Board

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 (SNOA367) for more information). Texas Instruments suggests the following evaluation boards in Table 4 as a guide for high-frequency layout and as an aid in device testing and characterization:

Table 4. Evaluation Board Guide

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LMP8350MA	SOIC	LMH730154

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering*, SNOA549
- AN-236 *An Introduction to the Sampling Theorem*, SNAA079
- OA-15 *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, SNOA367

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

LMP, E2E are trademarks of Texas Instruments.
PowerWise is a trademark of National Semiconductor Corporation.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP8350MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMP83 50MA
LMP8350MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMP83 50MA
LMP8350MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMP83 50MA
LMP8350MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMP83 50MA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

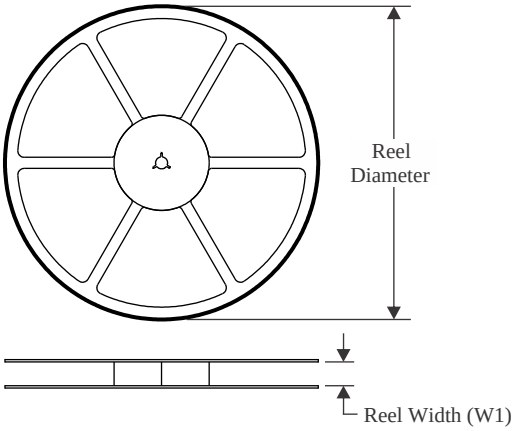
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

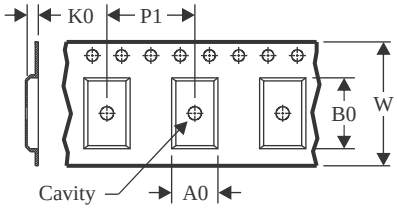
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

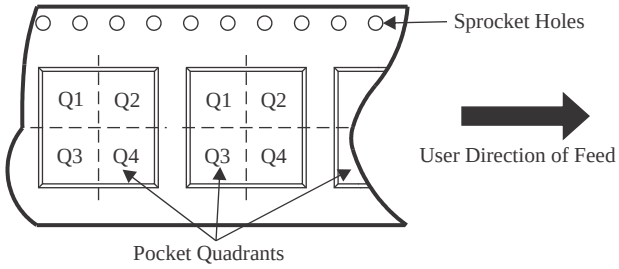


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

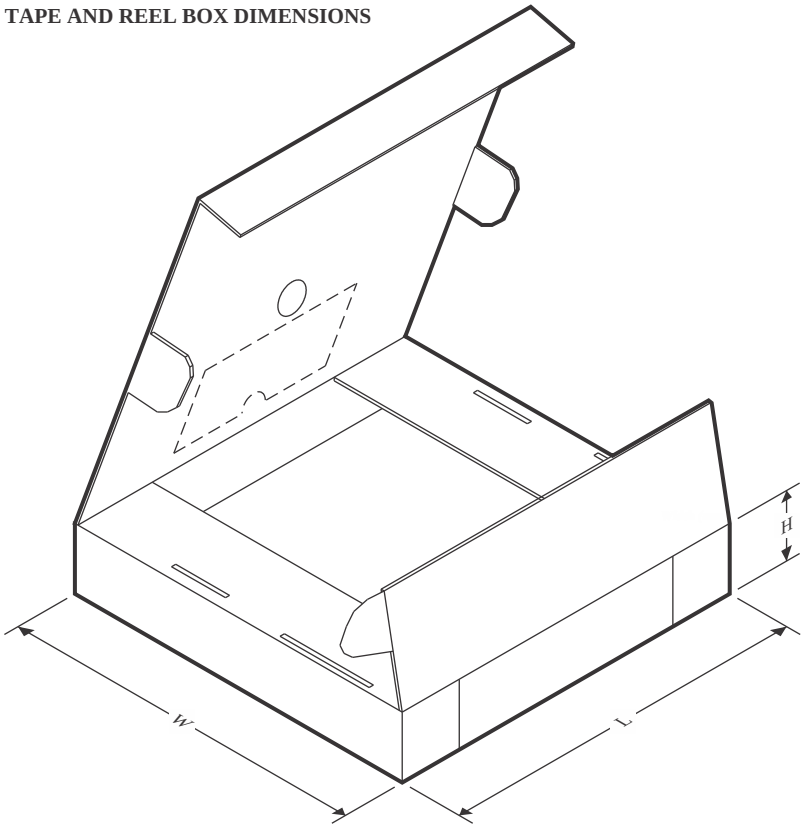
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8350MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

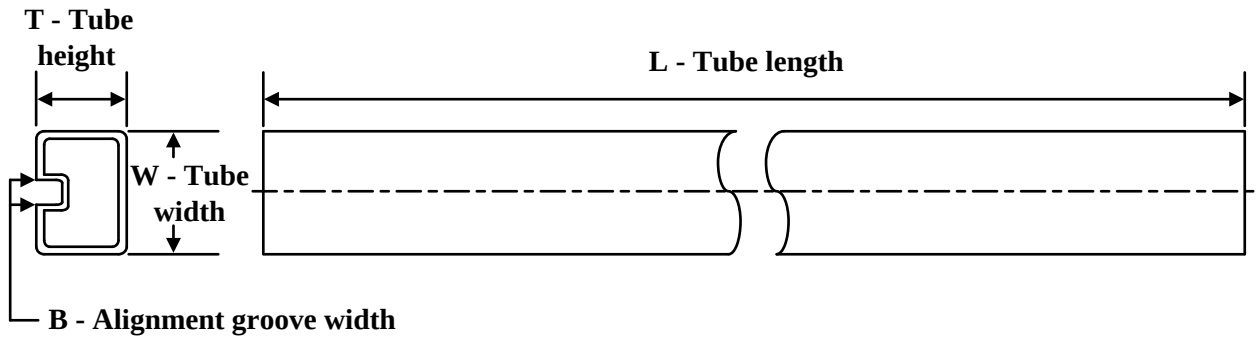
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

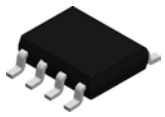
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8350MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP8350MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP8350MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

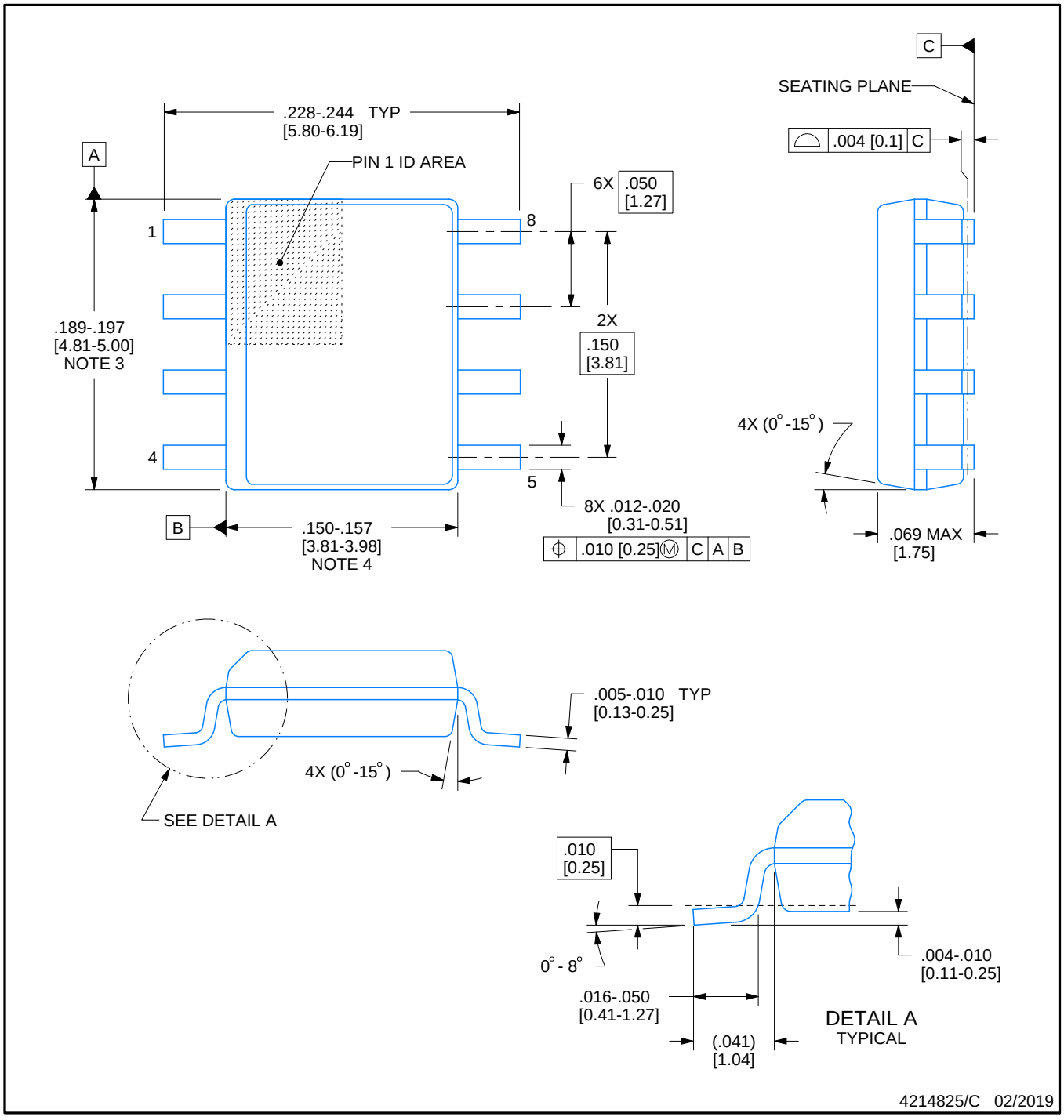


PACKAGE OUTLINE

D0008A

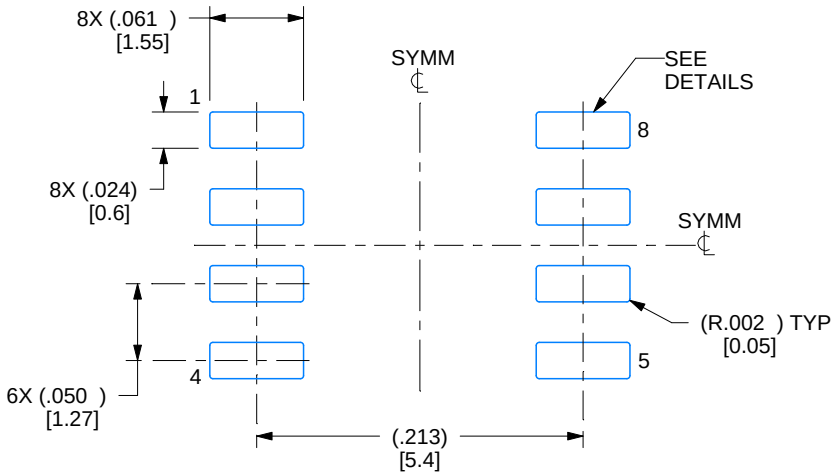
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

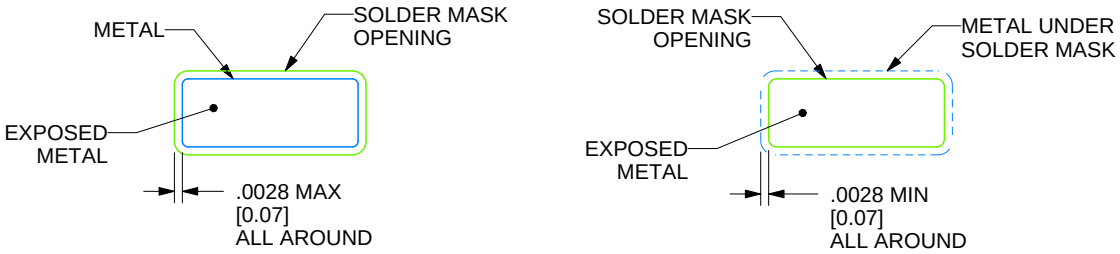


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

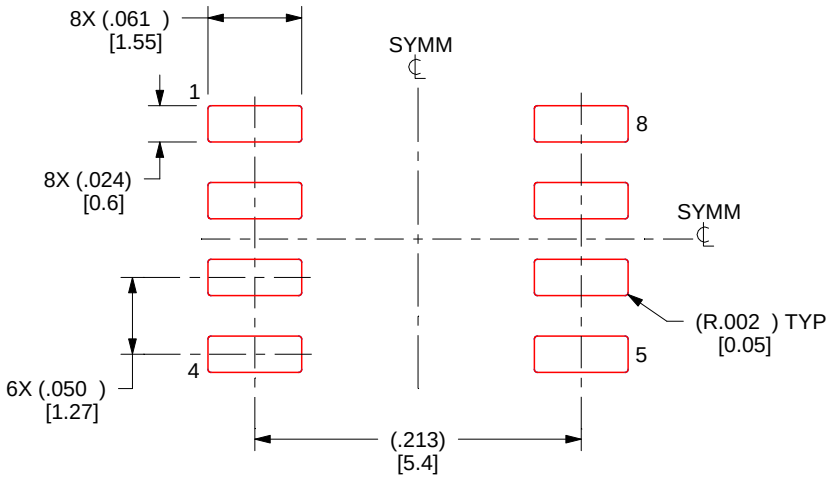
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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