采用 WSON 封装的 LMR10530 5.5V、3A、1.5MHz 或 3MHz 降压稳压器

1 特性

- 输入电压范围：3V 至 5.5V
- 输出电压范围：0.6V 至 4.5V
- 1.5MHz (LMR10530X) 和 3MHz (LMR10530Y) 开关频率
- 3A 稳定状态输出电流
- 低关断 I_Q，典型值为 300nA
- 56mΩ PMOS 开关
- 内部软启动
- 内部补偿峰值电流模式控制
- 逐周期电流限制和热关断
- WSON (3 × 3 × 0.8mm) 封装
- 使用 LMR10530 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 从 3.3V 和 5V 电源轨到负载点的转换
- 空间受限型 应用

3 说明

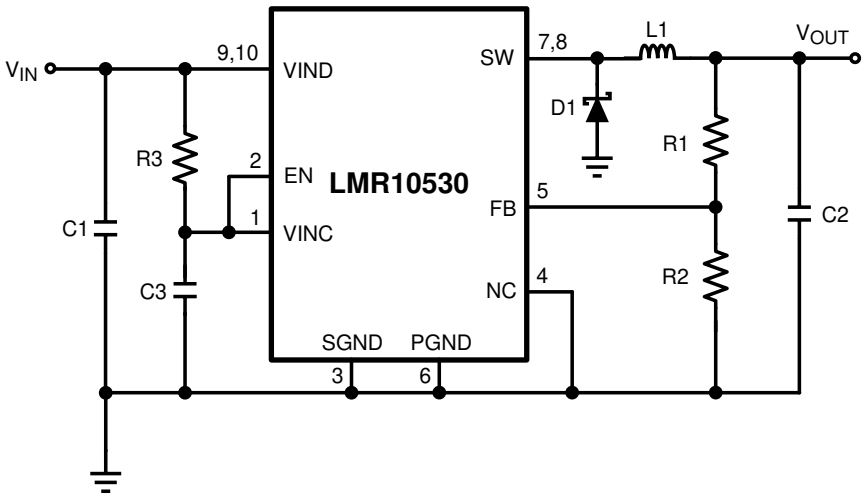
LMR10530 稳压器是一款采用 10 引脚 WSON 封装的单片、高频、PWM 降压直流/直流转换器。该器件包含所有有效功能，从而在尽可能最小的 PCB 区域内提供具有快速瞬态响应和精确调节功能的本地直流/直流转换。LMR10530 具有最少的外部组件，因而易于使用。该器件能够通过采用最先进的 0.5µm BiCMOS 技术的内部 56mΩ PMOS 开关来驱动 3A 负载，从而实现最佳的功率密度。该控制电路可实现低至 30ns 的导通时间，从而在整个 3V 至 5.5V 输入工作范围内支持极高频转换，最低输出电压为 0.6V。开关频率在内部设置为 1.5MHz 或 3MHz，从而允许使用极小的表面贴装电感器和电容器。尽管工作频率很高，但仍可以轻松实现高达 93% 的效率。包括外部关断功能，该功能具有 300nA 的超低待机电流。LMR10530 利用峰值电流模式控制和内部补偿在各种运行条件下提供高性能调节。其他 功能 包括用于减小浪涌电流的内部软启动电路、逐周期电流限制、频率折返、热关断和输出过压保护。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMR10530	WSON (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (April 2013) to Revision B **Page**

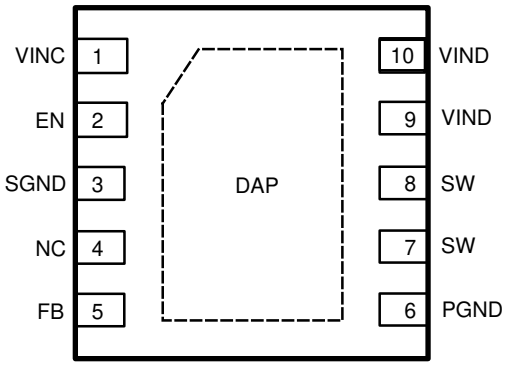
- 仅有编辑更改；添加了 WEBENCH 链接 1

Changes from Original (April 2013) to Revision A **Page**

- 已更改 将美国国家半导体数据表的布局更改为 TI 格式 1

5 Pin Configuration and Functions

DSC Package
10-Pin WSON
Top View



Pin Descriptions

PIN		DESCRIPTION
NO.	NAME	
1	VINC	Input supply for internal bias and control circuitry. Need to locally bypass this pin to GND.
2	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or subject to voltages greater than V_{IN} + 0.3V.
3	SGND	Signal (analog) ground. Place the bottom resistor of the feedback network as close as possible to this pin for good load regulation.
4	NC	No user function, connect this pin to GND.
5	FB	Feedback pin. Connect this pin to the external resistor divider to set output voltage.
6	PGND	Power ground pin. Provides ground return path for the internal driver.
7, 8	SW	Switch pins. Connect these pins to the inductor and catch diode.
9, 10	VIND	Input supply voltage. Connect a bypass capacitor locally from these pins to PGND.
DAP	Die Attach Pad	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.

6 Specifications

6.1 Absolute Maximum Ratings

See notes(1)(2).

VINC, VIND	-0.5V to 7V
FB Voltage	-0.5V to 3V
EN Voltage	-0.5V to V_{IN}+o.3V
SW Voltage	-0.5V to 7V
ESD Susceptibility(3)	2kV
Junction Temperature(4)	150°C
Storage Temperature	-65°C to +150°C
Soldering Information Infrared/Convection Reflow (15 sec)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF.
(4) Thermal shutdown occurs if the junction temperature exceeds the maximum junction temperature of the device.

6.2 Recommended Operating Ratings

VINC, VIND	3V to 5.5V
Junction Temperature	-40°C to +125°C

6.3 Electrical Characteristics

Unless otherwise specified under the **Conditions** column, V_{IN} = 5 V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback Voltage	WSON-10 Package	**0.588**	0.600	**0.612**	V
$\Delta V_{FB}/(\Delta V_{IN} x V_{FB})$	Feedback Voltage Line Regulation	V_{IN} = 3V to 5.5V		0.08		%/V
I_B	Feedback Input Bias Current			0.1	**100**	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.70	**2.90**	V
		V_{IN} Falling	**1.85**	2.35		
	UVLO Hysteresis			0.35		V
f_{SW}	Switching Frequency	LMR10530X	**1.1**	1.5	**1.95**	MHz
		LMR10530Y	**2.25**	3.0	**3.75**	
D_{MAX}	Maximum Duty Cycle	LMR10530X	**86%**	95%		
		LMR10530Y	**80%**	90%		
D_{MIN}	Minimum Duty Cycle	LMR10530X		5%		
		LMR10530Y		7%		
$R_{DS(ON)}$	Switch On Resistance			58	**90**	mΩ
I_{CL}	Switch Current Limit		**3.4**	4.4		A
V_{EN_TH}	Enable Threshold Voltage		**1.8**			V
	Shutdown Threshold Voltage				**0.4**	
I_{SW}	Switch Leakage			100		nA
I_{EN}	Enable Pin Current	Sink/Source		100		nA
I_Q	Quiescent Current (switching)	LMR10530X, V_{FB} = 0.55		3.2	**5**	mA
		LMR10530Y, V_{FB} = 0.55		4.3	**6.5**	
	Quiescent Current (shutdown)	All Options V_{EN} = 0V		300		nA
V_{FB_F}	FB Frequency Foldback Threshold	All Options		0.32		V
f_{FB}	Foldback Frequency	LMR10530X, V_{FB} = 0V		400		kHz
		LMR10530Y, V_{FB} = 0V		800		
θ_{JA}	Junction to Ambient 0 LFPM Air Flow (1)			53		°C/W
θ_{JC}	Junction to Case (1)			12		°C/W
T_{SD}	Thermal Shutdown Threshold (2)	Junction Temperature Rising		165		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	Junction Temperature Falling		15		°C

(1) Applies for packages soldered directly onto a 4” × 3” 4-layer standard JEDEC board in still air.
(2) Thermal shutdown occurs if the junction temperature exceeds the maximum junction temperature of the device.

6.4 Typical Characteristics

Unless otherwise specified, V_{IN} = 5 V and T_A = 25°C

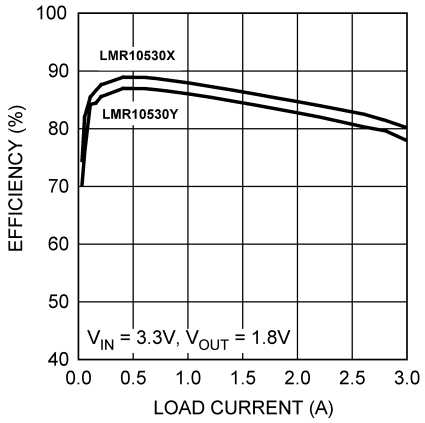


Figure 1. Efficiency vs Load Current - Both Options

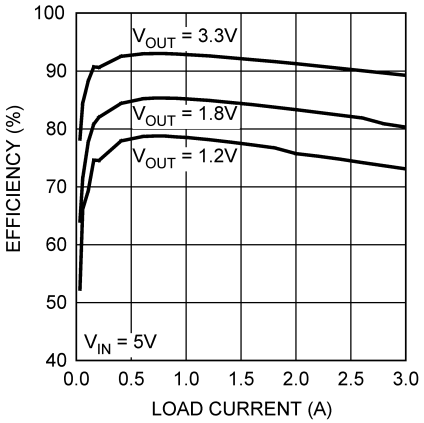


Figure 2. Efficiency vs Load Current - LMR10530X

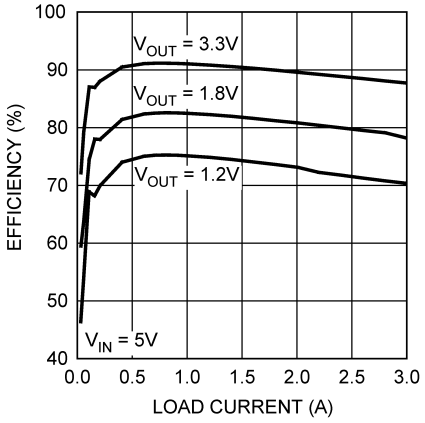


Figure 3. Efficiency vs Load Current - LMR10530Y

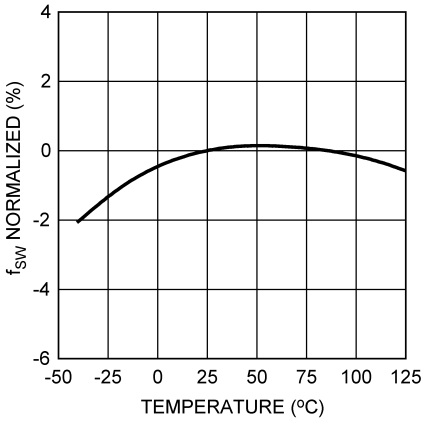


Figure 4. Oscillator Frequency vs Temperature - LMR10530X

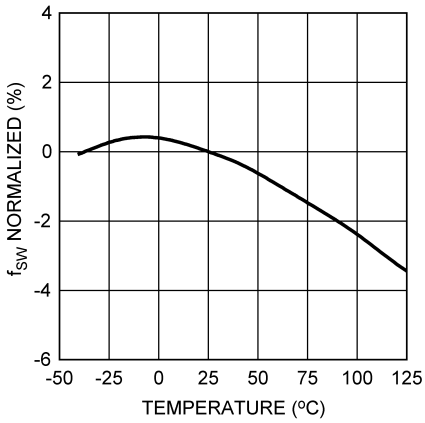


Figure 5. Oscillator Frequency vs Temperature - LMR10530Y

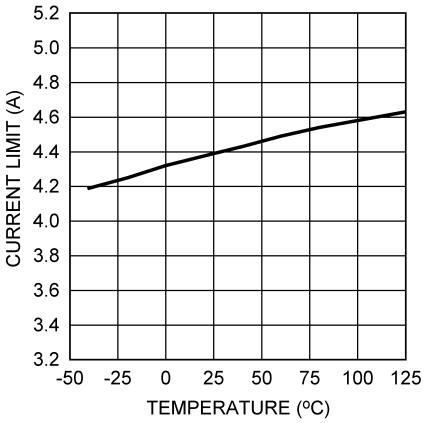


Figure 6. Current Limit vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 5 V and T_A = 25°C

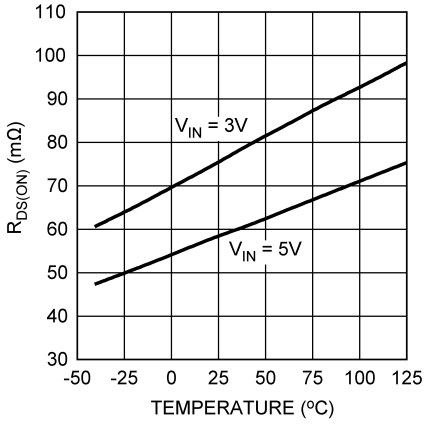


Figure 7. $R_{DS(ON)}$ vs Temperature

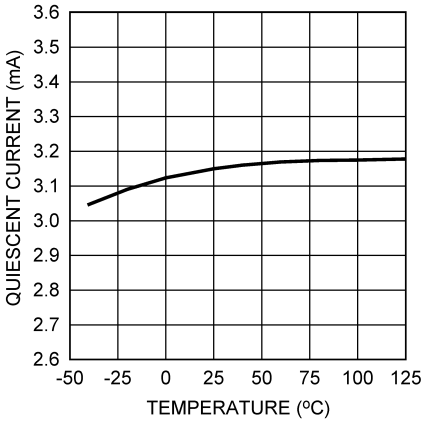


Figure 8. LMR10530X I_Q (Switching)

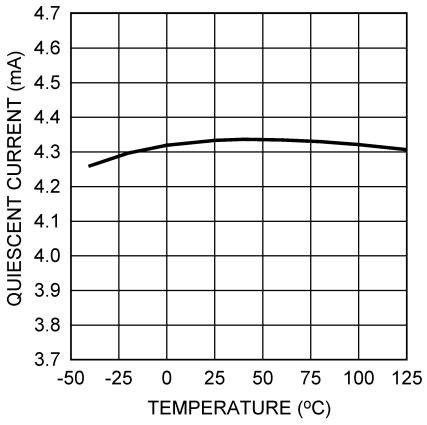


Figure 9. LMR10530Y I_Q (Switching)

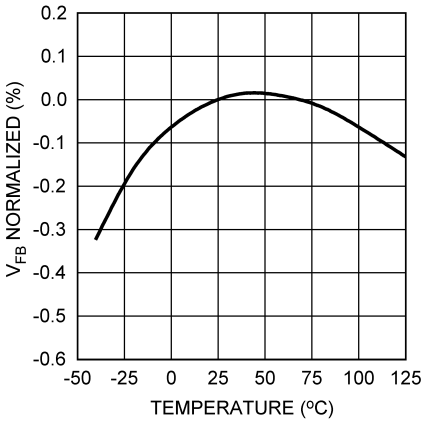


Figure 10. V_{FB} vs Temperature

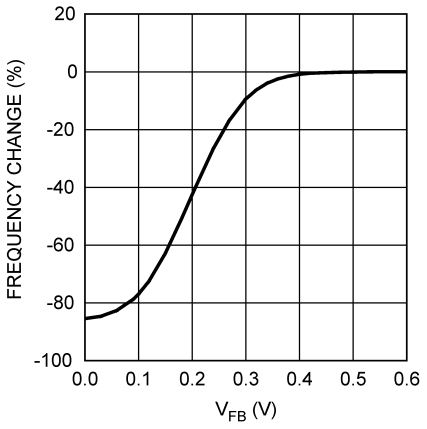


Figure 11. Frequency Foldback

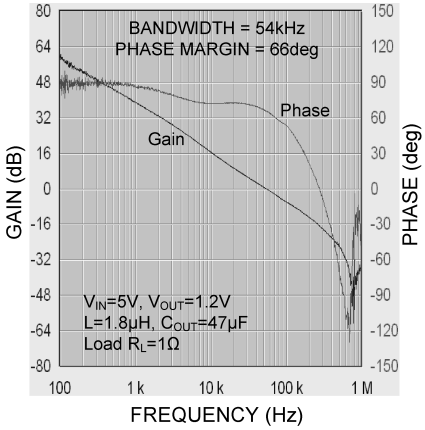


Figure 12. Loop Gain and Phase - LMR10530X

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 5 V and T_A = 25°C

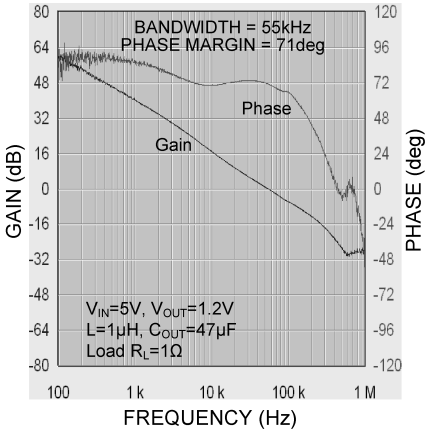


Figure 13. Loop Gain And Phase - LMR10530Y

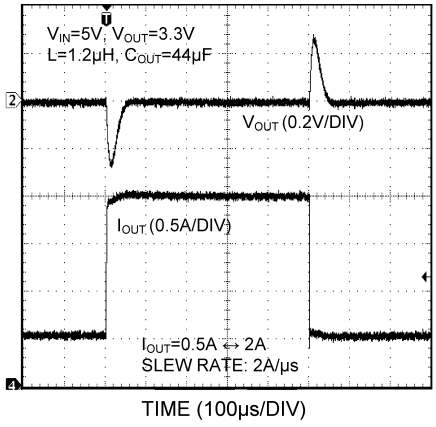


Figure 14. Load Step Response - LMR10530X

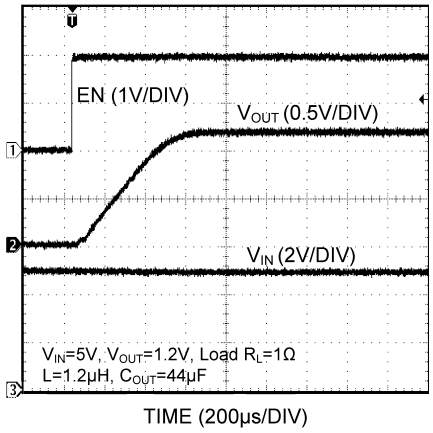


Figure 15. Start-up by EN - LMR10530X

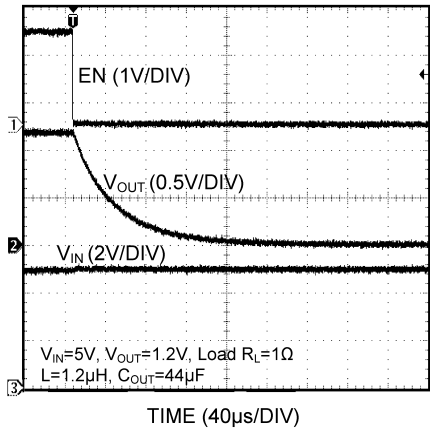


Figure 16. Shutdown by EN - LMR10530X

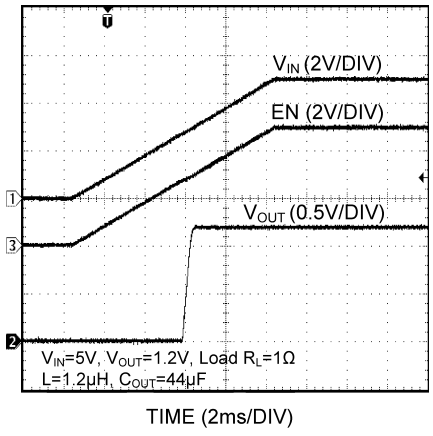


Figure 17. Startup With EN Tied to V_{IN} - LMR10530X

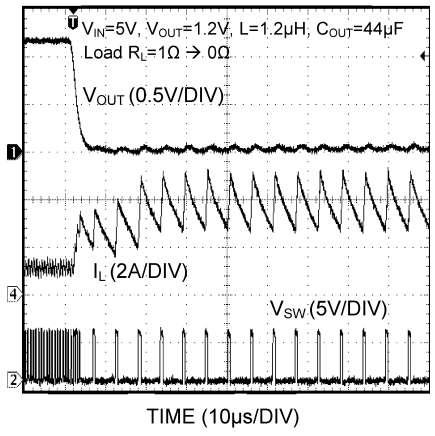


Figure 18. Short-Circuit Triggering - LMR10530X

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 5 V and T_A = 25°C

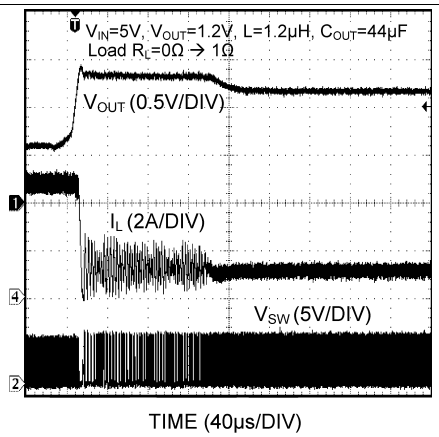


Figure 19. Short-Circuit Release - LMR10530X

7 Detailed Description

7.1 Overview

The LMR10530 is a constant frequency PWM buck regulator IC that delivers a 3-A load current. The regulator is available in preset switching frequencies of 1.5 MHz or 3 MHz. This high frequency allows the LMR10530 to operate with small surface mount capacitors and inductors, resulting in a DC/DC converter that requires a minimum amount of board space. The LMR10530 is internally compensated, therefore it is simple to use and requires few external components. The LMR10530 uses peak current-mode control to regulate the output voltage. The following description of operation of the LMR10530 will refer to the Figure 30, to the waveforms in Figure 20 and simplified block diagram in *Functional Block Diagram*. The LMR10530 supplies a regulated output voltage by switching the internal PMOS power switch at a constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal PMOS power switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the internal power switch turns off until the next switching cycle begins. During the switch off-time, the inductor current discharges through the catch diode D1, which forces the SW pin to swing below ground by the forward voltage (V_D) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

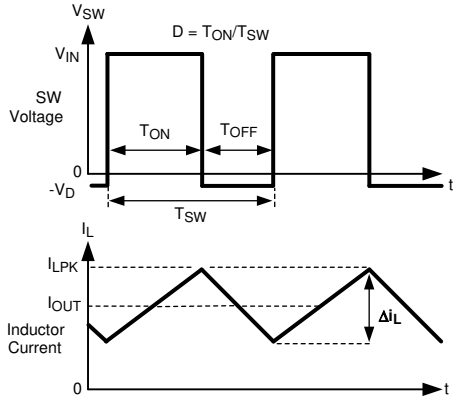
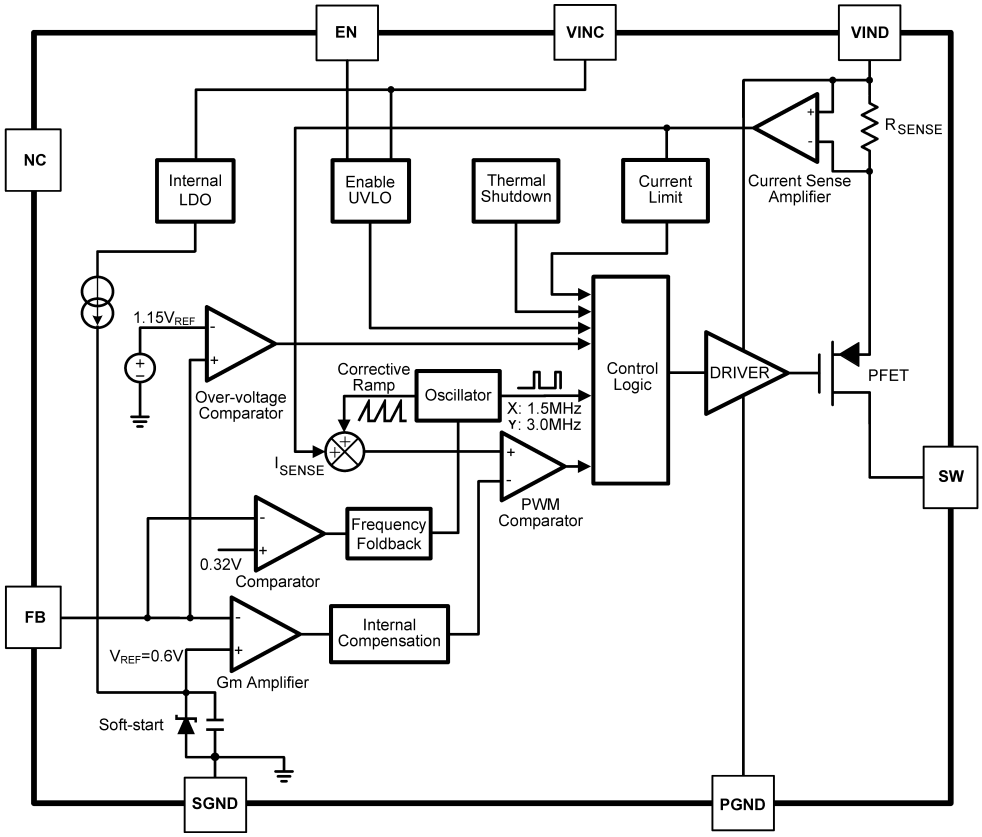


Figure 20. Typical Waveforms

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Frequency Foldback

The LMR10530 uses frequency foldback to help limit switch current and power dissipation during start-up, short-circuit and over load conditions by sensing if the feedback voltage is below 0.32 V (typical). The LMR10530 reduces the switching frequency from the nominal fixed value (1.5 MHz or 3 MHz) down to 400 kHz (LMR10530X) or 800 kHz (LMR10530Y) when the feedback voltage drops to 0 V. See Figure 11 plot in the *Typical Characteristics* section.

7.3.2 Load Step Response

The LMR10530 has a fixed internal loop compensation, which results in a small-signal loop bandwidth highly related to the output voltage level. In general, the loop bandwidth at low voltage is larger than at high voltage due to the increased overall loop gain. The limited bandwidth at high output voltage may pose a challenge when loop step response is concerned. In this case, one effective approach to improving loop step response is to add a feed-forward capacitor C_{FF}) in the range of 27 nF to 100 nF in parallel with the upper feedback resistor (assuming the lower feedback resistor is 2 kΩ), as shown in Figure 21. The feedforward capacitor introduces a zero-pole pair which helps compensate the loop. The position of the zero-pole pair is a function of the feedback resistors and capacitor:

$$\omega_z = \frac{1}{R1 \times C_{FF}} \text{ (rad/s)} \quad (1)$$

$$\omega_p = \frac{1}{R1 \times C_{FF}} \left(1+\frac{R1}{R2}\right) \text{ (rad/s)} \quad (2)$$

Note the factor in parenthesis is the ratio of the output voltage to the feedback voltage. As the output voltage gets close to 0.6V, the pole moves towards the zero, tending to cancel it out. Consequently, adding C_{FF} will have less effect on the step response at lower output voltages.

As an example, Figure 23 shows that at the output voltage of 3.3 V, 47 nF of C_{FF} can boost the loop bandwidth to 117kHz, from the original 23kHz as shown in Figure 22. Correspondingly, the responses to a load step between 0.3 A and 3 A without and with C_{FF} are shown in Figure 24 and Figure 25 respectively. The higher loop bandwidth as a result of C_{FF} reduces the total output excursion by more than half.

Aside from the above approach, increasing the output capacitance is generally also effective to reduce the excursion in output voltage caused by a load step. This approach remains valid for applications where the desired output voltages are close to the feedback voltage.

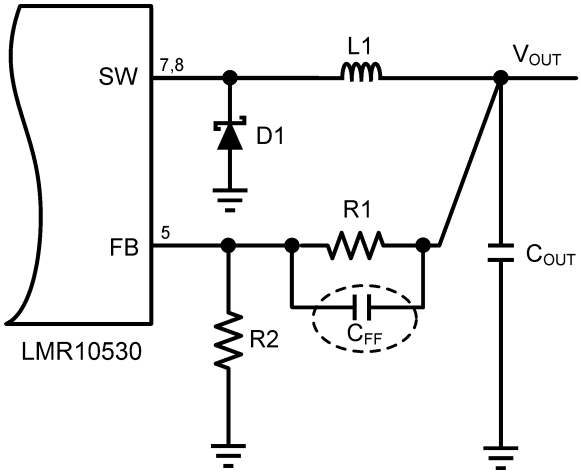


Figure 21. Adding a C_{FF} Capacitor

Feature Description (continued)

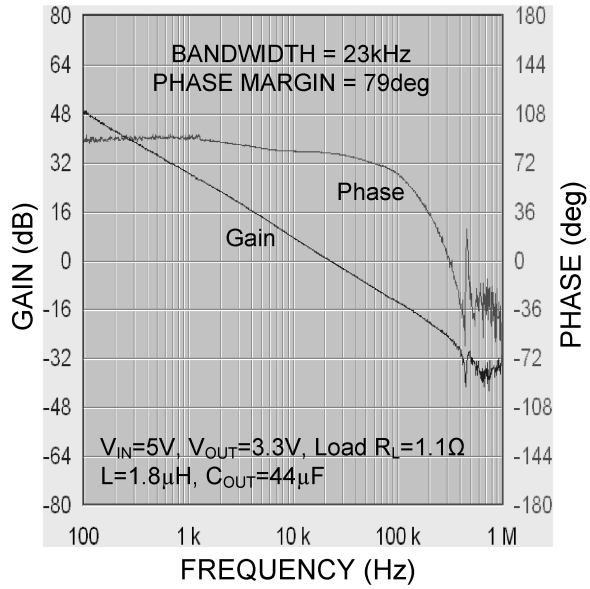


Figure 22. Loop Gain and Phase Without C_{FF}

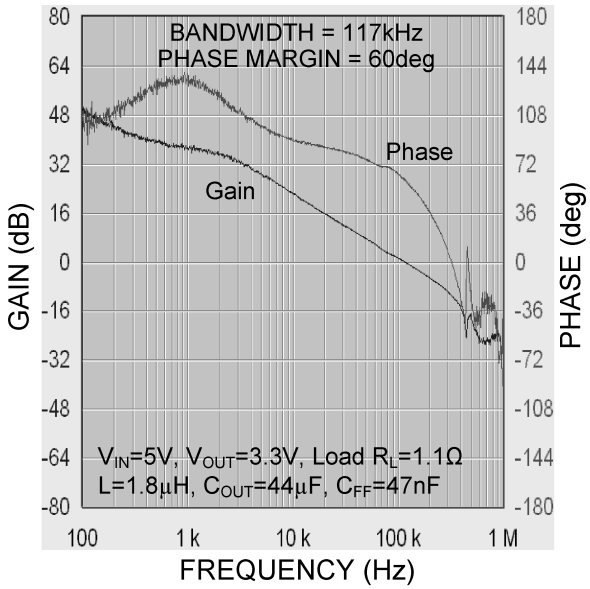


Figure 23. Loop Gain and Phase With C_{FF}

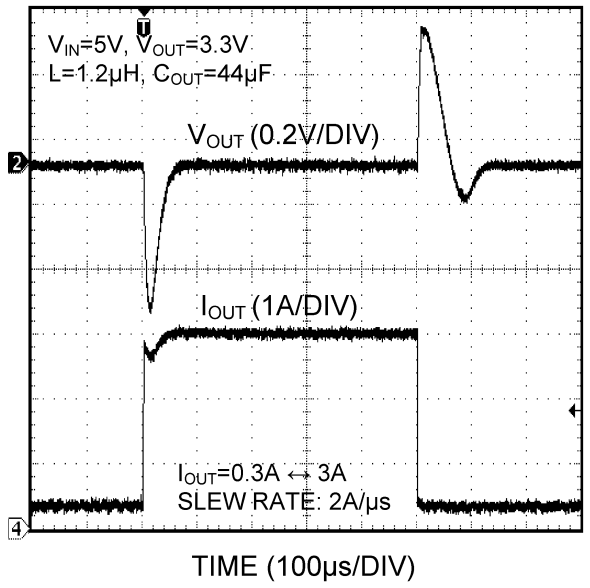


Figure 24. Load Step Response Without C_{FF}

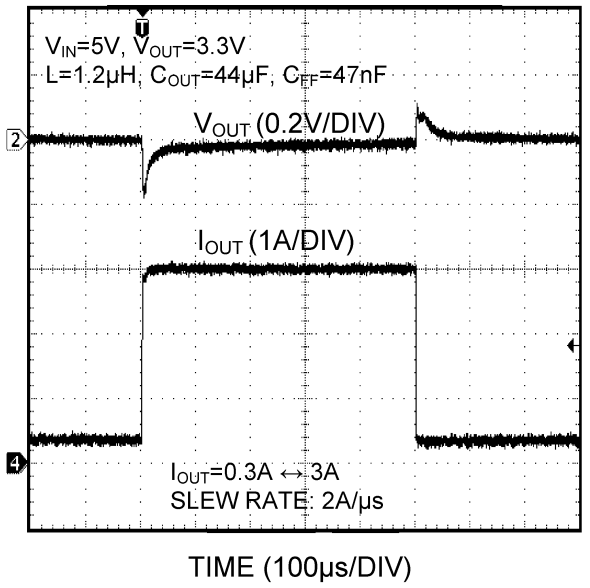


Figure 25. Load Step Response With C_{FF}

7.3.3 Output Overvoltage Protection

The LMR10530 has a builtin output overvoltage comparator that compares the FB pin voltage to a threshold voltage that is 15% higher than the internal reference V_{REF}. Once the FB pin voltage exceeds this threshold level (typically 0.69 V), the internal PMOS power switch is turned off, which allows the output voltage to decrease towards regulation.

7.3.4 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LMR10530 from operating until the input voltage exceeds 2.7 V (typical). The UVLO threshold has approximately 350 mV of hysteresis, so the device operates until V_{IN} drops below 2.35 V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

Feature Description (continued)

7.3.5 Current Limit

The LMR10530 uses cycle-by-cycle current limiting to protect the internal power switch. During each switching cycle, a current limit comparator detects if the power switch current exceeds 4.4 A (typical), and turns off the switch until the next switching cycle begins.

7.3.6 Soft Start/Shutdown

The LMR10530 has both enable and shutdown modes that are controlled by the EN pin. Connecting a voltage source greater than 1.8 V to the EN pin enables the operation of the LMR10530, while reducing this voltage below 0.4 V places the part in a low quiescent current (300 nA typical) shutdown mode. There is no internal pull-up on EN pin, therefore an external signal is required to initiate switching. Do not allow this pin to float or rise to 0.3 V above V_{IN}. It should be noted that when the EN pin voltage rises above 1.8 V while the input voltage is greater than UVLO, there is 15-µs delay before switching starts. During this delay the LMR10530 goes through a power on reset state after which the internal soft-start process commences. During soft-start, the error amplifier's reference voltage ramps from 0V to its nominal value of 0.6 V in approximately 600 µs. This forces the regulator output to ramp up in a controlled fashion, which helps reduce inrush current seen at the input and minimizes output voltage overshoot.

The simplest way to enable the operation of the LMR10530 is to connect the EN pin to V_{IN} which allows self start-up of the LMR10530 whenever the input voltage is applied. However, when an input voltage of slow rise time is used to power the application and if both the input voltage and the output voltage are not fully established before the soft-start time elapses, the control circuit commands maximum duty cycle operation of the internal power switch to bring up the output voltage rapidly. When the feedback pin voltage exceeds 0.6 V, the duty cycle will have to reduce from the maximum value accordingly, to maintain regulation. The reduction of duty cycle takes a finite amount of time and can result in a transient in output voltage for a short duration, as shown in Figure 26. In applications where this output voltage overshoot is undesirable, one simple solution is to add a feed-forward capacitor C_{FF}) across the top feedback resistor R1 to speed Gm Amplifier recovery. In practice, a 27-nF to 100-nF ceramic capacitor is usually a good choice to remove the overshoot completely or limit the overshoot to an insignificant level during startup, as shown in Figure 27. Another more effective solution is to control EN pin voltage by a separate logic signal, and pull the signal high only after V_{IN} is fully established. In this way, the chip can execute a normal, complete soft start process, minimizing any output voltage overshoot. Under some circumstances at cold temperature, this approach may also be required to minimize any unwanted output voltage transients that may occur when the input voltage rises slowly. For a fast rising input voltage (100 µs for example), there is no need to control EN separately or add a feedforward capacitor since the soft start can bring up output voltage smoothly as shown in Figure 28.

During startup, the LMR10530 gradually increases the switching frequency from 400 kHz (LMR10530X) or 800 kHz (LMR10530Y) to the nominal fixed value, as the feedback voltage increases (see Frequency Foldback section for more information). Since the internal corrective ramp signal adjusts its slope dynamically, and is proportional to the switching frequency during startup, a larger output capacitance may be required to insure a smooth output voltage rise, at low programmed output voltage and high output load current.

Feature Description (continued)

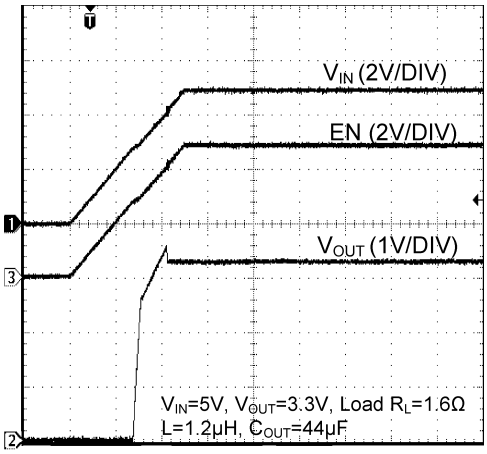


Figure 26. Start-up Response to V_{IN}

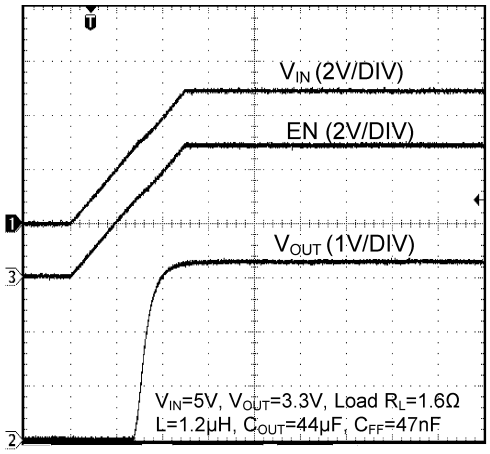


Figure 27. Start-up Response to V_{IN} With C_{FF}

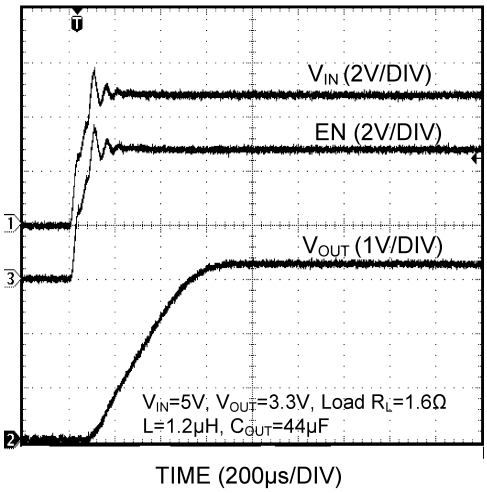


Figure 28. Startup Response To V_{IN} With 100-µs Rise Time

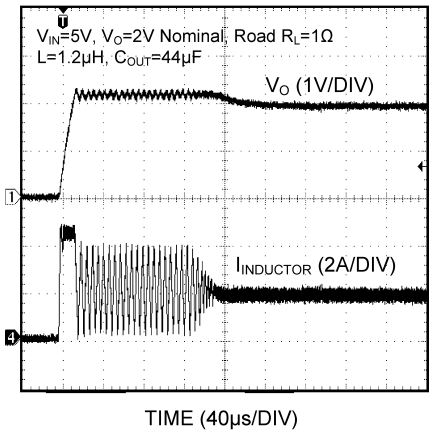


Figure 29. Recovery From Thermal Shutdown - "LMR10530X"

7.3.7 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal power switch when the IC junction temperature typically exceeds 165°C. After thermal shutdown occurs, the power switch does not turn on again until the junction temperature drops below approximately 150°C.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMR10530 regulator is a monolithic, high frequency, PWM step-down DC/DC converter available in a 10-pin WSON package. It contains all the active functions to provide local DC/DC conversion with fast transient response and accurate regulation in the smallest possible PCB area. With a minimum of external components, the LMR10530 is easy to use. Switching frequency is internally set to 1.5 MHz or 3 MHz, allowing the use of extremely small surface mount inductors and capacitors. Even though the operating frequency is high, efficiencies up to 93% are easy to achieve.

8.2 Typical Application

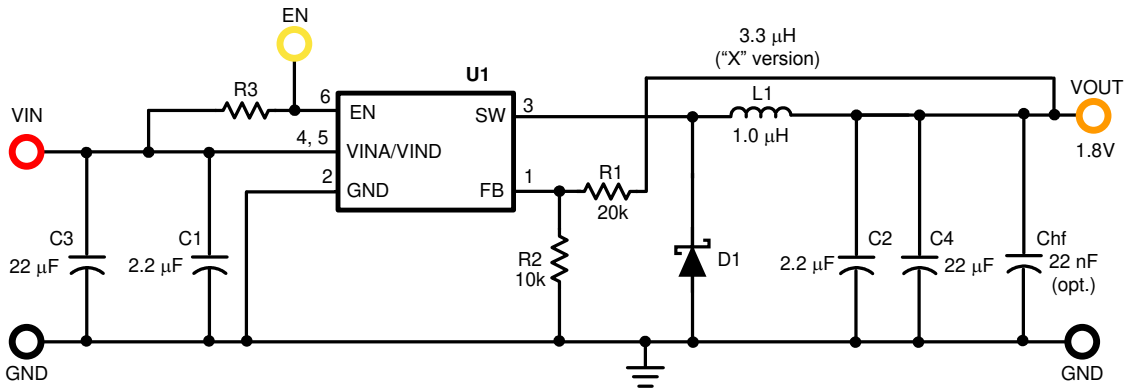


Figure 30. Typical Application Schematic

8.2.1 Detailed Design Procedure

8.2.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR10530 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Typical Application (continued)

8.2.1.2 Inductor Selection

The duty cycle (D) can be approximated quickly using the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal PMOS must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{4}$$

V_{SW} can be approximated by:

$$V_{SW} = I_{OUT} \times R_{DS(ON)}$$

where

- I_{OUT} is output load current. (5)

The diode forward drop (V_D) can range from 0.3 V to 0.7 V depending on the quality of the diode. The lower the V_D, the higher the operating efficiency of the converter.

The inductor value determines the output ripple current (Δi_L, as defined in). Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value decreases the output ripple current. In general, the ratio of ripple current to the output current is optimized when it is set between 0.2 and 0.4 for output currents above 2 A. This ratio r is defined as:

$$r = \frac{\Delta i_L}{I_{OUT}} \tag{6}$$

One must ensure that the minimum current limit (3.4 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L/2 \tag{7}$$

When the designed maximum output current is reduced, the ratio r can be increased. At a current of 0.1 A, r can be made as high as 0.9. The ripple ratio can be increased at lighter loads because the net ripple is actually quite low, and if r remains constant the inductor value can be made quite large. An equation empirically developed for the maximum ripple ratio at any current below 2 A is:

$$r = 0.387 \times I_{OUT}^{-0.3667} \tag{8}$$

Note that this is just a guideline, and it needs to be combined with two important factors for proper selection of inductance values at any operating condition. The first consideration is at output voltage above 2.5 V, one needs to ensure that the inductance given by the above guideline should not be less than 1 µH for the LMR10530X or 0.5 µH for the LMR10530Y. Because the LMR10530 has a fixed internal corrective ramp signal, a very low inductance value at high output voltage generates a very steep down slope of inductor current, which results in an insufficient slope compensation, and cause instability known as sub-harmonic oscillation. Another consideration is at low load current, one needs to ensure that the inductance value given by the guideline should not exceed 10 µH for the LMR10530X and 4.7 µH for the LMR10530Y, since too much inductance effectively flattens the down slope of the inductor current, and may significantly limit the system bandwidth and phase margin resulting in instability.

The LMR10530 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the Output Capacitor section for more details on calculating output voltage ripple.

Now that the ripple current is determined, the inductance is calculated by:

$$L = \frac{V_{OUT} + V_D}{I_{OUT} \times r \times f_{SW}} \times (1\text{-}D)$$

where

- f_{SW} is the switching frequency. (9)

Typical Application (continued)

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating properly. Because of the operating frequency of the LMR10530, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety and availability of ferrite-based inductors is large. Lastly, inductors with lower series resistance (DCR) will provide better operating efficiency. For recommended inductor selection, refer to *Other System Examples*.

8.2.1.3 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage rating, RMS current rating, and equivalent series inductance (ESL). The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS-IN} = I_{OUT} \times \sqrt{D \times \left(1 - D + \frac{r^2}{12}\right)} \tag{10}$$

Neglecting inductor ripple simplifies the above equation to:

$$I_{RMS-IN} = I_{OUT} \times \sqrt{D \times \left(1 - D\right)} \tag{11}$$

It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle D is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. As a rule of thumb, a large leaded capacitor will have high ESL and a 1206 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LMR10530, leaded capacitors may have an ESL so large that the resulting impedance (2 πfL) will be higher than that required to provide stable operation. TI strongly recommends usin ceramic capacitors due to their low ESR and low ESL. A 22-µF multilayer ceramic capacitor (MLCC) is a good choice for most applications. In cases where large capacitance is required, use surface mount capacitors such as Tantalum capacitors and place at least a 4.7-µF ceramic capacitor close to the V_{IN} pin. For MLCCs TI recommends using X7R or X5R dielectrics. Consult capacitor manufacturer datasheet to see how rated capacitance varies over operating conditions.

8.2.1.4 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \tag{12}$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LMR10530, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum of 22-µF output capacitance. In the case of low output voltage, a larger output capacitance is required to ensure sufficient phase margin. Capacitance can often, but not always, be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types. Again, verify actual capacitance at the desired operating voltage and temperature. Check the RMS current rating of the capacitor. The maximum RMS current rating of the capacitor is:

$$I_{RMS-OUT} = I_{OUT} \times \frac{r}{\sqrt{12}} \tag{13}$$

One may select a 1206 size MLCC for output capacitor, since its current rating is typically above 1 A, more than enough for the requirement.

Typical Application (continued)

8.2.1.5 Catch Diode

The catch diode conducts during the switch off-time. TI recommends a Schottky diode for its fast switching time and low forward voltage drop. The catch diode should be chosen such that its current rating is greater than:

$$I_D = I_{OUT} \times (1\text{-}D) \quad (14)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward voltage drop.

8.2.1.6 Output Voltage

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin. A good value for R2 is 2 kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (15)$$

$$V_{REF} = 0.6\ V \quad (16)$$

8.2.1.7 Efficiency Estimation

The complete LMR10530 DC/DC converter efficiency can be calculated in the following manner:

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (17)$$

or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (18)$$

Calculations for determining the most significant power losses are shown in the following examples. Other losses totaling less than 2% are not discussed.

The main power loss (P_{LOSS}) in the converter includes two basic types of losses: switching loss and conduction loss. In addition, there is loss associated with the power required for the internal circuitry of IC. Conduction losses usually dominate at higher output loads, whereas switching losses dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \quad (19)$$

V_{SW} is the voltage drop across the internal power switch when it is on, and is equal to:

$$V_{SW} = I_{OUT} \times R_{DS(ON)} \quad (20)$$

V_D is the forward voltage drop across the catch diode. It can be obtained from the diode manufactures Electrical Characteristics section. If the DC voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_D + V_{DCR}}{V_{IN} + V_D - V_{SW}} \quad (21)$$

The conduction losses in the catch diode are calculated as follows:

$$P_{DIODE} = V_D \times I_{OUT} \times (1\text{-}D) \quad (22)$$

Often this is the single most significant power loss in the circuit. Take care to choose a Schottky diode with a low forward-voltage drop.

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (23)$$

The LMR10530 conduction loss is mainly associated with the internal power switch:

Typical Application (continued)

$$P_{COND} = (I_{OUT}^2 \times D) \times \left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) \times R_{DS\,(ON)} \quad (24)$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to:

$$P_{COND} = I_{OUT}^2 \times R_{DS(ON)} \times D \quad (25)$$

Switching losses are also associated with the internal power switch. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows:

$$P_{SWR} = 0.5 \times (V_{IN} \times I_{OUT} \times f_{SW} \times T_{RISE}) \quad (26)$$

$$P_{SWF} = 0.5 \times (V_{IN} \times I_{OUT} \times f_{SW} \times T_{FALL}) \quad (27)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (28)$$

The power loss required for operation of the internal circuitry is given by:

$$P_Q = I_Q \times V_{IN} \quad (29)$$

I_Q is the quiescent operating current, and is typically around 3.2 mA for the LMR10530X, and 4.3 mA for the LMR10530Y.

An example of efficiency calculation for a typical application is shown in Table 1:

Table 1. Power Loss Tabulation

CONDITIONS		POWER LOSS	
V_{IN}	5 V		
V_{OUT}	3.3 V		
I_{OUT}	3 A	P_{OUT}	9.9 W
V_D	0.33 V	P_{DIODE}	277 mW
$R_{DS(ON)}$	56 mΩ	P_{COND}	363 mW
f_{SW}	1.5 MHz		
T_{RISE}	10 ns	P_{SW}	225 mW
T_{FALL}	10 ns		
IND_{DCR}	28 mΩ	P_{IND}	252 mW
I_Q	3.2 mA	P_Q	16 mW
η	89.7%		
D is calculated to be 0.72			

$$P_{LOSS} = \Sigma\,(P_{COND} + P_{SW} + P_Q + P_{IND} + P_{DIODE}) \quad (30)$$

$$P_{LOSS} = 1.133W \quad (31)$$

8.2.2 Application Curve

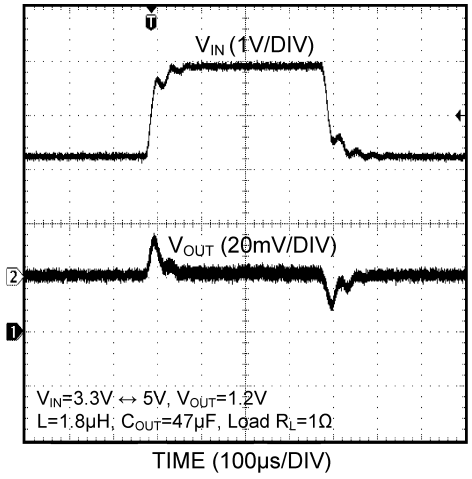
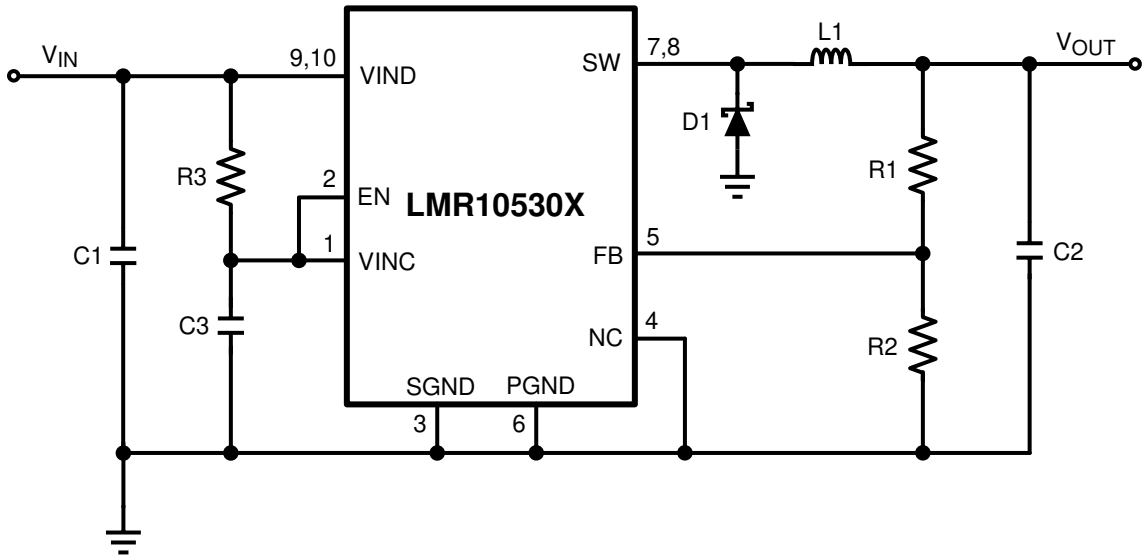


Figure 31. Line Transient Response - "LMR10530X"

8.2.3 Other System Examples

8.2.3.1 LMR10530X Design Example 1



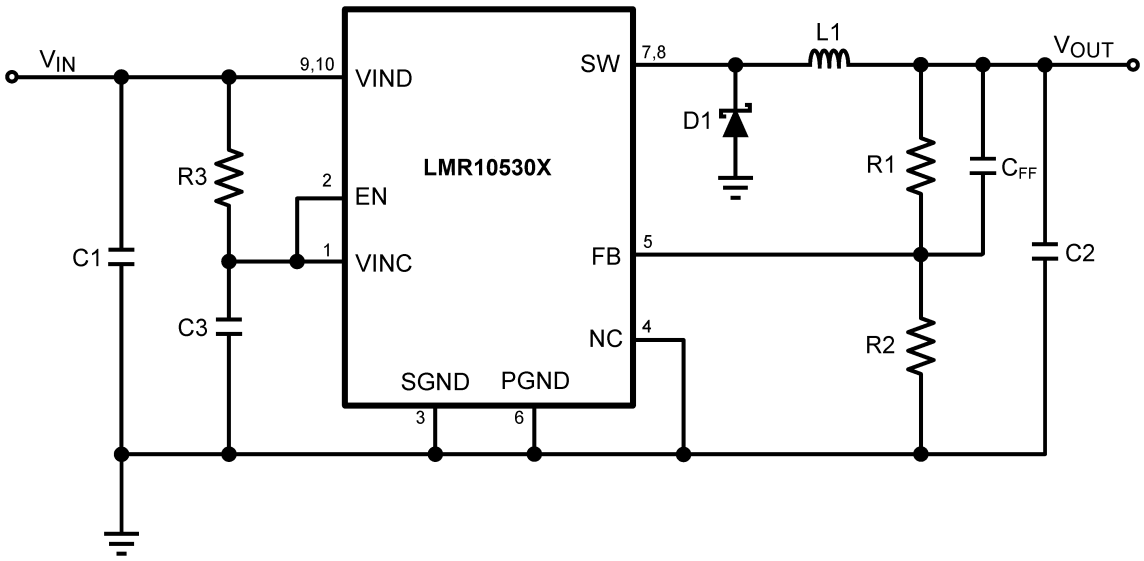
V_{IN} = 3.3 V V_{OUT} = 1.2 V I_{OUT} = 3 A

Figure 32. LMR10530X (1.5 MHz)

Table 2. Bill Of Materials

DEVICE ID	DEVICE VALUE	MANUFACTURER	DEVICE NUMBER
U1	3-A buck regulator	TI	LMR10530X
C1, Input Capacitor	22 µF, 6.3 V, X5R	TDK	C3216X5R0J226M
C2, Output Capacitor	47 µF, 6.3 V, X5R	TDK	C3216X5R0J476M
C3, Bypass Capacitor	0.22 µF, 10 V, X7R	Murata	GRM216R71A224KC01D
D1, Catch Diode	Schottky, 0.33 V at 3 A, V_R= 30 V	Toshiba	CMS01
L1	1.8 µH, 3.6 A	TDK	LTF5022T-1R8N3R6
R1	2 kΩ, 1%	Vishay	CRCW08052K00FKEA
R2	2 kΩ, 1%	Vishay	CRCW08052K00FKEA
R3	10 Ω, 1%	Vishay	CRCW080510R0FKEA

8.2.3.2 LMR10530X Design Example 2



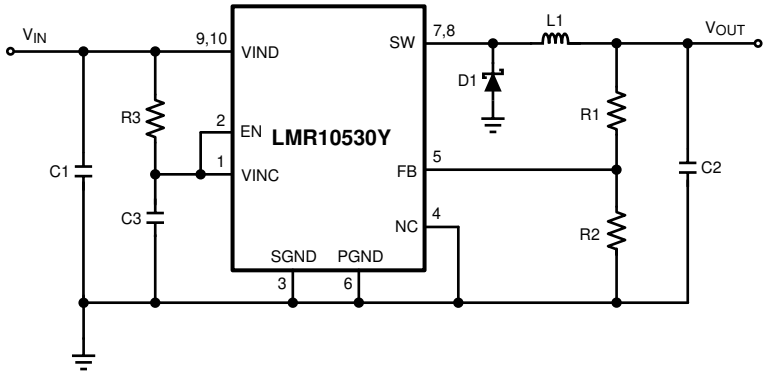
V_{IN} = 5 V V_{OUT} = 3.3 V I_{OUT} = 3 A

Figure 33. LMR10530X (1.5 MHz)

Table 3. Bill Of Materials

DEVICE ID	DEVICE VALUE	MANUFACTURER	DEVICE NUMBER
U1	3-A buck regulator	TI	LMR10530X
C1, Input Capacitor	22 µF, 6.3 V, X5R	TDK	C3216X5R0J226M
C2, Output Cap	47 µF, 6.3 V, X5R	TDK	C3216X5R0J476M
C3, Bypass Capacitor	0.22 µF, 10 V, X7R	Murata	GRM216R71A224KC01D
C_{FF}, Feed-forward Capacitor	47 nF, 10 V, X7R	AVX	0805ZC473JAZ2A
D1, Catch Diode	Schottky, 0.43 V at 3 A, V_R= 30 V	Vishay	SSA33L-E3/61T
L1	1.2 µH, 4.2 A	TDK	LTF5022T-1R2N4R2
R1	10.2 kΩ, 1%	Vishay	CRCW080510K2FKEA
R2	2.26 kΩ, 1%	Vishay	CRCW08052K26FKEA
R3	10 Ω, 1%	Vishay	CRCW080510R0FKEA

8.2.3.3 LMR10530Y Design Example 3



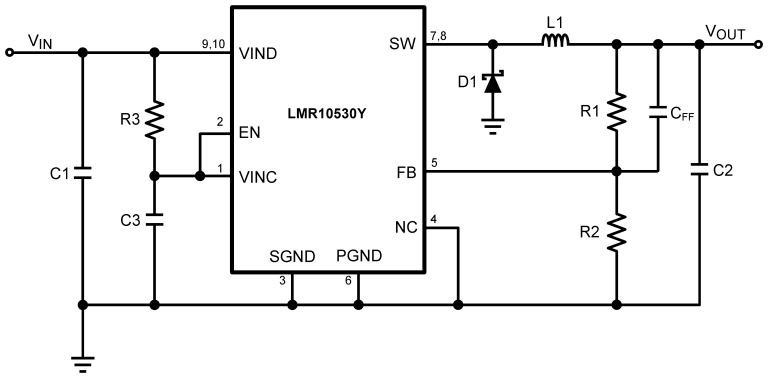
V_{IN} = 3.3 V V_{OUT} = 1.2 V I_{OUT} = 3 A

Figure 34. LMR10530Y (3 MHz)

Table 4. Bill Of Materials

DEVICE ID	DEVICE VALUE	MANUFACTURER	DEVICE NUMBER
U1	3-A buck regulator	TI	LMR10530Y
C1, Input Capacitor	22 µF, 6.3 V, X5R	TDK	C3216X5R0J226M
C2, Output Capacitor	47µF, 6.3 V, X5R	TDK	C3216X5R0J476M
C3, Bypass Capacitor	0.22µF, 10 V, X7R	Murata	GRM216R71A224KC01D
D1, Catch Diode	Schottky, 0.33 V at 3 A, V_R= 30 V	Toshiba	CMS01
L1	1 µH, 4 A	Taiyo Yuden	NP04SZB1R0N
R1	2 kΩ, 1%	Vishay	CRCW08052K00FKEA
R2	2 kΩ, 1%	Vishay	CRCW08052K00FKEA
R3	10 Ω, 1%	Vishay	CRCW080510R0FKEA

8.2.3.4 LMR10530Y Design Example 4



V_{IN} = 5 V V_{OUT} = 3.3 V I_{OUT} = 3 A

Figure 35. LMR10530Y (3 MHz)

Table 5. Bill Of Materials

DEVICE ID	DEVICE VALUE	MANUFACTURER	DEVICE NUMBER
U1	3-A buck regulator	TI	LMR10530Y
C1, Input Capacitor	22 µF, 6.3 V, X5R	TDK	C3216X5R0J226M
C2, Output Capacitor	47 µF, 6.3 V, X5R	TDK	C3216X5R0J476M
C3, Bypass Capacitor	0.22 µF, 10 V, X7R	Murata	GRM216R71A224KC01D
C_{FF}, Feedforward Capacitor	47 nF, 10 V, X7R	AVX	0805ZC473JAZ2A
D1, Catch Diode	Schottky, 0.43 V at 3 A, V_R= 30 V	Vishay	SSA33L-E3/61T
L1	1 µH, 4 A	Taiyo Yuden	NP04SZB1R0N
R1	10.2 kΩ, 1%	Vishay	CRCW080510K2FKEA
R2	2.26 kΩ, 1%	Vishay	CRCW08052K26FKEA
R3	10 Ω, 1%	Vishay	CRCW080510R0FKEA

9 Layout

9.1 Layout Considerations

When planning layout there are a few things to consider to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor Cin and the catch diode D1. These ground ends should be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. The next consideration is the location of the GND connection of the output capacitor Co, which should be near the GND connections of C1 and D1. There must be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. Tie the signal ground SGND (pin 3) and power ground PGND (pin 6) together and connected to ground plane through vias.

The FB pin is a high impedance node—take care to make the FB trace short to avoid noise pickup that causes inaccurate regulation. The feedback resistors must be placed as close as possible to the IC, with the GND of Rfbb placed as close as possible to the SGND of the IC. Route the V_{OUT} trace to Rfb1 away from the inductor and any other traces that are switching.

High AC currents flow through the V_{IN}, SW, and V_{OUT} traces, so they must be as short and wide as possible. Radiated noise can be decreased by choosing a shielded inductor.

Place the remaining components as close as possible to the IC. See Application Note AN-2280 for further considerations and the LMR10530 demo board as an example of a four-layer layout.

10 器件和文档支持

10.1 器件支持

10.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

10.1.2 开发支持

10.1.2.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 LMR10530 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

10.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 商标

E2E is a trademark of Texas Instruments.
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10.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR10530XSD/NOPB	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L287B
LMR10530XSD/NOPB.A	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L287B
LMR10530XSDX/NOPB	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L287B
LMR10530XSDX/NOPB.A	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L287B
LMR10530XSDX/NOPB.B	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMR10530YSD/NOPB	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L286B
LMR10530YSD/NOPB.A	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L286B
LMR10530YSDX/NOPB	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L286B
LMR10530YSDX/NOPB.A	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L286B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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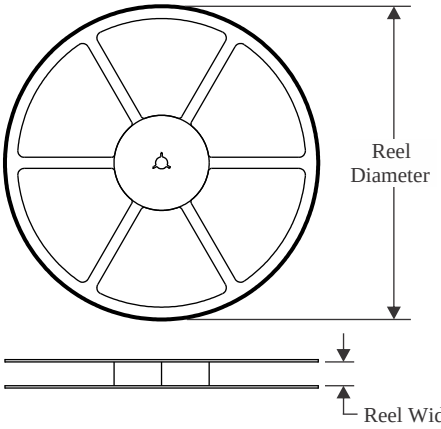
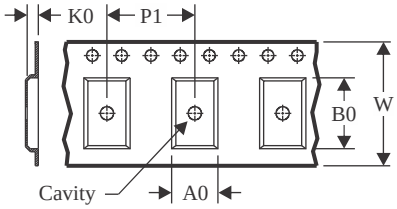
TAPE AND REEL INFORMATION

REEL DIMENSIONS

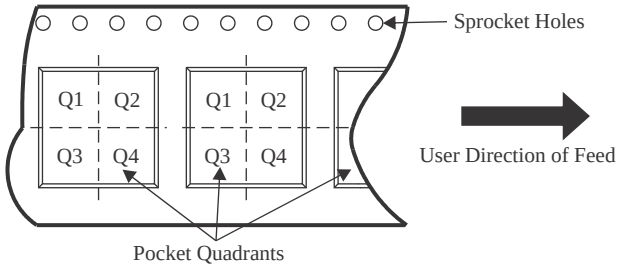


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

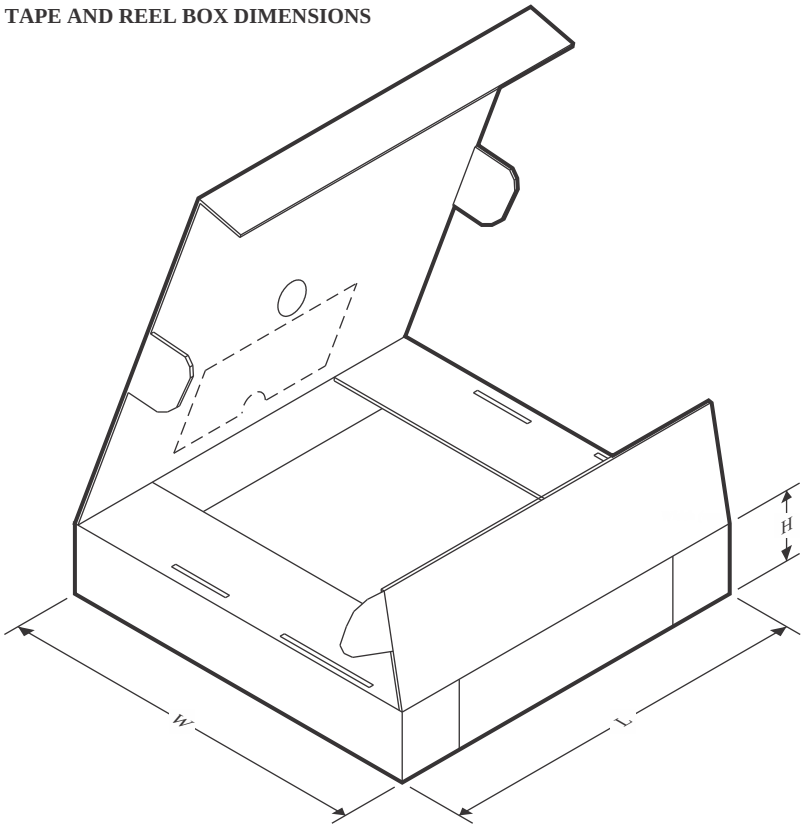
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR10530XSD/NOPB	WSON	DSC	10	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10530XSDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10530YSD/NOPB	WSON	DSC	10	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10530YSDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

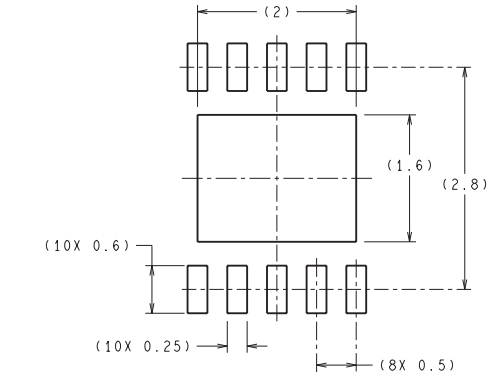
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

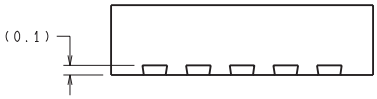
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR10530XSD/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LMR10530XSDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0
LMR10530YSD/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LMR10530YSDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

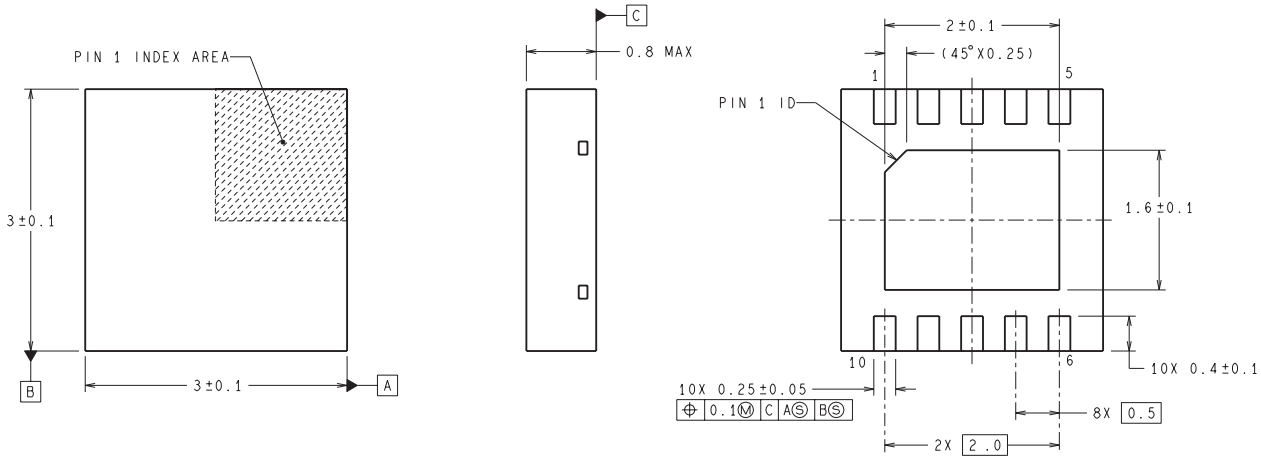
DSC0010A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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