

LMT85 1.8、SC70/TO-92/TO-92S

模拟温度传感器

1 特性

- LMT85LPG (TO-92S 封装) 具有快速热时间常量, 典型值为 10s (气流速度为 1.2m/s)
- 非常精确: 典型值 $\pm 0.4^{\circ}\text{C}$
- 1.8V 低压运行
- $-8.2\text{mV}/^{\circ}\text{C}$ 的平均传感器增益
- $5.4\mu\text{A}$ 低静态电流
- 宽温度范围: -50°C 至 150°C
- 输出受到短路保护
- 具有 $\pm 50\mu\text{A}$ 驱动能力的推挽输出
- 封装尺寸兼容符合行业标准的 LM20/19 和 LM35 温度传感器
- 具有成本优势的热敏电阻替代产品

2 应用

- 汽车
- 信息娱乐系统与仪表组
- 动力传动系统
- 烟雾和热量探测器
- 无人机
- 电器

3 说明

LMT85 是一款高精度 CMOS 温度传感器, 其典型精度为 $\pm 0.4^{\circ}\text{C}$ (最大值为 $\pm 2.7^{\circ}\text{C}$), 且线性模拟输出电压与温度成反比关系。1.8V 工作电源电压、 $5.4\mu\text{A}$ 静态电流和 0.7ms 开通时间可实现有效的功率循环架构, 以最大限度地降低无人机和传感器节点等电池供电应用的功耗。LMT85LPG 穿孔 TO-92S 封装快速热时间常量支持非板载时间温度敏感型应用, 例如烟雾和热量探测器。得益于宽工作范围内的精度和其他特性, 使得 LMT85 成为热敏电阻的优质替代产品。

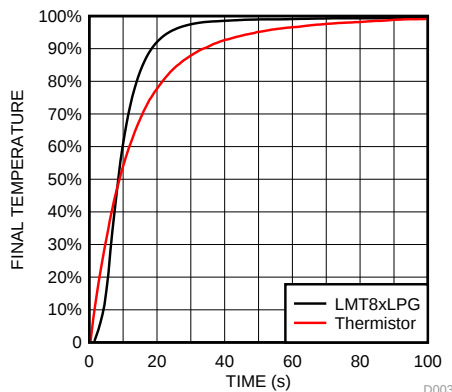
对于具有不同平均传感器增益和类似精度的器件, 请参阅 [类似替代器件](#) 了解 LMT8x 系列中的替代器件。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
LMT85	SOT (5)	2.00mm × 1.25mm
	TO-92 (3)	4.30mm × 3.50mm
	TO-92S (3)	4.00mm × 3.15mm

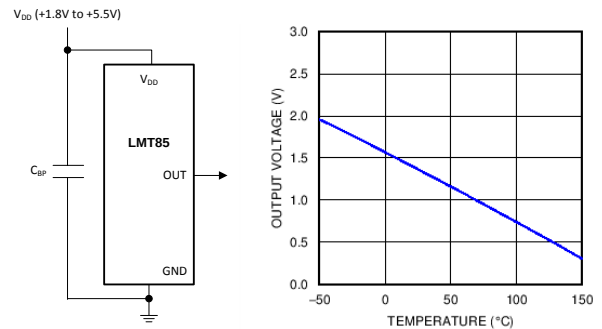
(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

热时间常量



* 快速热响应 NTC

输出电压与温度间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (June 2017) to Revision E	Page
• 将汽车器件移到了单独的数据表中 (SNIS200)	1
• Changed TO-92 GND pin number from: 1 to: 3	4
• Changed TO-92 V _{DD} pin number from: 3 to: 1	4

Changes from Revision C (October 2015) to Revision D	Page
• 将数据表更新为最新的文档和翻译标准	1
• 将 AEC-Q100 汽车标准项目符号添加到了“特性”中	1
• 添加了时间常量图	1
• 将磁盘驱动器、游戏、无线收发器和手机从“应用”中进行了删除	1
• Added LPG (TO-92S) package	4
• Added Figure 10 to <i>Typical Characteristics</i>	7

Changes from Revision B (May 2014) to Revision C	Page
• 已删除 所有涉及 TO-126 封装的内容	1
• Added TO-92 LPM pin configuration graphic	4
• Changed Handling Ratings to ESD Ratings and moved Storage Temperature to Absolute Maximum Ratings table	5
• Changed KV to V	5
• Added TO-92 LP and LPM layout recommendations	15

Changes from Revision A (June 2013) to Revision B	Page
• 已更改 更改了数据表流程和布局，以符合 TI 新标准。在整个文档内添加了以下章节：应用范围和实施、电源建议、布局布线、器件和文档支持、机械、封装和可订购信息。	1
• 已添加 在文档中增加了 TO-92 和 TO-126 封装信息。	1
• Changed from 450°C/W to 275 °C/W. New specification is derived using TI 's latest methodology.	5

- Changed Temperature Accuracy Conditions from 70°C to 20°C and V_{DD} from 1.9V to 1.8V..... 6
- Deleted Note: The input current is leakage only and is highest at high temperature. It is typically only 0.001 μ A. The 1 μ A limit is solely based on a testing limitation and does not reflect the actual performance of the part..... 6

5 Device Comparison Tables

Table 1. Available Device Packages

ORDER NUMBER ⁽¹⁾	PACKAGE	PIN	BODY SIZE (NOM)	MOUNTING TYPE
LMT85DCK	SOT (AKA ⁽²⁾ : SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount
LMT85LP	TO-92 (AKA ⁽²⁾ : LP)	3	4.30 mm × 3.50 mm	Through-hole; straight leads
LMT85LPG	TO-92S (AKA ⁽²⁾ : LPG)	3	4.00 mm × 3.15 mm	Through-hole; straight leads
LMT85LPM	TO-92 (AKA ⁽²⁾ : LPM)	3	4.30 mm × 3.50 mm	Through-hole; formed leads
LMT85DCK-Q1	SOT (AKA ⁽²⁾ : SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount

(1) For all available packages and complete order numbers, see the Package Option addendum at the end of the data sheet.

(2) AKA = Also Known As

Table 2. Comparable Alternative Devices

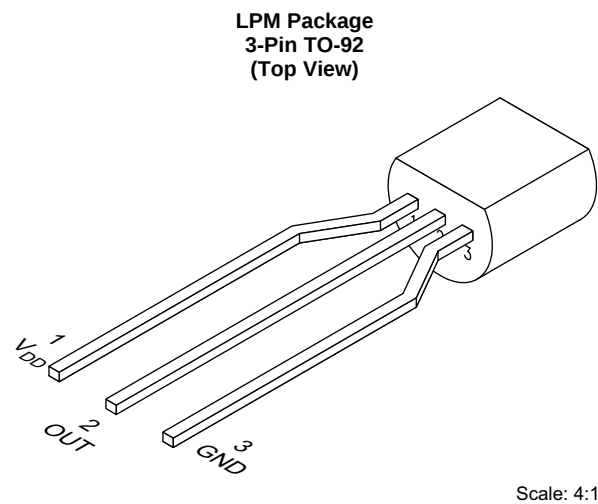
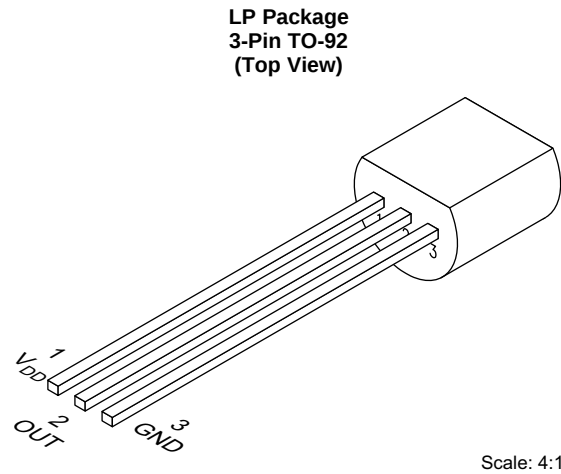
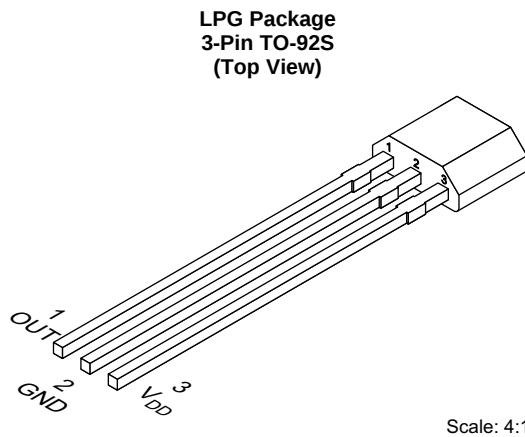
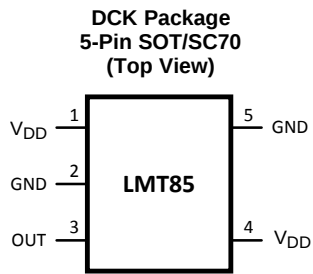
DEVICE NAME	AVERAGE OUTPUT SENSOR GAIN	POWER SUPPLY RANGE
LMT84	–5.5 mV/°C	1.5 V to 5.5 V
LMT85	–8.2 mV/°C	1.8 V to 5.5 V
LMT86	–10.9 mV/°C	2.2 V to 5.5 V
LMT87	–13.6 mV/°C	2.7 V to 5.5 V

LMT85

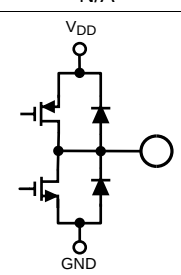
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www.ti.com.cn

6 Pin Configuration and Functions



Pin Functions

NAME	PIN			TYPE	DESCRIPTION	
	SOT (SC70)	TO-92	TO-92S		EQUIVALENT CIRCUIT	FUNCTION
GND	2 ⁽¹⁾ , 5	3	2	Ground	N/A	Power Supply Ground
OUT	3	2	1	Analog Output		Outputs a voltage that is inversely proportional to temperature
V _{DD}	1, 4	1	3	Power	N/A	Positive Supply Voltage

(1) Direct connection to the back side of the die

7 Specifications

7.1 Absolute Maximum Ratings

See ⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Supply voltage	−0.3	6	V
Voltage at output pin	−0.3	(V _{DD} + 0.5)	V
Output current	−7	7	mA
Input current at any pin ⁽³⁾	−5	5	mA
Maximum junction temperature (T _{JMAX})		150	°C
Storage temperature, T _{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.
- (3) When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > V), the current at that pin should be limited to 5 mA.

7.2 ESD Ratings

	VALUE	UNIT
LMT85LP in TO-92/TO-92S package		
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾⁽²⁾	±2500
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±1000
LMT85DCK in SC70 package		
V _(ESD) Electrostatic discharge	Human-body model (HBM), per JESD22-A114 ⁽²⁾	±2500
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Specified temperature	T _{MIN} ≤ T _A ≤ T _{MAX}		°C
	−50 ≤ T _A ≤ 150		°C
Supply voltage (V _{DD})	1.8	5.5	V

7.4 Thermal Information⁽¹⁾

THERMAL METRIC ⁽²⁾		LMT85/ LMT85-Q1	LMT85LP	LMT85LPG	UNIT
		DCK (SOT/SC70)	LP/LPM (TO-92)	LPG (TO-92S)	
		5 PINS	3 PINS	3 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽³⁾⁽⁴⁾	275	167	130.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	84	90	64.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	56	146	106.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.2	35	14.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	55	146	106.2	°C/W

- (1) For information on self-heating and thermal response time, see section [Mounting and Thermal Conductivity](#).
- (2) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.
- (3) The junction to ambient thermal resistance (R_{θJA}) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
- (4) Changes in output due to self-heating can be computed by multiplying the internal dissipation by the thermal resistance.

7.5 Accuracy Characteristics

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in [Table 3](#).

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
Temperature accuracy ⁽³⁾	$T_A = T_J = 20^{\circ}\text{C}$ to 150°C ; $V_{DD} = 1.8\text{ V}$ to 5.5 V	-2.7	± 0.4	2.7	$^{\circ}\text{C}$
	$T_A = T_J = 0^{\circ}\text{C}$ to 150°C ; $V_{DD} = 1.9\text{ V}$ to 5.5 V	-2.7	± 0.7	2.7	$^{\circ}\text{C}$
	$T_A = T_J = 0^{\circ}\text{C}$ to 150°C ; $V_{DD} = 2.6\text{ V}$ to 5.5 V		± 0.3		$^{\circ}\text{C}$
	$T_A = T_J = -50^{\circ}\text{C}$ to 0°C ; $V_{DD} = 2.3\text{ V}$ to 5.5 V	-2.7	± 0.7	2.7	$^{\circ}\text{C}$
	$T_A = T_J = -50^{\circ}\text{C}$ to 0°C ; $V_{DD} = 2.9\text{ V}$ to 5.5 V		± 0.25		$^{\circ}\text{C}$

- (1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
- (2) Typical values are at $T_J = T_A = 25^{\circ}\text{C}$ and represent most likely parametric norm.
- (3) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Transfer Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in $^{\circ}\text{C}$). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

7.6 Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$. MIN and MAX limits apply for $T_A = T_J = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted; typical values apply for $T_A = T_J = 25^{\circ}\text{C}$.

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
Average sensor gain (output transfer function slope)	-30°C and 90°C used to calculate average sensor gain		-8.2		$\text{mV}/^{\circ}\text{C}$
Load regulation ⁽³⁾	Source $\leq 50\text{ }\mu\text{A}$, $(V_{DD} - V_{\text{OUT}}) \geq 200\text{ mV}$	-1	-0.22		mV
	Sink $\leq 50\text{ }\mu\text{A}$, $V_{\text{OUT}} \geq 200\text{ mV}$		0.26	1	mV
Line regulation ⁽⁴⁾			200		$\mu\text{V}/\text{V}$
I_S Supply current	$T_A = T_J = 30^{\circ}\text{C}$ to 150°C , $(V_{DD} - V_{\text{OUT}}) \geq 100\text{ mV}$		5.4	8.1	μA
	$T_A = T_J = -50^{\circ}\text{C}$ to 150°C , $(V_{DD} - V_{\text{OUT}}) \geq 100\text{ mV}$		5.4	9	μA
C_L Output load capacitance			1100		pF
Power-on time ⁽⁵⁾	$C_L = 0\text{ pF}$ to 1100 pF		0.7	1.9	ms
Output drive	$T_A = T_J = 25^{\circ}\text{C}$	-50		+50	μA

- (1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
- (2) Typical values are at $T_J = T_A = 25^{\circ}\text{C}$ and represent most likely parametric norm.
- (3) Source currents are flowing out of the LMT85. Sink currents are flowing into the LMT85.
- (4) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in [Output Voltage Shift](#).
- (5) Specified by design and characterization.

7.7 Typical Characteristics

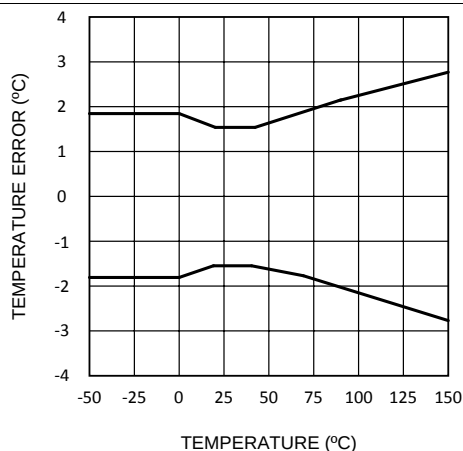


Figure 1. Temperature Error vs Temperature

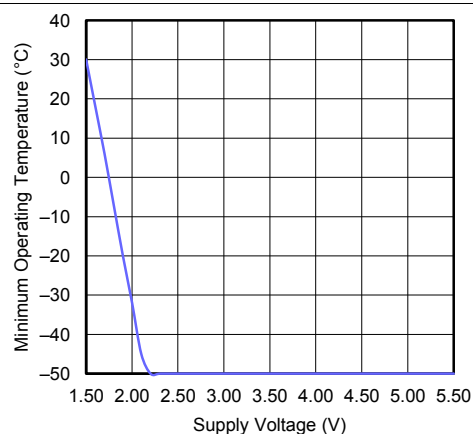


Figure 2. Minimum Operating Temperature vs Supply Voltage

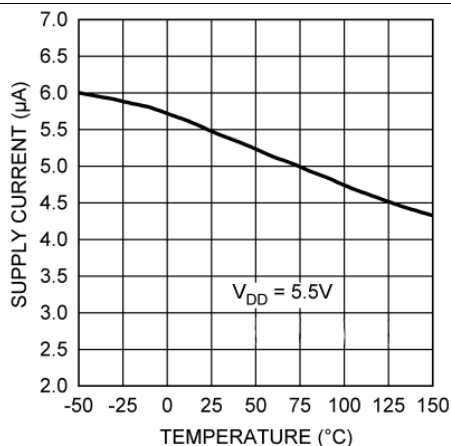


Figure 3. Supply Current vs Temperature

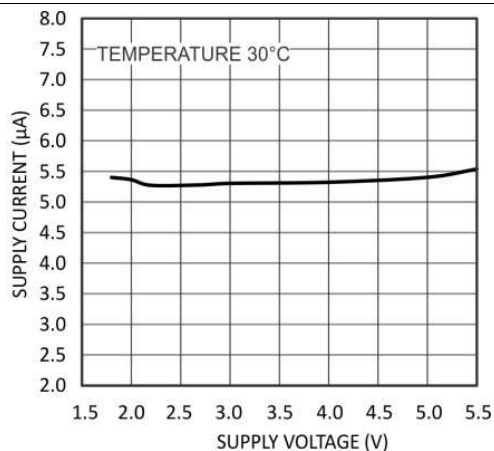


Figure 4. Supply Current vs Supply Voltage

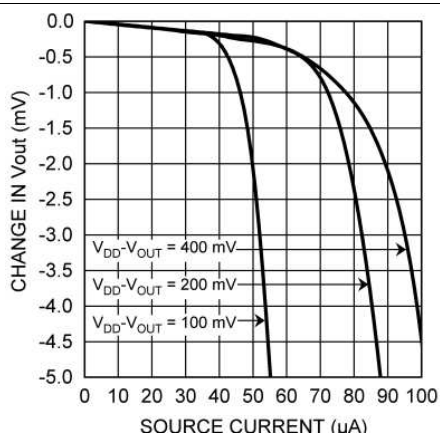


Figure 5. Load Regulation, Sourcing Current

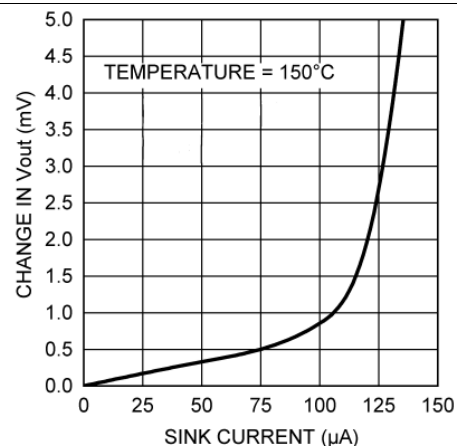


Figure 6. Load Regulation, Sinking Current

Typical Characteristics (continued)

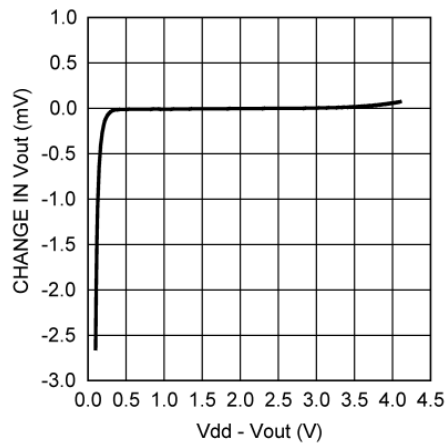


Figure 7. Change in Vout vs Overhead Voltage

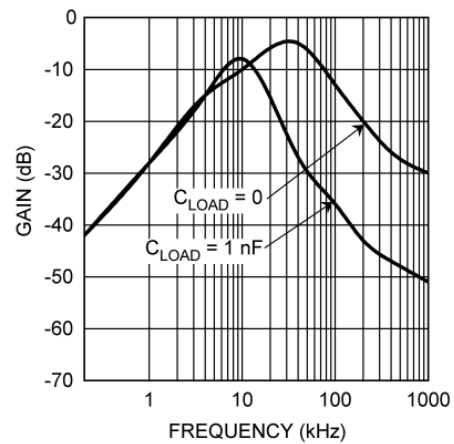


Figure 8. Supply-Noise Gain vs Frequency

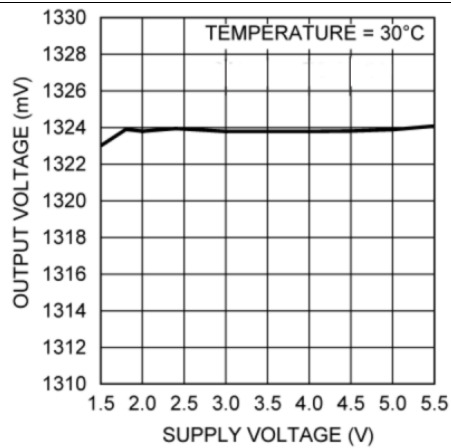


Figure 9. Output Voltage vs Supply Voltage

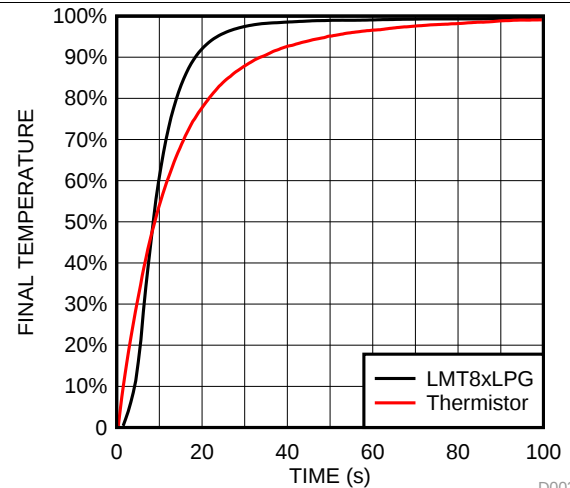


Figure 10. LMT85LPG Thermal Response vs Common Leaded Thermistor With 1.2-m/s Airflow

D003

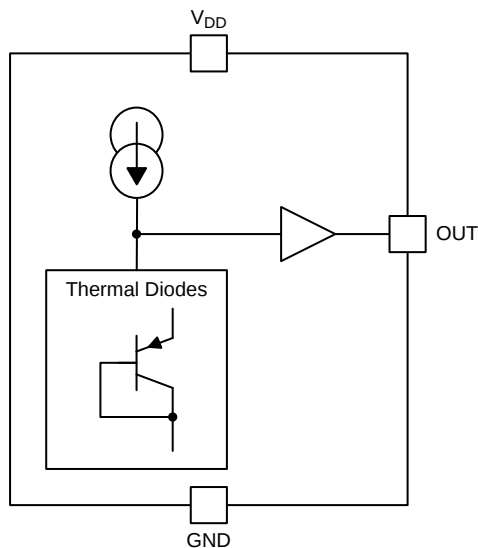
8 Detailed Description

8.1 Overview

The LMT85 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature-sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source.

8.2 Functional Block Diagram

Full-Range Celsius Temperature Sensor (–50°C to 150°C).



8.3 Feature Description

8.3.1 LMT85 Transfer Function

The output voltage of the LMT85, across the complete operating temperature range, is shown in [Table 3](#). This table is the reference from which the LMT85 accuracy specifications (listed in the [Accuracy Characteristics](#) section) are determined. This table can be used, for example, in a host processor look-up table. A file containing this data is available for download at the [LMT85](#) product folder under *Tools and Software Models*.

Table 3. LMT85 Transfer Table

TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)
-50	1955	-10	1648	30	1324	70	991	110	651
-49	1949	-9	1639	31	1316	71	983	111	642
-48	1942	-8	1631	32	1308	72	974	112	634
-47	1935	-7	1623	33	1299	73	966	113	625
-46	1928	-6	1615	34	1291	74	957	114	617
-45	1921	-5	1607	35	1283	75	949	115	608
-44	1915	-4	1599	36	1275	76	941	116	599
-43	1908	-3	1591	37	1267	77	932	117	591
-42	1900	-2	1583	38	1258	78	924	118	582
-41	1892	-1	1575	39	1250	79	915	119	573
-40	1885	0	1567	40	1242	80	907	120	565
-39	1877	1	1559	41	1234	81	898	121	556
-38	1869	2	1551	42	1225	82	890	122	547

Feature Description (continued)
Table 3. LMT85 Transfer Table (continued)

TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)
-37	1861	3	1543	43	1217	83	881	123	539
-36	1853	4	1535	44	1209	84	873	124	530
-35	1845	5	1527	45	1201	85	865	125	521
-34	1838	6	1519	46	1192	86	856	126	513
-33	1830	7	1511	47	1184	87	848	127	504
-32	1822	8	1502	48	1176	88	839	128	495
-31	1814	9	1494	49	1167	89	831	129	487
-30	1806	10	1486	50	1159	90	822	130	478
-29	1798	11	1478	51	1151	91	814	131	469
-28	1790	12	1470	52	1143	92	805	132	460
-27	1783	13	1462	53	1134	93	797	133	452
-26	1775	14	1454	54	1126	94	788	134	443
-25	1767	15	1446	55	1118	95	779	135	434
-24	1759	16	1438	56	1109	96	771	136	425
-23	1751	17	1430	57	1101	97	762	137	416
-22	1743	18	1421	58	1093	98	754	138	408
-21	1735	19	1413	59	1084	99	745	139	399
-20	1727	20	1405	60	1076	100	737	140	390
-19	1719	21	1397	61	1067	101	728	141	381
-18	1711	22	1389	62	1059	102	720	142	372
-17	1703	23	1381	63	1051	103	711	143	363
-16	1695	24	1373	64	1042	104	702	144	354
-15	1687	25	1365	65	1034	105	694	145	346
-14	1679	26	1356	66	1025	106	685	146	337
-13	1671	27	1348	67	1017	107	677	147	328
-12	1663	28	1340	68	1008	108	668	148	319
-11	1656	29	1332	69	1000	109	660	149	310
								150	301

Although the LMT85 is very linear, its response does have a slight umbrella parabolic shape. This shape is very accurately reflected in [Table 3](#). The Transfer Table can be calculated by using the parabolic equation ([Equation 1](#)).

$$V_{TEMP} (mV) = 1324.0mV - \left[8.194 \frac{mV}{^{\circ}C} (T - 30^{\circ}C) \right] - \left[0.00262 \frac{mV}{^{\circ}C^2} (T - 30^{\circ}C)^2 \right] \quad (1)$$

The parabolic equation is an approximation of the transfer table and the accuracy of the equation degrades slightly at the temperature range extremes. [Equation 1](#) can be solved for T resulting in:

$$T = \frac{8.194 - \sqrt{(-8.194)^2 + 4 \times 0.00262 \times (1324 - V_{TEMP} (mV))}}{2 \times -0.00262} + 30 \quad (2)$$

For an even less accurate linear transfer function approximation, a line can easily be calculated over the desired temperature range using values from the Table and a two-point equation ([Equation 3](#)):

$$V - V_1 = \left(\frac{V_2 - V_1}{T_2 - T_1} \right) \times (T - T_1)$$

where

- V is in mV,
- T is in °C,
- T₁ and V₁ are the coordinates of the lowest temperature,
- and T₂ and V₂ are the coordinates of the highest temperature.

(3)

For example, if the user wanted to resolve this equation, over a temperature range of 20°C to 50°C, they would proceed as follows:

$$V - 1405 \text{ mV} = \left(\frac{1159 \text{ mV} - 1405 \text{ mV}}{50^\circ\text{C} - 20^\circ\text{C}} \right) \times (T - 20^\circ\text{C}) \quad (4)$$

$$V - 1405 \text{ mV} = (-8.20 \text{ mV} / ^\circ\text{C}) \times (T - 20^\circ\text{C}) \quad (5)$$

$$V = (-8.20 \text{ mV} / ^\circ\text{C}) \times T + 1569 \text{ mV} \quad (6)$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

8.4 Device Functional Modes

8.4.1 Mounting and Thermal Conductivity

The LMT85 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good thermal conductivity, the backside of the LMT85 die is directly attached to the GND pin. The temperatures of the lands and traces to the other leads of the LMT85 will also affect the temperature reading.

Alternatively, the LMT85 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT85 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the output to ground or V_{DD} , the output from the LMT85 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction to ambient ($R_{\theta JA}$ or θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. Use [Equation 7](#) to calculate the rise in the LMT85 die temperature:

$$T_J = T_A + \theta_{JA} [(V_{DD} I_S) + (V_{DD} - V_{OUT}) I_L]$$

where

- T_A is the ambient temperature,
 - I_S is the supply current,
 - I_L is the load current on the output,
 - and V_O is the output voltage.
- (7)

For example, in an application where $T_A = 30^\circ\text{C}$, $V_{DD} = 5 \text{ V}$, $I_S = 5.4 \mu\text{A}$, $V_{OUT} = 1324 \text{ mV}$, and $I_L = 2 \mu\text{A}$, the junction temperature would be 30.014°C , showing a self-heating error of only 0.014°C . Because the junction temperature of the LMT85 is the actual temperature being measured, take care to minimize the load current that the LMT85 is required to drive. [Thermal Information](#) shows the thermal resistance of the LMT85.

8.4.2 Output and Noise Considerations

A push-pull output gives the LMT85 the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. The LMT85 device is ideal for this and other applications which require strong source or sink current.

The LMT85 supply-noise gain (the ratio of the AC signal on V_{OUT} to the AC signal on V_{DD}) was measured during bench tests. The typical attenuation is shown in [Figure 8](#) found in the [Typical Characteristics](#). A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 5 centimeters of the LMT85.

Device Functional Modes (continued)

8.4.3 Capacitive Loads

The LMT85 handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the LMT85 can drive a capacitive load less than or equal to 1100 pF as shown in [Figure 11](#). For capacitive loads greater than 1100 pF, a series resistor may be required on the output, as shown in [Figure 12](#).

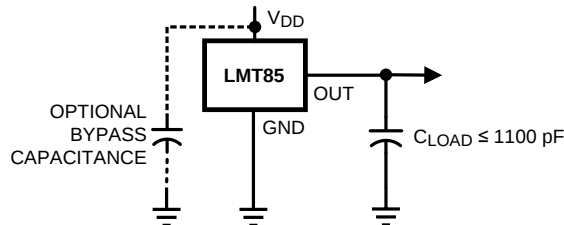


Figure 11. LMT85 No Decoupling Required for Capacitive Loads Less Than 1100 pF

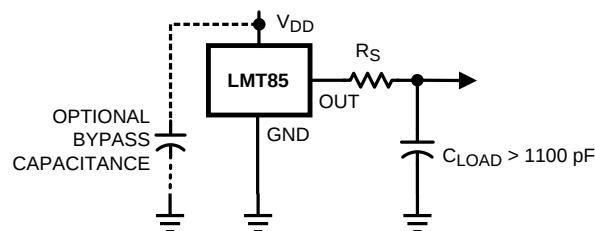


Figure 12. LMT85 with Series Resistor for Capacitive Loading Greater Than 1100 pF

Table 4. Recommended Series Resistor Values

C_{LOAD}	MINIMUM R_S
1.1 nF to 99 nF	3 k Ω
100 nF to 999 nF	1.5 k Ω
1 μ F	800 Ω

8.4.4 Output Voltage Shift

The LMT85 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{OUT} . The shift typically occurs when $V_{DD} - V_{OUT} = 1$ V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{OUT} . Because the shift takes place over a wide temperature change of 5°C to 20°C, V_{OUT} is always monotonic. The accuracy specifications in the [Accuracy Characteristics](#) table already include this possible shift.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMT85 features make it suitable for many general temperature-sensing applications. It can operate down to 1.8-V supply with 5.4- μ A power consumption, making it ideal for battery powered devices. Package options like the through-hole TO-92 package allow the LMT85 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations in the same application.

9.2 Typical Applications

9.2.1 Connection to an ADC

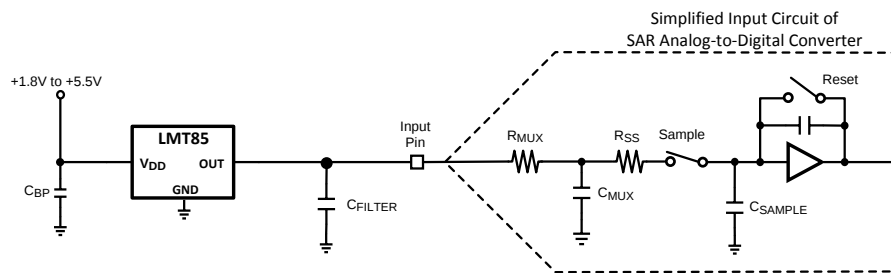


Figure 13. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

9.2.1.1 Design Requirements

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT85 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor (C_{FILTER}).

9.2.1.2 Detailed Design Procedure

The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Because not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

9.2.1.3 Application Curve

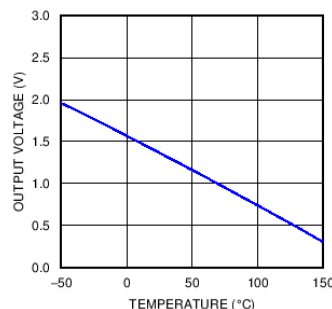


Figure 14. Analog Output Transfer Function

Typical Applications (continued)

9.2.2 Conserving Power Dissipation With Shutdown

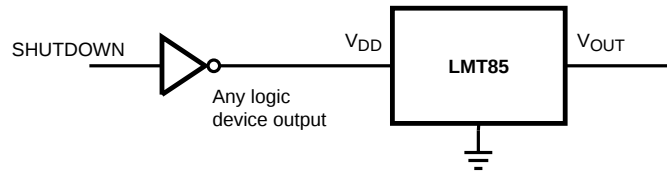


Figure 15. Simple Shutdown Connection of the LMT85

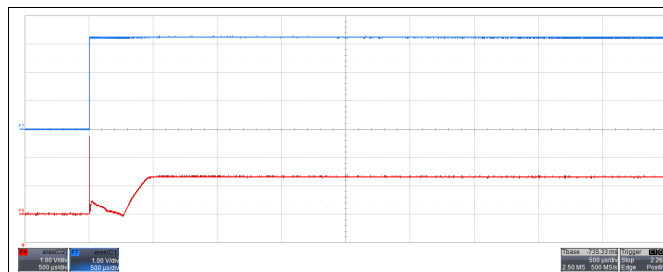
9.2.2.1 Design Requirements

Because the power consumption of the LMT85 is less than 9 μA , it can simply be powered directly from any logic gate output and therefore not require a specific shutdown pin. The device can even be powered directly from a micro controller GPIO. In this way, it can easily be turned off for cases such as battery-powered systems where power savings are critical.

9.2.2.2 Detailed Design Procedure

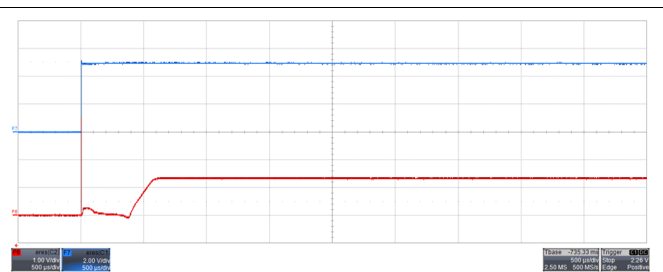
Simply connect the V_{DD} pin of the LMT85 directly to the logic shutdown signal from a microcontroller.

9.2.2.3 Application Curves



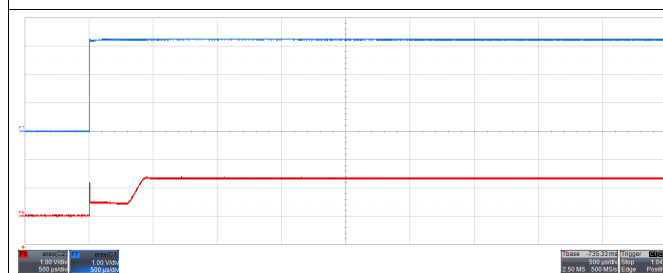
Time: 500 $\mu\text{s}/\text{div}$; Top Trace: V_{DD} 1 V/div;
Bottom Trace: OUT 1 V/div

Figure 16. Output Turnon Response Time Without a Capacitive Load and $V_{\text{DD}} = 3.3 \text{ V}$



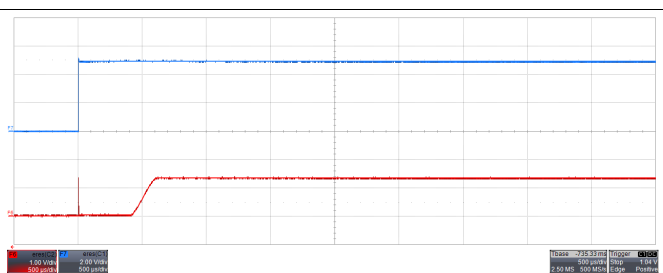
Time: 500 $\mu\text{s}/\text{div}$; Top trace: V_{DD} 2 V/div;
Bottom trace: OUT 1 V/div

Figure 17. Output Turnon Response Time Without a Capacitive Load and $V_{\text{DD}} = 5 \text{ V}$



Time: 500 $\mu\text{s}/\text{div}$; Top trace: V_{DD} 1 V/div;
Bottom trace: OUT 1 V/div

Figure 18. Output Turnon Response Time With 1.1-nF Capacitive Load and $V_{\text{DD}} = 3.3 \text{ V}$



Time: 500 $\mu\text{s}/\text{div}$; Top trace: V_{DD} 2 V/div;
Bottom trace: OUT 1 V/div

Figure 19. Output Turnon Response Time With 1.1-nF Capacitive Load and $V_{\text{DD}} = 5 \text{ V}$

10 Power Supply Recommendations

The low supply current and supply range (1.8 V to 5.5 V) of the LMT85 allow the device to easily be powered from many sources. Power supply bypassing is optional and is mainly dependent on the noise on the power supply used. In noisy systems it may be necessary to add bypass capacitors to lower the noise that is coupled to the output of the LMT85.

11 Layout

11.1 Layout Guidelines

The LMT85 is extremely simple to layout. If a power-supply bypass capacitor is used, it should be connected as shown in the [Layout Example](#)

11.2 Layout Example

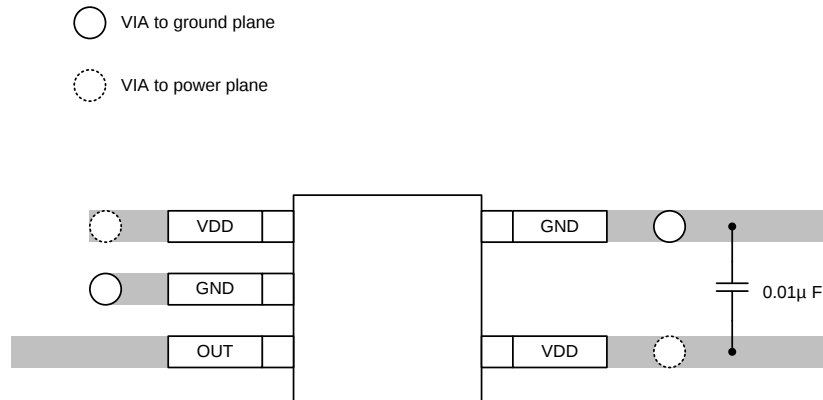


Figure 20. SC70 Package Recommended Layout

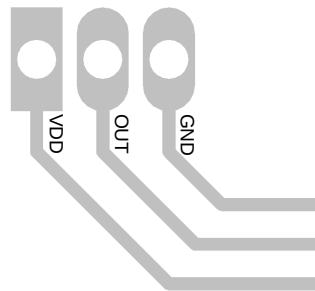


Figure 21. TO-92 LP Package Recommended Layout

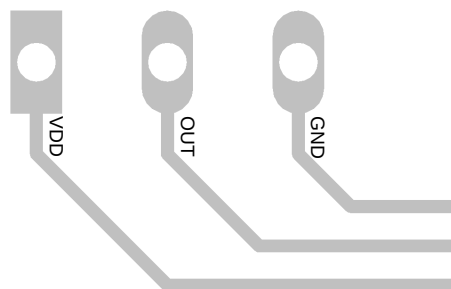


Figure 22. TO-92 LPM Package Recommended Layout

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMT85DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-50 to 150	BPA
LMT85DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-50 to 150	BPA
LMT85DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-50 to 150	BPA
LMT85DCKT	Obsolete	Production	SC70 (DCK) 5	-	-	Call TI	Call TI	-50 to 150	BPA
LMT85LP	Active	Production	TO-92 (LP) 3	1800 LARGE T&R	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LP.A	Active	Production	TO-92 (LP) 3	1800 LARGE T&R	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LP.B	Active	Production	TO-92 (LP) 3	1800 LARGE T&R	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPG	Active	Production	TO-92 (LPG) 3	1000 BULK	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPG.A	Active	Production	TO-92 (LPG) 3	1000 BULK	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPG.B	Active	Production	TO-92 (LPG) 3	1000 BULK	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPGM	Active	Production	TO-92 (LPG) 3	3000 AMMO	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPGM.A	Active	Production	TO-92 (LPG) 3	3000 AMMO	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPGM.B	Active	Production	TO-92 (LPG) 3	3000 AMMO	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPM	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPM.A	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85
LMT85LPM.B	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	-50 to 150	LMT85

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

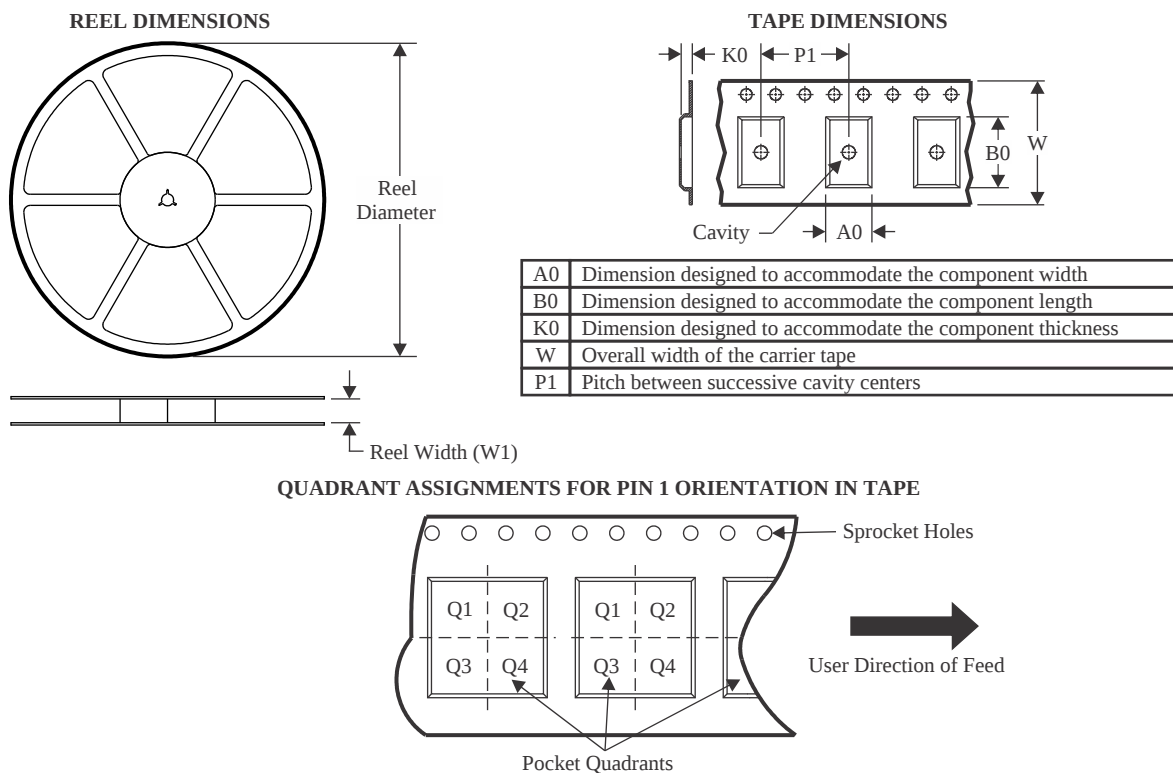
OTHER QUALIFIED VERSIONS OF LMT85 :

- Automotive : [LMT85-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

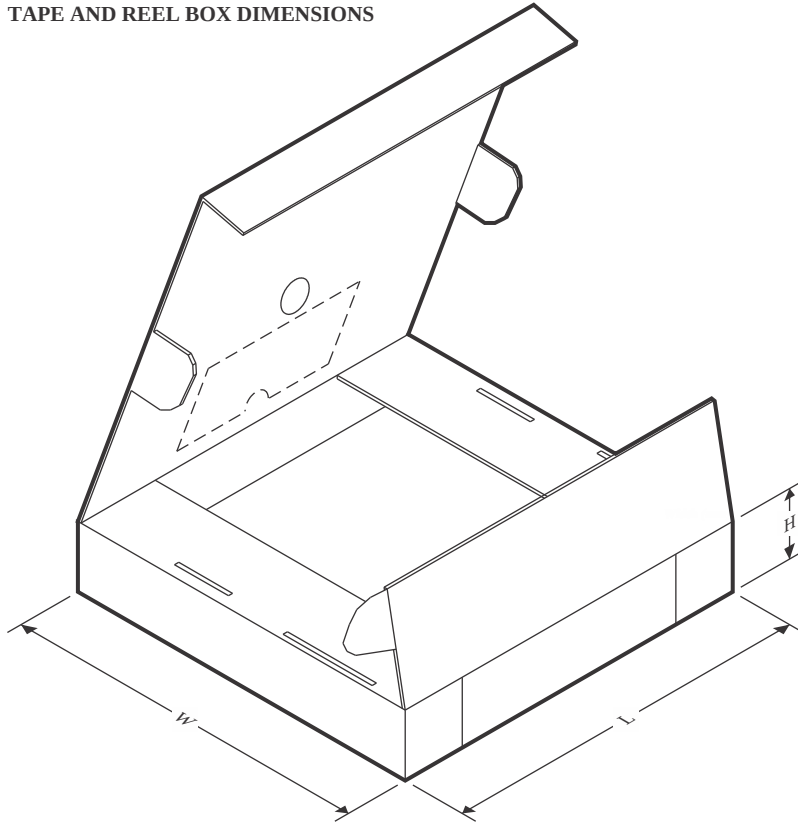
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMT85DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMT85DCKR	SC70	DCK	5	3000	208.0	191.0	35.0



PACKAGE OUTLINE

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

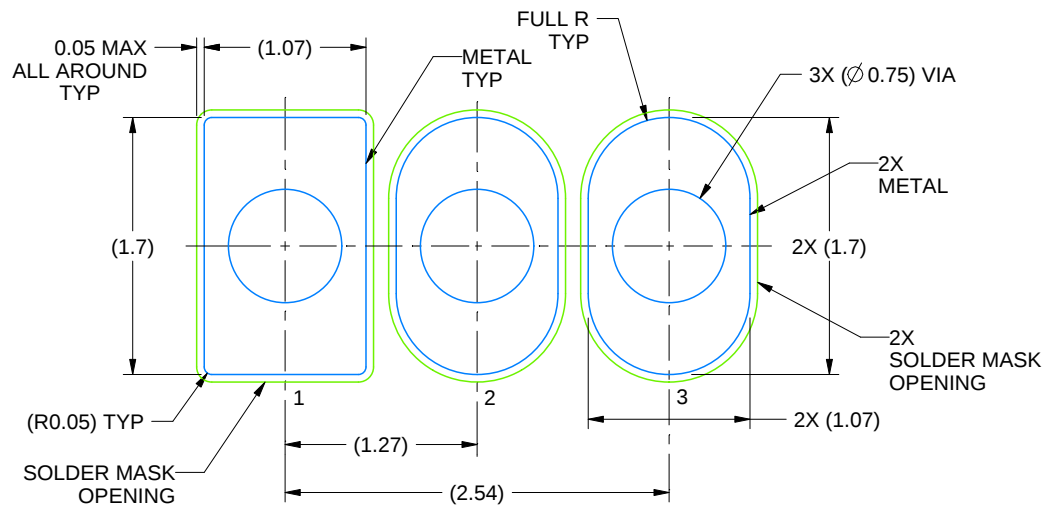
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

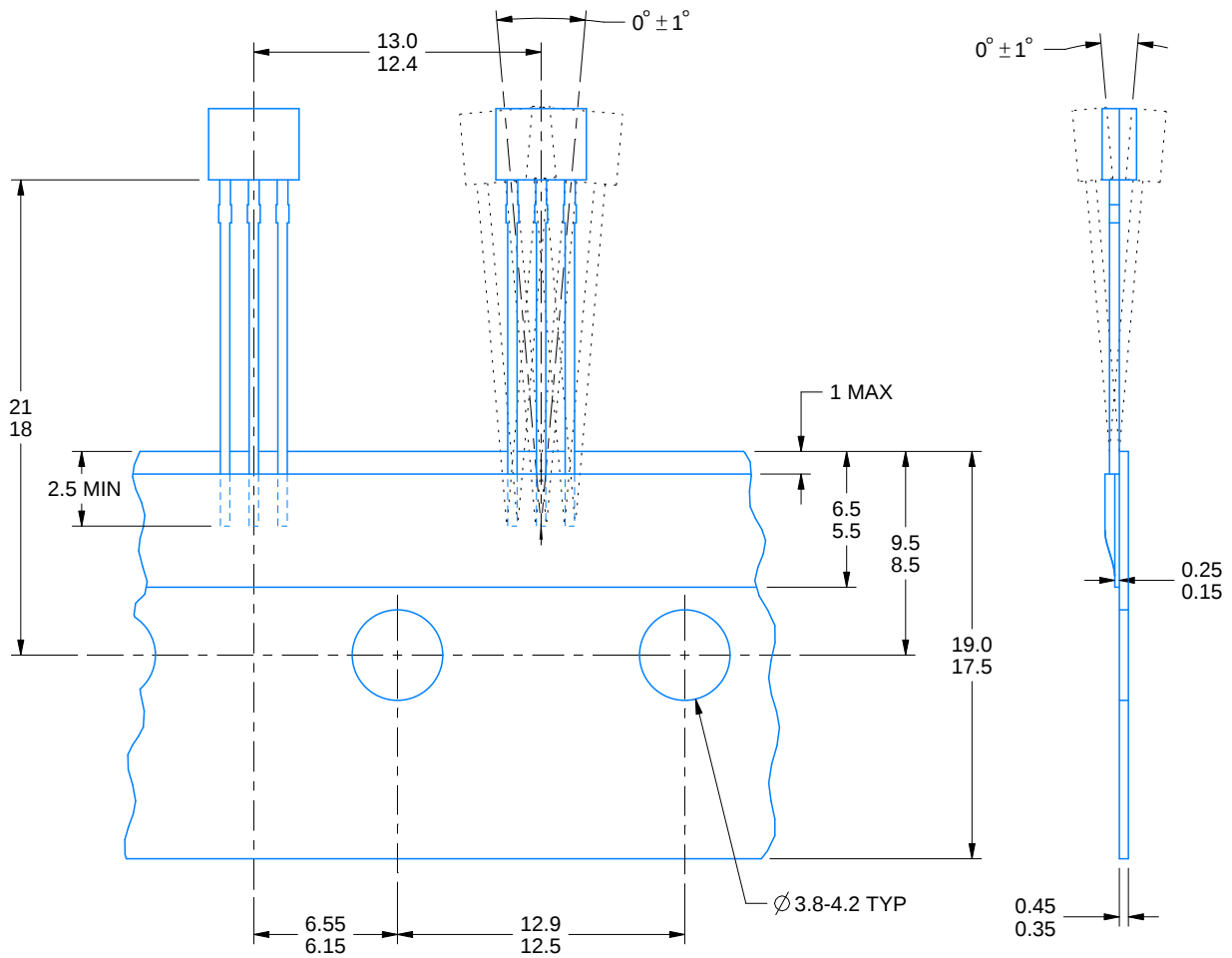
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018



SOT - 1.1 max height

Technical drawing of a mechanical part showing three views: front, side, and top.

Front View Dimensions:

- Overall width: 2.4 (1.8)
- Overall height: 2.15 (1.85)
- Horizontal hole positions: 1.4 (1.1)
- Vertical hole positions: 1.3 (1.3)
- Hole diameters: (0.15), (0.1)
- Feature **NOTE 4** is indicated.
- Hatched area labeled **PIN 1 INDEX AREA**.

Side View Dimensions:

- Width: 1.1 MAX
- Thickness: 0.1
- Angle: 4X 0° -12°

Top View Dimensions:

- Width: 0.46 TYP
- Height: 0.22 TYP
- Angle: 8° 0° TYP
- Feature **NOTE 5** is indicated.

Feature Control Frames:

- Top View:** ϕ 0.1 M C A B
- Side View:** 0.1 C

Other Labels:

- GAGE PLANE** (indicated on the top view)
- SEATING PLANE** (indicated on the top view)
- NOTE 4** (points to a feature on the front view)
- NOTE 5** (points to a feature on the top view)

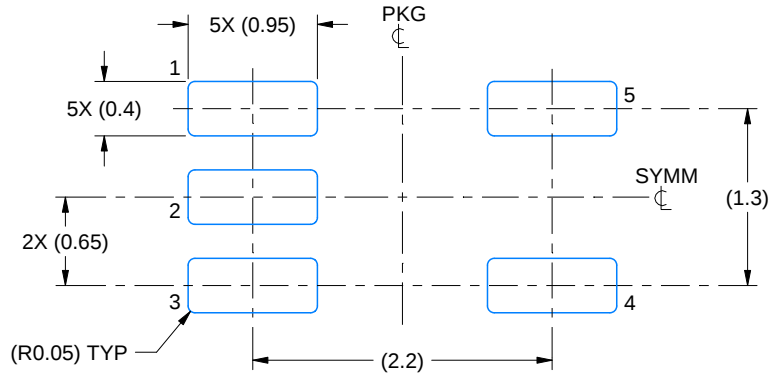
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

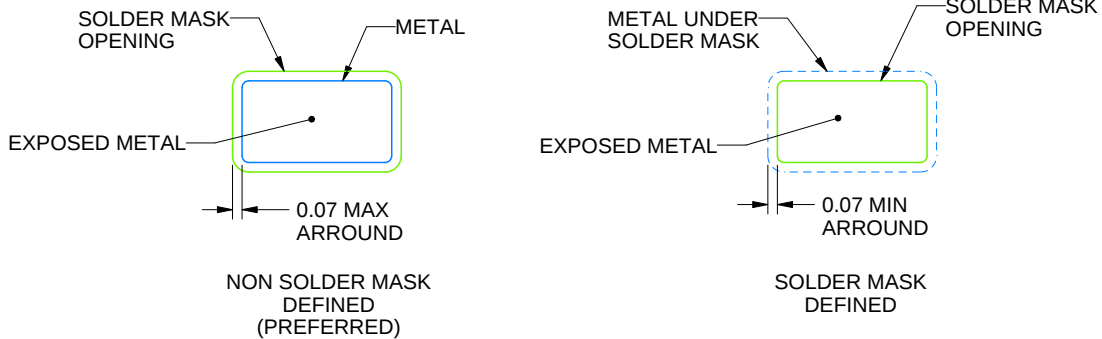
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

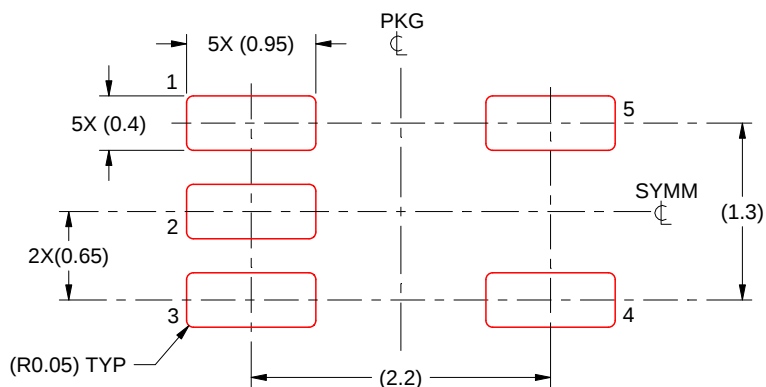


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



TO-92 - 5.34 mm max height

Technical drawing of a 12-pin connector showing two views: a side view on the left and a top view on the right.

Side View Dimensions:

- Overall width: $2 \times \frac{2.9}{2.4}$
- Pin width: $2 \times 4 \text{ MAX}$
- Seating Plane

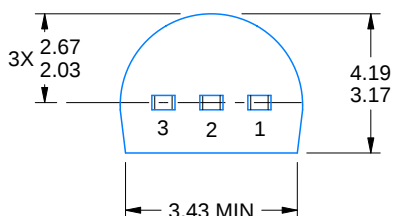
Top View Dimensions:

- Overall width: $5.21 / 4.44$
- Pin pitch: $(2.54) \text{ NOTE 3}$
- Pin width: $6 \times 0.076 \text{ MAX}$
- Seating Plane
- Pin length: $3 \times 12.7 \text{ MIN}$
- Pin diameter: $3 \times \frac{0.55}{0.38}$
- Pin spacing: $2 \times 1.27 \pm 0.13$
- Pin diameter: $3 \times \frac{0.43}{0.35}$

Notes:

- EJECTOR PIN OPTIONAL

STRAIGHT LEAD OPTION



NOTES:

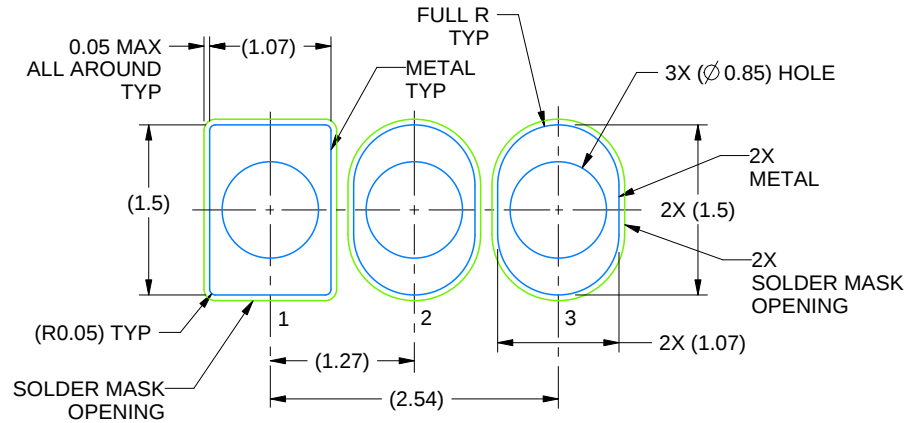
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
 - a. Straight lead option available in bulk pack only.
 - b. Formed lead option available in tape and reel or ammo pack.
 - c. Specific products can be offered in limited combinations of shipping medium and lead options.
 - d. Consult product folder for more information on available options.

EXAMPLE BOARD LAYOUT

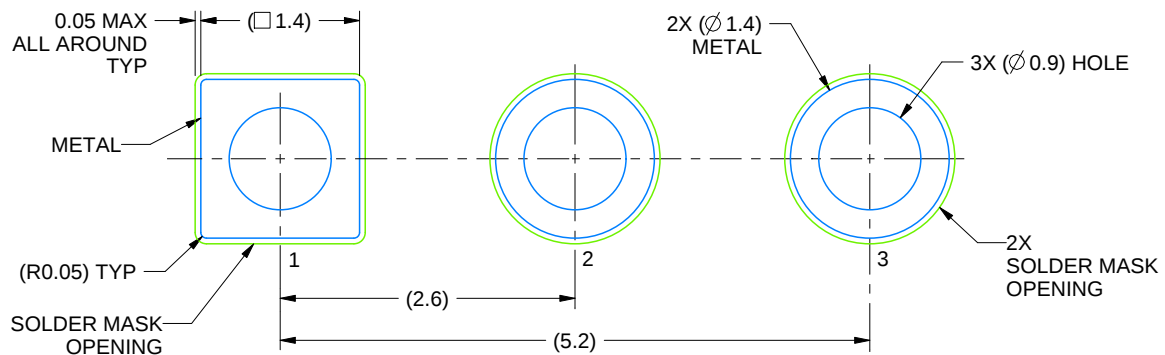
LP0003A

TO-92 - 5.34 mm max height

TO-92



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

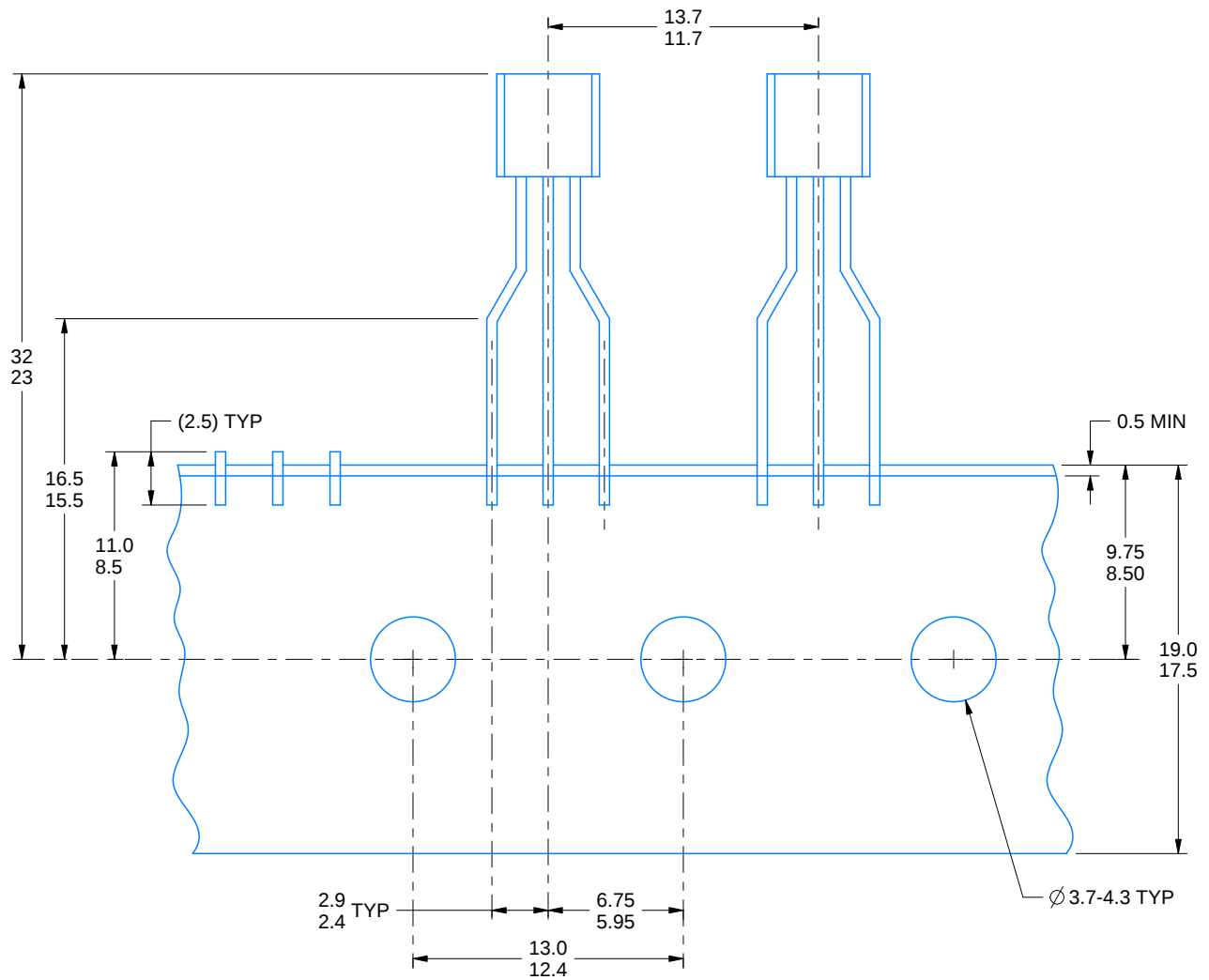
4215214/C 04/2025

TAPE SPECIFICATIONS

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/C 04/2025

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