具有相位同步功能和 JESD204B 支持的 LMX2595 20GHz 宽带 PLLATINUM™ 射频合成器

1 特性

- 10MHz 至 20GHz 输出频率
- 在 100KHz 偏频和 15GHz 载波的情况下具有 -110dBc/Hz 的相位噪声
- 7.5GHz 时，具有 45fs rms 抖动（100Hz 至 100MHz）
- 可编程输出功率
- PLL 主要规格
  - 品质因数：-236dBc/Hz
  - 标称 1/f 噪声：-129dBc/Hz
  - 最高相位检测器频率
    - 400MHz 整数模式
    - 300MHz 分数模式
  - 32 位分数 N 分频器
- 用可编程输入乘法器消除整数边界杂散
- 跨多个设备实现输出相位同步
- 支持具有 9ps 分辨率可编程延迟的 SYSREF
- 用于 FMCW 应用的频率斜升和线性调频脉冲生成能力
- 小于 20µs VCO 校准速度
- 3.3V 单电源运行

2 应用

- 5G 和毫米波无线基础设施
- 测试和测量设备
- 雷达
- MIMO
- 相控阵天线和波束形成
- 高速数据转换器时钟（支持 JESD204B）

3 说明

LMX2595 高性能宽带合成器可生成 10MHz 至 20GHz 范围内的任何频率。集成加倍器用于生成 15GHz 以上的频率。品质因数为 -236dBc/Hz 的高性能 PLL 和高相位检测器频率可实现非常低的带内噪声和集成抖动。高速 N 分频器没有预分频器，从而显著减少了杂散的振幅和数量。还有一个可减轻整数边界杂散的可编程输入乘法器。

LMX2595 允许用户同步多个器件的输出，并可在 输入和输出之间确定需要延迟的情况下 应用。频率斜升发生器可在自动斜坡生成选项或手动选项中最多合成 2 段斜坡，以实现最大的灵活性。通过快速校准算法可将频率加快至 20µs 以上。LMX2595 增添了对生成或重复 SYSREF（符合 JESD204B 标准）的支持，此 SYSREF 是高速数据转换器的理想低噪声时钟源。此配置中提供了精细的延迟调节（9ps 分辨率），以解决板迹线的延迟差异。

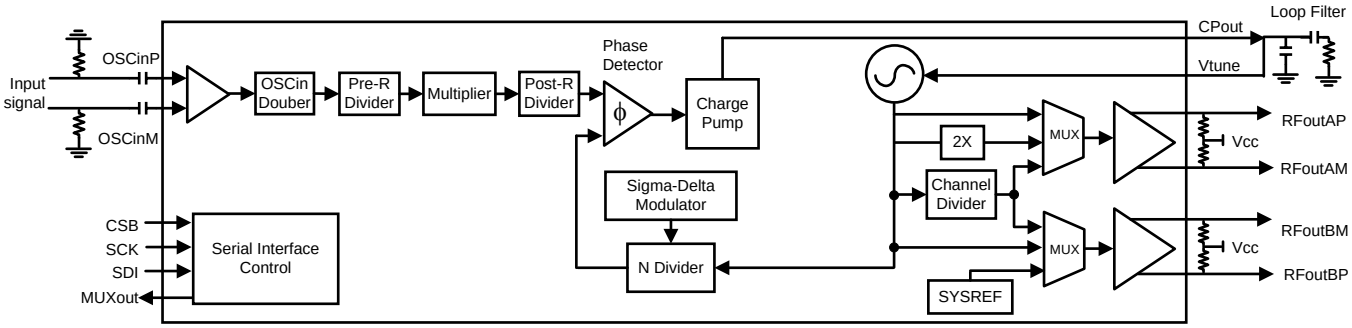
LMX2595 中的输出驱动器在载波频率为 15GHz 时提供高达 7dBm 的输出功率。该器件采用单个 3.3V 电源供电，并具有集成的 LDO，无需板载低噪声 LDO。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMX2595	VQFN (40)	6.00mm × 6.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 6
6 **Specifications** ... 8
6.1 Absolute Maximum Ratings ... 8
6.2 ESD Ratings ... 8
6.3 Recommended Operating Conditions ... 8
6.4 Thermal Information ... 8
6.5 Electrical Characteristics ... 9
6.6 Timing Requirements ... 12
6.7 Typical Characteristics ... 15
7 **Detailed Description** ... 20
7.1 Overview ... 20
7.2 Functional Block Diagram ... 21
7.3 Feature Description ... 21
7.4 Device Functional Modes ... 41
7.5 Programming ... 42
7.6 Register Maps ... 43
8 **Application and Implementation** ... 61
8.1 Application Information ... 61
8.2 Typical Application ... 64
9 **Power Supply Recommendations** ... 67
10 **Layout** ... 68
10.1 Layout Guidelines ... 68
10.2 Layout Example ... 69
11 器件和文档支持 ... 70
11.1 器件支持 ... 70
11.2 文档支持 ... 70
11.3 接收文档更新通知 ... 70
11.4 社区资源 ... 70
11.5 商标 ... 70
11.6 静电放电警告 ... 70
11.7 术语表 ... 70
12 机械、封装和可订购信息 ... 71

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (March 2018) to Revision C — **Page**

- 已更改 将数据表中的最大输出频率从 19GHz 统改为 20GHz。为 DBLR_IBIAS_CTRL1 (R25[15:0]) 新建议的值扩大了输出频率范围，提高了高频性能。DBLR_IBIAS_CTRL1 的原值 (1572) 仍支持高达 19GHz 的输出频率以及电气特性 表中确定的规格。新值 (3115) 可进一步提高性能。 ... 1
- Deleted the recommended bypass capacitor values for Vcc pins 7, 11, 15, 21, 26 and 37, as these capacitor values are not mandatory and the power supply filtering design is up to the user. ... 7
- Added test condition "DBLR_IBIAS_CTRL1 = 1572" for P_{OUT}, L_{VCO2X} and H1/2, in order to emphasize that these data are taken while DBLR_IBIAS_CTRL1 is set to the old value (1572). With this register set to 3115, these specs can be improved. The details can be found in the applications section. ... 9
- Added a new row for VCO doubler output range in EC table with DBLR_IBIAS_CTRL1 set to 3115. The frequency range is extended to 20 GHz. ... 9
- Added table note for EC table stating that the performance of 1/2 harmonic, output power and noise floor with doubler enabled can be improved by setting DBLR_IBIAS_CTRL1 = 3115. ... 9
- Changed all the 'FRAC_ORDER' to 'MASH_ORDER' to avoid confusion ... 10
- Changed the names of timing specs to align with timing diagram: changed t_{CE} to t_{ES}, t_{CS} to t_{DCS}, t_{CH} to t_{CDH}, and t_{CES} to t_{ECS} ... 12
- Changed the names of timing specs to align with timing diagram: changed t_{ES} to t_{CE}, t_{CES} to t_{ECS}, added t_{DCS} and t_{CDH}, and changed t_{CS} to t_{CR} ... 13
- Changed the serial data input timing diagram and corrected the typo for 'SCK' ... 13
- Deleted the note 'The CSB transition from high to low must occur when SCK is low' from the serial data input timing diagram, because SPI mode 4 (CPOL = 1, CPHA = 1) is also supported, and SCK is held high when idle in mode 4 ... 13
- Added note for the serial data input timing diagram to explain the t_{CE} requirement for mode 4 (CPOL = 1, CPHA = 1) of SPI, because the diagram only indicated SPI mode 1 (CPOL = 0, CPHA = 0) ... 13
- Changed the serial data readback timing diagram ... 14
- Changed the note about MUXout clocking out and emphasized the effect of t_{CR} on the readback data available time ... 14
- Added phase noise plot for 16-, 17- and 20-GHz frequency output ... 15
- Changed the phase noise plot for 18- and 19-GHz frequency output after changing DBLR_IBIAS_CTRL1 (R25[15:0]) to the new value ... 15

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修订历史记录 (接下页)

- Changed the f_{OUT} test conditions in the *Closed-Loop Phase Noise at 3.5 GHz* graph from: 14 GHz / 2 = 3.5 GHz to: to 14 GHz / 4 = 3.5 GHz 16
- Changed the *Output Power vs Pull-up* graph. Output power below 15GHz is shown in "output power across frequency"; output power above 15GHz is shown in "output power vs temperature with doubler". 17
- Split the *Output Power vs Temperature* typical performance plot into two plots: *Output Power vs Temperature Without Doubler*, which goes up to 15 GHz, and *Output Power vs Temperature With Doubler* that is between 15 GHz and 21 GHz. The data for "without doubler" is unchanged because change of DBLR_IBIAS_CTRL1 does not impact performance under 15 GHz, while the data for "with doubler" plot is taken with DBLR_IBIAS_CTRL1 (R25[15:0]) set to the new value (3115) 17
- Added *Normalized Output Power Across OUTA_PWR With Resistor Pullup* graph 17
- Changed "Vtune" to "Indirect Vtune" when LD_TYPE = 1 23
- Changed description for LD_TYPE. 23
- Added description of Indirect Vtune. 24
- Added description for the 'no assist' mode, mphasized the effect of VCO_SEL, VCO_DACISET_STRT and VCO_CAPCTRL_STRT under 'no assist' mode, and added recommended values for these registers 25
- Added description for the 'full assist' mode to allow the user to set VCO amplitude and capcode using linear interpolation under certain conditions 25
- Changed *OUTx_PWR Recommendations for Resistor Pullup* table 27
- Added description for category 3 of SYNC feature stating that FCAL_EN needs to be 1. 31
- Changed description of MASH_SEED 31
- Added 10-ms wait time before re-programming register R0 in recommended initial power-up sequence 42
- Added the *General Programming Requirements* section based on frequently asked questions 42
- Changed register R4 in the register map to: exposed ACAL_CMP_DLY 43
- Changed the register R20[14] value from 0 to 1 in the full register map to match the R20 register description 43
- Changed register R25 in the register map; exposed the register 'DBLR_IBIAS_CTRL1 44
- Changed the R0[14] register field name in the register map from VCO_PHASE_SYNC_EN to VCO_PHASE_SYNC. to align with the rest of the data sheet 48
- Added recommended value for register CAL_CLK_DIV when lock time is not of concern 48
- Changed the typo for register 'VCO_DACISET' in the register map. Bit 0 of this register was not included in the map. The full register map and register description were correct 50
- Added description to the R4[15:8]: ACAL_CMP_DLY register 50
- Deleted the bit description '0: disabled; 1: enabled' for register 'PLL_N' 51
- Added description to the R60[15:0] LD_DLY register 53
- Added description for register R25[15:0]: DBLR_IBIAS_CTRL1 and changed the default register value from 0x0624 to 0x0C2B 55
- Changed the R31[14] register name from CHDIV_DIV2 to SEG1_EN to align with the naming in the TICS Pro GUI 55
- Changed the R105[1:0] field name from RAMP_NEXT_TRIG to RAMP1_NEXT_TRIG 60
- Added application section "Performance Comparison Between 1572 (0x0624) and 3115 (0x0C2B) For Register DBLR_IBIAS_CTRL1 (R25[15:0])" to compare the performance with old and new DBLR_IBIAS_CTRL1 (R25[15:0]) values. 62
- Added the *Bias Levels of Pins* table 67

Changes from Revision A (August 2017) to Revision B **Page**

- Changed all the VCO Gain typical values in the *Electrical Characteristics* table. This is due to improved measurement methods and NOT a change in the device itself 12
- Moved the high-level output voltage parameter V_{CC} – 0.4 value from the MAX column to the MIN 12
- Moved the high-level output current parameter 0.4 value from the MIN column to the MAX 12
- Changed bulleted text: data is clocked out on MUXout, not SDI pin 14

- Added comment that OSCin is clocked on rising edges of the signal. and reformatted with bulleted list 21
- Added description of the state machine clock 22
- Changed example from: 200 MHz / 2^{32} to: 200 MHz / (2^{32} – 1) 23
- Changed LD_DLY description in Table 4 and removed duplicated text in the *Lock Detect* section 23
- Changed name from VCO_AMPCAL to VCO_DACISET_STRT 25
- Added more programmable settings to Table 5 25
- Changed *VCO Gain* table 26
- Added that OUTx_PWR states 32 to 47 are redundant and reworded section 27
- Added term "IncludedDivide" for clarity 28
- Changed Fixed Diagram to show SEG0, SEG1, SEG2, and SEG3 29
- Changed included channel divide to IncludedDivide and 2 X SEG0 to 2 X SEG1. Also clarified IncludedDivide calculations 31
- Added more description on conditions for phase adust 31
- Changed text from: (VCO_PHASE_SYNC = 1) to: (VCO_PHASE_SYNC = 0) 31
- Changed text so the user does not incorrectly assume that MASH_SEED varies from part ot part 32
- Changed the RAMP_THRESH programming from: 0 to ± 2^{32} to: 0 to ± 2^{33} – 1 32
- Removed comment that RAMP_TRIG_CAL only applies in automatic ramping mode 32
- Changed the RAMP_LOW and _HIGH programming from: 0 to ± 2^{31} to: 0 to ± 2^{33} – 1 32
- Changed description to be in terms of state machine cycles 33
- Changed RAMP_MODE to RAMP_MANUAL in the *Manual Pin Ramping* and *Automatic Ramping* sections 33
- Added that the RampCLK pin input is reclocked to the phase detector frequency 33
- Added that RampDir rising edges should be targeted away from rising edges of RampCLK pin 33
- Changed programming enumerations for RAMP0_INC and RAMP1_INC 35
- Changed programming enumerations for RAMP_THRESH, RAMPx_LEN, and RAMP1_INC 36
- Changed Figure 35 36
- Changed SysRef description 37
- Added divide by 2 to figure 37
- Changed some entries in the table 37
- Changed $f_{INTERPOLATOR}$ SYSREF setup equation in Table 19 37
- Changed SysRef delay from: 224 and 225 to: 225 and 226 38
- Changed "generator" mode to "master" mode. They mean the same thing 38
- Changed description for SYSREF_DIV 38
- Changed Figure 37 39
- Changed wording for repeater mode and master mode 40
- Changed description of a few of the steps 41
- Changed typo in R17 and R19 50
- Deleted reference to VCO_SEL_STRT_EN. This is always 1 50
- Added VCO_SEL_STRT_EN reference. This is always 1 50
- Changed the enumerations 0-3 and added content to the INPIN_LVL field description 52
- Added Divide by 1' to SYSREF_DIV_PRE register description. Also fixed the name misspelling 54
- Deleted redundant formula for Fout and also clarified SYSREF_DIV starts at 4 and counts by 2 54
- Deleted reference to VCO_CAPCTRL_EN, which is always 1, and clarified 56
- Changed text from: f_{MAX} to: f_{HIGH} 57
- Changed text from: RAMP_LIMIT_LOW=2^{32} - (f_{LOW} - f_{VCO}) / f_{PD} × 16777216 to: RAMP_LIMIT_LOW=2^{33} - 16777216 x (f_{VCO} - f_{LOW}) / f_{PD} 57
- Removed the *OSCin Configuration* table and added content to the *OSCin Configuration* section 61
- Changed pin 27 recommendation from 10 µF to 1 µF in Figure 62 64

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Changes from Original (June 2017) to Revision A **Page**

- Clarified that output power assumes that load is matched and losses are de-embedded 9
- Changed "SDA" pin name mispelled. Should be "SDI". Also fixed in timing diagrams. Also added CE Pin 12
- Swapped SDI and SCK in diagram 13
- Added section on fine tune adjustments 32
- Added INPIN_IGNORE, INPIN_LVL, and INPIN_HYST 45
- Removed RAMP0_FL from register map 47
- Clarified MASH_RESET_N. 0 = RESET (integer mode), 1 = Fractional mode 51
- Changed OUT_ISEL to OUTI_SET 52
- Added section for input register descriptions 52
- Fixed TYPO table to match main register map. 55
- Corrected RAMP_BURST_TRIG description to match other place in data sheet 58
- Removed duplicate error in R101[2] 59
- Changed RAMP1_INC from RAMP0 to RAMP1 59
- Clarified that the delay was in state machine cycles 59
- Fixed pin names in schematic 64

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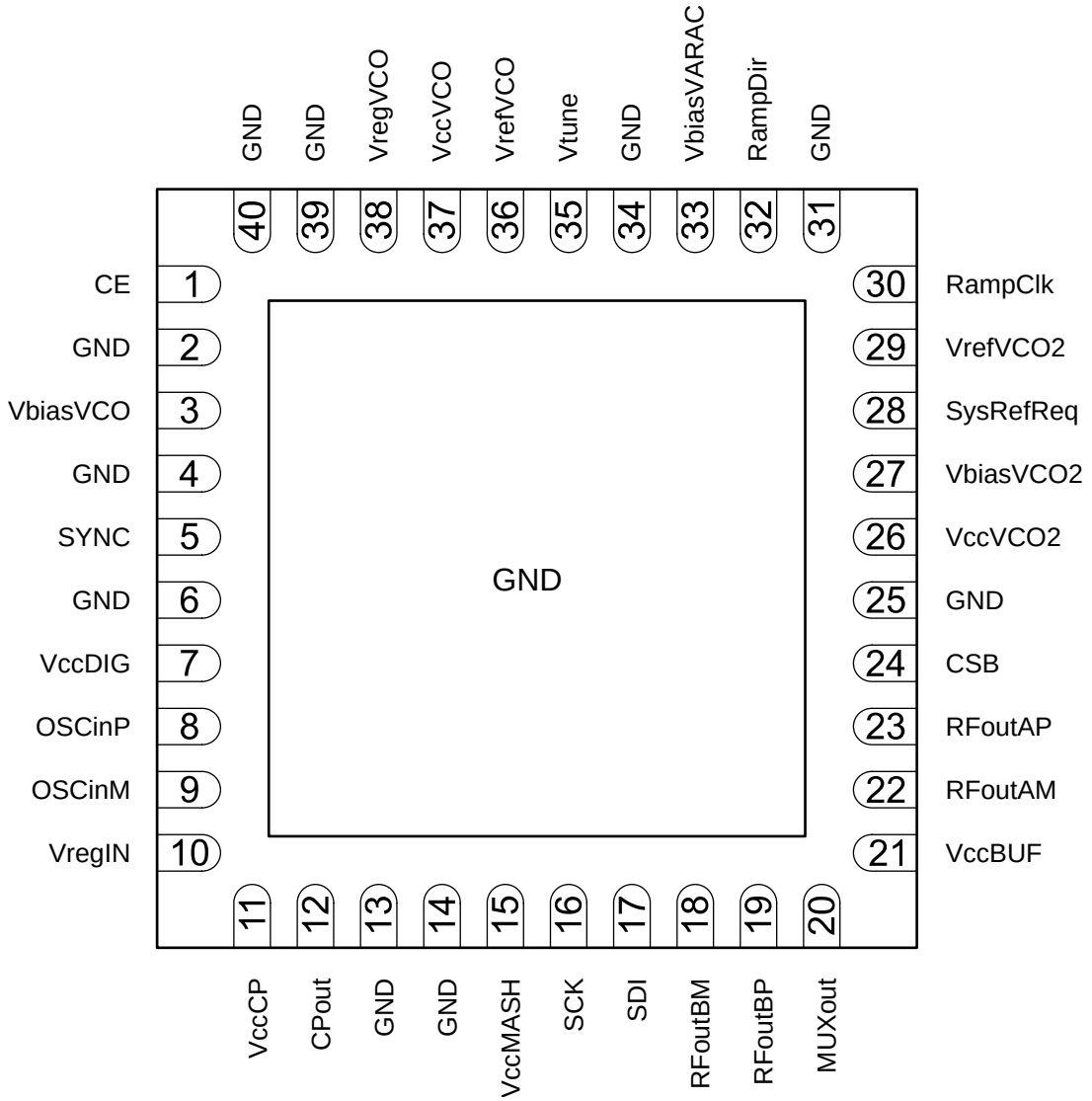
5 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



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Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CE	Input	Chip enable input. Active HIGH powers on the device.
2, 4, 25, 31, 34, 39, 40	GND	Ground	VCO ground.
3	VbiasVCO	Bypass	VCO bias. Requires a 10-µF capacitor connected to VCO ground. Place close to pin.
5	SYNC	Input	Phase synchronization pin. Has programmable threshold.
6, 14	GND	Ground	Digital ground.
7	VccDIG	Supply	Digital supply. TI recommends bypassing with decoupling capacitor to digital ground.
8	OSCinP	Input	Reference input clock (+). High-impedance self-biasing pin. Requires AC-coupling capacitor. (0.1 µF recommended)
9	OSCinM	Input	Reference input clock (–). High impedance self-biasing pin. Requires AC-coupling capacitor. (0.1 µF recommended)
10	VregIN	Bypass	Input reference path regulator output. Requires a 1-µF capacitor connected to ground. Place close to pin.
11	VccCP	Supply	Charge pump supply. TI recommends bypassing with decoupling capacitor to charge pump ground.
12	CPout	Output	Charge pump output. TI recommends connecting C1 of loop filter close to pin.
13	GND	Ground	Charge pump ground.
15	VccMASH	Supply	Digital supply. TI recommends bypassing with decoupling capacitor to digital ground.
16	SCK	Input	SPI clock. High impedance CMOS input. 1.8-V to 3.3-V logic.
17	SDI	Input	SPI data. High impedance CMOS input. 1.8-V to 3.3-V logic.
18	RFoutBM	Output	Differential output B (–). Requires a pullup (typically 50-Ω resistor) connected to Vcc as close to the pin as possible. Can be used as an output signal or SYSREF output.
19	RFoutBP	Output	Differential output B (+). Requires a pullup (typically 50-Ω resistor) connected to Vcc as close to the pin as possible. Can be used as an output signal or SYSREF output.
20	MUXout	Output	Multiplexed output pin — lock detect, readback, diagnostics, ramp status.
21	VccBUF	Supply	Output buffer supply. TI recommends bypassing with decoupling capacitor to RFout ground.
22	RFoutAM	Output	Differential output A (–). Requires connecting a 50-Ω resistor pullup to Vcc as close to the pin as possible.
23	RFoutAP	Output	Differential output A (+). Requires connecting a 50-Ω resistor pullup to Vcc as close to the pin as possible.
24	CSB	Input	SPI latch. *Chip Select Bar*. High-impedance CMOS input. 1.8-V to 3.3-V logic.
26	VccVCO2	Supply	VCO supply. TI recommends bypassing with decoupling capacitor to VCO ground.
27	VbiasVCO2	Bypass	VCO bias. Requires a 1-µF capacitor connected to VCO ground.
28	SysRefReq	Input	SYSREF request input for JESD204B support.
29	VrefVCO2	Bypass	VCO supply reference. Requires a 10-µF capacitor connected to VCO ground.
30	RampClk	Input	Input pin for ramping mode that can be used to clock the ramp in manual ramping mode or as a trigger input.
32	RampDir	Input	Input pin for ramping mode that can be used to change ramp direction in manual ramping mode or as a trigger input.
33	VbiasVARAC	Bypass	VCO Varactor bias. Requires a 10-µF capacitor connected to VCO ground.
35	Vtune	Input	VCO tuning voltage input.
36	VrefVCO	Bypass	VCO supply reference. Requires a 10-µF capacitor connected to VCO ground.
37	VccVCO	Supply	VCO supply. Recommend bypassing with decoupling capacitor to ground.
38	VregVCO	Bypass	VCO regulator node. Requires a 1-µF capacitor connected to ground.
DAP	GND	Ground	Die Attached Pad. Used for RFout ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	–0.3	3.6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions. Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions. Pins listed as ±YYY V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	3.15	3.3	3.45	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction temperature			125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMX2595 RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance [2]	15.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) DAP

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6.5 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage			3.15	3.3	3.45	V
I_{CC}	Supply current	OUTA_PD = 0, OUTB_PD = 1 OUTA_MUX = OUTB_MUX = 1 OUTA_PWR = 31, CPG=7 f_{OSC}= f_{PD} = 100 MHz, f_{VCO} = f_{OUT} = 14 GHz p_{OUT} = 3 dBm with 50-Ω resistor pullup			340		mA
	Power-on reset current	RESET=1			170		
	Power-down current	POWERDOWN=1			5		
OUTPUT CHARACTERISTICS							
p_{OUT}	Single-ended output power(1)(2)	50-Ω resistor pullup OUTx_PWR = 50	f_{OUT} = 8 GHz		5		dBm
			f_{OUT} = 15 GHz		2		
		1-nH inductor pullup OUTx_PWR = 50	f_{OUT} = 8 GHz		10		
			f_{OUT} = 15 GHz		7		
P_{OUT}	Single-ended output power with doubler enabled(3)	50-Ω resistor pullup OUTx_PWR = 20 VCO2X_EN = 1 DBLR_IBIAS_CTRL1 = 1572	f_{OUT}= 15 GHz		0		dBm
			f_{OUT}= 19 GHz		–4		
		1-nH inductor pullup OUTx_PWR = 20 VCO2X_EN = 1 DBLR_IBIAS_CTRL1 = 1572	f_{OUT}= 15 GHz		6		
			f_{OUT}= 19 GHz		–1		
f_{VCO2X}	VCO doubler output range	VCO doubler enabled	DBLR_IBIAS_CTRL1 = 1572	15		19	GHz
			DBLR_IBIAS_CTRL1 = 3115	15		20	GHz
L_{VCO2X}	VCO doubler noise floor(3)	50-Ω resistor pullup OUTx_PWR = 20 DBLR_IBIAS_CTRL1 = 1572	f_{OUT}= 18 GHz		–148		dBc/Hz
Xtalk	Isolation between outputs A and B. Measured on output A	OUTA_MUX = VCO OUTB_MUX = channel divider			–50		dBc
H1/2	1/2 haromnic spur(3)	OUTA_MUX=VCO2X f_{VCO} = 9 GHz DBLR_IBIAS_CTRL1 = 1572			–10		dBc
H2	Second harmonic(2)	OUTA_MUX = VCO f_{VCO} = 8 GHz			–20		dBc
		OUTA_MUX = VCO f_{VCO} = 11 GHz			–30		
H3	Third harmonic(2)	OUTA_MUX = VCO f_{VCO} = 8 GHz			–50		dBc
INPUT SIGNAL PATH							
f_{OSCin}	Reference input frequency	OSC_2X = 0		5		1400	MHz
		OSC_2X = 1		5		200	
v_{OSCin}	Reference input voltage	AC-coupled required (4)		0.2		2	Vpp

(1) Single ended output power obtained after de-embedding microstrip trace losses and matching with a manual tuner. Unused port terminated to 50 ohm load.
(2) Output power, spurs, and harmonics can vary based on board layout and components.
(3) 1/2 harmonic, output power and noise floor with doubler enabled are specified in EC table with DBLR_IBIAS_CTRL1 = 1572. However, these specs can be improved by setting DBLR_IBIAS_CTRL1 = 3115. See Performance Comparison Between 1572 (0x0624) and 3115 (0x0C2B) for Register DBLR_IBIAS_CTRL1 (R25[15:0]) for more information.
(4) For lower VCO frequencies, the N divider minimum value can limit the phase-detector frequency.

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Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{MULT}	Multiplier frequency (only applies when multiplier is enabled)	Input range		30		70	MHz
		Output range		180		250	
PHASE DETECTOR AND CHARGE PUMP							
f_{PD}	Phase detector frequency(4)	Integer mode	MASH_ORDER = 0	0.125		400	MHz
		Fractional mode	MASH_ORDER= 1, 2, 3	5		300	
			MASH_ORDER = 4	5		240	
I_{CPout}	Charge-pump leakage current	CPG = 0			15		nA
	Effective charge pump current. This is the sum of the up and down currents	CPG = 4			3		mA
		CPG = 1			6		
		CPG = 5			9		
		CPG = 3			12		
		CPG = 7			15		
$PN_{PLL_1/f}$	Normalized PLL 1/f noise	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(5)(5)(5)(5)			–129		dBc/Hz
PN_{PLL_flat}	Normalized PLL noise floor				–236		dBc/Hz

(5) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20 × log(Fvco/Fpd) + 10 × log(Fpd / 1Hz). PLL_flicker (offset) = PLL_flicker_Norm + 20 × log(Fvco / 1GHz) – 10 × log(offset / 10kHz). Once these two components are found, the total PLL noise can be calculated as PLL_Noise = 10 × log($10^{PLL_Flat / 10} + 10^{PLL_flicker / 10}$)

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Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VCO CHARACTERISTICS							
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8 GHz	10 kHz		–80		dBc/Hz
			100 kHz		–107		
			1 MHz		–128		
			10 MHz		–148		
			90 MHz		–157		
		VCO2 f_{VCO} = 9.2 GHz	10 kHz		–79		
			100 kHz		–105		
			1 MHz		–127		
			10 MHz		–147		
			90 MHz		–157		
		VCO3 f_{VCO} = 10.3 GHz	10 kHz		–77		
			100 kHz		–104		
			1 MHz		–126		
			10 MHz		–147		
			90 MHz		–157		
		VCO4 f_{VCO} = 11.3 GHz	10 kHz		–76		
			100 kHz		–103		
			1 MHz		–125		
			10 MHz		–145		
			90 MHz		–158		
		VCO5 f_{VCO} = 12.5 GHz	10 kHz		–74		
			100 kHz		–100		
			1 MHz		–123		
			10 MHz		–144		
			90 MHz		–157		
		VCO6 f_{VCO} = 13.3 GHz	10 kHz		–73		
			100 kHz		–100		
			1 MHz		–122		
			10 MHz		–143		
			90 MHz		–155		
		VCO7 f_{VCO} = 14.5 GHz	10 kHz		–73		
			100 kHz		–99		
			1 MHz		–121		
			10 MHz		–143		
			90 MHz		–152		
t_{VCOCAL}	VCO calibration speed	Switch across the entire frequency band f_{OSC} = 200 MHz, f_{PD} = 100 MHz (6)	No assist		50		µs
			Partial assist		35		
			Close frequency		20		
			Full assist		5		

(6) See *Application and Implementation* for more details on the different VCO calibration modes.

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Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
K_{VCO}	VCO gain	8 GHz			92		MHz/V
		9.2 GHz			91		
		10.3 GHz			115		
		11.3 GHz			121		
		12.5 GHz			195		
		13.3 GHz			190		
		14.5 GHz			213		
$\lvert\Delta T_{CL}\rvert$	Allowable temperature drift when VCO is not recalibrated	RAMP_EN = 0 or RAMP_MANUAL= 1			125		°C
H2	VCO second harmonic	f_{VCO} = 8 GHz, divider disabled			–20		dBc
H3	VCO third haromonic	f_{VCO} = 8 GHz, divider disabled			–50		
SYNC PIN AND PHASE ALIGNMENT							
f_{OSCin}SYNC	Maximum usable OSCin with sync pin (Figure 33)	Category 3		0		100	MHz
		Categories1 and 2		0		1400	
DIGITAL INTERFACE **Applies to SLK, SDI, CSB, CE, RampDir, RampClk, MUXout, SYNC (CMOS Mode), SysRefReq (CMOS Mode)**							
V_{IH}	High-level input voltage			1.4		Vcc	V
V_{IL}	Low-level input voltage			0		0.4	V
I_{IH}	High-level input current			–25		25	µA
I_{IL}	Low-level input current			–25		25	µA
V_{OH}	High-level output voltage	MUXout pin	Load current = –10 mA	V_{CC} – 0.4			V
V_{OL}	Low-level output voltage		Load current = 10 mA			0.4	V

6.6 Timing Requirements

(3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C, except as specified. Nominal values are at V_{CC} = 3.3 V, T_A = 25°C)

			MIN	NOM	MAX	UNIT
SYNC, SYSRefReq, RampClk, and RampDIR Pins						
t_{SETUP}	Setup time for pin relative to OSCin rising edge	SYNC pin	2.5			ns
		SysRefReq pin	2.5			
t_{HOLD}	Hold time for SYNC pin relative to OSCin rising edge	SYNC pin	2			ns
		SysRefReq pin	2			
DIGITAL INTERFACE WRITE SPECIFICATIONS						
f_{SPI}Write	SPI write speed	t_{CWL} + t_{CWH} > 13.333 ns			75	MHz
t_{CE}	Clock to enable low time	See Figure 1	5			ns
t_{DCS}	Data to clock setup time		2			ns
t_{CDH}	Clock to data hold time		2			ns
t_{CWH}	Clock pulse width high		5			ns
t_{CWL}	Clock pulse width low		5			ns
t_{ECS}	Enable to clock setup time		5			ns
t_{EWH}	Enable pulse width high		2			ns

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Timing Requirements (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ +85°C, except as specified. Nominal values are at V_{CC} = 3.3 V, T_A = 25°C)

			MIN	NOM	MAX	UNIT
DIGITAL INTERFACE READBACK SPECIFICATIONS						
f_{SPI}Readback	SPI readback speed	See Figure 2			50	MHz
t_{CE}	Clock to enable low time		10			ns
t_{DCS}	Data to clock setup time		2			ns
t_{CDH}	Clock to data hold time		2			ns
t_{CR}	Clock falling edge to available readback data wait time.		0		10	ns
t_{CWH}	Clock pulse width high		10			ns
t_{CWL}	Clock pulse width low		10			ns
t_{ECS}	Enable to clock setup time		10			ns
t_{EWH}	Enable pulse width high		10			ns

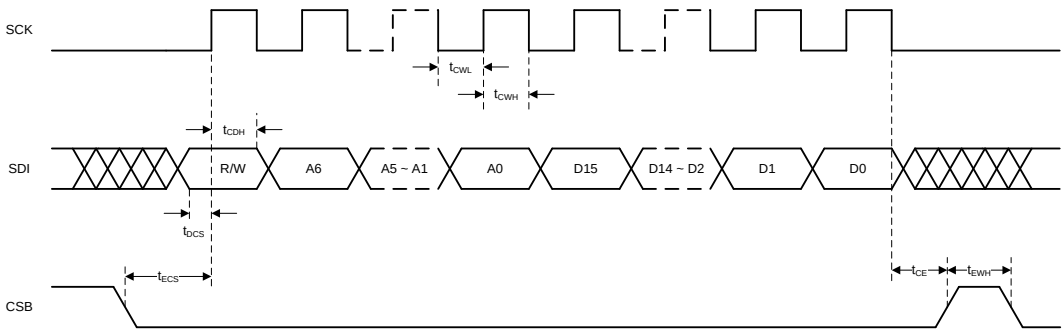

Figure 1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CSB must be held low for data to be clocked. Device will ignore clock pulses if CSB is held high.
- When SCK and SDI lines are shared between devices, TI recommends to hold the CSB line high on the device that is not to be clocked.
- Note that t_{CE} is only a valid spec if CPOL (Clock Polarity) = 0 and CPHA (Clock Phase) = 0 is used for SPI protocol. For SPI mode (CPOL = 1 and CPHA = 1), the minimum distance required between the last rising edge of clock and the rising edge of CSB is t_{CE} + clock_period/2.

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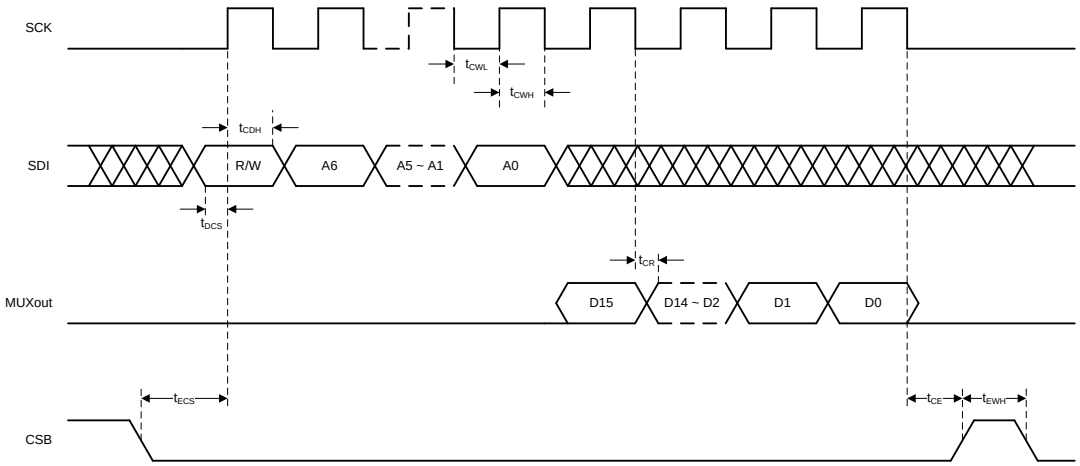

Figure 2. Serial Data Readback Timing Diagram

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXout pin will always be low for the address portion of the transaction.
- The data on MUXout is clocked out at t_{CR} after the falling edge of SCK. In other words, the readback data will be available at the MUXout pin t_{CR} after the clock falling edge.
- The data portion of the transition on the SDI line is always ignored.

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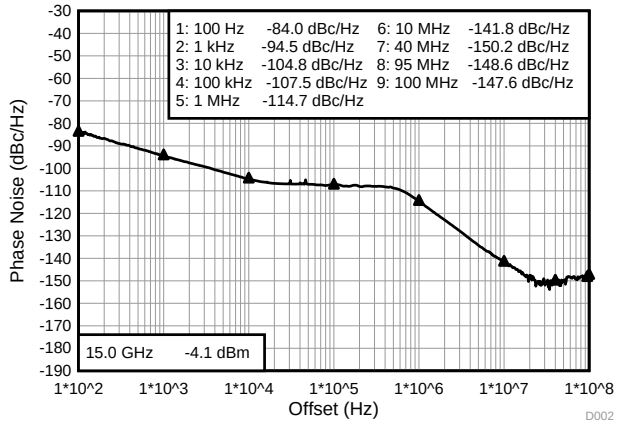
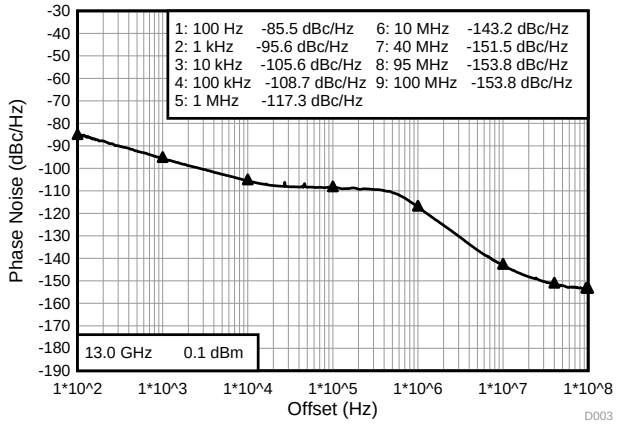
6.7 Typical Characteristics



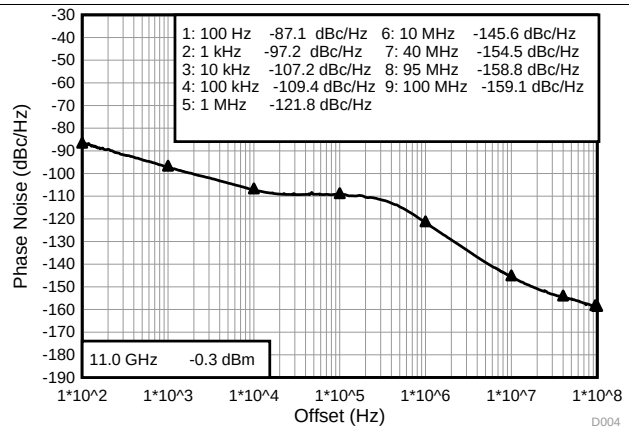
f_{OSC} = 100 MHz Jitter = 55.8 fs (100 Hz - 100 MHz)
f_{PD} = 200 MHz

Figure 3. Closed-Loop Phase Noise at 15 GHz



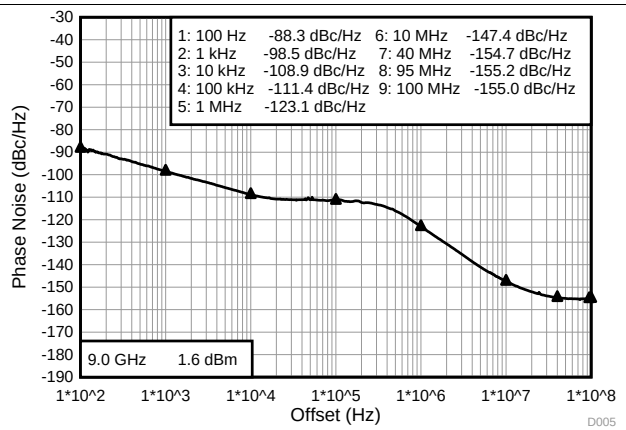
f_{OSC} = 100 MHz Jitter = 52.6 fs (100 Hz - 100 MHz)
f_{PD} = 200 MHz

Figure 4. Closed-Loop Phase Noise at 13 GHz



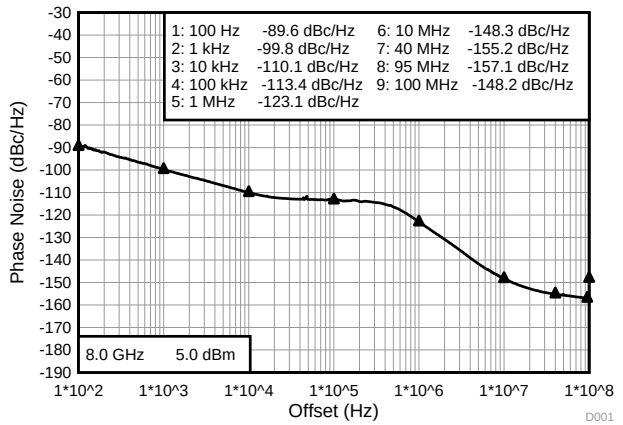
f_{OSC} = 100 MHz Jitter = 46.8 fs (100 Hz - 100 MHz)
f_{PD} = 200 MHz

Figure 5. Closed-Loop Phase Noise at 11 GHz



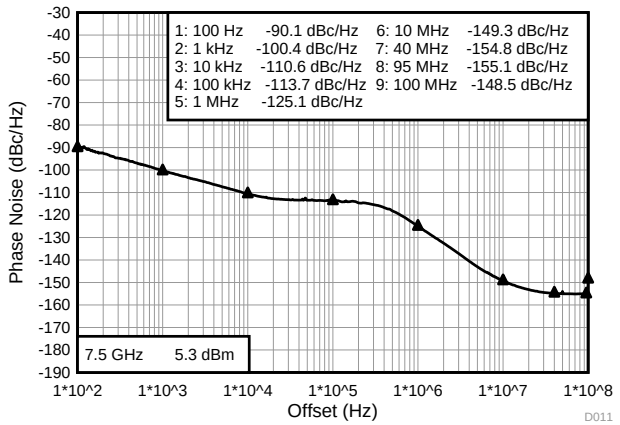
f_{OSC} = 100 MHz Jitter = 46.9 fs (100 Hz - 100 MHz)
f_{PD} = 200 MHz

Figure 6. Closed-Loop Phase Noise at 9 GHz



f_{OSC} = 100 MHz Jitter = 46.87 fs (100 Hz - 100 MHz)
f_{PD} = 200 MHz

Figure 7. Closed-Loop Phase Noise at 8 GHz



f_{OSC} = 100 MHz Jitter = 44.1 fs (100 Hz - 100 MHz)
f_{PD} = 200 MHz

Figure 8. Closed-Loop Phase Noise at 7.5 GHz

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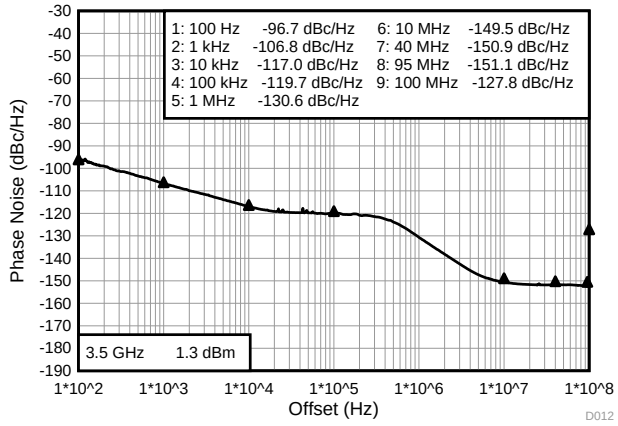
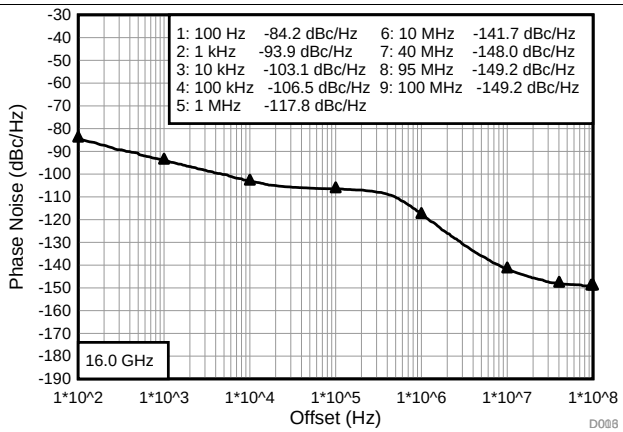
Typical Characteristics (continued)



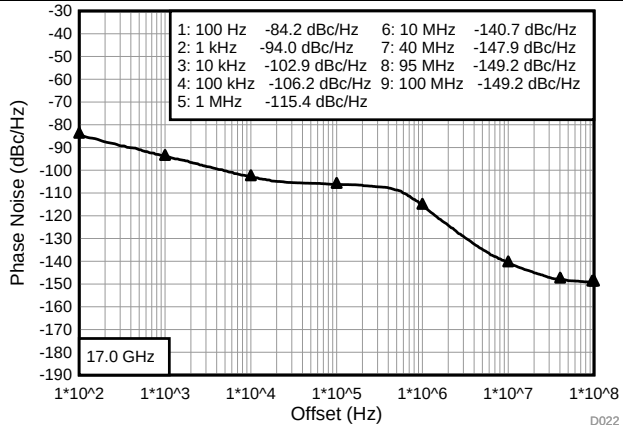
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{VCO} = 14 GHz
f_{OUT} = 14 GHz / 4 = 3.5 GHz
Jitter = 49.4 fs (100 Hz - 100 MHz)

Figure 9. Closed-Loop Phase Noise at 3.5 GHz



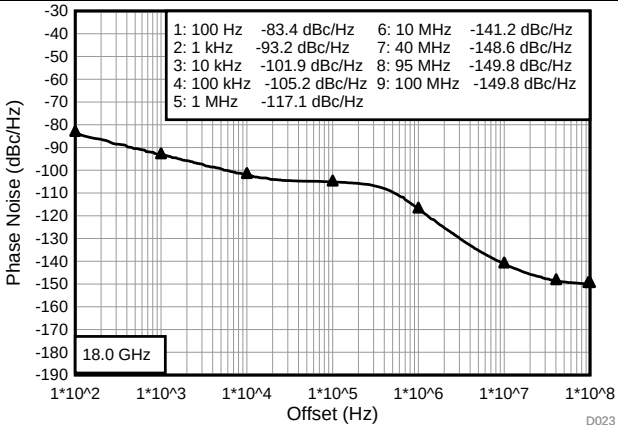
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{OUT} = 2 × 8 GHz = 16 GHz
Jitter = 52.9 fs (100 Hz - 100 MHz)

Figure 10. Closed-Loop Phase Noise at 16 GHz



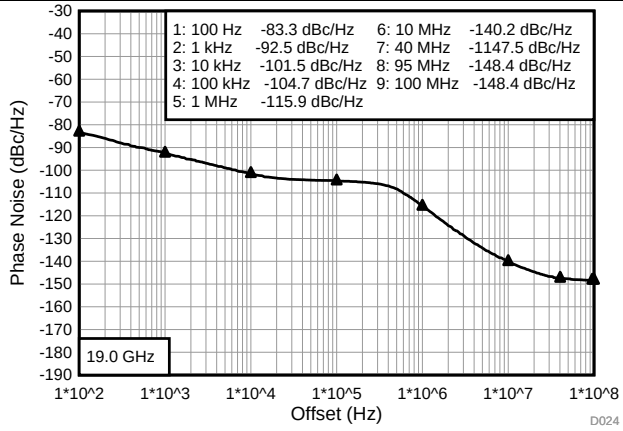
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{OUT} = 2 × 8.5 GHz = 17 GHz
Jitter = 55.0 fs (100 Hz - 100 MHz)

Figure 11. Closed-Loop Phase Noise at 17 GHz



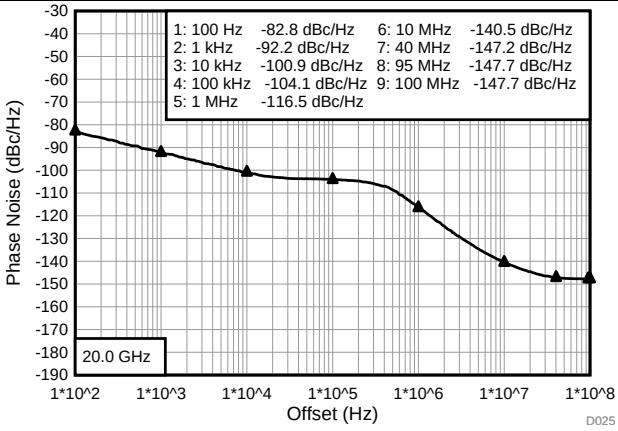
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{OUT} = 2 × 9 GHz = 18 GHz
Jitter = 52.6 fs (100 Hz - 100 MHz)

Figure 12. Closed-Loop Phase Noise at 18 GHz



f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{OUT} = 2 × 9.5 GHz = 19 GHz
Jitter = 54.7 fs (100 Hz - 100 MHz)

Figure 13. Closed-Loop Phase Noise at 19 GHz



f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{OUT} = 2 × 10 GHz = 20 GHz
Jitter = 52.7 fs (100 Hz - 100 MHz)

Figure 14. Closed-Loop Phase Noise at 20 GHz

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Typical Characteristics (continued)

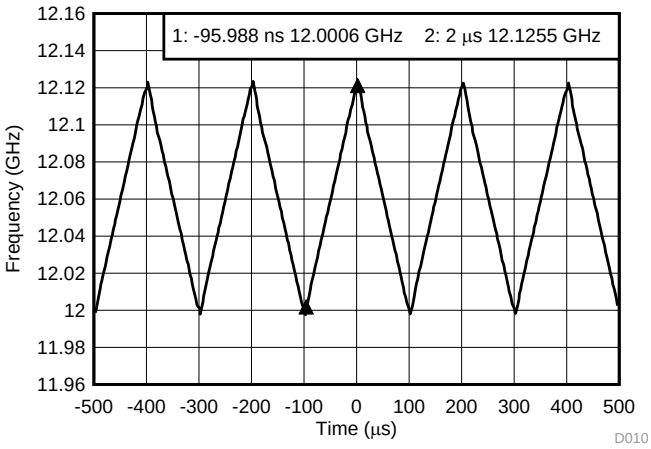
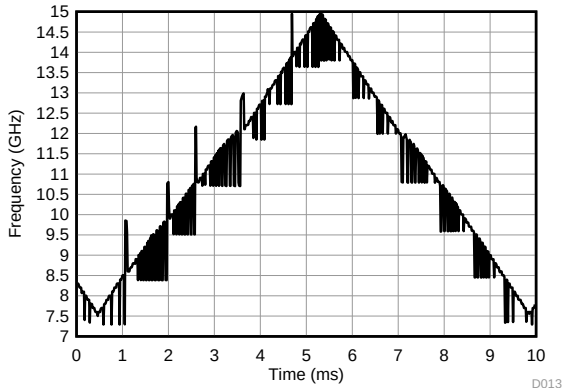
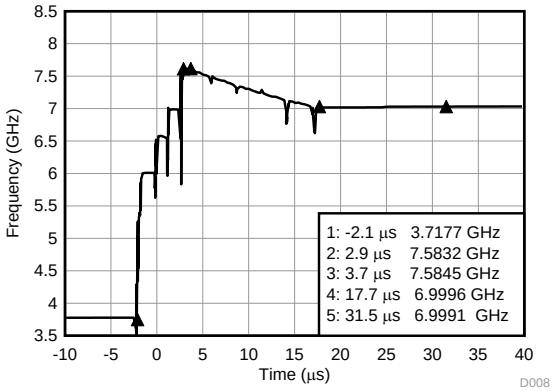


Figure 15. VCO Ramping 12-GHz to 12.125-GHz Calibration Free



The glitches in the plot are due to the inability of the measurement equipment to track the VCO while calibrating.

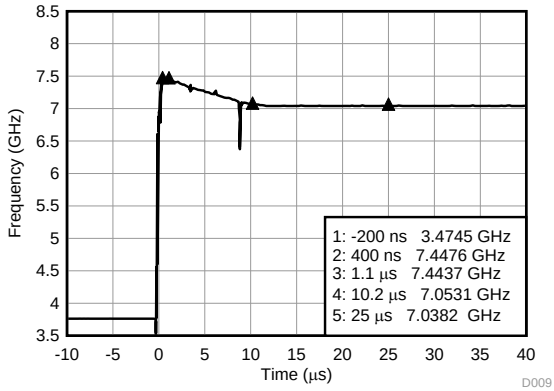
Figure 16. VCO Ramping 7.5-GHz to 15-GHz Triangle Wave With VCO Calibration



CalTime = 33.6 µs = 5.8 µs (Core) + 14 µs (Fcal) + 13.8 µs (Ampcal)

f_{OSC} = 200 MHz, f_{PD} = 100 MHz, f_{VCO} = 7.5 - 14 GHz, CHDIV = 2

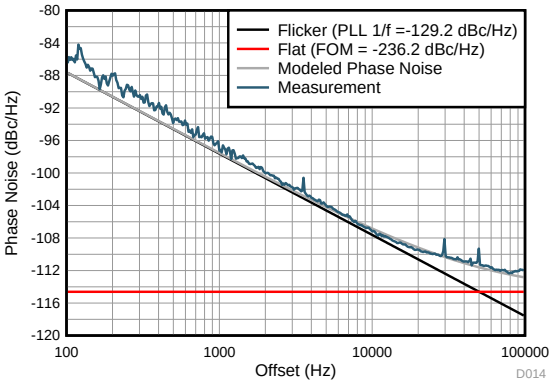
Figure 17. VCO Unassisted Calibration



CalTime = 25.2 µs = 1.3 µs (Core) + 9.1 µs (Fcal) +14.8 µs (Ampcal)

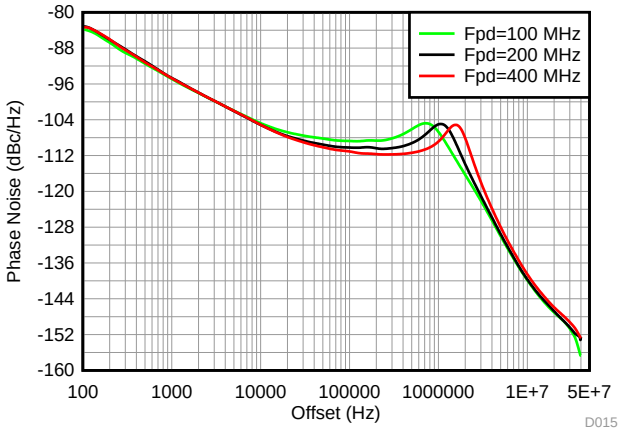
f_{OSC} = 200 MHz, f_{PD} = 100 MHz, f_{VCO} = 7.5 GHz - 14 GHz, CHDIV = 2

Figure 18. VCO Calibration With Partial Assist



f_{VCO} = 12 GHz f_{PD} = 100 MHz

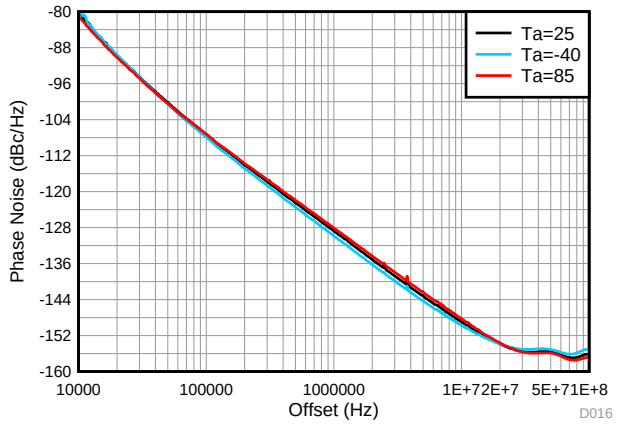
Figure 19. Calculation of PLL Noise Metrics



f_{OSC} = 200 MHz f_{VCO} = 14.8 GHz

Figure 20. PLL Phase Noise Variation vs. f_{PD}

Typical Characteristics (continued)



f_{VCO} = 8 GHz, Narrow Loop Bandwidth (<100 Hz)

Figure 21. VCO Phase Noise Over Temperature

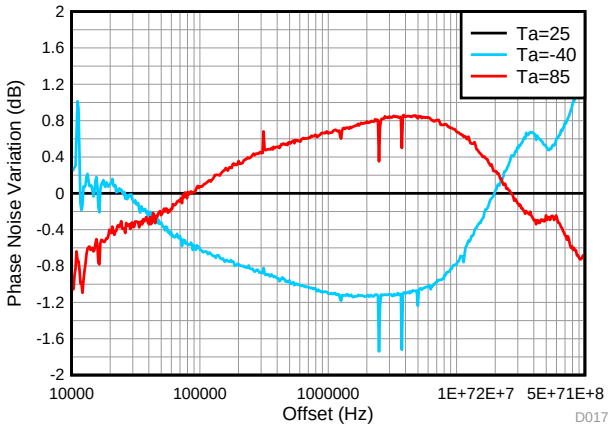
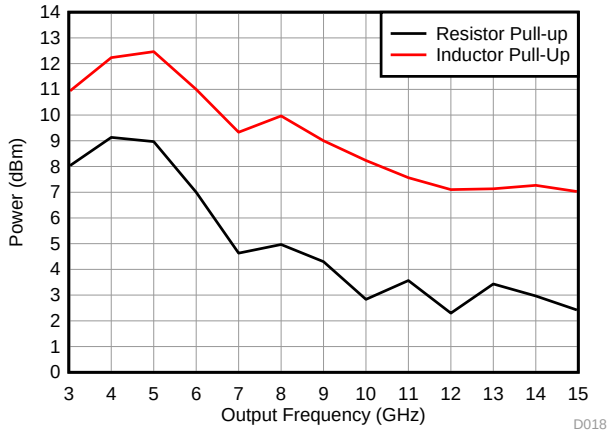
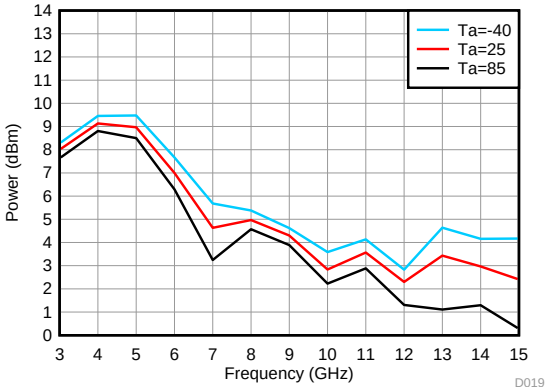


Figure 22. CHANGE in 8-GHz VCO Phase Noise Over Temperature



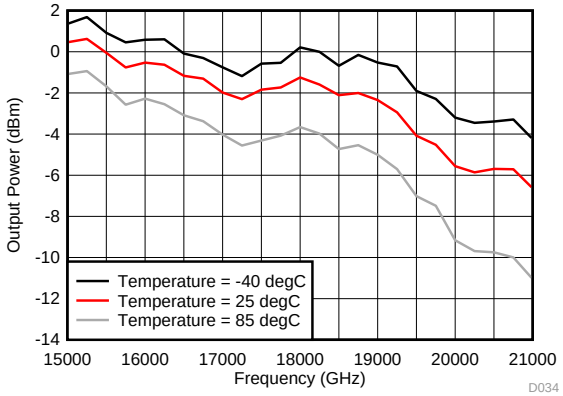
Single-Ended Output OUTx_PWR = 50
VCO2X_EN = 0

Figure 23. Output Power Across Frequency



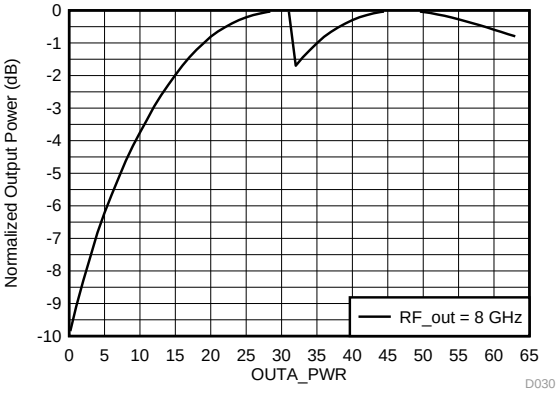
Single-ended output with resistor pullup and OUTx_PWR = 50. Note that Near 13.3 to 14.3 GHz, output power can be impacted at hot temperature. See the *Application Information* section for more information.

Figure 24. Output Power vs Temperature Without Doubler



Single-ended output with resistor pullup. OUTA_PWR = 20
DBLR_IBIAS_CTRL1 = 3115

Figure 25. Output Power vs. Temperature With Doubler



Resistor pullup Normalized to maximum output power.

Figure 26. Output Power Normalized To Maximum Across OUTA_PWR With Resistor Pullup

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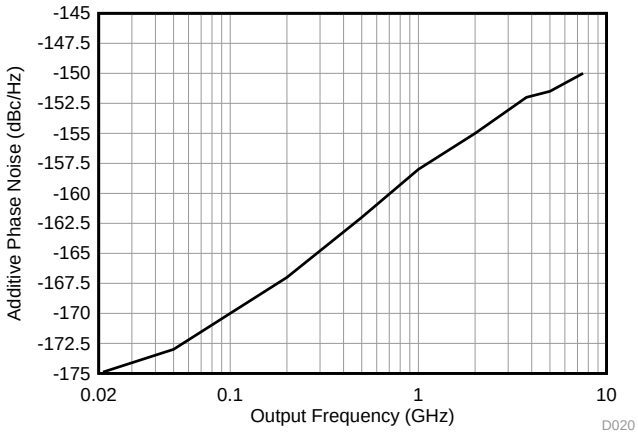
Typical Characteristics (continued)



This noise adds to the scaled VCO Noise when the channel divider is used.

Figure 27. Additive VCO Divider Noise Floor

7 Detailed Description

7.1 Overview

The LMX2595 is a high-performance, wideband frequency synthesizer with integrated VCO and output divider. The VCO operates from 7.5 GHz to 15 GHz, and this can be combined with the output divider to produce any frequency in the range of 10 MHz to 15 GHz. The LMX2595 also features a VCO doubler that can be used to produce frequencies up to 20 GHz. Within the input path, there are two dividers and a multiplier for flexible frequency planning. The multiplier also allows the reduction of spurs by moving the frequencies away from the integer boundary.

The PLL is fractional-N PLL with a programmable delta-sigma modulator up to 4th order. The fractional denominator is a programmable 32-bit long, which can easily provide fine frequency steps below 1-Hz resolution, or be used to do exact fractions like 1/3, 7/1000, and many others. The phase frequency detector goes up to 300 MHz in fractional mode or 400 MHz in integer mode, although minimum N-divider values must also be taken into account.

For applications where deterministic or adjustable phase is desired, the SYNC pin can be used to get the phase relationship between the OSCin and RFout pins deterministic. When this is done, the phase can be adjusted in very fine steps of the VCO period divided by the fractional denominator.

The ultra-fast VCO calibration is designed for applications where the frequency must be swept or abruptly changed. The frequency can be manually programmed, or the device can be set up to do ramps and chirps.

The JESD204B support includes using the RFoutB output to create a differential SYSREF output that can be either a single pulse or a series of pulses that occur at a programmable distance away from the rising edges of the output signal.

The LMX2595 device requires only a single 3.3-V power supply. The internal power supplies are provided by integrated LDOs, eliminating the need for high-performance external LDOs.

The digital logic for the SPI interface and is compatible with voltage levels from 1.8 V to 3.3 V.

Table 1 shows the range of several of the dividers, multipliers, and fractional settings.

Table 1. Range of Dividers, Multipliers, and Fractional Settings

PARAMETER	MIN	MAX	COMMENTS
Outputs enabled	0	2	
OSCin doubler	0 (1X)	1 (2X)	The low noise doubler can be used to increase the phase detector frequency to improve phase noise and avoid spurs. This is in reference to the OSC_2X bit.
Pre-R divider	1 (bypass)	128	Only use the Pre-R divider if the multiplier is used and the input frequency is too high for the multiplier.
Multiplier	3	7	This is in reference to the MULT word.
Post-R divider	1 (bypass)	255	The maximum input frequency for the Post-R divider is 250 MHz. Use the Pre-R divider if necessary.
N divider	≥ 28	524287	The minimum divide depends on modulator order and VCO frequency. See *N-Divider and Fractional Circuitry* for more details.
Fractional numerator/ denominator	1 (Integer mode)	$2^{32} – 1 = 4294967295$	The fractional denominator is programmable and can assume any value between 1 and 2^{32}–1; it is not a fixed denominator.
Fractional order (MASH_ORDER)	0	4	Order 0 is integer mode and the order can be programmed
Channel divider	1 (bypass)	768	This is the series of several dividers. Also, be aware that above 10 GHz, the maximum allowable channel divider value is 6.
Output frequency	10 MHz	20 GHz	This is implied by the VCO frequency, channel divider, and VCO doubler.

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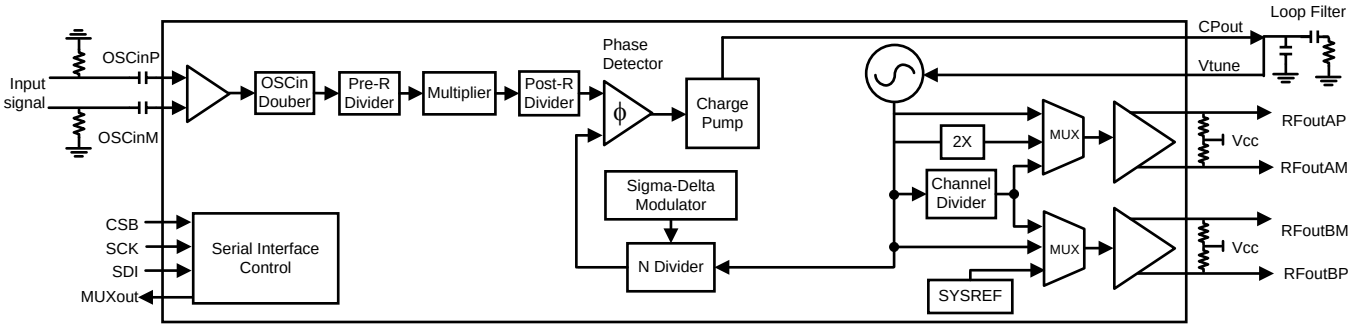
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference Oscillator Input

The OSCin pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling caps at the pin. A CMOS clock or XO can drive the single-ended OSCin pins. Differential clock input is also supported, making it easier to interface with high-performance system clock devices such as TI's LMK series clock devices. As the OSCin signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCin pin at the time of programming FCAL_EN.

7.3.2 Reference Path

The reference path consists of an OSCin doubler (OSC_2X), Pre-R divider, multiplier (MULT) and a Post-R divider.

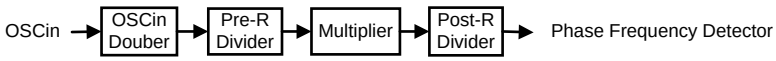


Figure 28. Reference Path Diagram

The OSCin doubler (OSC_2X) can double up low OSCin frequencies. Pre-R (PLL_R_PRE) and Post-R (PLL_R) dividers both divide frequency down while the multiplier (MULT) multiplies frequency up. The purposes of adding a multiplier is to reduce integer boundary spurs or to increase the phase detector frequency. Use Equation 1 to calculate the phase detector frequency, f_{PD}:

$$f_{PD} = f_{OSC} \times OSC_2X \times MULT / (PLL_R_PRE \times PLL_R) \quad (1)$$

- In the OSCin doubler or input multiplier is used, the OSCin signal should have a 50% duty cycle as both the rising and falling edges are used.
- If neither the OSCin doubler nor the input multiplier are used, only rising edges of the OSCin signal are used and duty cycle is not critical.
- The input multiplier and OSCin doubler should not both be used at the same time.

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Feature Description (continued)

7.3.2.1 OSCin Doubler (OSC_2X)

The OSCin doubler allows one to double the input reference frequency up to 400 MHz. This doubler adds minimal noise and is useful for raising the phase detector frequency for better phase noise and also to avoid spurs. When the phase-detector frequency is increased, the flat portion of the PLL phase noise improves.

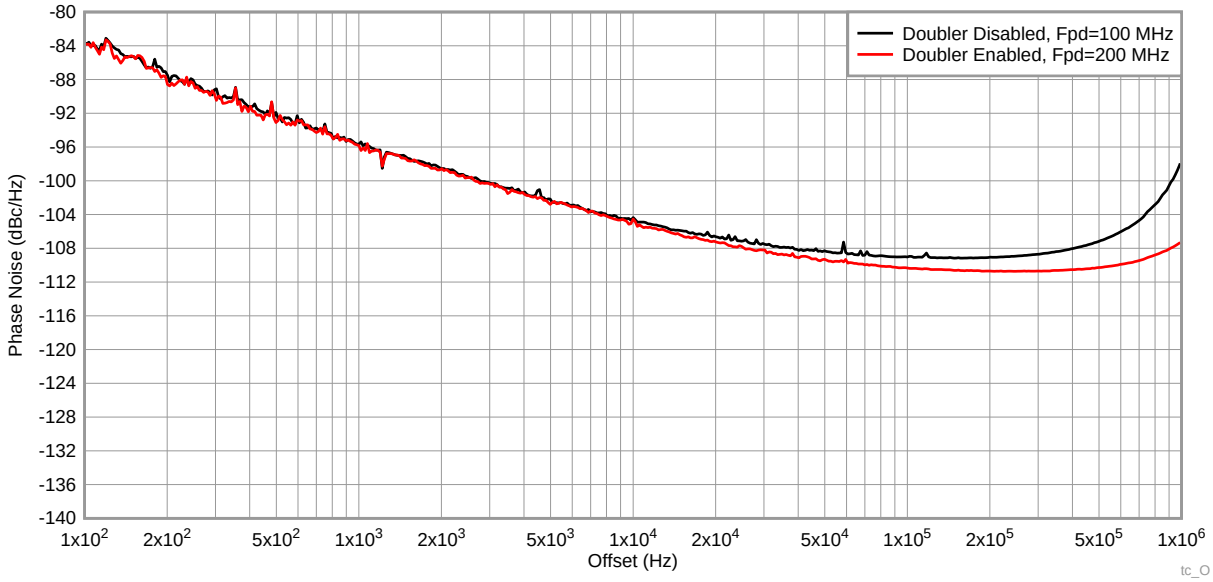

Figure 29. Benefit of Using the OSC_2X Doubler at 14 GHz

7.3.2.2 Pre-R Divider (PLL_R_PRE)

The Pre-R divider is useful for reducing the input frequency so that the programmable multiplier (MULT) can be used to help meet the maximum 250-MHz input frequency limitation to the PLL-R divider. Otherwise, it does not have to be used.

7.3.2.3 Programmable Multiplier (MULT)

The MULT is useful for shifting the phase-detector frequency to avoid integer boundary spurs. The multiplier allows a multiplication of 3, 4, 5, 6, or 7. Be aware that unlike the doubler, the programmable multiplier degrades the PLL figure of merit. This only would matter, however, for a clean reference and if the loop bandwidth was wide.

7.3.2.4 Post-R Divider (PLL_R)

The Post-R divider can be used to further divide down the frequency to the phase detector frequency. When it is used (PLL_R > 1), the input frequency to this divider is limited to 250 MHz.

7.3.2.5 State Machine Clock

The state machine clock is a divided down version of the OSCin signal that is used internally in the device. This divide value is 1, 2, 4, or 8, and is determined by CAL_CLK_DIV programming word (described in the *Programming* section). This state machine clock impacts various features like the lock detect delay, VCO calibration, and ramping. The state machine clock is calculated as $f_{smclk} = f_{OSC} / 2^{CAL_CLK_DIV}$.

7.3.3 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-R divider and N-divider, and generates a correction current corresponding to the phase error until the two signals are aligned in-phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed-loop bandwidth of the PLL. See the *Application Information* section for more information.

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Feature Description (continued)

7.3.4 N-Divider and Fractional Circuitry

The N-divider includes fractional compensation and can achieve any fractional denominator from 1 to (2^{32} – 1). The integer portion of N is the whole part of the N-divider value, and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. In general, the total N-divider value is determined by N + NUM / DEN. The N, NUM and DEN are software programmable. The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200 MHz, the output can increment in steps of 200 MHz / (2^{32} – 1) = 0.047 Hz. Equation 2 shows the relationship between the phase detector and VCO frequencies. Note that in SYNC mode, there is an extra divider that is not shown in Equation 2.

$$f_{VCO} = f_{pd} \times \left(N + \frac{NUM}{DEN}\right) \tag{2}$$

The sigma-delta modulator that controls this fractional division is also programmable from integer mode to fourth order. To make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

The N-divider has minimum value restrictions based on the modulator order and VCO frequency. Furthermore, the PFD_DLY_SEL bit must be programmed in accordance to the Table 2.

Table 2. Minimum N-Divider Restrictions

MASH_ORDER	f_{VCO} (MHz)	MINIMUM N	PFD_DLY_SEL
0	≤ 12500	28	1
	> 12500	32	2
1	≤ 10000	28	1
	10000-12500	32	2
	>12250	36	3
2	≤ 10000	32	2
	>10000	36	3
3	≤ 10000	36	3
	>10000	40	4
4	≤ 10000	44	5
	>10000	48	6

7.3.5 MUXout Pin

The MUXout pin can be used to readback programmable states of the device or for lock detect.

Table 3. MUXout Pin Configurations

MUXOUT_SEL	FUNCTION
0	Readback
1	Lock Detect

7.3.5.1 Lock Detect

The MUXout pin can be configured for lock detect done in by reading back the rb_LD_VTUNE field or using the pin as shown in the Table 4.

Table 4. Configuring the MUXout Pin for Lock Detect

FIELD	PROGRAMMING	DESCRIPTION
LD_TYPE	0 = VCO Calibration Status 1 = Indirect Vtune	Select Lock Detect Type.
LD_DLY	0 to 65535	Only valid for Vtune lock detect. This is a delay in state machine cycles.
OUT_MUTE	0 = Disabled 1 = Enabled	Turns off outputs when lock detect is low.

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VCO calibration status lock detect works by indicating a low signal on the MUXout pin whenever the VCO is calibrating or the LD_DLY counter is running. The delay from the LD_DLY is added to the true VCO calibration time (t_{VCOCAL}), so it can be used to account for the analog lock time of the PLL.

Indirect Vtune lock detect is based on internally generated voltage that is related to (but not the same as) the Vtune voltage of the charge pump. It indicates a high signal on MUXout pin or reads back state 2 of rb_LD_VTUNE when the device is locked.

7.3.5.2 Readback

The MUXout pin can be configured to read back useful information from the device. Common uses for readback are:

1. Read back registers to ensure that they have been programmed to the correct value.
2. Read back the lock detect status to determine if the PLL is in lock.
3. Read back VCO calibration information so that it can be used to improve the lock time.
4. Read back information to help troubleshoot.

7.3.6 VCO (Voltage-Controlled Oscillator)

The LMX2595 includes a fully integrated VCO. The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies is shown in Equation 3:

$$f_{VCO} = f_{PD} \times \text{N divider} \tag{3}$$

7.3.6.1 VCO Calibration

To reduce the VCO tuning gain and therefore improve the VCO phase-noise performance, the VCO frequency range is divided into several different frequency bands. The entire range, 7.5 to 15 GHz, covers an octave that allows the divider to take care of frequencies below the lower bound. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. It is important that a valid OSCin signal must present before VCO calibration begins.

The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed.

The optimum internal settings for this are temperature dependent. If the temperature is allowed to drift too much without being recalibrated, some minor phase noise degradation could result. The maximum allowable drift for continuous lock, ΔT_{CL}, is stated in the electrical specifications. For this device, a number of 125°C means the device never loses lock if the device is operated under the *Recommended Operating Conditions*.

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The LMX2595 allows the user to assist the VCO calibration. In general, there are three kinds of assistance, as shown in Table 5:

Table 5. Assisting the VCO Calibration Speed

ASSISTANCE LEVEL	DESCRIPTION	PROGRAMMABLE SETTINGS
No assist	User does nothing to improve VCO calibration speed, but the user-specified VCO_SEL, VCO_DACISET_STRT and VCO_CAPCTRL_STRT values do affect the starting point of VCO calibration. For oscillation to start up properly and for VCO to calibrate correctly, TI recommends setting VCO_SEL = 7, VCO_DACISET_STRT = 300 and VCO_CAPCTRL_STRT = 183 for all frequencies except 11.9 GHz ~ 12.1 GHz. For frequencies within 11.9 ~ 12.1 GHz, user must use VCO_SEL = 4 for proper VCO calibration.	QUICK_RECAL_EN=0 VCO_SEL_FORCE=0 VCO_DACISET_FORCE=0 VCO_CAPCTRL_FORCE=0
Partial assist	Upon every frequency change, before the FCAL_EN bit is checked, the user provides the initial starting point for the VCO core (VCO_SEL), band (VCO_CAPCTRL_STRT), and amplitude (VCO_DACISET_STRT) based on Table 6.	QUICK_RECAL_EN=0 VCO_SEL_FORCE=0 VCO_DACISET_FORCE=0 VCO_CAPCTRL_FORCE=0
Close Frequency Assist	Upon initialization of the device, user enables QUICK_RECAL_EN bit. The VCO uses the current VCO_CAPCTRL and VCO_DACISET_STRT settings as the initial starting point.	QUICK_RECAL_EN=1 VCO_SEL_FORCE=0 VCO_DACISET_FORCE=0 VCO_CAPCTRL_FORCE=0
Full assist	The user forces the VCO core (VCO_SEL), amplitude settings (VCO_DACISET), and frequency band (VCO_CAPCTRL) and manually sets the value. If the two frequency points are no more than 5MHz apart and on the same VCO core, the user can set the VCO amplitude and capcode for any frequency between those two points using linear interpolation.	QUICK_RECAL_EN=0 VCO_SEL_FORCE=1 VCO_DACISET_FORCE=1 VCO_CAPCTRL_FORCE=1

To do the partial assist for the VCO calibration, follow this procedure:

1. Determine the VCO Core

   Find a VCO Core that includes the desired VCO frequency. If at the boundary of two cores, choose one based on phase noise or performance.

2. Calculate the VCO CapCode as follows:

   $$VCO_CAPCTRL_STRT = round\ (C_{CoreMin} - (C_{CoreMin} - C_{CoreMax}) \times (f_{VCO} - f_{CoreMin}) / (f_{CoreMax} - f_{CoreMin}))$$

3. Get the VCO amplitude setting from Table 6.

   $$VCO_DACISET_STRT = round\ (A_{CoreMin} + (A_{CoreMax} - A_{CoreMin}) \times (f_{VCO} - f_{CoreMin})/(f_{CoreMax} - f_{CoreMin}))$$

Table 6. VCO Core Ranges

VCO CORE	$f_{CoreMin}$	$f_{CoreMax}$	$C_{CoreMin}$	$C_{CoreMax}$	$A_{CoreMin}$	$A_{CoreMax}$
VCO1	7500	8600	164	12	299	240
VCO2	8600	9800	165	16	356	247
VCO3	9800	10800	158	19	324	224
VCO4	10800	12000	140	0	383	244
VCO5	12000	12900	183	36	205	146
VCO6	12900	13900	155	6	242	163
VCO7	13900	15000	175	19	323	244

NOTE

In the range of 11900 MHz to 12100 MHz, VCO assistance cannot be used, and the settings must be: VCO_SEL = 4, VCO_DACISET_STRT = 300, and VCO_CAPCTRL_STRT = 1. Outside this range, in the partial assist for the VCO calibration, the VCO calibration runs. This means that if the settings are incorrect, the VCO still locks with the correct settings. The only consequence is that the calibration time might be a little longer. The closer the calibration settings are to the true final settings, the faster the VCO calibration will be.

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7.3.6.2 Determining the VCO Gain

The VCO gain varies between the seven cores and is the lowest at the lowest end of the band and highest at the highest end of each band. For a more accurate estimation, use Table 7:

Table 7. VCO Gain

CORE	f1	f2	Kvco1	Kvco2
VCO1	7500	8600	73	114
VCO2	8600	9800	61	121
VCO3	9800	10800	98	132
VCO4	10800	12000	106	141
VCO5	12000	12900	170	215
VCO6	12900	13900	172	218
VCO7	13900	15000	182	239

Based on Table 7, Equation 4 can estimate the VCO gain for an arbitrary VCO frequency of f_{VCO}:

$$Kvco = Kvco1 + (Kvco2 - Kvco1) \times (f_{VCO} - f1) / (f2 - f1) \quad (4)$$

7.3.7 Channel Divider

To go below the VCO lower bound of 7.5 GHz, the channel divider can be used. The channel divider consists of four segments, and the total division value is equal to the multiplication of them. Therefore, not all values are valid.

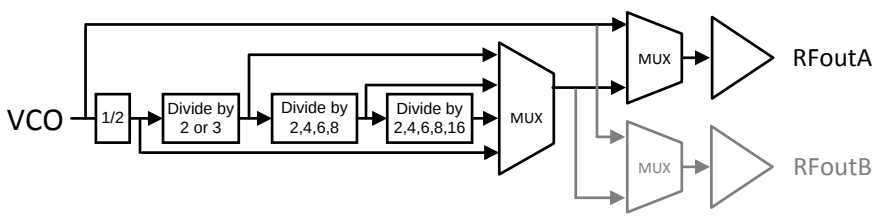

Figure 30. Channel Divider

When the channel divider is used, there are limitations on the values. Table 8 shows how these values are implemented and which segments are used.

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Table 8. Channel Divider Segments

EQUIVALENT DIVISION VALUE	FREQUENCY LIMITATION	OutMin (MHz)	OutMax (MHz)	CHDIV[4:0]	SEG0	SEG1	SEG2	SEG3
2	None	3750	7500	0	2	1	1	1
4		1875	3750	1	2	2	1	1
6		1250	2500	2	2	3	1	1
8	f_{VCO} ≤ 11.5 GHz	937.5	1437.5	3	2	2	2	1
12		625	958.333	4	2	3	2	1
16		468.75	718.75	5	2	2	4	1
24		312.5	479.167	6	2	2	6	1
32		234.375	359.375	7	2	2	8	1
48		156.25	239.583	8	2	3	8	1
64		117.1875	179.6875	9	2	2	8	2
72		104.167	159.722	10	2	3	6	2
96		78.125	119.792	11	2	3	8	2
128		58.594	89.844	12	2	2	8	4
192		39.0625	59.896	13	2	2	8	6
256		29.297	44.922	14	2	2	8	8
384		19.531	29.948	15	2	3	8	8
512		14.648	22.461	16	2	2	8	16
768		9.766	14.974	17	2	3	8	16
Invalid	n/a	n/a	n/a	18-31	n/a	n/a	n/a	n/a

The channel divider is powered up whenever an output (OUTx_MUX) is selected to the channel divider or SysRef, regardless of whether it is powered down or not. When an output is not used, TI recommends selecting the VCO output to ensure that the channel divider is not unnecessarily powered up.

Table 9. Channel Divider

OUTA MUX	OUTB MUX	CHANNEL DIVIDER
Channel Divider	X	Powered up
X	Channel Divider or SYSREF	Powered up
All Other Cases		Powered down

7.3.8 VCO Doubler

The VCO doubler allows the VCO frequency to be doubled, but it has a limitation of 20 GHz. The doubler can be chosen for output A only with OUTA_MUX. When this is chosen, the VCO2X_EN bit must also be enabled. The doubler can also be used in phase sync mode, provided that OUTB_MUX is not set for the channel divider.

Table 10. VCO Doubler Programming

VCO DOUBLER	PROGRAMMING
Disabled	OUTA_MUX <> 2 VCO2X_EN = 0
Enabled	OUTA_MUX = 2 VCO2X_EN = 1

7.3.9 Output Buffer

The RF output buffer type is open collector and requires an external pullup to Vcc. This component may be a 50-Ω resistor to target 50-Ω output impedance match, or an inductor for higher output power at the expense of the output impedance being far from 50 Ω. If inductor is used, it is recommended to follow with resistive pad for better impedance matching. The current to the output buffer increases for states 0 to 31 and then again from states 48 to 63. States 32 to 47 are redundant and mimic states 16 to 31. If using a resistor, limit the OUTx_PWR setting to 50. Higher settings may actually reduce power due to the voltage drop across the resistor.

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Table 11. OUTx_PWR Recommendations for Resistor Pullup

f_{OUT}	RECOMMENDATION		COMMENTS
	HIGHEST POWER	LOWEST NOISE FLOOR	
10 MHz ≤ f_{OUT} < 13.3 GHz	OUTx_PWR = 50	OUTx_PWR = 50	-
13.3 GHz ≤ f_{OUT} ≤ 14.3 GHz	OUTx_PWR = 15	OUTx_PWR = 15	TI recommends to set OUTx_PWR ≤ 15 to avoid the power drop at hot temperature.
14.3 GHz < f_{OUT} ≤ 15 GHz	OUTx_PWR = 31	OUTx_PWR = 20	-
15 GHz < f_{OUT} ≤ 20 GHz	OUTx_PWR = 31	OUTx_PWR = 20	-

7.3.10 Power-Down Modes

The LMX2595 can be powered up and down using the CE pin or the POWERDOWN bit. When the device comes out of the powered down state, either by resuming the POWERDOWN bit to zero or by pulling back CE pin HIGH, register R0 must be programmed with FCAL_EN high again to re-calibrate the device.

7.3.11 Phase Synchronization

7.3.11.1 General Concept

The SYNC pin allows one to synchronize the LMX2595 such that the delay from the rising edge of the OSCin signal to the output signal is deterministic. Initially, the devices are locked to the input, but are not synchronized. The user sends a synchronization pulse that is reclocked to the next rising edge of the OSCin pulse. After a given time, t_1, the phase relationship from OSCin to f_{OUT} will be deterministic. This time is dominated by the sum of the VCO calibration time, the analog setting time of the PLL loop, and the MASH_RST_CNT if used in fractional mode.

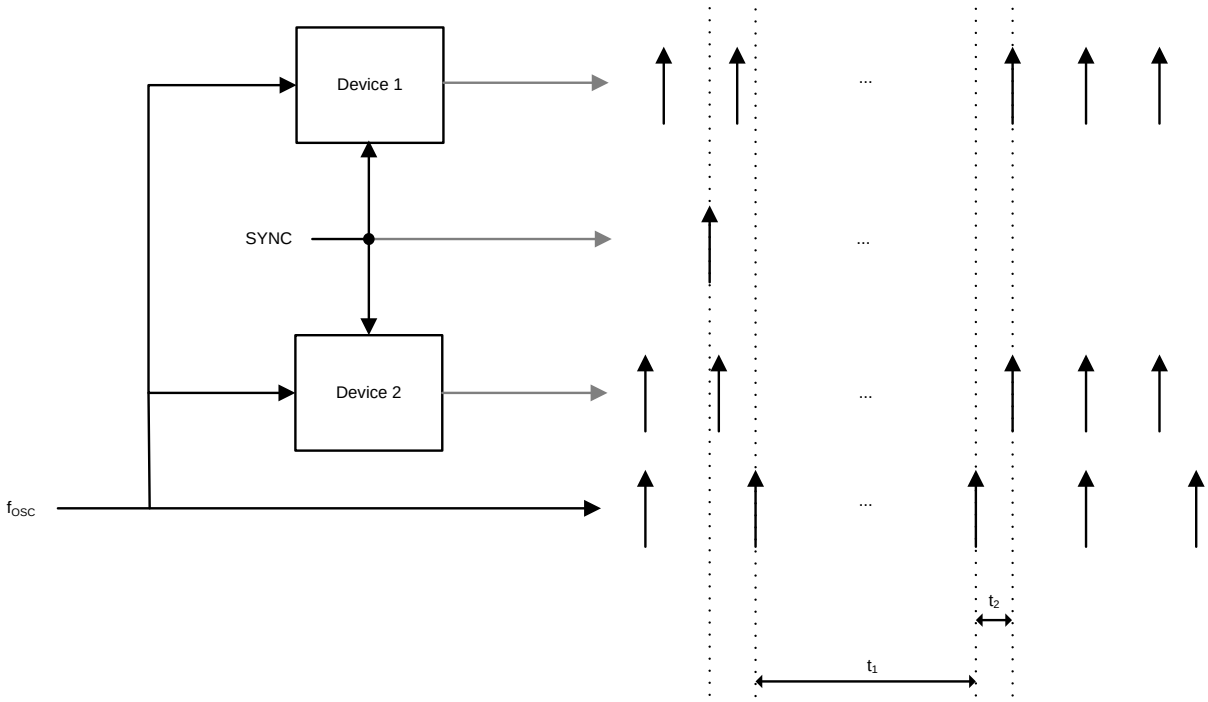

Figure 31. Devices Are Now Synchronized to OSCin Signal

When the SYNC feature is enabled, part of the channel divide may be included in the feedback path. This will be referred to as *IncludedDivide*

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Table 12. IncludedDivide With VCO_PHASE_SYNC = 1

OUTx_MUX	CHANNEL DIVIDER	INCLUDEDDIVIDE
OUTB_MUX = 1 ("VCO") OUTA_MUX = 1 "VCO" or 2 "VCO Doubler"	Don't Care	1
All Other Valid Conditions	Divisible by 3, but NOT 24 or 192	SEG0 × SEG1 = 6
	All other values	SEG0 × SEG1 = 4

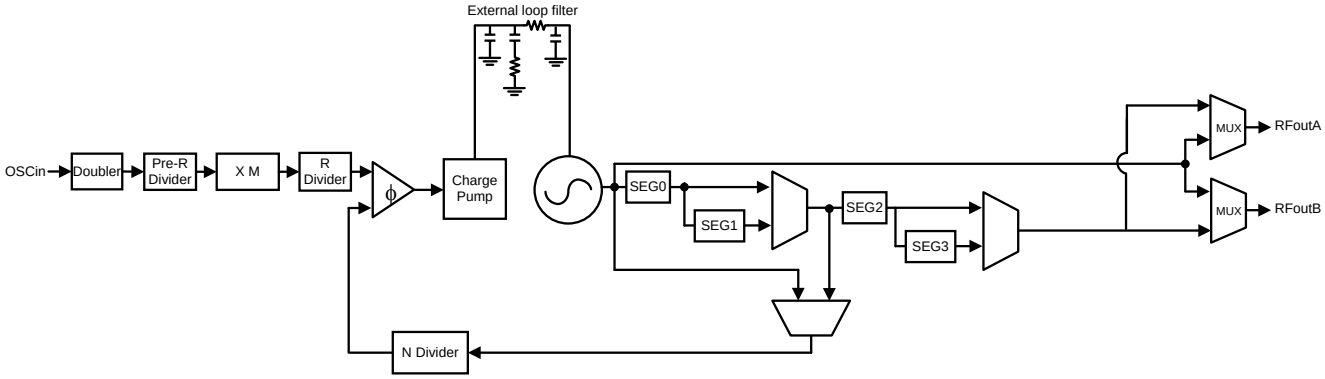

Figure 32. Phase SYNC Diagram

7.3.11.2 Categories of Applications for SYNC

The requirements for SYNC depend on certain setup conditions. In cases that the SYNC is not timing critical, it can be done through software by toggling the VCO_PHASE_SYNC bit from 0 to 1. When it is timing critical, then it must be done through the pin and the setup and hold times for the OSCin pin are critical. Figure 33 gives the different categories.

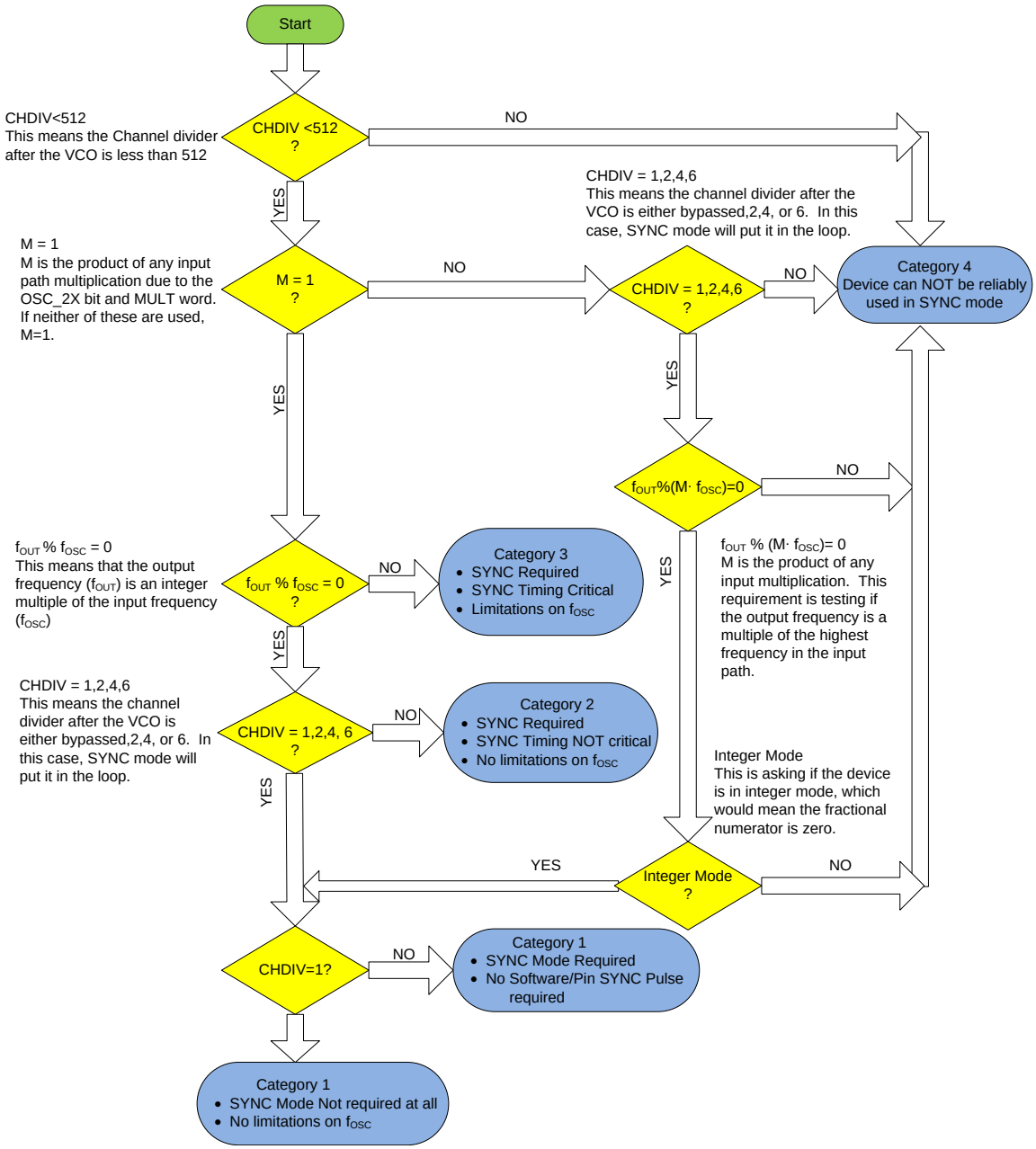

Figure 33. Determining the SYNC Category

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7.3.11.3 Procedure for Using SYNC

This procedure must be used to put the device in SYNC mode.

1. Use the flowchart to determine the SYNC category.
2. Make determinations for OSCin and using SYNC based on the category.
   1. If Category 4, SYNC cannot be performed in this setup.
   2. If category 3, ensure that the maximum f_{OSC} frequency for SYNC is not violated and there are hardware accommodations to use the SYNC pin.
3. Determine the value of IncludedDivide:
   1. If OUTA_MUX is not channel divider and OUTB_MUX is not channel divider or SysRef, then IncludedDivide = 1.
   2. Otherwise, IncludedDivide = 2 × SEG1. In the case that the channel divider is 2, then IncludedDivide=4.
4. If not done already, divide the N-divider and fractional values by IncludedDivide to account for the IncludedDivide.
5. Program the device with the VCO_PHASE_SYNC = 1. Note that this does not count as applying a SYNC to device (for category 2).
6. Apply the SYNC, if required:
   1. If category 2, VCO_PHASE_SYNC can be toggled from 0 to 1. Alternatively, a rising edge can be sent to the SYNC pin and the timing of this is not critical.
   2. If category 3, the SYNC pin must be used, and the timing must be away from the rising edge of the OSCin signal. Toggling the SYNC pin runs VCO calibration when FCAL_EN = 1. If FCAL_EN = 0 then SYNC pin does not function.

7.3.11.4 SYNC Input Pin

The SYNC input pin can be driven either in CMOS or LVDS mode. However, if not using SYNC mode (VCO_PHASE_SYNC = 0), then the INPIN_IGNORE bit must be set to one, otherwise it causes issues with lock detect. If the pin is desired for to be used and VCO_PHASE_SYNC = 1, then set INPIN_IGNORE = 0. LVDS or CMOS mode may be used. LVDS works to 250 mVPP, but is not ensured in production.

7.3.12 Phase Adjust

The MASH_SEED word can use the sigma-delta modulator to shift output signal phase with respect to the input reference. If a SYNC pulse is sent (software or pin) or the MASH is reset with MASH_RST_N, then this phase shift is from the initial phase of zero. If the MASH_SEED word is written to, then this phase is added. Use Equation 5 to calculate the phase shift.

$$\text{Phase shift in degrees} = 360 \times (\text{MASH_SEED} / \text{PLL_DEN}) \times (\text{IncludedDivide} / \text{CHDIV}) \quad (5)$$

Example:

Mash seed = 1

Denominator = 12

Channel divider = 16

Phase shift (VCO_PHASE_SYNC = 0) = 360 × (1/12) × (1/16) = 1.875 degrees

Phase Shift (VCO_PHASE_SYNC = 1) = 360 × (1/12) × (4/16) = 7.5 degrees

There are several considerations with phase shift with MASH_SEED:

- Phase shift can be done with a FRAC_NUM = 0, but MASH_ORDER must be greater than zero. For MASH_ORDER = 1, the phase shifting only occurs when MASH_SEED is a multiple of PLL_DEN.
- For the phase adjust, the condition PLL_DEN > PLL_NUM + MASH_SEED must be satisfied.
- When MASH_SEED and Phase SYNC are used together with IncludedDivide > 1, additional constraints may be necessary to produce a monotonic relationship between MASH_SEED and the phase shift, especially when the VCO frequency is below 10 GHz. These constraints are application specific, but some general guidelines are to reduce modulator order and increase the N divider. One possible guideline is for PLL_N ≥ 45 (2nd order modulator), PLL_N ≥ 49 (3rd Order modulator), PLL_N ≥ 54 (4th Order Modulator).

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7.3.13 Fine Adjustments for Phase Adjust and Phase SYNC

Phase SYNC refers to the process of getting the same phase relationship for every power-up cycle and each time assuming that a given programming procedure is followed. However, there are some adjustments that can be made to get the most accurate results. As for the consistency of the phase SYNC, the only source of variation could be if the VCO calibration chooses a different VCO core and capacitor, which can introduce a bimodal distribution with about 10 ps of variation. If this 10 ps is not desirable, then it can be eliminated by reading back the VCO core, capcode, and DACISET values and forcing these values to ensure the same calibration settings every time. The delay through the device varies from part to part and can be on the order of 60 ps. This part to part variation can be calibrated out with the MASH_SEED. The variation in delay through the device also changes on the order of +2.5 ps/°C, but devices on the same board likely have similar temperatures, so this will somewhat track. In summary, the device can be made to have consistent delay through the part and there are means to adjust out any remaining errors with the MASH_SEED. This tends only to be an issue at higher output frequencies when the period is shorter.

7.3.14 Ramping Function

The LMX2595 supports the ability to make ramping waveforms using manual mode or automatic mode. In manual mode, the user defines a step and uses the RampClk and RampDir pins to create the ramp. In automatic mode, the user sets up the ramp with up to two linear segments in advance and the device automatically creates this ramp. Table 13 fields apply in both automatic mode and manual pin mode.

Table 13. Ramping Field Descriptions

FIELD	PROGRAMMING	DESCRIPTION
GENERAL COMMANDS		
RAMP_EN	0 = Disabled 1 = Enabled	RAMP_EN must be 1 for any ramping functions to work.
RAMP_MANUAL	0 = Automatic ramping mode 1 = Manual pin ramping mode	In automatic ramping mode, the ramping is automatic and the clock is based on the phase detector. In manual pin ramping mode, the clock is based on rising edges on the RampClk pin.
RAMPx_INC	0 to $2^{30} – 1$	This is the amount the fractional numerator is increased for each phase detector cycle in the ramp.
RAMPx_DLY	0 to 65535	This is the length of the ramp in phase detector cycles.
DEALING WITH VCO CALIBRATION		
RAMP_THRESH	0 to $\pm 2^{33} – 1$	Whenever the fractional numerator changes this much (either positive or negative) because the VCO was last calibrated, the VCO is forced to recalibrate.
RAMP_TRIG_CAL	0 = Disabled 1 = Enabled	When enabled, the VCO is forced to recalibrate at the beginning each ramp.
PLL_DEN	4294967295	In ramping mode, the denominator must be fixed to this forced value of $2^{32} – 1$. However, the effective denominator in ramping mode is 2^{24}.
LD_DLY	0	This must be zero to avoid interfering with calibration.
RAMP LIMITS		
RAMP_LIMIT_LOW RAMP_LIMIT_HIGH	0 to $\pm 2^{33} – 1$	2's complement of the total value of the ramp low and high limits can never go beyond. If this value is exceeded, then the frequency is limited.

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Table 14. General Restrictions for Ramping

RULE	RESTRICTION	EXPLANATION
Phase Detector Frequency	$f_{OSC}/2^{CAL_CLK_DIV} \leq f_{PD} \leq$ 125 MHz	**Minimum Phase Detector Frequency when Ramping** The phase detector frequency cannot be less than the state machine clock frequency, which is calculated from expression on the left-hand side of the inequality. This is satisfied provided there is no division in the input path. However, if the PLL R-divider is used, it is necessary to adjust CAL_CLK_DIV to adjust the state machine clock frequency. This also implies a maximum R divide of 8 this is the maximum value of $2^{CAL_CLK_DIV}$. **Maximum Phase Detector Frequency** TI recommends to set the phase-detector frequency ≤ 125 MHz because, if the phase detector frequency is too high, it can lead to distortion in the ramp. Higher phase-detector frequency may be possible, but this distortion is application specific.

7.3.14.1 Manual Pin Ramping

Manual pin ramping is enabled by setting RAMP_EN = 1 and RAMP_MANUAL = 1. The rising edges are applied to the RampClk pin are reclocked to the phase detector frequency. The RampDir pin controls the size of the change. If a rising edge is seen on the RampClk pin while the VCO is calibrating, then this rising edge is ignored. The frequency for the RampClk must be limited to a frequency of 250 kHz or less, and the rising edge of the RampDir signal must be targeted away from the rising edges of the RampCLK pin.

Table 15. RAMP_INC

RampDir PIN	STEP SIZE
Low	Add RAMP0_INC
High	Add RAMP1_INC

7.3.14.1.1 Manual Pin Ramping Example

In this ramping example, assume that we want to use the pins for UP/Down control of the ramp for 10-MHz steps and the phase detector is 100 MHz.

Table 16. Step Ramping Example

FIELD	PROGRAMMING	DESCRIPTION
RAMP_EN	1 = Enabled	
RAMP_MANUAL	1 = Manual pin ramping mode	
RAMP0_INC	1677722	(10 MHz)/ (100 MHz) × 16777216 = 1677722 2's complement = 1677722
RAMP1_INC	1072064102	(–10 MHz)/ (100 MHz) × 16777216 = –1677722 2's complement = 2^{30} – 1677722 = 1072064102
RAMP_TRIG_CAL	1	Recalibrate at every clock cycle

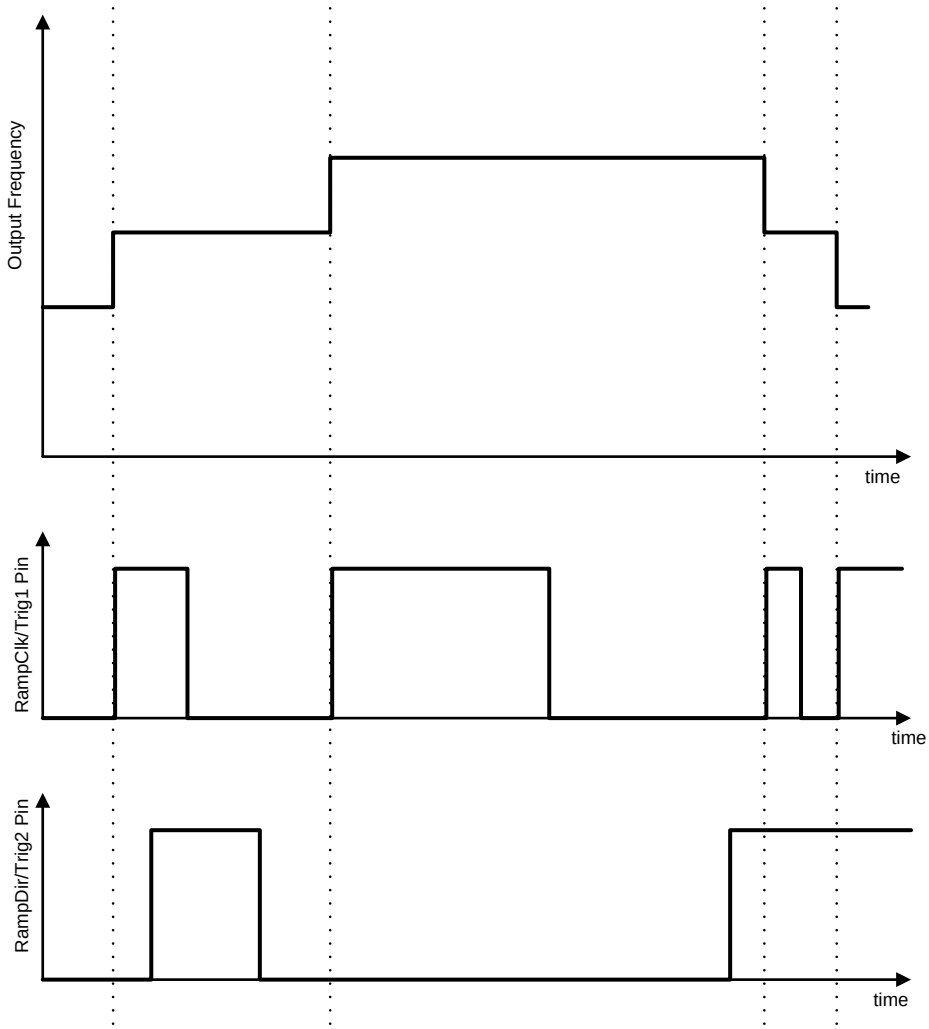

Figure 34. Step Ramping Example

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7.3.14.2 Automatic Ramping

Automatic ramping is enabled when RAMP_EN = 1 and RAMP_MANUAL = 0. The action of programming FCAL = 1 starts the ramping. In this mode, there are two ramps that one can use to set the length and frequency change. In addition to this, there are ramp limits that can be used to create more complicated waveforms.

Automatic ramping can really be divided into two classes depending on if the VCO must calibrate in the middle of the ramping waveform or not. If the VCO can go the entire range without calibrating, this is calibration-free ramping, which is shown in *Typical Characteristics*. Note that this range is less at hot temperatures and for lower frequency VCOs. This range is not ensured, so margin must be built into the design.

For waveforms that are NOT calibration free, the slew rate of the ramp must be kept less than 250 kHz/µs. Also, for all automatic ramping waveforms, be aware that there is a very small phase disturbance as the VCO crosses over the integer boundary, so one might consider using the input multiplier to avoid these or timing the VCO calibrations at integer boundaries.

Table 17. Automatic Ramping Field Descriptions

FIELD	PROGRAMMING	DESCRIPTION
RAMP_DLY	0 = One clock cycle 1 = Two clock cycles	Normally, the ramp clock is equal to the phase detector frequency. When this feature is enabled, it reduces the ramp clock by a factor of 2.
RAMP0_LEN RAMP1_LEN	0 to 65535	This is the length of the ramp in clock cycles. Note that the VCO calibration time is added to this time.
RAMP0_INC RAMP1_INC	0 to $2^{30} – 1$	2's complement of the value for the ramp increment.
RAMP0_NEXT RAMP1_NEXT	0 = RAMP0 1 = RAMP1	Defines which ramp comes after the current ramp.
RAMP0_NEXT_TRIG RAMP1_NEXT_TRIG	0 = Timeout counter 1 = Trigger A 2 = Trigger B 3 = Reserved	Determines what triggers the action of the next ramp occurrence.
RAMP_TRIG_A RAMP_TRIG_B	0 = Disabled 1 = RampClk rising edge 2 = RampDir rising edge 4 = Always triggered 9 = RampClk falling edge 10 = RampDir falling edge All other States = invalid	This field defines the ramp trigger.
RAMP0_RST RAMP1_RST	0 = Disabled 1 = Enabled	Enabling this bit causes the ramp to reset to the original value when the ramping started. This is useful for roundoff errors.
RAMP_BURST_COUNT	0 to 8191	This is the number the ramping pattern repeats and only applies for a terminating ramping pattern.
RAMP_BURST_TRIG	0 = Ramp Transition 1 = Trigger A 2 = Trigger B 3 = Reserved	This defines what causes the RAMP_COUNT to increment.

7.3.14.2.1 Automatic Ramping Example (Triangle Wave)

Suppose user wants to generate a sawtooth ramp that goes from 8 to 10 GHz in 2 ms (including calibration breaks) with a phase-detector frequency of 50 MHz. Divide this into segments of 50 MHz where the VCO ramps for 25 µs, then calibrates for 25 µs, for a total of 50 µs. There would therefore be 40 such segments which span over a 2-GHz range and would take 2 ms, including calibration time.

Table 18. Sawtooth Ramping Example

FIELD	PROGRAMMING	DESCRIPTION
RAMP_EN	1 = Enabled	
RAMP_MANUAL	0 = Automatic ramping mode	
RAMP_TRIG_CAL	0 = Disabled	
RAMP_THRESH	16777216 (= 50-MHz ramp_thresh)	50 MHz / 50 MHz × 2^{24} = 16777216
RAMP_DLY	0 = 1 clock cycle	
RAMPx_LEN	50000	1000 µs × 50 MHz = 50000
RAMP0_INC	13422	(2000 MHz) / (50 MHz) × 2^{24} / 50000 = 13422
RAMP1_INC	1073728402	(–2000 MHz) / (50 MHz) × 2^{24} / 50000 = –13422 2's complement = 2^{30} – 13422 = 1073728402
RAMP0_NEXT	1 = RAMP1	
RAMP1_NEXT	0 = RAMP0	
RAMPx_NEXT_TRIG	0 = Timeout counter	
RAMP_TRIG_x	0 = Disabled	
RAMP0_RST	1 = Enabled	Not necessary, but good practice to reset.
RAMP1_RST	0 = Disabled	Do not reset this, or ramp does not work.
RAMP_BURST_COUNT	0	
RAMP_BURST_TRIG	0 = Ramp Transition	

NOTE

To calculate ramp_scale_count and ramp_dly_cnt, remember that the desired calibration time is 25 µs.

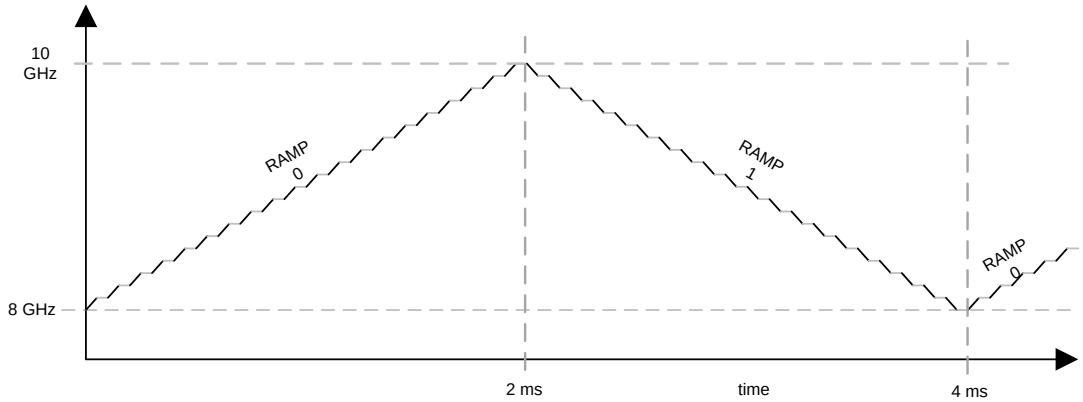

Figure 35. Triangle Waveform Example

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7.3.15 SYSREF

The LMX2595 can generate a SYSREF output signal that is synchronized to f_{OUT} with a programmable delay. This output can be a single pulse, series of pulses, or a continuous stream of pulses. To use the SYSREF capability, the PLL must first be placed in SYNC mode with VCO_PHASE_SYNC = 1.

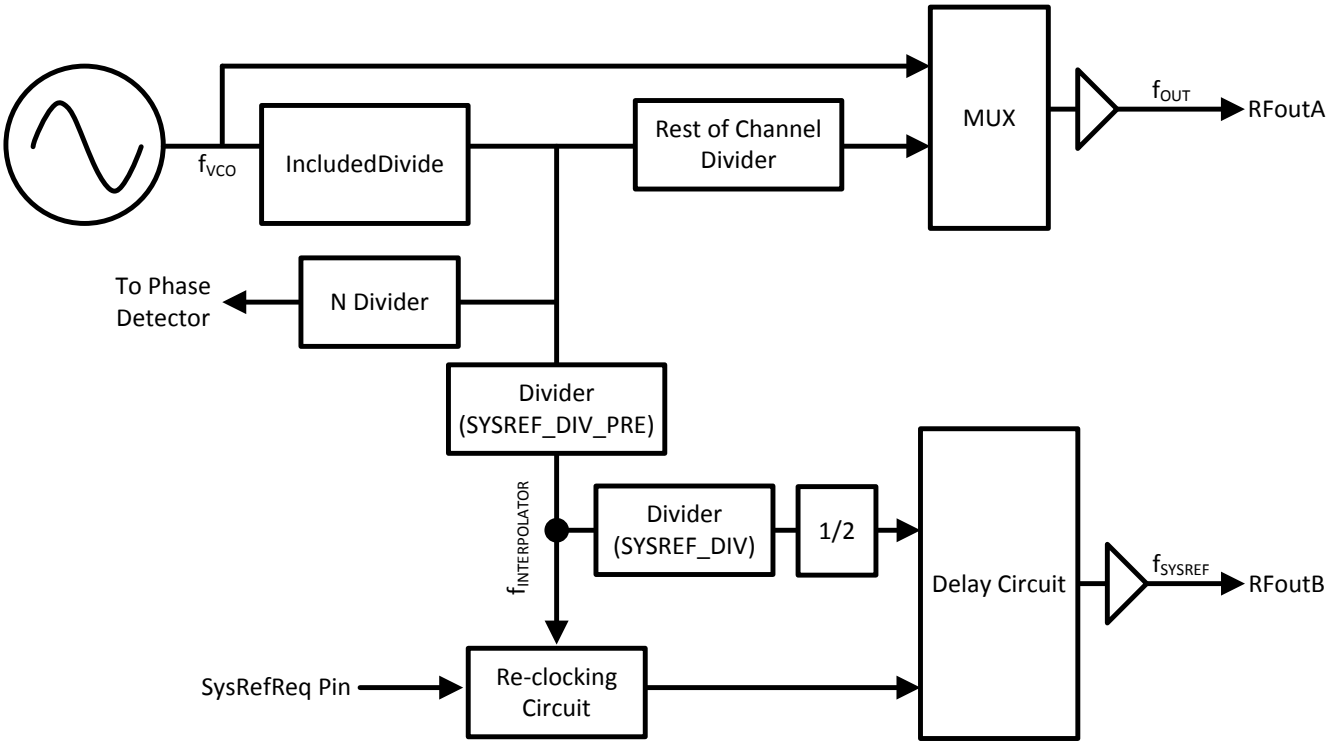

Figure 36. SYSREF Setup

As Figure 36 shows, the SYSREF feature uses IncludedDivide and SYSREF_DIV_PRE divider to generate $f_{INTERPOLATOR}$. This frequency is used for reclocking of the rising and falling edges at the SysRefReq pin. In master mode, the $f_{INTERPOLATOR}$ is further divided by 2 × SYSREF_DIV to generate finite series or continuous stream of pulses.

Table 19. SYSREF Setup

PARAMETER	MIN	TYP	MAX	UNIT
f_{VCO}	7.5		15	GHz
$f_{INTERPOLATOR}$	0.8		1.5	GHz
IncludedDivide		4 or 6		
SYSREF_DIV_PRE	1, 2, or 4			
SYSREF_DIV	4,6,8, ... , 4098			
$f_{INTERPOLATOR}$	$f_{INTERPOLATOR} = f_{VCO}$ / (IncludedDivide × SYSREF_DIV_PRE)			
f_{SYSREF}	$f_{SYSREF} = f_{INTERPOLATOR}$ / (2 × SYSREF_DIV)			
Delay step size		9		ps
Pulses for pulsed mode (SYSREF_PULSE_CNT)	0		15	n/a

The delay can be programmed using the JESD_DAC1_CTRL, JESD_DAC2_CTRL, JESD_DAC3_CTRL, and JESD_DAC4_CTRL words. By concatenating these words into a larger word called "SYSREFPHASESHIFT", the relative delay can be found. The sum of these words should always be 63.

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Table 20. SysRef Delay

SYSREFPHASESHIFT	DELAY	JESD_DAC1	JESD_DAC2	JESD_DAC3	JESD_DAC4
0	Minimum	36	27	0	0
...				0	0
36		0	63	0	0
37		62	1	0	0
...					
99		0	0	63	0
100		0	0	62	1
...					
161		0	0	1	62
162		0	0	0	63
163		1	0	0	62
225		63	0	0	0
226		62	1	0	0
247	Maximum	41	22	0	0
> 247	Invalid	Invalid	Invalid	Invalid	Invalid

7.3.15.1 Programmable Fields

Table 21 has the programmable fields for the SYSREF functionality.

Table 21. SYSREF Programming Fields

FIELD	PROGRAMMING	DEFAULT	DESCRIPTION
SYSREF_EN	0: Disabled 1: Enabled	0	Enables the SYSREF mode. SYSREF_EN should be 1 if and only if OUTB_MUX = 2 (SysRef).
SYSREF_DIV_PRE	1: DIV1 2: DIV2 4: DIV4 Other states: invalid		The output of this divider is $f_{INTERPOLATOR}$.
SYSREF_REPEAT	0: Master mode 1: Repeater mode	0	In master mode, the device creates a series of SYSREF pulses. In repeater mode, SYSREF pulses are generated with the SysRefReq pin.
SYSREF_PULSE	0: Continuous mode 1: Pulsed mode	0	Continuous mode continuously makes SYSREF pulses, where pulsed mode makes a series of SYSREF_PULSE_CNT pulses.
SYSREF_PULSE_CNT	0 to 15	4	In the case of using pulsed mode, this is the number of pulses. Setting this to zero is an allowable, but not practical state.
SYSREF_DIV	0: Divide by 4 1: Divide by 6 2: Divide by 8 ... 2047: Divide by 4098	0	This is one of the dividers between the VCO and SysRef output used in master mode.

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7.3.15.2 Input and Output Pin Formats

7.3.15.2.1 Input Format for SYNC and SysRefReq Pins

These pins are single-ended, but a differential signal can be converted to drive them. In the LVDS mode, if the INPIN_FMT is set to LVDS mode, then the bias level can be adjusted with INPIN_LVL and the hysteresis can be adjusted with INPIN_HYST.

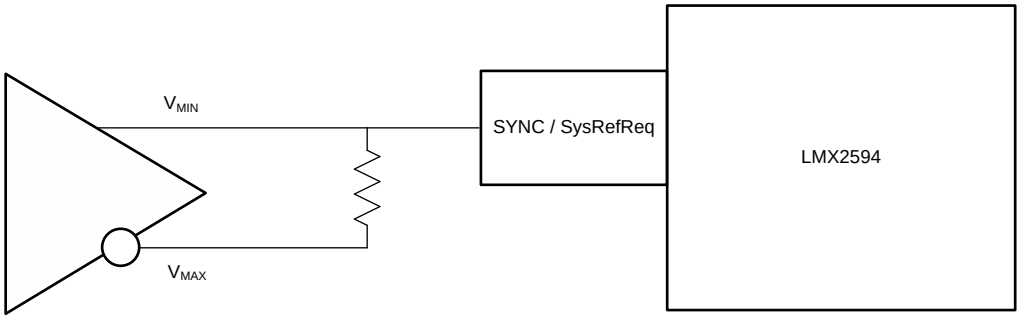

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Figure 37. Driving SYNC/SYSREF With Differential Signal

7.3.15.2.2 SYSREF Output Format

The SYSREF output comes in differential format through RFoutB. This will have a minimum voltage of about 2.3 V and a maximum of 3.3 V. If DC coupling cannot be used, there are two strategies for AC coupling.

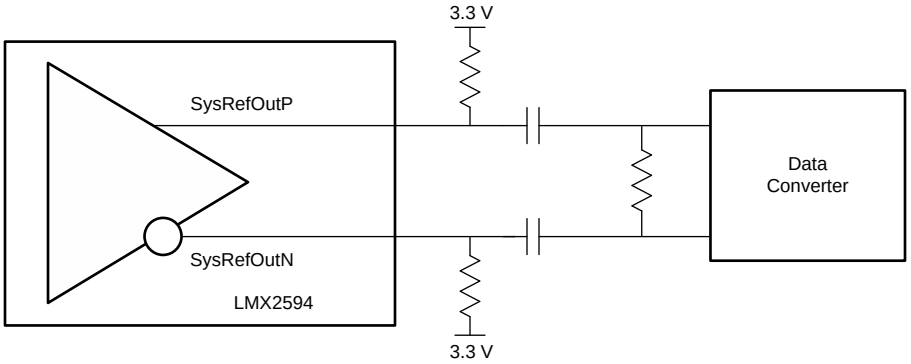

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Figure 38. SYSREF Output

1. Send a series of pulses to establish a DC-bias level across the AC-coupling capacitor.
2. Establish a bias voltage at the data converter that is below the threshold voltage by using a resistive divider.

7.3.15.3 Examples

The SysRef can be used in a repeater mode (SYSREF_REPEAT = 1), which just echos the SysRefReq pin, after being reclocked to the $f_{INTERPOLATOR}$ frequency and then f_{OUT} (from RFoutA).

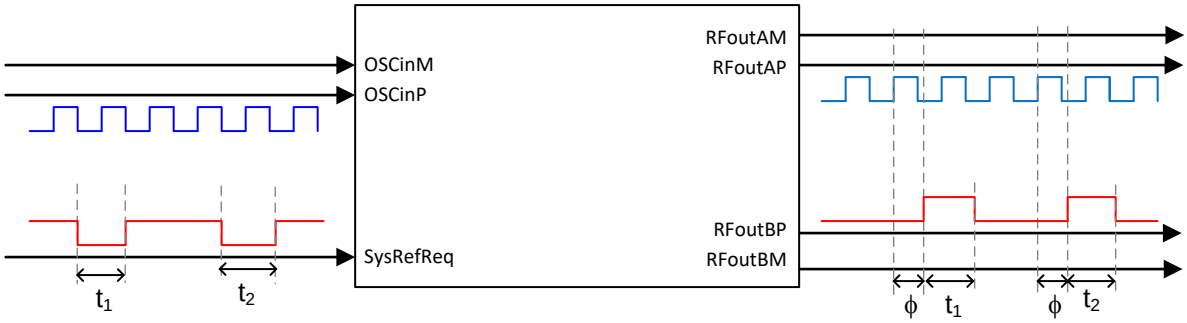

Figure 39. SYSREF Out In Repeater Mode

In master mode (SYSREF_REPEAT = 0), rising and falling edges at the SysRefReq pin are first reclocked to the f_{OSC}, then $f_{INTERPOLATOR}$, and finally to f_{OUT}. A programmable number of pulses is generated with a frequency equal to f_{VCO} / (2 × IncludedDivide × SYSREF_DIV_PRE × SYSREF_DIV). In continuous mode (SYSREF_PULSE = 0), the SysRefReq pin is held high to generate a continuous stream of pulses. In pulse mode (SYSREF_PULSE = 1), a finite number of pulses determined by SYSREF_PULSE_CNT is sent for each rising edge of the SysRefReq pin.

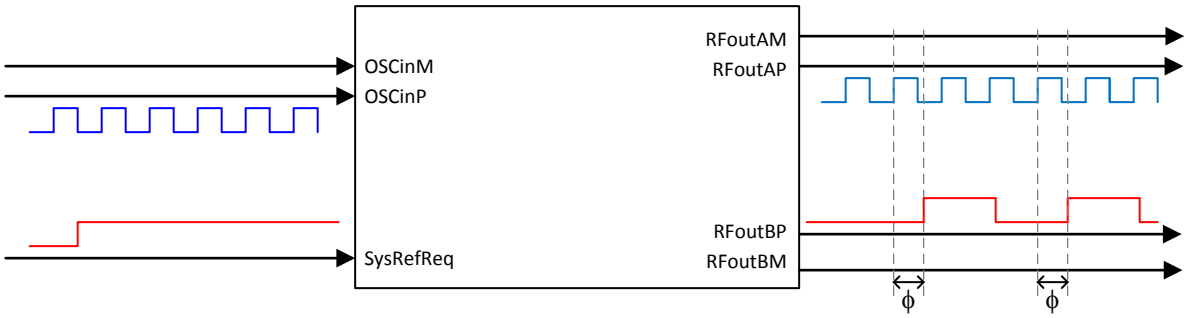

Figure 40. Figure 1. SYSREF Out In Pulsed/Continuous Mode

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7.3.15.4 SYSREF Procedure

To use SYSREF, do the these steps:

1. Put the device in SYNC mode using the procedure already outlined.
2. Figure out IncludedDivide the same way it is done for SYNC mode.
3. Calculate the SYSREF_DIV_PRE value such that the interpolator frequency ($f_{INTERPOLATOR}$) is in the range of 800 to 1500 MHz. $f_{INTERPOLATOR} = f_{VCO}$/IncludedDivide/SYSREF_DIV_PRE. Make this frequency a multiple of f_{OSC} if possible.
4. If using continuous mode (SYSREF_PULSE = 0), ensure the SysRefReq pin is high.
5. If using pulse mode (SYSREF_PULSE = 1), set up the pulse count as desired. Pulses are created by toggling the SysRefReq pin.
6. Adjust the delay between the RFoutA and RFoutB signal using the JESD_DACx_CTL fields.

7.3.16 SysRefReq Pin

The SysRefReq pin can be used in CMOS all the time, or LVDS mode is also optional if SYSREF_REPEAT = 1. LVDS mode cannot be used in master mode.

7.4 Device Functional Modes

Although there are a vast number of ways to configure this device, only one is really functional.

Table 22. Device Functional Modes

MODE	DESCRIPTION	SOFTWARE SETTINGS
RESET	Registers are held in their reset state. This device does have a power on reset, but it is good practice to also do a software reset if there is any possibility of noise on the programming lines, especially if there is sharing with other devices. Also realize that there are registers not disclosed in the data sheet that are reset as well.	RESET = 1, POWERDOWN = 0
POWERDOWN	Device is powered down.	POWERDOWN = 1 or CE Pin = Low
Normal operating mode	This is used with at least one output on as a frequency synthesizer.	
SYNC mode	This is used where part of the channel divider is in the feedback path to ensure deterministic phase.	VCO_PHASE_SYNC = 1
SYSREF mode	In this mode, RFoutB is used to generate pulses for SYSREF.	VCO_PHASE_SYNC =1, SYSREF_EN = 1

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7.5 Programming

The LMX2595 is programmed using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W bit, 0 is for write, and 1 is for read. The address field ADDRESS[6:0] is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When CSB goes high, data is transferred from the data field into the selected register bank. See Figure 1 for timing details.

7.5.1 Recommended Initial Power-Up Sequence

For the most reliable programming, TI recommends this procedure::

1. Apply power to device.
2. Program RESET = 1 to reset registers.
3. Program RESET = 0 to remove reset.
4. Program registers as shown in the register map in REVERSE order from highest to lowest.
5. Wait 10 ms.
6. Program register R0 one additional time with FCAL_EN = 1 to ensure that the VCO calibration runs from a stable state.

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Change the N-divider value.
2. Program the PLL numerator and denominator.
3. Program FCAL_EN (R0[3]) = 1.

7.5.3 General Programming Requirements

Follow these requirements when programming the device:

1. For register bits that do not have field names in Table 24, it is necessary to program these values just as shown in the register map.
2. Not all registers need to be programmed. Refer to Table 23 for details.
3. Power-on-reset register values may not be optimal, so it is always necessary to program all of the required registers after powering on the device. Note that the 'Reset' column in register descriptions is the power-on-reset value.

Table 23. Programming Requirement

Registers	Function	Comment
R107 – R112	Readback	These registers are for readback only and do not need to be programmed.
R79 – R106	Ramping	If ramping function is not used (RAMP_EN = 0), then these registers do not need to be programmed.
R0 – R78	General	These registers need to be programmed for all scenarios.

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7.6 Register Maps

Table 24. Full Register Map

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	RAMP_EN	VCO_PHASE_SYNC	1	0	0	1	OUT_MUTE	FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWERDOWN
R1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV		
R2	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0
R4	0	0	0	0	0	1	0	0	ACAL_CMP_DLY								0	1	0	0	0	0	1	1
R5	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
R6	0	0	0	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0
R7	0	0	0	0	0	1	1	1	0	OUT_FORCE	0	0	0	0	0	0	1	0	1	1	0	0	1	0
R8	0	0	0	0	1	0	0	0	0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0
R9	0	0	0	0	1	0	0	1	0	0	0	OSC_2X	0	1	1	0	0	0	0	0	0	1	0	0
R10	0	0	0	0	1	0	1	0	0	0	0	1	MULT					1	0	1	1	0	0	0
R11	0	0	0	0	1	0	1	1	0	0	0	0	PLL_R								1	0	0	0
R12	0	0	0	0	1	1	0	0	0	1	0	1	PLL_R_PRE											
R13	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R14	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	CPG			0	0	0	0
R15	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1
R16	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	VCO_DACISET								
R17	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	VCO_DACISET_STRT								
R18	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R19	0	0	0	1	0	0	1	1	0	0	1	0	0	1	1	1	VCO_CAPCTRL							
R20	0	0	0	1	0	1	0	0	1	1	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0
R21	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

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Register Maps (continued)

Table 24. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R22	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R23	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
R24	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0
R25	0	0	0	1	1	0	0	1	DBLR_IBIAS_CTRL1															
R26	0	0	0	1	1	0	1	0	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0
R27	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	VCO 2X _EN
R28	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0
R29	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0
R30	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0
R31	0	0	0	1	1	1	1	1	0	CHDIV _DIV 2	0	0	0	0	1	1	1	1	1	0	1	1	0	0
R32	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1
R33	0	0	1	0	0	0	0	1	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1
R34	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PLL_N[18:16]		
R35	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R36	0	0	1	0	0	1	0	0	PLL_N															
R37	0	0	1	0	0	1	0	1	MASH _SEED _EN	0	PFD_DLY_SEL						0	0	0	0	0	1	0	0
R38	0	0	1	0	0	1	1	0	PLL_DEN[31:16]															
R39	0	0	1	0	0	1	1	1	PLL_DEN[15:0]															
R40	0	0	1	0	1	0	0	0	[31:16]															
R41	0	0	1	0	1	0	0	1	[15:0]															
R42	0	0	1	0	1	0	1	0	PLL_NUM[31:16]															
R43	0	0	1	0	1	0	1	1	PLL_NUM[15:0]															
R44	0	0	1	0	1	1	0	0	0	0	OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	0	0	MASH_ORDER		
R45	0	0	1	0	1	1	0	1	1	1	0	OUTA_MUX		OUT_ISET		0	1	1	OUTB_PWR					
R46	0	0	1	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	OUTB_MUX	

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Register Maps (continued)

Table 24. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R47	0	0	1	0	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R48	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R49	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0
R50	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R52	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
R53	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R54	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R55	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R56	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R57	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R58	0	0	1	1	1	0	1	0	INPIN_IGNORE	INPIN_HYST	INPIN_LVL		INPIN_FMT			0	0	0	0	0	0	0	0	1
R59	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_TYPE
R60	0	0	1	1	1	1	0	0	LD_DLY															
R61	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
R62	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0
R63	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R64	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0
R65	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R66	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
R67	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R68	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0
R69	0	1	0	0	0	1	0	1	MASH_RST_COUNT[31:16]															
R70	0	1	0	0	0	1	1	0	MASH_RST_COUNT[15:0]															
R71	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	0	1
R72	0	1	0	0	1	0	0	0	0	0	0	0	0	SYSREF_DIV										
R73	0	1	0	0	1	0	0	1	0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL					

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Register Maps (continued)

Table 24. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R74	0	1	0	0	1	0	1	0	SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL					
R75	0	1	0	0	1	0	1	1	0	0	0	0	1	CHDIV					0	0	0	0	0	0
R76	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R77	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R78	0	1	0	0	1	1	1	0	0	0	0	0	RAMP_THRESH[32]	0	QUICK_RECAL_EN	VCO_CAPCTRL_STRT								1
R79	0	1	0	0	1	1	1	1	RAMP_THRESH[31:16]															
R80	0	1	0	1	0	0	0	0	RAMP_THRESH[15:0]															
R81	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_HIGH[32]
R82	0	1	0	1	0	0	1	0	RAMP_LIMIT_HIGH[31:16]															
R83	0	1	0	1	0	0	1	1	RAMP_LIMIT_HIGH[15:0]															
R84	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_LOW[32]
R85	0	1	0	1	0	1	0	1	RAMP_LIMIT_LOW[31:16]															
R86	0	1	0	1	0	1	1	0	RAMP_LIMIT_LOW[15:0]															
R87	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R88	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R89	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R90	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R91	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R92	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R93	0	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R94	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R95	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R96	0	1	1	0	0	0	0	0	RAMP_BURST_EN	RAMP_BURST_COUNT													0	0

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Register Maps (continued)

Table 24. Full Register Map (continued)

	R/W	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R97	0	1	1	0	0	0	0	1	RAMP0_RST	0	0	0	1	RAMP_TRIGB				RAMP_TRIGA				0	RAMP_BURST_TRIG	
R98	0	1	1	0	0	0	1	0	RAMP0_INC[29:16]														0	RAMP0_DLY
R99	0	1	1	0	0	0	1	1	RAMP0_INC[15:0]															
R100	0	1	1	0	0	1	0	0	RAMP0_LEN															
R101	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	RAMP1_DLY	RAMP1_RST	RAMP0_NEXT	0	0	RAMP0_NEXT_TRIG	
R102	0	1	1	0	0	1	1	0	0	0	RAMP1_INC[29:16]													
R103	0	1	1	0	0	1	1	1	RAMP1_INC[15:0]															
R104	0	1	1	0	1	0	0	0	RAMP1_LEN															
R105	0	1	1	0	1	0	0	1	RAMP_DLY_CNT										RAMP_MANUAL	RAMP1_NEXT	0	0	RAMP1_NEXT_TRIG	
R106	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_TRIG_CAL	0	RAMP_SCALE_COUNT		
R107	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R108	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R109	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R110	0	1	1	0	1	1	1	0	0	0	0	0	0	rb_LD_VTUNE		0	rb_VCO_SEL			0	0	0	0	0
R111	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL							
R112	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	rb_VCO_DACISET								

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7.6.1 General Registers R0, R1, & R7

Figure 41. Registers Excluding Address

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	RAMP_EN	VCO_PHASE_SYNC_EN	1	0	0	1	OUT_MUTE	FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWERDOWN
R1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV		
R7	0	OUT_FORCE	0	0	0	0	0	0	1	0	1	1	0	0	1	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Field Descriptions

Location	Field	Type	Reset	Description
R0[15]	RAMP_EN	R/W	0	0: Disable frequency ramping mode 1: Enable frequency ramping mode
R0[14]	VCO_PHASE_SYNC	R/W	0	0: Disable phase SYNC mode 1: Enable phase SYNC mode
R0[9]	OUT_MUTE	R/W	0	Mute the outputs when the VCO is calibrating. 0: Disabled. If disabled, also be sure to enable OUT_FORCE 1: Enabled. If enabled, also be sure to disable OUT_FORCE
R0[8:7]	FCAL_HPFD_ADJ	R/W		Set this field in accordance to the phase-detector frequency for optimal VCO calibration. 0: $f_{PD} \leq 100$ MHz 1: 100 MHz < $f_{PD} \leq 150$ MHz 2: 150 MHz < $f_{PD} \leq 200$ MHz 3: f_{PD} >200 MHz
R0[6:5]	FCAL_LPFD_ADJ	R/W	0	Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0: $f_{PD} \geq 10$ MHz 1: 10 MHz > $f_{PD} \geq 5$ MHz 2: 5 MHz > $f_{PD} \geq 2.5$ MHz 3: $f_{PD} < 2.5$ MHz
R0[3]	FCAL_EN	R/W	0	Enable the VCO frequency calibration. Also note that the action of programming this bit to a 1 activates the VCO calibration
R0[2]	MUXOUT_LD_SEL	R/W	0	Selects the state of the function of the MUXout pin 0: Readback 1: Lock detect
R0[1]	RESET	R/W	0	Resets and holds all state machines and registers to default value. 0: Normal operation 1: Reset
R0[0]	POWERDOWN	R/W	0	Powers down entire device 0: Normal operation 1: Powered down
R1[2:0]	CAL_CLK_DIV	R/W	3	Sets divider for VCO calibration state machine clock based on input frequency. 0: Divide by 1. Use for $f_{OSC} \leq 200$ MHz 1: Divide by 2. Use for $f_{OSC} \leq 400$ MHz 2: Divide by 4. Use for $f_{OSC} \leq 800$ MHz 3: Divide by 8. All f_{OSC} If user is not concerned with lock time, it is recommended to set this value to 3. By slowing down the VCO calibration, the best and most repeatable VCO phase noise can be attained
R7[14]	OUT_FORCE	R/W	0	Works with OUT_MUTE in disabling outputs when VCO calibrating.

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7.6.2 Input Path Registers

Figure 42. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R9	0	0	0	OSC_2X	0	1	1	0	0	0	0	0	0	1	0	0
R10	0	0	0	1	MULT					1	0	1	1	0	0	0
R11	0	0	0	0	PLL_R								1	0	0	0
R12	0	1	0	1	PLL_R_PRE											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Field Descriptions

Location	Field	Type	Reset	Description
R9[12]	OSC_2X	R/W	0	Low=noise OSCin frequency doubler. 0: Disabled 1: Enabled
R10[11:7]	MULT	R/W	1	Programmable input frequency multiplier 0,2,,8-31: Reserved 1: Byapss 3: 3X ... 7: 7X
R11[11:4]	PLL_R	R/W	1	Programmable input path divider after the programmable input frequency multiplier.
R12[11:0]	PLL_R_PRE	R/W	1	Programmable input path divider before the programmable input frequency multiplier.

7.6.3 Charge Pump Registers (R13, R14)

Figure 43. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R14	0	0	0	1	1	1	1	0	0	CPG			0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Field Descriptions

Location	Field	Type	Reset	Description
R14[6:4]	CPG	R/W	7	Effective charge-pump current. This is the sum of up and down currents. 0: 0 mA 1: 6 mA 2: Reserved 3: 12 mA 4: 3 mA 5: 9 mA 6: Reserved 7: 15 mA

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7.6.4 VCO Calibration Registers

Figure 44. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R4	ACAL_CMP_DLY								0	1	0	0	0	0	1	1
R8	0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0
R16	0	0	0	0	0	0	0	VCO_DACISET								
R17	0	0	0	0	0	0	0	VCO_DACISET_STRT								
R19	0	0	1	0	0	1	1	1	VCO_CAPCTRL							
R20	1	1	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Field Descriptions

Location	Field	Type	Reset	Description
R4[15:8]	ACAL_CMP_DELAY	R/W	10	VCO amplitude calibration delay. Lowering this value can speed up VCO calibration, but lowering it too much may degrade VCO phase noise. The minimum allowable value for this field is 10 and this allows the VCO to calibrate to the correct frequency for all scenarios. To yield the best and most repeatable VCO phase noise, this relationship should be met: ACAL_CMP_DLY > Fsmclk / 10 MHz, where Fsmclk = Fosc / $2^{CAL_CLK_DIV}$ and Fosc is the input reference frequency. If calibration time is of concern, then it is recommended to set this register to ≥ 25.
R8[14]	VCO_DACISET_FORCE	R/W	0	This forces the VCO_DACISET value
R8[11]	VCO_CAPCTRL_FORCE	R/W	0	This forces the VCO_CAPCTRL value
R16[8:0]	VCO_DACISET	R/W	128	This sets the final amplitude for the VCO calibration in the case that amplitude calibration is forced.
R17[8:0]	VCO_DACISET_STRT	R/W	250	This sets the initial starting point for the VCO amplitude calibration.
R19[7:0]	VCO_CAPCTRL	R/W	183	This sets the final VCO band when VCO_CAPCTRL is forced.
R20[13:11]	VCO_SEL	R/W	7	This sets VCO start core for calibration and the VCO when it is forced. 0: Not Used 1: VCO1 2: VCO2 3: VCO3 4: VCO4 5: VCO5 6: VCO6 7: VCO7
R20[10]	VCO_SEL_FORCE	R/W	0	This forces the VCO to use the core specified by VCO_SEL. It is intended mainly for diagnostic purposes. 0: Disabled (recommended) 1: Enabled

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7.6.5 N Divider, MASH, and Output Registers

Figure 45. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R34	0	0	0	0	0	0	0	0	0	0	0	0	0	PLL_N[18:16]		
R36	PLL_N															
R37	MASH_SEED_EN	0	PFD_DLY_SEL						0	0	0	0	0	1	0	0
R38	PLL_DEN[31:16]															
R39	PLL_DEN[15:0]															
R40	[31:16]															
R41	[15:0]															
R42	PLL_NUM[31:16]															
R43	PLL_NUM[15:0]															
R44	0	0	OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	0	0	MASH_ORDER		
R45	1	1	0	OUTA_MUX		OUT_ISET		0	1	1	OUTB_PWR					
R46	0	0	0	0	0	1	1	1	1	1	1	1	1	1	OUTB_MUX	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Field Descriptions

Location	Field	Type	Reset	Description
R34[2:0] R36[15:0]	PLL_N	R/W	100	The PLL_N divider value is in the feedback path and divides the VCO frequency.
R37[15]	MASH_SEED_EN	R/W	0	Enabling this bit allows the to be applied to shift the phase at the output or optimize spurs.
R37[13:8]	PFD_DLY_SEL	R/W	2	The PFD_DLY_SEL must be adjusted in accordance to the N-divider value. This is with the functional description for the N-divider.
R38[15:0] R39[15:0]	PLL_DEN	R/W	4294967295	The fractional denominator.
R40[15:0] R41[15:0]	MASH_SEED	R/W	0	The initial state of the MASH engine first accumulator. Can be used to shift phase or optimize fractional spurs. Every time the field is programmed, it ADDS this MASH seed to the existing one. To reset it, use the MASH_RESET_N bit.
R42[15:0] R43[15:0]	PLL_NUM	R/W	0	The fractional numerator
R44[13:8]	OUTA_PWR	R/W	31	Adjusts output power. Higher numbers give more output power to a point, depending on the pullup component used.
R44[7]	OUTB_PD	R/W	1	Powers down output B 0: Output B active 1: Output B powered down
R44[6]	OUTA_PD	R/W	0	Powers down output A 0: Output A Active 1: Output A powered down
R44[5]	MASH_RESET_N	R/W	1	Resets MASH circuitry to an initial state 0: MASH held in reset. All fractions are ignored 1: Fractional mode enabled. MASH is NOT held in reset.
R44[2:0]	MASH_ORDER	R/W	0	Sets the MASH order 0: Integer mode 1: First order modulator 2: Second order modulator 3: Third order modulator 4: Fourth order modulator 5-7: Reserved

Table 29. Field Descriptions (continued)

Location	Field	Type	Reset	Description
R45[12:11]	OUTA_MUX	R/W	1	Selects what signal goes to RFoutA 0: Channel divider 1: VCO 2: VCO2X (Also ensure VCO2X_EN=1) 3: High impedance
R45[10:9]	OUT_ISET	R/W	0	Setting to a lower value allows slightly higher output power at higher frequencies at the expense of higher current consumption. 0: Maximum output power boost ... 3: No output power boost
R45[5:0]	OUTB_PWR	R/W	31	Output power setting for RFoutB.
R46[1:0]	OUTB_MUX	R/W	1	Selects what signal goes to RFoutB 0: Channel divider 1: VCO 2: SysRef (also ensure SYSREF_EN=1) 3: High impedance

7.6.6 SYNC and SysRefReq Input Pin Register

Figure 46. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R58	INPIN_IGNORE	INPIN_HYST	INPIN_LVL		INPIN_FMT			0	0	0	0	0	0	0	0	1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Field Descriptions

Location	Field	Type	Reset	Description
R58[15]	INPIN_IGNORE	R/W	1	Ignore SYNC and SysRefReq Pins 0: Pins are used. Only valid for VCO_PHASE_SYNC = 1 1: Pin is ignored
R58[14]	INPIN_HYST	R/W	0	High Hysteresis for LVDS mode 0: Disabled 1: Enabled
R58[13:12]	INPIN_LVL	R/W	0	Sets bias level for LVDS mode. In LVDS mode, a voltage divider can be inserted to reduce susceptibility to common-mode noise of an LVDS line because the input is single-ended. With a reasonable setup, TI recommends using INPIN_LVL = 1 (Vin) to use the entire signal swing of an LVDS line. 0: Vin/4 1: Vin 2: Vin/2 3: Invalid
R58[11:9]	INPIN_FMT	R/W	0	0: SYNC = SysRefReq = CMOS 1: SYNC = LVDS, SysRefReq=CMOS 2: SYNC = CMOS, SysRefReq = LVDS 3: SYNC = SysRefReq = LVDS 4: Invalid 5: Invalid 6: Invalid 7: Invalid

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7.6.7 Lock Detect Registers

Figure 47. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R59	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_TYPE
R60	LD_DLY															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Field Descriptions

Location	Field	Type	Reset	Description
R59[0]	LD_TYPE	R/W	1	Lock detect type 0: VCO calibration status 1: VCO calibration status and Indirect Vtune
R60[15:0]	LD_DLY	R/W	1000	Lock Detect Delay. This is the delay added to the lock detect after the VCO calibration is successful and before the lock detect is asserted high. The delay added is in phase-detector cycles. If set to 0, the lock detect immediately becomes high after the VCO calibration is successful.

7.6.8 MASH_RESET

Figure 48. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R69	MASH_RST_COUNT[31:16]															
R70	MASH_RST_COUNT[15:0]															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Field Descriptions

Location	Field	Type	Reset	Description
R69[15:0] R70[15:0]	MASH_RST_COUNT	R/W	50000	If the designer does not use this device in fractional mode with VCO_PHASE_SYNC = 1, then this field can be set to 0. In phase-sync mode with fractions, this bit is used so that there is a delay for the VCO divider after the MASH is reset. This delay must be set to greater than the lock time of the PLL. It does impact the latency time of the SYNC feature.

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7.6.9 SysREF Registers

Figure 49. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R71	0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	0	1
R72	0	0	0	0	0	SYSREF_DIV										
R73	0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL					
R74	SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Field Descriptions

Location	Field	Type	Reset	Description
R71[7:5]	SYSREF_DIV_PRE	R/W	4	Pre-divider for SYSREF 1: Divide by 1 2: Divide by 2 4: Divide by 4 All other states: invalid
R71[4]	SYSREF_PULSE	R/W	0	Enable pulser mode in master mode 0: Disabled 1: Enabled
R71[3]	SYSREF_EN	R/W	0	Enable SYSREF
R71[2]	SYSREF_REPEAT	R/W	0	Enable repeater mode 0: Master mode 1: Repeater mode
R72[10:0]	SYSREF_DIV	R/W	0	Divider for the SYSREF 0: Divide by 4 1: Divide by 6 2: Divide by 8 ... 2047: Divide by 4098
R73[5:0]	JESD_DAC1_CTRL	R/W	63	These are the adjustments for the delay for the SYSREF. Two of these must be zero and the other two values must sum to 63.
R73[11:6]	JESD_DAC2_CTRL	R/W	0	
R74[5:0]	JESD_DAC3_CTRL	R/W	0	
R74[11:6]	JESD_DAC4_CTRL	R/W	0	
R74[15:12]	SYSREF_PULSE_CNT	R/W	0	Number of pulses in pulse mode in master mode

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7.6.10 CHANNEL Divider And VCO Doubler Registers

Figure 50. Registers Excluding Address

Reg	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R25	DBLR_IBIAS_CTRL1															
R27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	VCO2X_EN
R31	0	CHDIV_DIV2	0	0	0	0	1	1	1	1	1	0	1	1	0	0
R75	0	0	0	0	1	CHDIV					0	0	0	0	0	0

Table 34. Field Descriptions

Location	Field	Type	Reset	Description
R25[15:0]	DBLR_IBIAS_CTRL1	R/W	0x0624	VCO doubler current bias control. This value was originally set to 1572 (0x0624). There is no problem with the original value, but setting this to 3115 (0x0C2B) can yield better output power, and 1/2 harmonic and noise floor. This register affects only the doubler, and frequency outputs below 15 GHz are not influenced.
R27[0]	VCO2X_EN	R/W	0	VCO doubler 0: Disabled 1: Enabled
R31[14]	SEG1_EN	R/W	0	Enable driver buffer for CHDIV > 2 0: Disabled (only valid for CHDIV = 2) 1: Enabled (use for CHDIV > 2)
R75[10:6]	CHDIV	R/W	0	VCO divider value 0: 2 1: 4 2: 6 3: 8 4: 12 5: 16 6: 24 7: 32 8: 48 9: 64 10: 72 11: 96 12: 128 13: 192 14: 256 15: 384 16: 512 17: 768 18-31: Reserved

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7.6.11 Ramping and Calibration Fields

Figure 51. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R78	0	0	0	0	RAMP_THRESH[32]	0	QUICK_RECAL_EN	VCO_CAPCTRL_STRT								1
R79	RAMP_THRESH[31:16]															
R80	RAMP_THRESH[15:0]															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Field Descriptions

Location	Field	Type	Reset	Description
R78[11] R79[15:0] R80[15:0]	RAMP_THRESH	R/W	0	This sets how much the ramp can change the VCO frequency before calibrating. If this frequency is chosen to be Δf, then it is calculated as follows: RAMP_THRESH = $(\Delta f / f_{PD}) \times 16777216$
R78[9]	QUICK_RECAL_EN	R/W	0	Causes the initial VCO_CORE, VCO_CAPCTRL, and VCO_DACISET to be based on the last value. Useful if the frequency change is small, as is often the case for ramping. 0: Disabled 1: Enabled
R78[8:1]	VCO_CAPCTRL_STRT	R/W	0	This sets the initial value for VCO_CAPCTRL if not overridden by other settings. Smaller values yield a higher frequency band within a VCO core. Valid number range is 0 to 183.

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7.6.12 Ramping Registers

These registers are only relevant for ramping functions and are enabled if and only if RAMP_EN (R0[15]) = 1.

7.6.12.1 Ramp Limits

Figure 52. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R81	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_HIGH[32]
R82	RAMP_LIMIT_HIGH[31:16]															
R83	RAMP_LIMIT_HIGH[15:0]															
R84	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_LOW[32]
R85	RAMP_LIMIT_LOW[31:16]															
R86	RAMP_LIMIT_LOW[15:0]															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Field Descriptions

Location	Field	Type	Reset	Description
R81[0] R82[15:0] R83[15:0]	RAMP_LIMIT_HIGH	R/W	0	This sets a maximum frequency that the ramp can not exceed so that the VCO does not get set beyond a valid frequency range. Suppose f_{HIGH} is this frequency and f_{VCO} is the starting VCO frequency then: For $f_{HIGH} \geq f_{VCO}$: RAMP_LIMIT_HIGH = $(f_{HIGH} – f_{VCO})/f_{PD} \times 16777216$ For $f_{HIGH} < f_{VCO}$ this is not a valid condition to choose.
R84[0] R85[15:0] R86[15:0]	RAMP_LIMIT_LOW	R/W	0	This sets a minimum frequency that the ramp can not exceed so that the VCO does not get set beyond a valid frequency range. Suppose f_{LOW} is this frequency and f_{VCO} is the starting VCO frequency then: For $f_{LOW} \leq f_{VCO}$: RAMP_LIMIT_LOW = $2^{33} – 16777216 \times (f_{VCO} – f_{LOW}) / f_{PD}$ For $f_{LOW} > f_{VCO}$, this is not a valid condition to choose.

7.6.12.2 Ramping Triggers, Burst Mode, and RAMP0_RST

Figure 53. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R96	RAMP_BURST_EN	RAMP_BURST_COUNT													0	0
R97	RAMP0_RST	0	0	0	1	RAMP_TRIGB				RAMP_TRIGA				0	RAMP_BURST_TRIG	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. Field Descriptions

Location	Field	Type	Reset	Description
R96[15]	RAMP_BURST_EN	R/W	0	Enables burst ramping mode. In this mode, a RAMP_BURST_COUNT ramps are sent out when RAMP_EN is set from 0 to 1. 0: Disabled 1: Enabled
RAMP96[14:2]	RAMP_BURST_COUNT	R/W	0	Sets how many ramps are run in burst ramping mode.
R97[15]	RAMP0_RST	R/W	0	Resets RAMP0 at start of ramp to eliminate round-off errors. Must only be used in automatic ramping mode. 0: Disabled 1: Enabled
R97[6:3]	RAMP_TRIGA	R/W	0	Multipurpose Trigger A definition: 0: Disabled 1: RampClk pin rising edge 2: RampDir pin rising edge 4: Always triggered 9: RampClk pin falling edge 10: RampDir pin falling edge All other states: reserved
R97[10:7]	RAMP_TRIGB	R/W	0	Multipurpose trigger B definition: 0: Disabled 1: RampClk pin Rising Edge 2: RampDir pin Rising Edge 4: Always Triggered 9: RampClk pin Falling Edge 10: RampDir pin Falling Edge All other states: Reserved
R97[1:0]	RAMP_BURST_TRIG	R/W	0	Ramp burst trigger definition that triggers the next ramp in the count. Note that RAMP_EN starts the count, not this word. 0: Ramp Transition 1: Trigger A 2: Trigger B 3: Reserved

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7.6.12.3 Ramping Configuration

Figure 54. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R98	RAMP0_INC[29:16]														0	RAMP0_DLY
R99	RAMP0_INC[15:0]															
R100	RAMP0_LEN															
R101	0	0	0	0	0	0	0	0	0	RAMP1_DLY	RAMP1_RST	RAMP0_NEXT	0	0	RAMP0_NEXT_TRIG	
R102	0	0	RAMP1_INC[29:16]													
R103	RAMP1_INC[15:0]															
R104	RAMP1_LEN															
R105	RAMP_DLY_CNT										RAMP_MANUAL	RAMP1_NEXT	0	0	RAMP1_NEXT_TRIG	
R106	0	0	0	0	0	0	0	0	0	0	0	RAMP_TRIG_CAL	0	RAMP_SCALE_COUNT		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. Field Descriptions

Location	Field	Type	Reset	Description
R98[15:2] R99[15:0]	RAMP0_INC	R/W	0	2's complement of the amount the RAMP0 is incremented in phase detector cycles.
R98[0]	RAMP0_DLY	R/W	0	Enabling this bit uses two clocks instead of one to clock the ramp. Effectively doubling the length. 0: Normal ramp length 1: Double ramp length
R100[15:0]	RAMP0_LEN	R/W	0	Length of RAMP0 in phase detector cycles
R101[6]	RAMP1_DLY	R/W	0	Enabling this bit uses two clocks instead of one to clock the ramp. Effectively doubling the length. 0: Normal ramp length 1: Double ramp length
R101[5]	RAMP1_RST	R/W	0	Resets RAMP1 to eliminate rounding errors. Must be used in automatic ramping mode. 0: Disabled 1: Enabled
R101[4]	RAMP0_NEXT	R/W	0	Defines what ramp comes after RAMP0 0: RAMP0 1: RAMP1
R101[1:0]	RAMP0_NEXT_TRIG	R/W	0	Defines what triggers the next ramp 0: RAMP0_LEN timeout counter 1: Trigger A 2: Trigger B 3: Reserved
R102[13:0] R103[15:0]	RAMP1_INC	R/W	0	2's complement of the amount the RAMP1 is incremented in phase detector cycles.
R104[15:0]	RAMP1_LEN	R/W	0	Length of RAMP1 in phase detector cycles
R105[15:6]	RAMP_DLY_CNT	R/W	0	This is the number of state machine clock cycles for the VCO calibration in automatic mode. If the VCO calibration is less, then it is this time. If it is more, then the time is the VCO calibration time.
R105[5]	RAMP_MANUAL	R/W	0	Enables manual ramping mode, or otherwise automatic mode 0: Automatic ramping mode 1: Manual ramping mode

Table 38. Field Descriptions (continued)

Location	Field	Type	Reset	Description
R105[4]	RAMP1_NEXT	R/W	0	Determines what ramp comes after RAMP1: 0: RAMP0 1: RAMP1
R105[1:0]	RAMP1_NEXT_TRIG	R/W	0	Defines what triggers the next ramp 0: RAMP1_LEN timeout counter 1: Trigger A 2: Trigger B 3: Reserved
R106[4]	RAMP_TRIG_CAL	R/W	0	Enabling this bit forces the VCO to calibrate after the ramp.
R106[2:0]	RAMP_SCALE_COUNT	R/W	7	Multiplies RAMP_DLY count by $2^{RAMP_SCALE_COUNT}$

7.6.13 Readback Registers

Figure 55. Registers Excluding Address

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R110	0	0	0	0	0	rb_LD_VTUNE		0	rb_VCO_SEL			0	0	0	0	0
R111	0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL							
R112	0	0	0	0	0	0	0	rb_VCO_DACISET								

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. Field Descriptions

Location	Field	Type	Reset	Description
R110[10:9]	rb_LD_VTUNE	R	0	Readback of Vtune lock detect 0: Unlocked (Vtune low) 1: Invalid State 2: Locked 3: Unlocked (Vtune High)
R110[7:5]	rb_VCO_SEL	R	0	Reads back the actual VCO that the calibration has selected. 0: Invalid 1: VCO1 ... 7: VCO7
R111[7:0]	rb_VCO_CAPCTRL	R	183	Reads back the actual CAPCTRL capcode value the VCO calibration has chosen.
R112[8:0]	rb_VCO_DACISET	R	170	Reads back the actual amplitude (DACISET) value that the VCO calibration has chosen.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 OSCin Configuration

The OSCin supports single-ended or differential clocks. There must be a AC-coupling capacitor in series before the device pin. The OSCin inputs are high-impedance CMOS with internal bias voltage. TI recommends putting termination shunt resistors to terminate the differential traces (if there are 50-Ω characteristic traces, place 50-Ω resistors). The OSCin and OSCin* side should be matched in layout. A series AC-coupling capacitors should immediately follow OSCin pins in the board layout, then the shunt termination resistors to ground should be placed after.

Input clock definitions are shown in Figure 56:

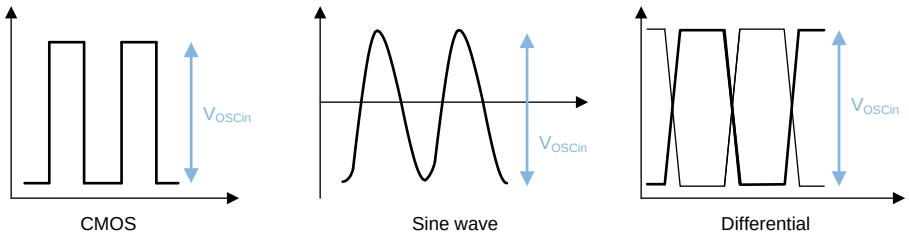

Figure 56. Input Clock Definitions

8.1.2 OSCin Slew Rate

The slew rate of the OSCin signal can impact the spurs and phase noise of the LMX2595 if it is too low. In general, a high slew rate and a lower amplitude signal, such as LVDS, can give best performance.

8.1.3 RF Output Buffer Power Control

The OUTA_PWR and OUTB_PWR registers can be used to control the output power of the output buffers. The setting for optimal power may depend on the pullup component, but is typically around 50. The higher the setting, the higher the current consumption of the output buffer.

8.1.4 RF Output Buffer Pullup

The choice of output buffer components is very important and can have a profound impact on the output power. Table 40 shows how to treat each pin. If using a single-ended output, a pullup is required, and the user can put a 50-Ω resistor after the capacitor.

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Application Information (continued)

Table 40. Different Methods for Pullup on Outputs

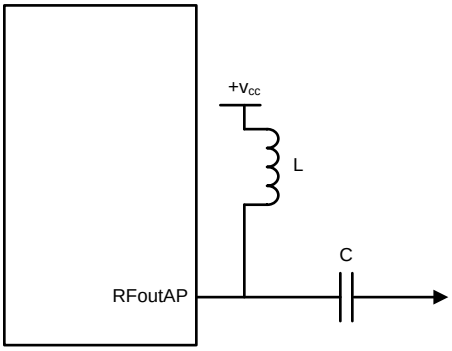
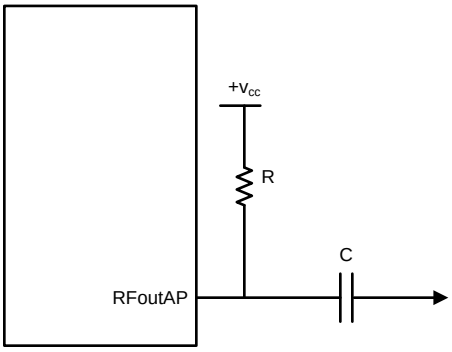
PULLUP STYLE	DIAGRAM	COMMENTS
Inductor		Potentially higher output power, but output impedance is far from 50 Ω. Consider also using with a resistive pad.
Resistor		More consistent matching

Table 41. Output Pullup Configuration

COMPONENT	VALUE	PART NUMBER
Inductor	Varies with frequency	
Resistor	50 Ω	Vishay FC0402E50R0BST1
Capacitor	Varies with frequency	ATC 520L103KT16T ATC 504L50R0FTNCFT

8.1.5 Performance Comparison Between 1572 (0x0624) and 3115 (0x0C2B) for Register DBLR_IBIAS_CTRL1 (R25[15:0])

There is a new setting for register DBLR_IBIAS_CTRL1 (R25[15:0]): from 1572 (0x0624) to 3115 (0x0C2B). The old setting can operate up to 19-GHz output, but the new setting can extend the frequency range to 20 GHz. The field name DBLR_IBIAS_CTRL1 is short for "Doubler Current Bias Control 1". It only impacts the doubler and does not affect the performance below 15 GHz. Shown in Figure 57 and Figure 58, with old R25 value, the output power and phase noise floor fall apart beyond 19 GHz. But with the new setting, they remain stable up to 20 GHz. Figure 59 and Figure 60 show that new R25 value leads to less output power variation with temperature at high frequencies. Figure 61 shows the improvement in half harmonic.

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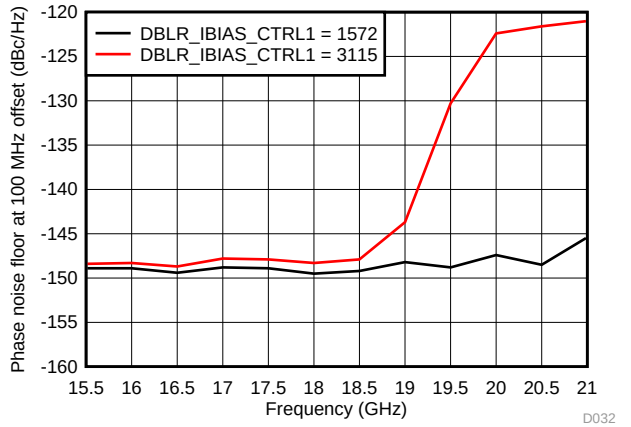
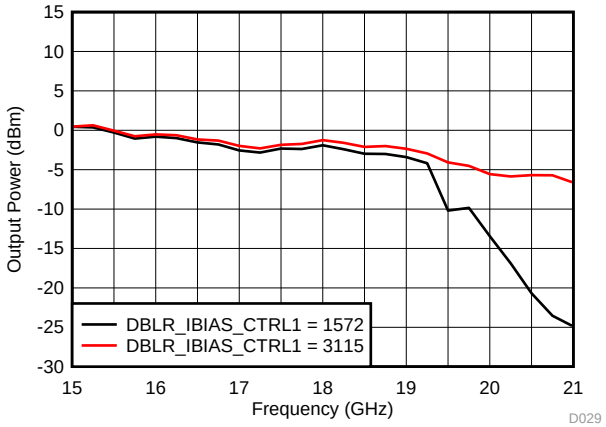


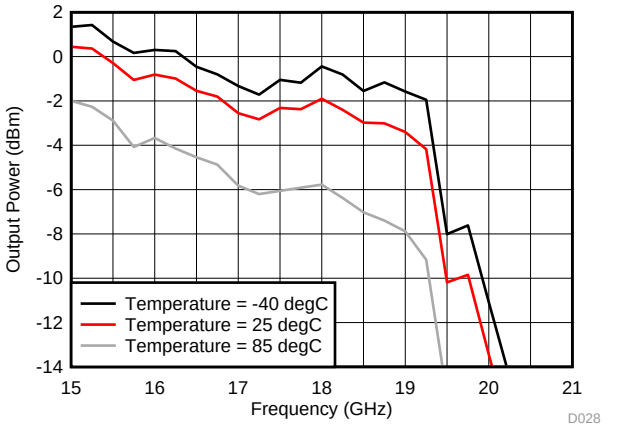
OUTA_PWR = 20 Single-ended output

Figure 57. Phase Noise Floor Across Frequency: DBLR_IBIAS_CTRL1 (R25[15:0]) Value Old vs New



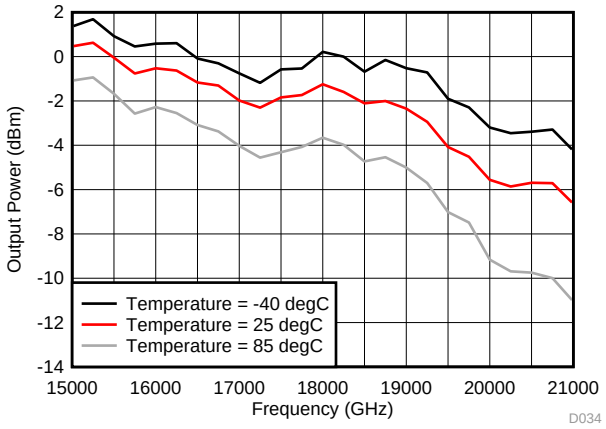
OUTA_PWR = 20 Single-ended output

Figure 58. Output Power Across Frequency: DBLR_IBIAS_CTRL1 (R25[15:0]) Value Old vs New



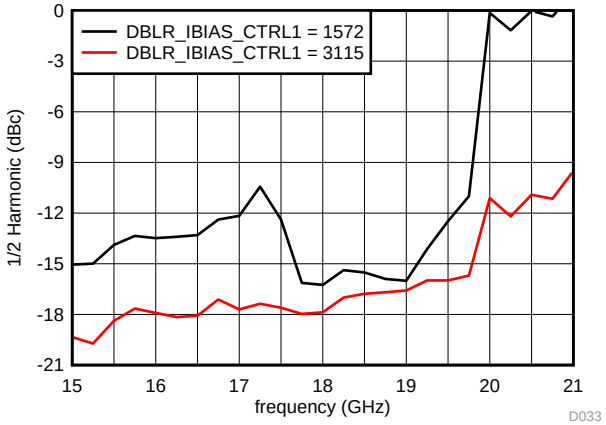
OUTA_PWR = 20 Single-ended output

Figure 59. Output Power Variation Versus Temperature: DBLR_IBIAS_CTRL1 = 1572



OUTA_PWR = 20 Single-ended output

Figure 60. Output Power Variation Versus Temperature: DBLR_IBIAS_CTRL1 = 3115



OUTA_PWR = 20 Single-ended output

Figure 61. 1/2 Harmonic Across Frequency: DBLR_IBIAS_CTRL1 (R25[15:0]) Value Old vs New

8.2 Typical Application

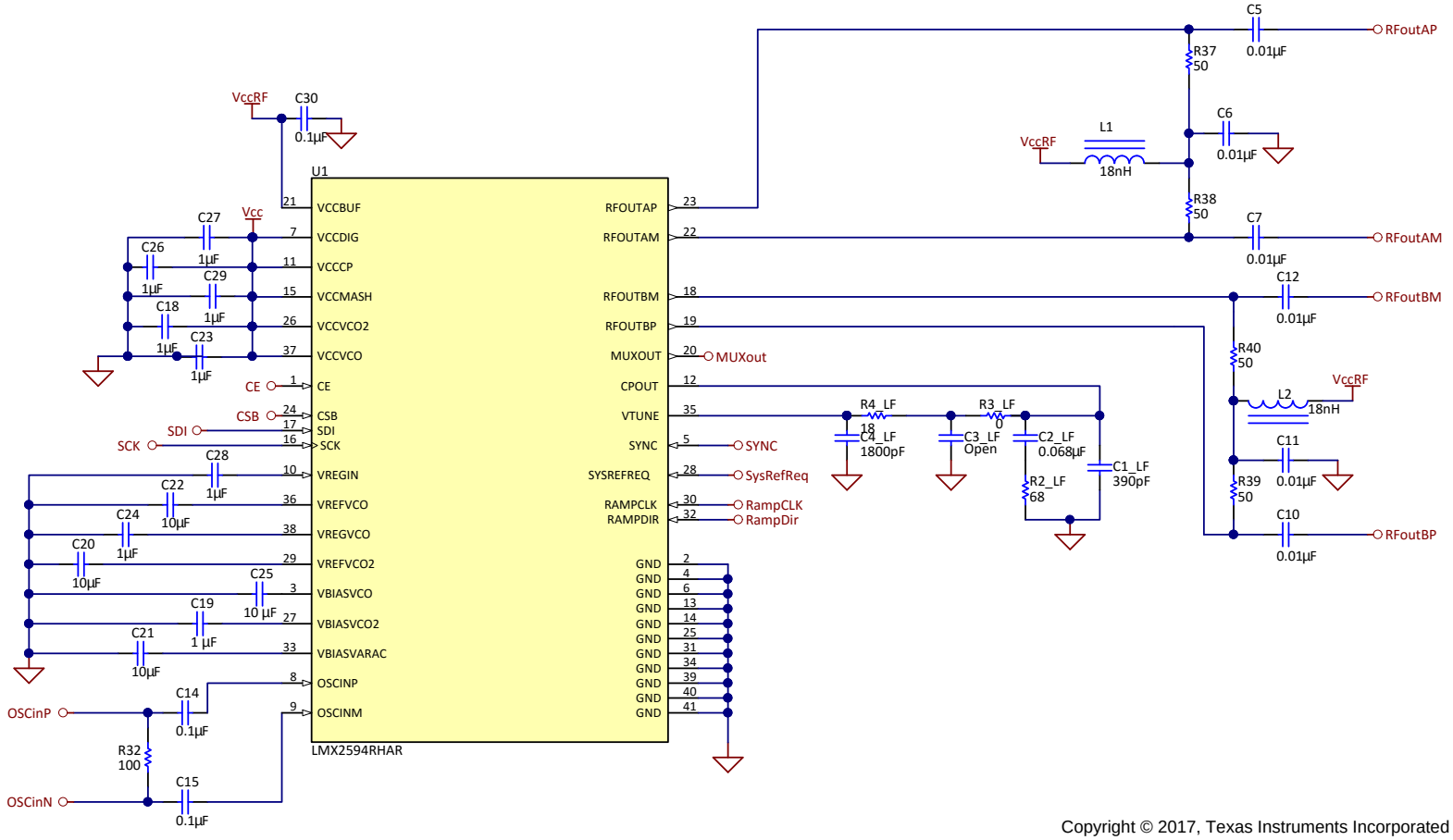


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Figure 62. Typical Application Schematic

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8.2.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLATINUM™ Sim software is an excellent resource for doing this and the design is shown in the Figure 63. For those interested in the equations involved, the *PLL Performance, Simulation, and Design Handbook* listed in the end of this document goes into great detail as to the theory and design of PLL loop filters.

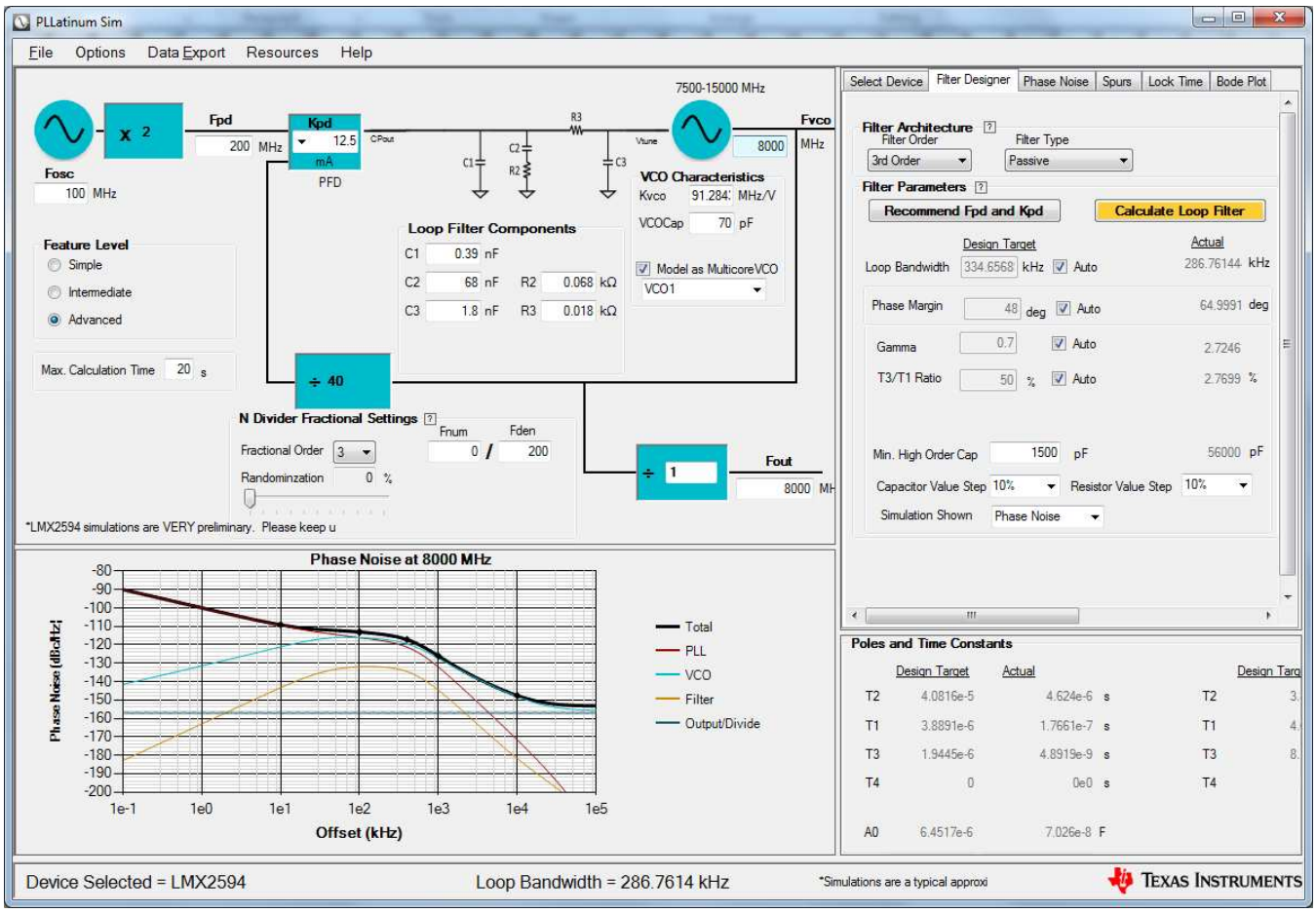

Figure 63. PLLATINUM™ Sim Design Screen

8.2.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. Generally, jitter is lowest if the loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this is that longer lock times and spurs must be considered in design as well.

8.2.3 Application Curve

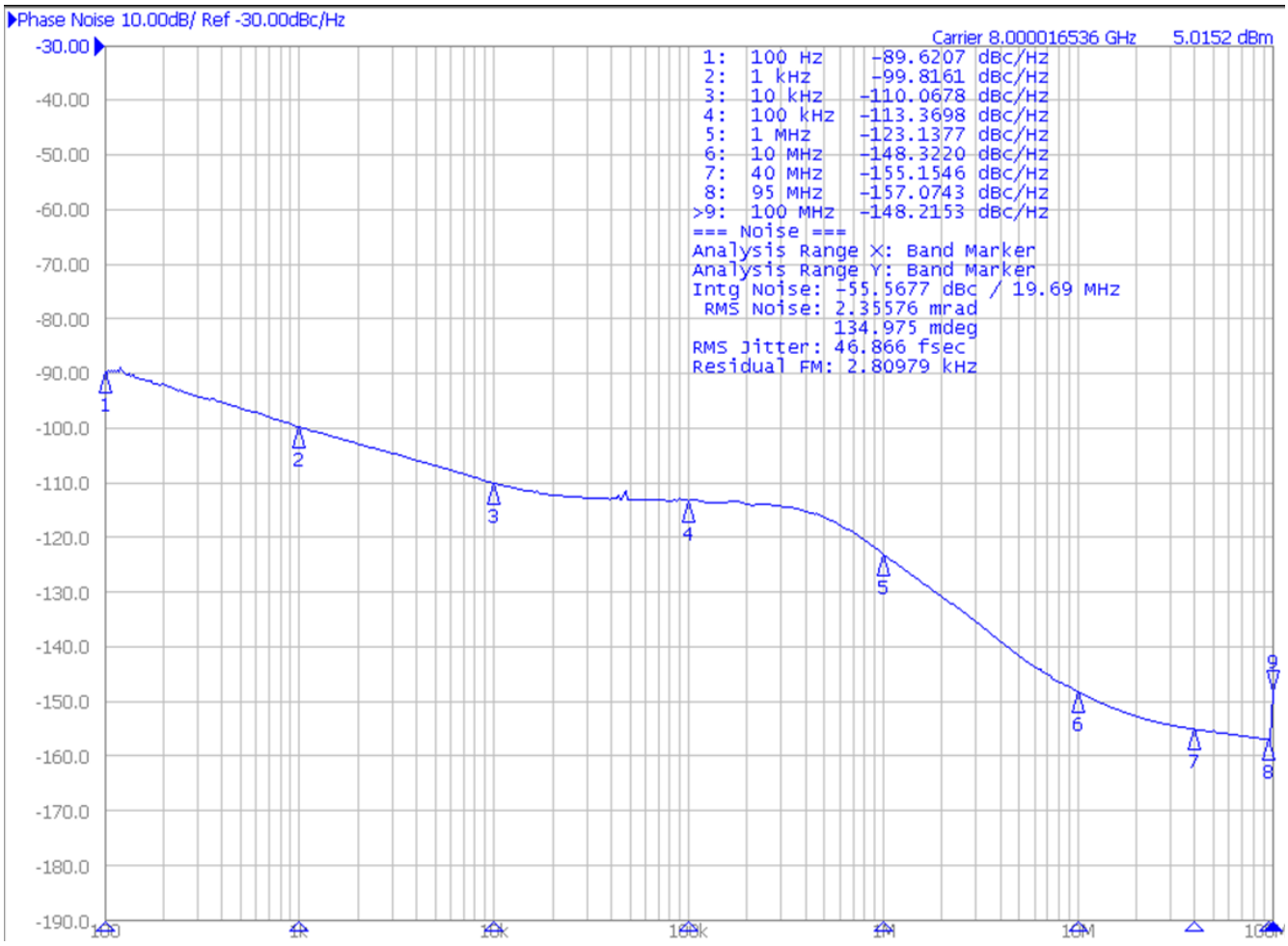

Figure 64. Typical Jitter

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9 Power Supply Recommendations

If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise. However, the pullup components on the RFoutA and RFoutB pins on the outputs have a direct connection to the power supply, take extra care to ensure that the voltage is clean for these pins. *Figure 65* is a typical application example.

This device can be powered by an external DC-DC buck converter, such as the TPS62150. Note that although Rtps, Rtps1, and Rtps2 are 0 Ω in the schematic, they could be potentially replaced with a larger resistor value or inductor value for better power supply filtering.

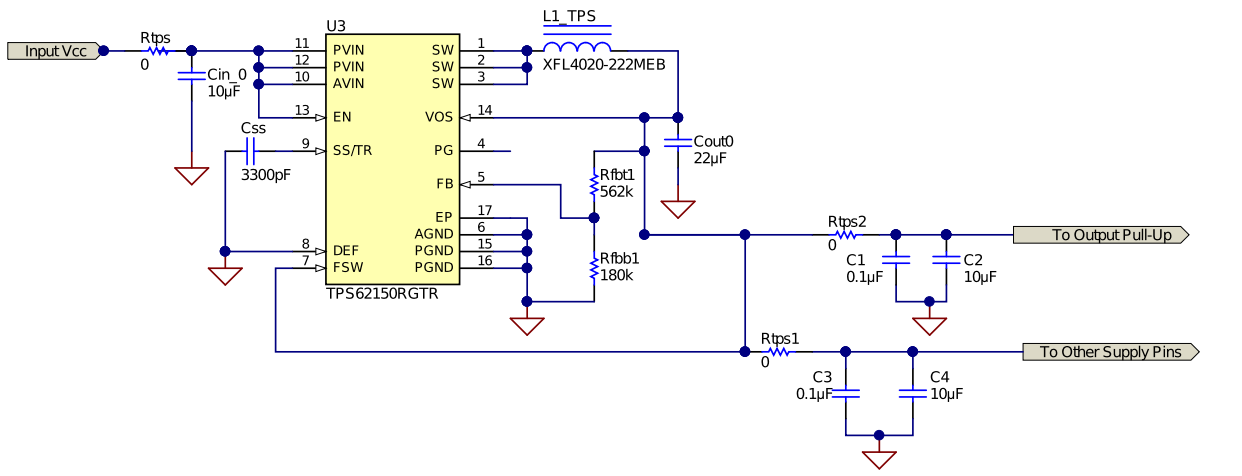

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Figure 65. Using the TPS62150 as a Power Supply

For DC bias levels, refer to .

Table 42. Bias Levels of Pins

Pin Number	Pin Name	Bias Level (1)
3	VBIASVCO	1.3
27	VBIASVCO2	0.7
29	VREFVCO2	2.9
33	VBIASVARAC	1.7
36	VREFVCO	2.9
38	VREGVCO	2.1

(1) The bias level is measured after following Recommended Initial Power-Up Sequence.

10 Layout

10.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines.

- GND pins may be routed on the package back to the DAP.
- The OSCin pins are internally biased and must be AC-coupled.
- If not used, RampClk, RampDir, and SysRefReq can be grounded to the DAP.
- For the Vtune pin, try to place a loop filter capacitor as close as possible to the pin. This may mean separating the capacitor from the rest of the loop filter.
- For the outputs, keep the pullup component as close as possible to the pin and use the same component on each side of the differential pair.
- If a single-ended output is needed, the other side must have the same loading and pullup. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, use the same pullup and make the load look equivalent to the side that is used.
- Ensure that DAP on device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the LMX2595 exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, such as Rogers 4003, for optimal output power.
- See instructions for the LMX2595EVM (*LMX2594 EVM Instructions, 15 GHz Wideband Low Noise PLL With Integrated VCO*) for more details on layout.

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10.2 Layout Example

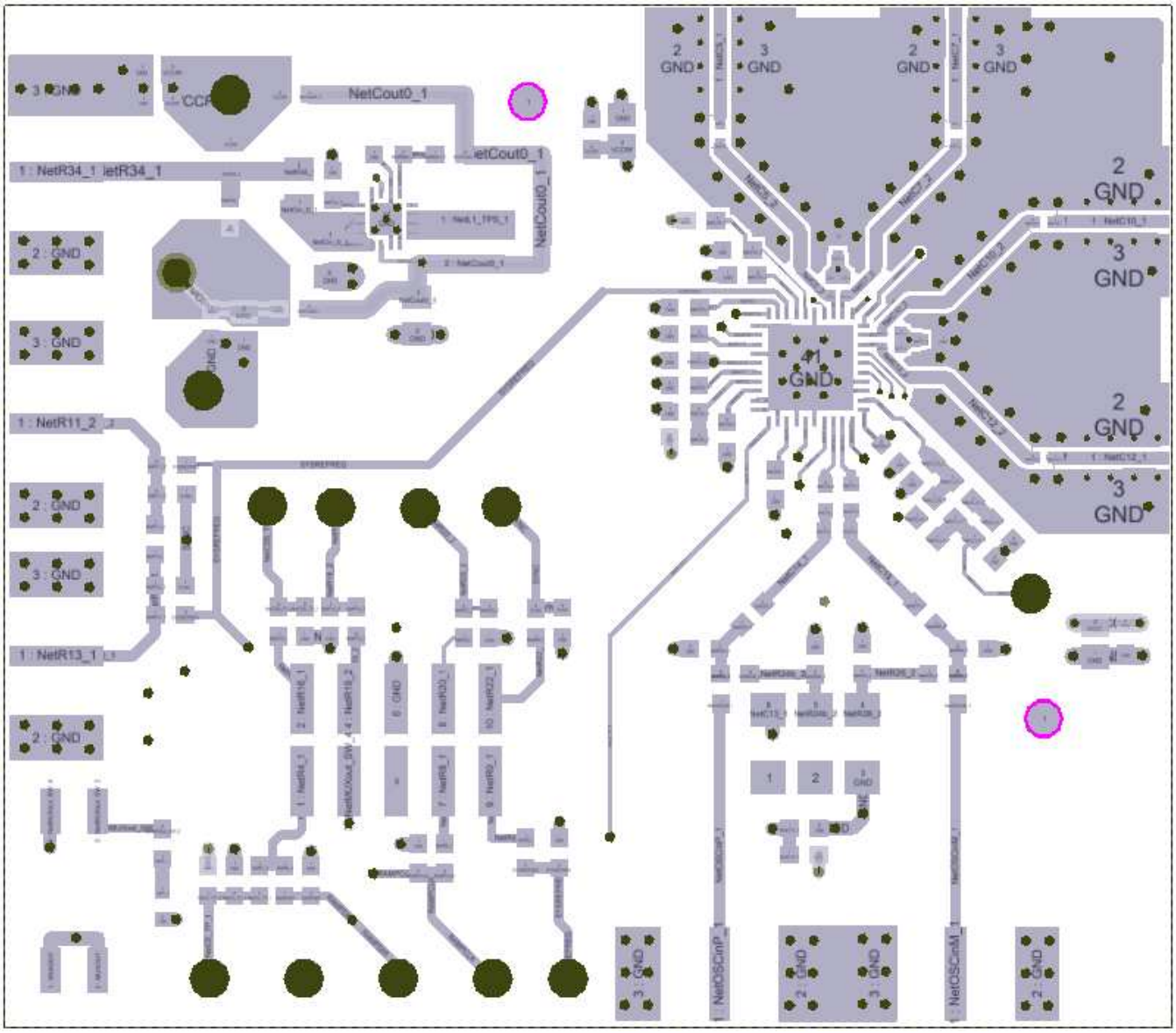

Figure 66. LMX2594 PCB Layout

11 器件和文档支持

11.1 器件支持

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- EVM 软件，用于了解如何对器件和 EVM 板进行编程。
- EVM 板说明，用于了解典型测量数据、详细测量条件以及完整设计的信息。
- PLLatinum Sim 程序，用于设计回路滤波器以及对相位噪声和杂散进行仿真。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *《AN-1879 分数 N 频率合成》*(SNAA062)
- *《PLL 性能、仿真和设计手册》*(SNAA106)
- *LMX2594 EVM 说明 - 带集成 VCO 的 15GHz 宽带低噪声 PLL* (SNAU210)

11.3 接收文档更新通知

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11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMX2595RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2595
LMX2595RHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2595
LMX2595RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2595
LMX2595RHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2595

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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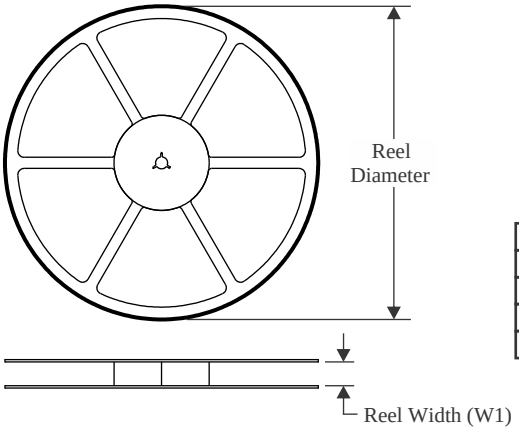
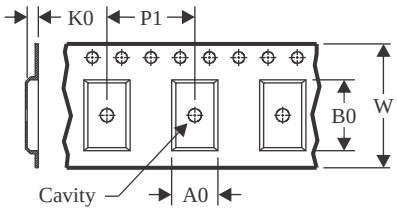
TAPE AND REEL INFORMATION

REEL DIMENSIONS

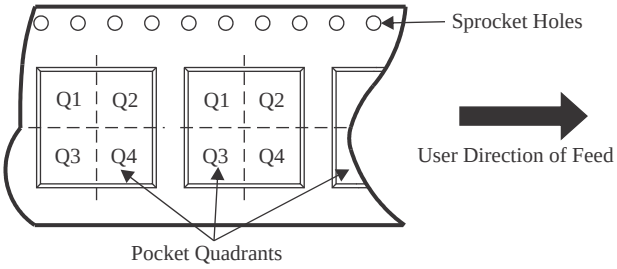


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

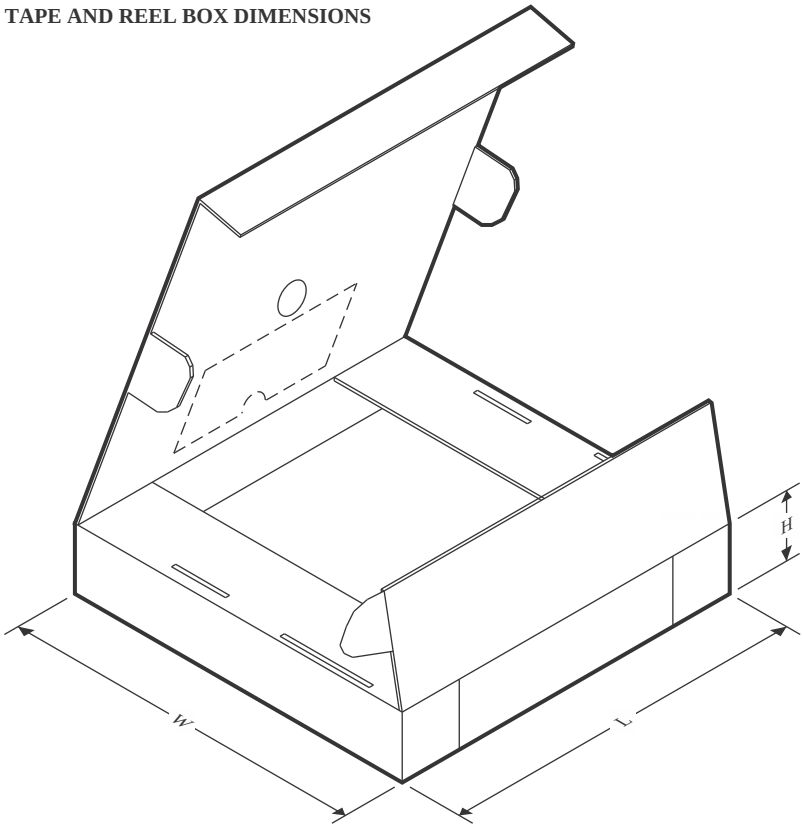
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2595RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMX2595RHAT	VQFN	RHA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2595RHAR	VQFN	RHA	40	2500	356.0	356.0	36.0
LMX2595RHAT	VQFN	RHA	40	250	208.0	191.0	35.0

GENERIC PACKAGE VIEW

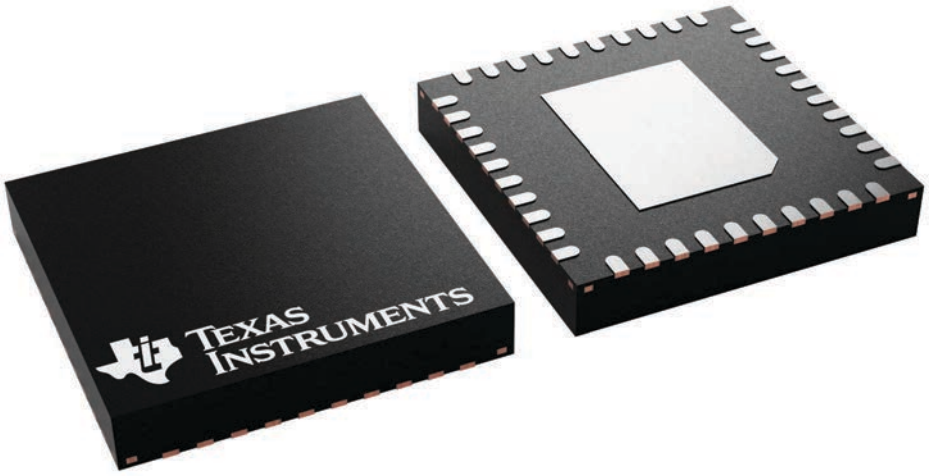
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

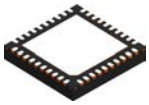
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

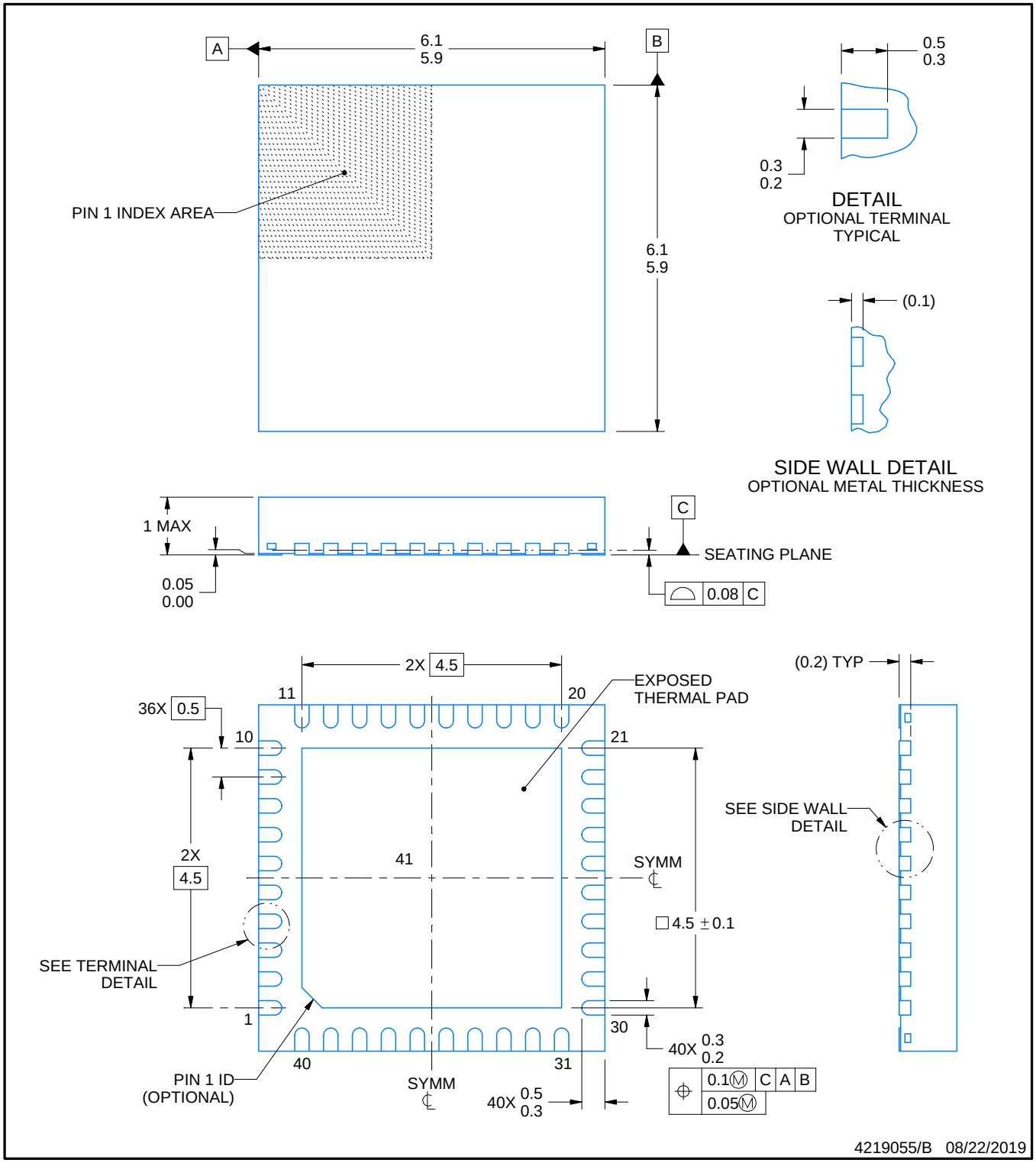
RHA0040H



PACKAGE OUTLINE

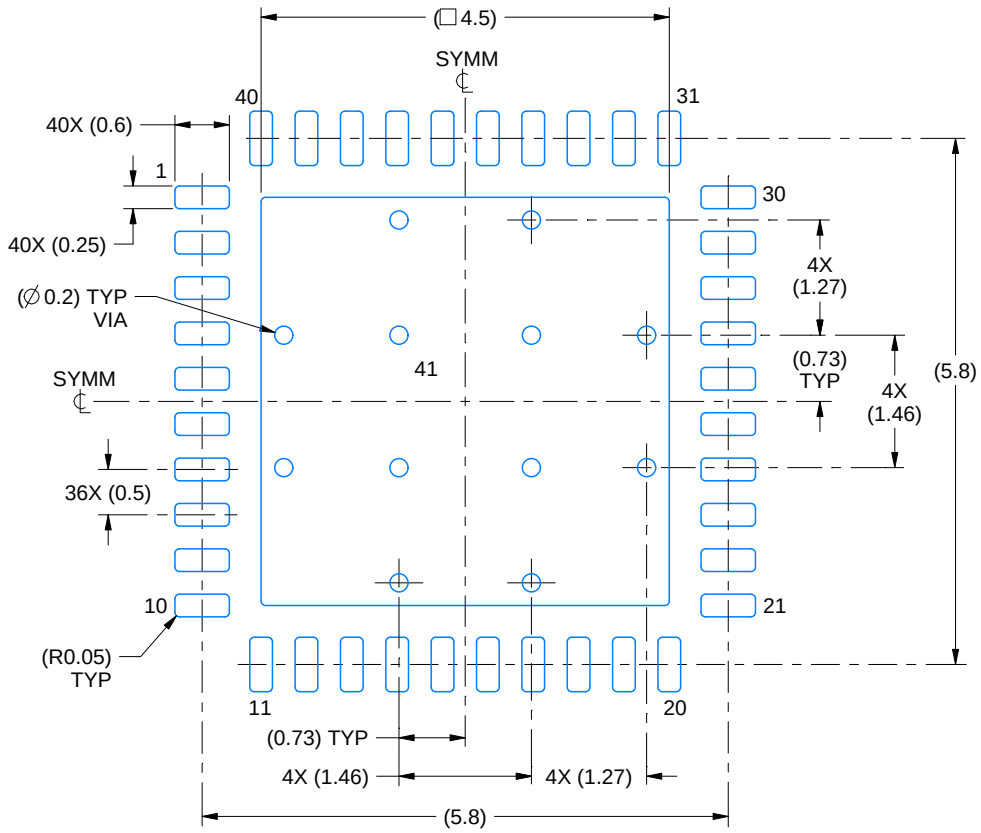
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

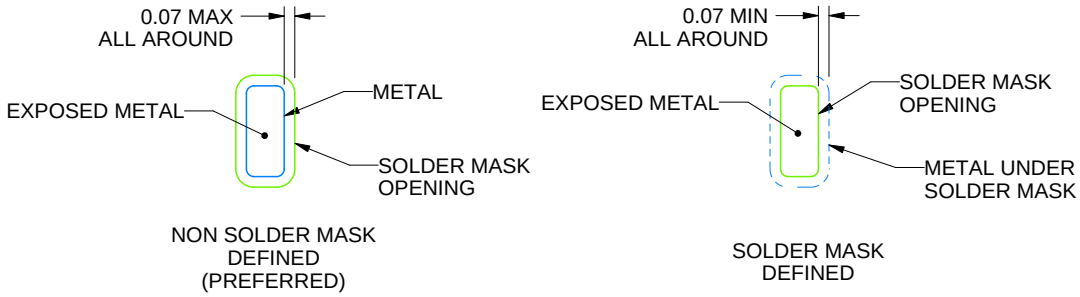


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

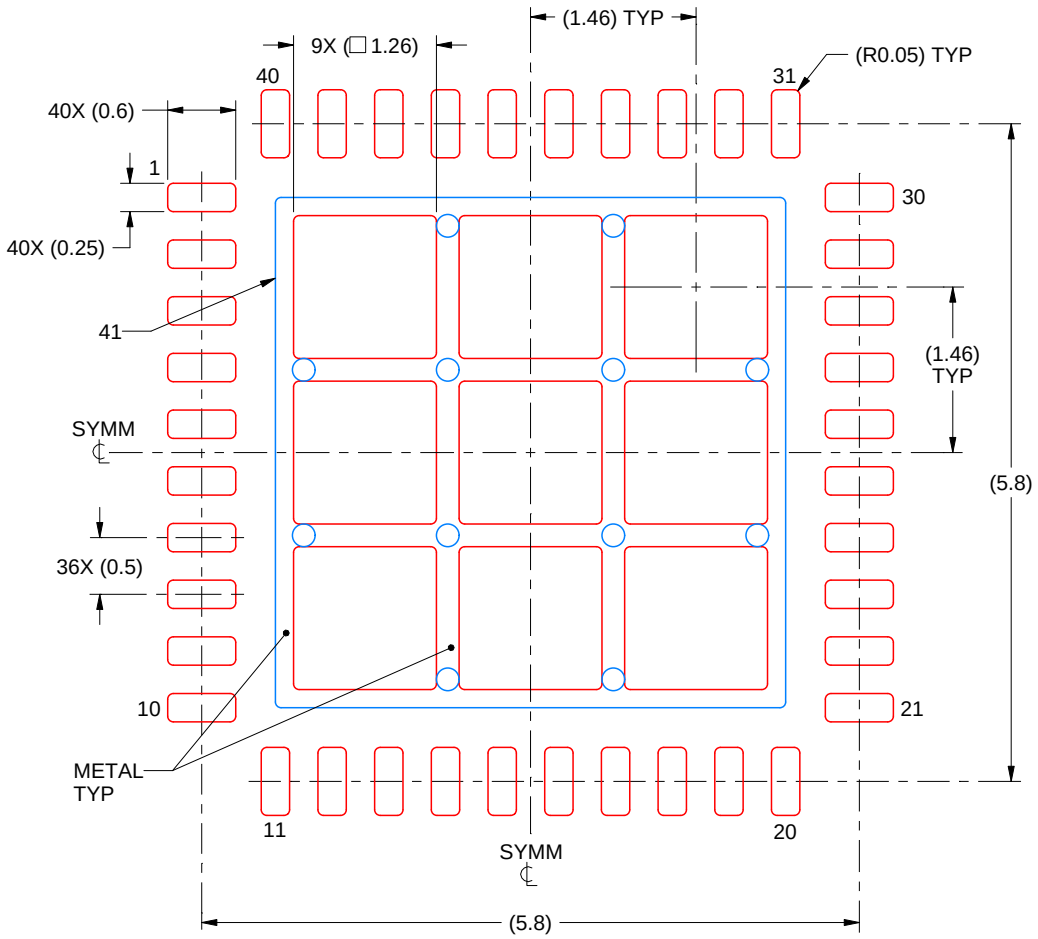


SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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