LMZ14201H SIMPLE SWITCHER® 6V 至 42V、1A 高输出电压电源模块

1 特性

- 集成屏蔽式电感器
- 简单的 PCB 布局
- 采用外部软启动和精密使能端实现灵活启动排序
- 防止浪涌电流
- 输入 UVLO 和输出短路保护
- -40°C 至 125°C 的结温范围
- 便于装配和制造的单个外露焊盘和标准引脚分配
- 低输出电压纹波
- 引脚对引脚兼容系列：
  - LMZ14203H/2H/1H（42V 最大 3A、2A、1A）
  - LMZ14203/2/1（42V 最大 3A、2A、1A）
  - LMZ12003/2/1（20V 最大 3A、2A、1A）
- 完全支持 WEBENCH® power designer
- 电气规范
  - 输出电流高达 1A
  - 输入电压范围：6V 至 42V
  - 输出电压低至 5V
  - 效率高达 97%
- 性能优势
  - 高效率有效降低系统产生的热量
  - 无需补偿
  - 低封装热阻
  - 低辐射 EMI（经 EN 55022 B 类标准测试）[1]

2 应用

- 中间总线转换为 12V 和 24V 电源轨
- 时间关键型项目
- 空间受限且散热要求较高的应用
- 负输出电压应用

3 描述

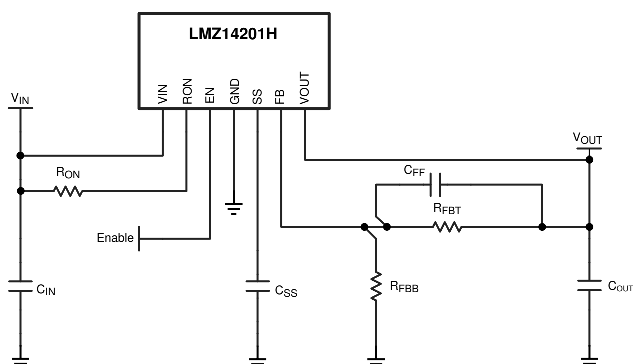
LMZ14201H SIMPLE SWITCHER® 电源模块是一款易于使用的降压直流/直流解决方案，可驱动高达 1A 的负载，并具有出色的电源转换效率、线路和负载调节以及输出精度。LMZ14201H 采用创新型封装，可提高热性能并支持手工或机器焊接。

LMZ14201H 支持 6V 至 42V 的输入电压轨范围，可提供低至 5V 的高精度可调节输出电压。LMZ14201H 仅需三个外部电阻和四个外部电容器即可完善电源解决方案。LMZ14201H 的设计可靠而稳健，并且具有以下保护特性：热关断、输入欠压锁定、输出过压保护、短路保护、输出限流以及预偏置输出的启动功能。单个电阻最高可将开关频率调节至 1MHz。

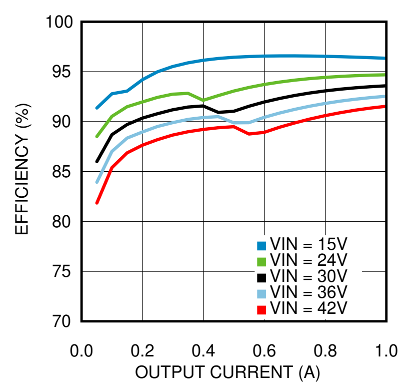
器件信息

器件型号(2)	封装(1)	封装尺寸（标称值）
LMZ14201H	TO-PMOD (7)	10.16mm × 9.85mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 峰值回流焊温度等于 245°C。请参阅 SNAA214 了解更多详细信息。



简化版应用原理图



效率 V_{OUT} = 12V，T_A = 25°C

[1] EN 55022:2006、+A1:2007、FCC 第 15 部分 B 子部分：2007。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (October 2015) to Revision I (August 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式。	1
• Updated 方程式 17	21

Changes from Revision G (August 2015) to Revision H (October 2015)	Page
• Added this new bullet in the Power Module SMT Guidelines section	23

5 Pin Configuration and Functions

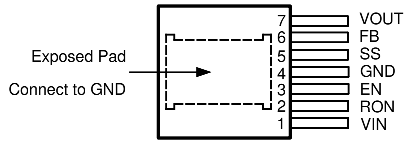


图 5-1. NDW Package 7-Pin TO-PMD (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN	Power	Supply input — Additional external input capacitance is required between this pin and the exposed pad (EP).
2	RON	Analog	ON-time resistor — An external resistor from V_{IN} to this pin sets the ON-time and frequency of the application. Typical values range from 100 kΩ to 700 kΩ.
3	EN	Analog	Enable — Input to the precision enable comparator. Rising threshold is 1.18 V.
4	GND	Ground	Ground — Reference point for all stated voltages. Must be externally connected to EP.
5	SS	Analog	Soft-Start — An internal 8 µA current source charges an external capacitor to produce the soft-start function.
6	FB	Analog	Feedback — Internally connected to the regulation, overvoltage, and short-circuit comparators. The regulation reference point is 0.8 V at this input pin. Connect the feedback resistor divider between the output and ground to set the output voltage.
7	VOUT	Power	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and the EP.
—	EP	Ground	Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)] [(3)]

	MIN	MAX	UNIT
VIN, RON to GND	–0.3	43.5	V
EN, FB, SS to GND	–0.3	7	V
Junction Temperature		150	°C
Peak Reflow Case Temperature (30 sec)		245	°C
Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications, refer to the following document: SNOA549

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{IN}	6	42	V
EN	0	6.5	V
Operation Junction Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]			LMZ14201H NDW (TO-PMD) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	4 layer printed-circuit-board, 7.62 cm x 7.62 cm (3 in x 3 in) area, 1 oz copper, no air flow	16	°C/W
		4 layer printed-circuit-board, 6.35 cm x 6.35 cm (2.5 in x 2.5 in) area, 1 oz copper, no air flow	18.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, V_{OUT} = 12 V, R_{ON} = 249 kΩ

PARAMETER		TEST CONDITIONS	MIN[(1)]	TYP[(2)]	MAX[(1)]	UNIT
SYSTEM PARAMETERS						
ENABLE CONTROL						
V_{EN}	EN threshold trip point	V_{EN} rising, T_J = –40°C to 125°C	1.10	1.18	1.25	V
V_{EN-HYS}	EN threshold hysteresis			90		mV
SOFT-START						
I_{SS}	SS source current	V_{SS} = 0 V, T_J = –40°C to 125°C	8	10	15	μA
I_{SS-DIS}	SS discharge current			–200		μA
CURRENT LIMIT						
I_{CL}	Current limit threshold	DC average, T_J = –40°C to 125°C	1.5	1.95	2.7	A
VIN UVLO						
VIN_{UVLO}	Input UVLO	EN pin floating V_{IN} rising		3.75		V
$VIN_{UVLO-HYST}$	Hysteresis	EN pin floating V_{IN} falling		130		mV
ON/OFF TIMER						
t_{ON-MIN}	ON timer minimum pulse width			150		ns
t_{OFF}	OFF timer pulse width			260		ns
REGULATION AND OVERVOLTAGE COMPARATOR						
V_{FB}	In-regulation feedback voltage	V_{IN} = 24 V, V_{OUT} = 12 V V_{SS} >+ 0.8 V T_J = –40°C to 125°C I_{OUT} = 10 mA to 1 A	0.782	0.803	0.822	V
		V_{IN} = 24 V, V_{OUT} = 12 V V_{SS} >+ 0.8 V T_J = 25°C I_{OUT} = 10 mA to 1 A	0.786	0.803	0.818	
V_{FB}	In-regulation feedback voltage	V_{IN} = 36 V, V_{OUT} = 24 V V_{SS} >+ 0.8 V T_J = –40°C to 125°C I_{OUT} = 10 mA to 1 A	0.780	0.803	0.823	V
		V_{IN} = 36 V, V_{OUT} = 24 V V_{SS} >+ 0.8 V T_J = 25°C I_{OUT} = 10 mA to 1 A	0.787	0.803	0.819	
V_{FB-OVP}	Feedback overvoltage protection threshold			0.92		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non-Switching Input Current	V_{FB}= 0.86 V		1		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0 V		25		μA
THERMAL CHARACTERISTICS						
T_{SD}	Thermal shutdown (rising)				165	°C
$T_{SD-HYST}$	Thermal shutdown hysteresis				15	°C
PERFORMANCE PARAMETERS						
ΔV_{OUT}	Output Voltage Ripple	V_{OUT} = 5 V, C_{OUT} = 100 μF 6.3 V X7R		8		mV_{PP}
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 16 V to 42 V, I_{OUT}= 1 A		0.01%		
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 24 V, I_{OUT}= 0 A to 1 A		1.5		mV/A

Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, V_{OUT} = 12 V, R_{ON} = 249 kΩ

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 0.5 A		94%		
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 1 A		92%		

(1) Minimum and Maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

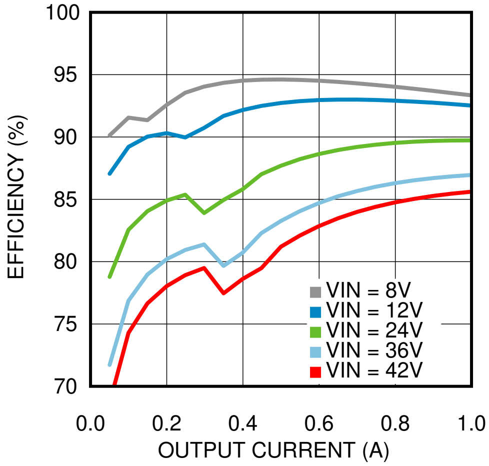


图 6-1. Efficiency V_{OUT} = 5 V, T_A = 25°C

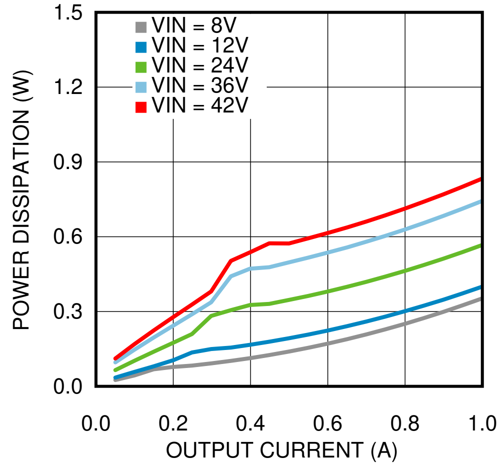


图 6-2. Power Dissipation V_{OUT} = 5 V, T_A = 25°C

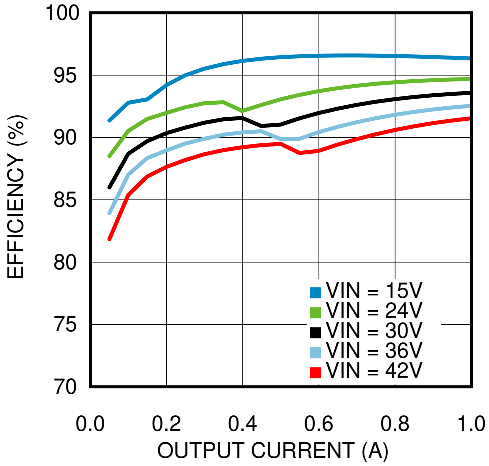


图 6-3. Efficiency V_{OUT} = 12 V, T_A = 25°C

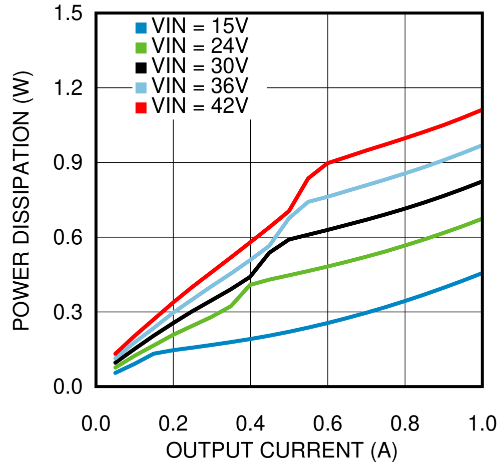


图 6-4. Power Dissipation V_{OUT} = 12 V, T_A = 25°C

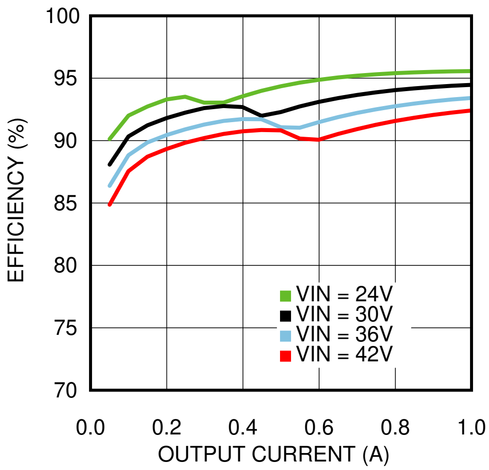


图 6-5. Efficiency V_{OUT} = 15 V, T_A = 25°C

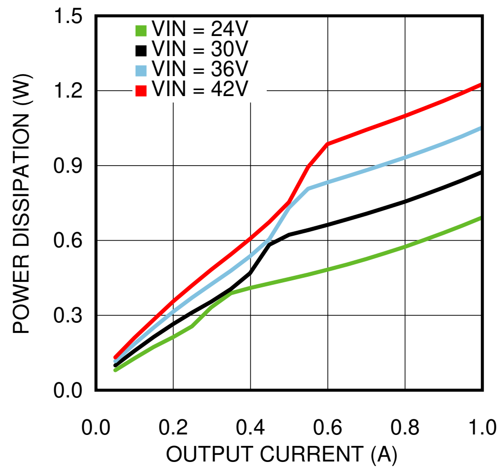


图 6-6. Power Dissipation V_{OUT} = 15 V, T_A = 25°C

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

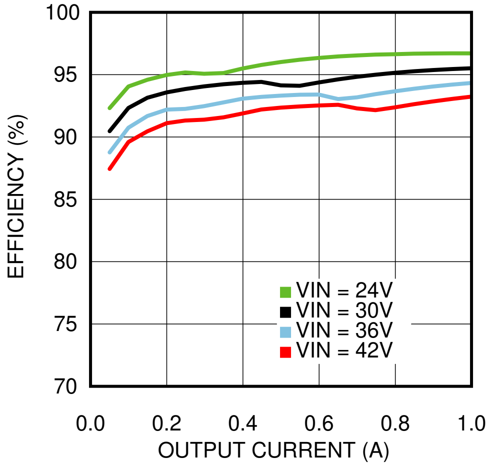


图 6-7. Efficiency V_{OUT} = 18 V, T_A = 25°C

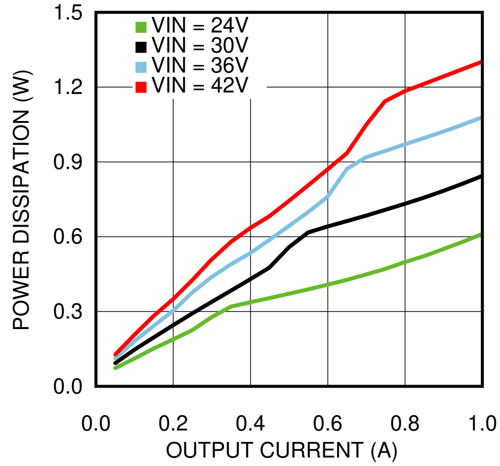


图 6-8. Power Dissipation V_{OUT} = 18 V, T_A = 25°C

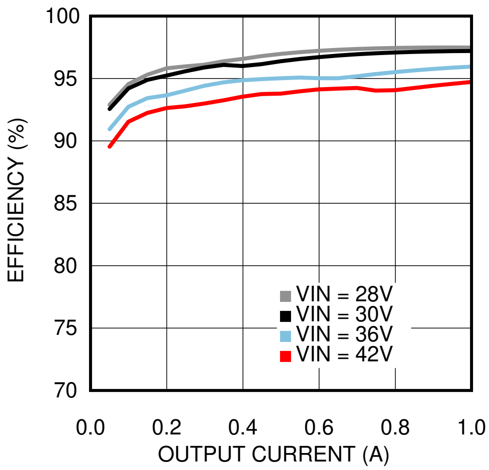


图 6-9. Efficiency V_{OUT} = 24 V, T_A = 25°C

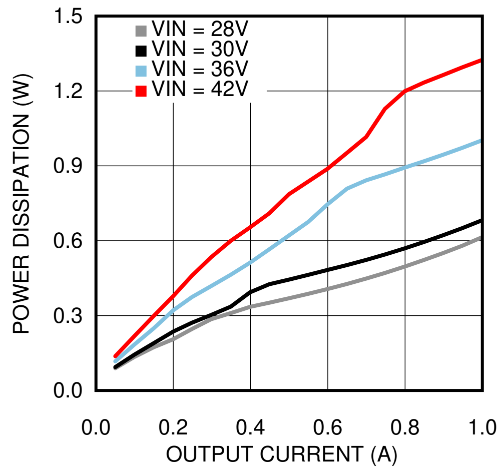


图 6-10. Power Dissipation V_{OUT} = 24 V, T_A = 25°C

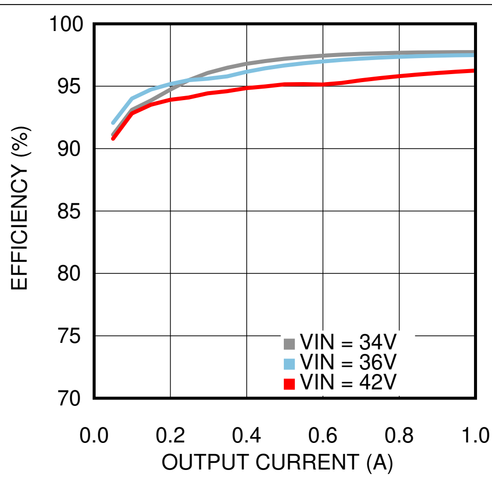


图 6-11. Efficiency V_{OUT} = 30 V, T_A = 25°C

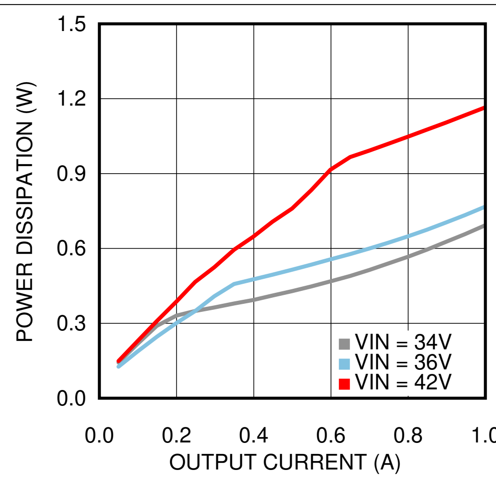


图 6-12. Power Dissipation V_{OUT} = 30 V, T_A = 25°C

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

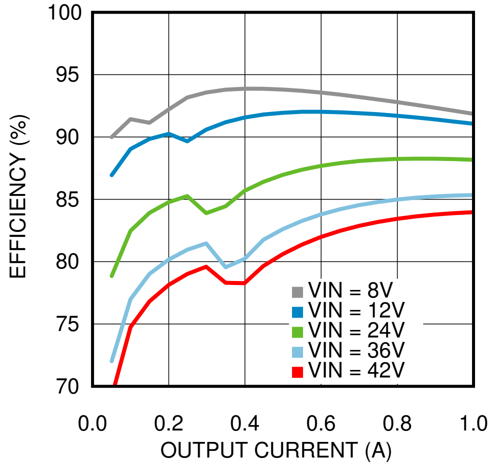


图 6-13. Efficiency V_{OUT} = 5 V, T_A = 85°C

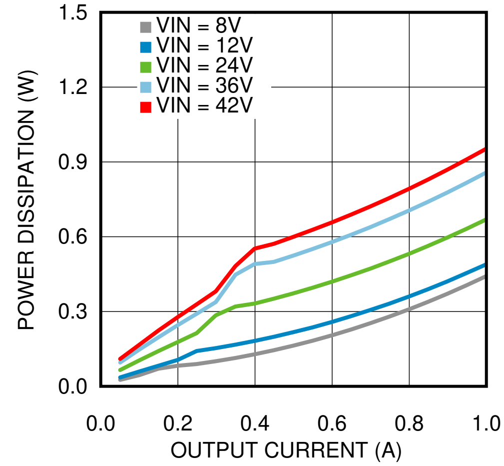


图 6-14. Power Dissipation V_{OUT} = 5 V, T_A = 85°C

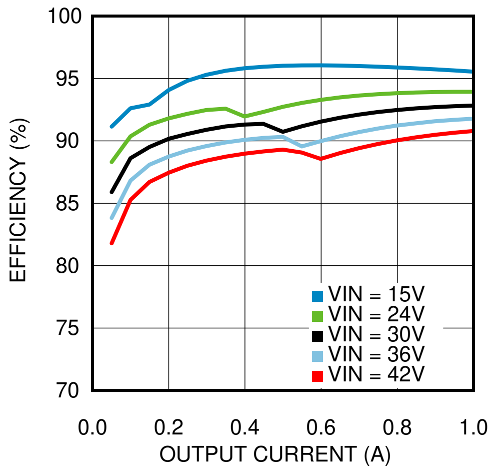


图 6-15. Efficiency V_{OUT} = 12 V, T_A = 85°C

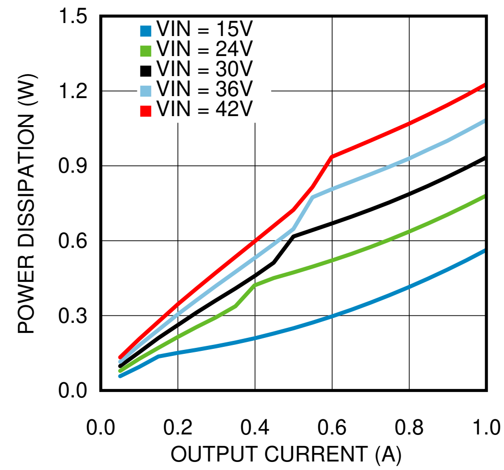


图 6-16. Power Dissipation V_{OUT} = 12 V, T_A = 85°C

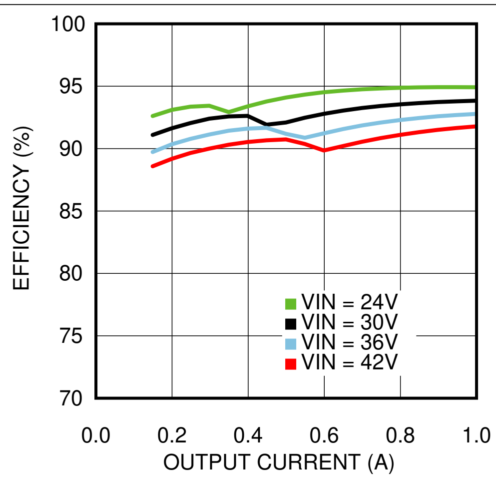


图 6-17. Efficiency V_{OUT} = 15 V, T_A = 85°C

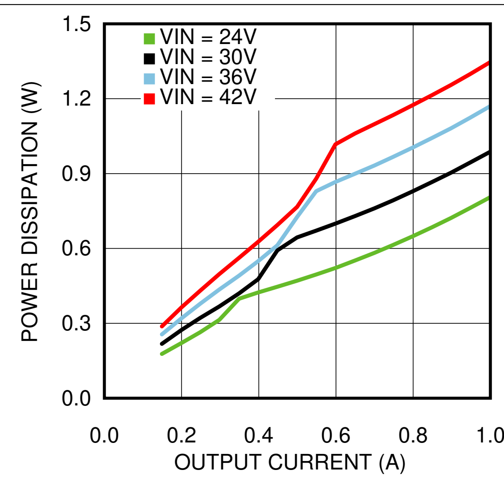


图 6-18. Power Dissipation V_{OUT} = 15 V, T_A = 85°C

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

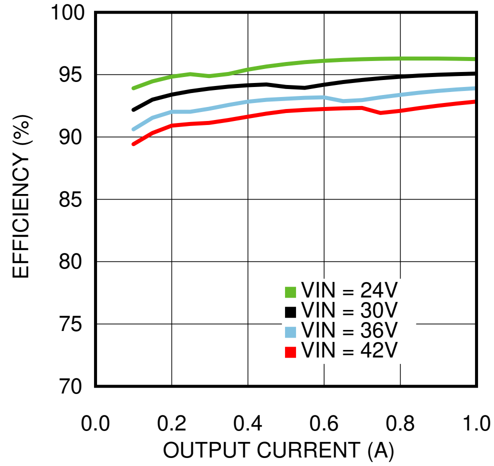


图 6-19. Efficiency V_{OUT} = 18 V, T_A = 85°C

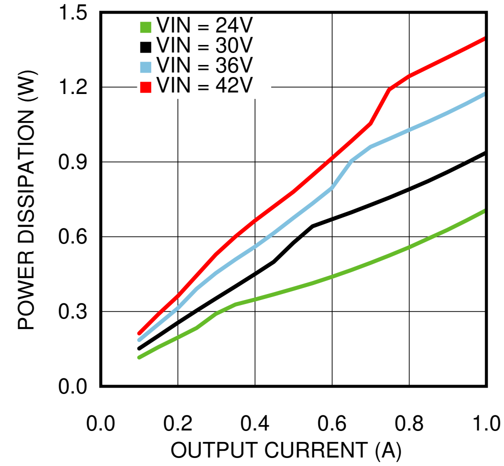


图 6-20. Power Dissipation V_{OUT} = 18 V, T_A = 85°C

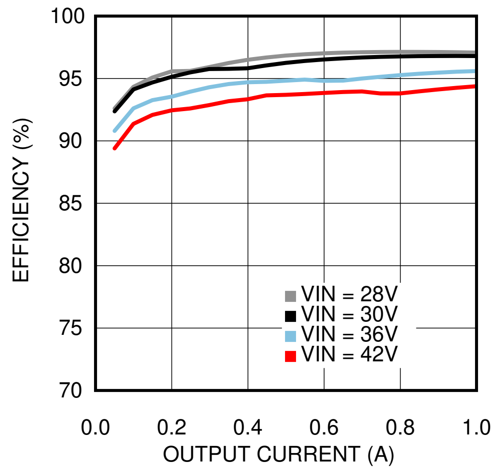


图 6-21. Efficiency V_{OUT} = 24 V, T_A = 85°C

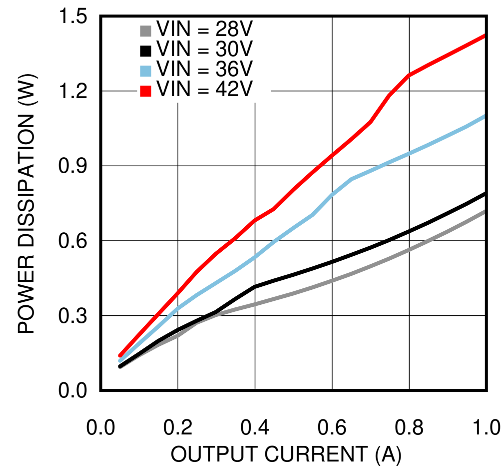


图 6-22. Power Dissipation V_{OUT} = 24 V, T_A = 85°C

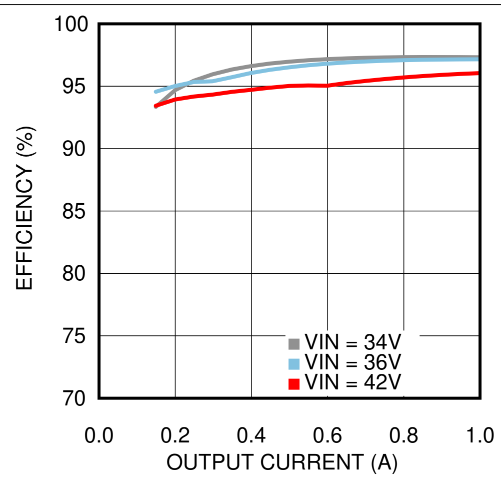


图 6-23. Efficiency V_{OUT} = 30 V, T_A = 85°C

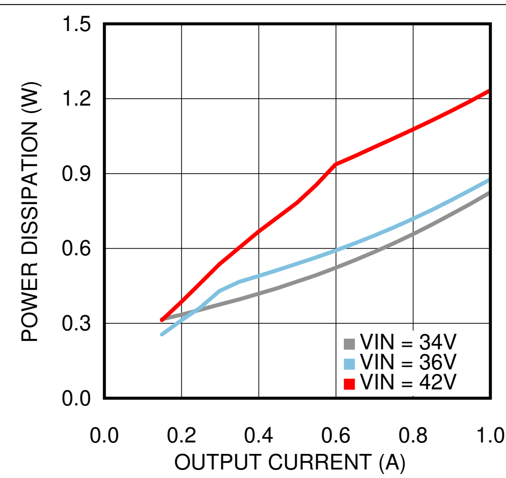


图 6-24. Power Dissipation V_{OUT} = 30 V, T_A = 85°C

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

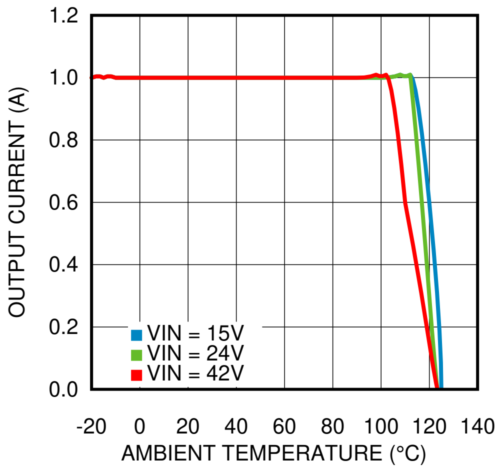


图 6-25. Thermal Derating V_{OUT} = 12 V, $R_{\theta JA}$ = 16°C/W

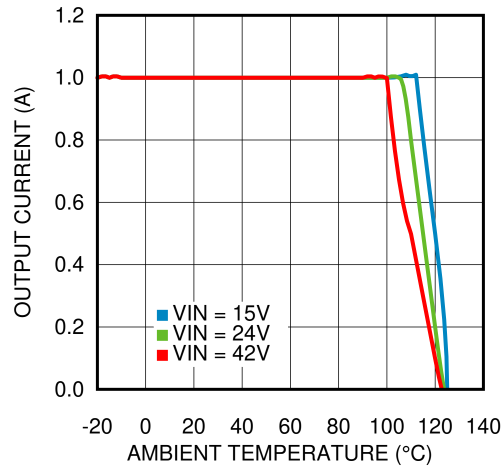


图 6-26. Thermal Derating V_{OUT} = 12 V, $R_{\theta JA}$ = 20°C/W

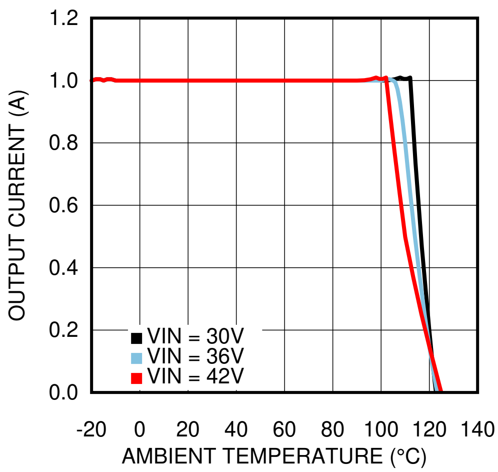


图 6-27. Thermal Derating V_{OUT} = 24 V, $R_{\theta JA}$ = 16°C/W

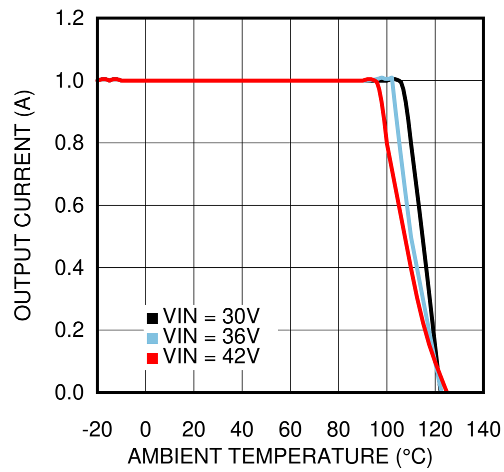


图 6-28. Thermal Derating V_{OUT} = 24 V, $R_{\theta JA}$ = 20°C/W

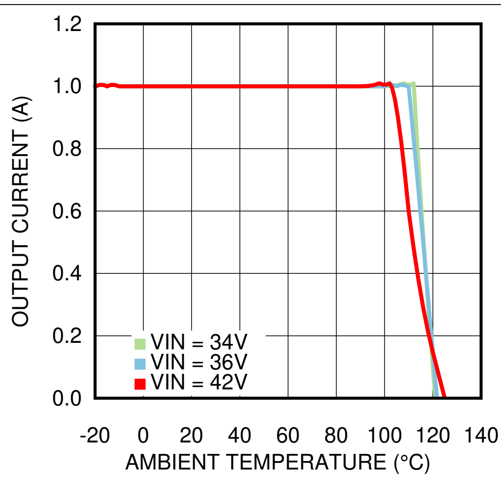


图 6-29. Thermal Derating V_{OUT} = 30 V, $R_{\theta JA}$ = 16°C/W

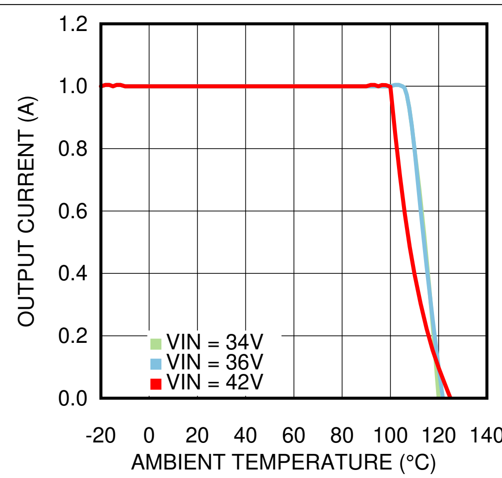


图 6-30. Thermal Derating V_{OUT} = 30 V, $R_{\theta JA}$ = 20°C/W

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

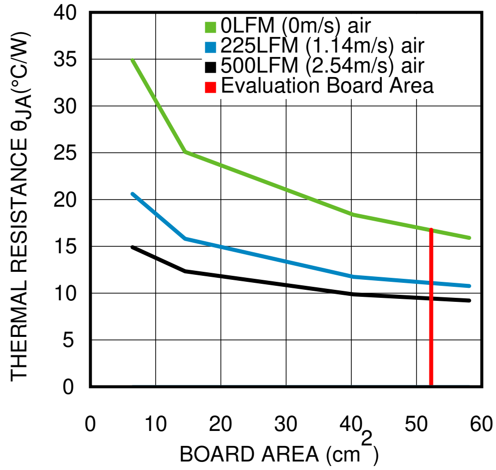


图 6-31. Package Thermal Resistance $R_{\theta JA}$ 4 Layer PCB With 1-oz Copper

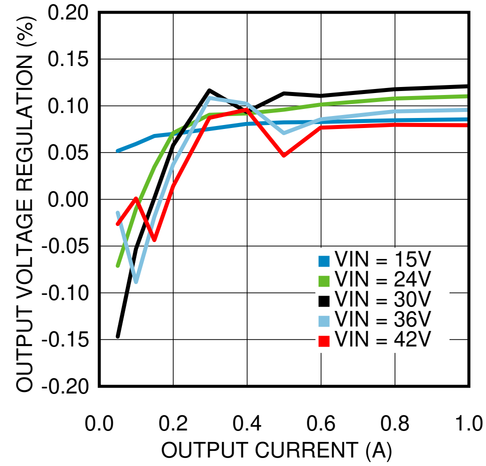


图 6-32. Line and Load Regulation T_A = 25°C

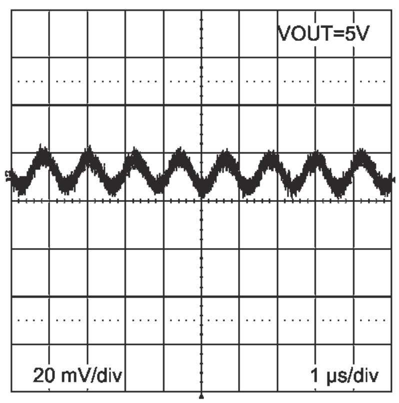


图 6-33. Output Ripple V_{IN} = 12 V, I_{OUT} = 1 A, Ceramic C_{OUT}, BW = 200 MHz

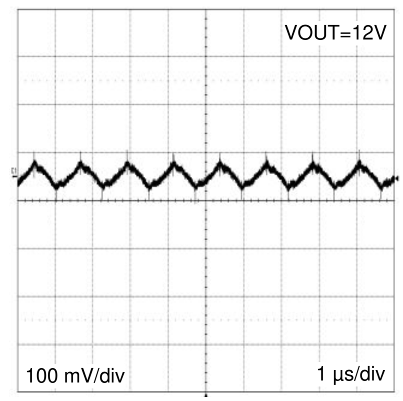


图 6-34. Output Ripple V_{IN} = 24 V, I_{OUT} = 1 A, Polymer Electrolytic C_{OUT}, BW = 200 MHz

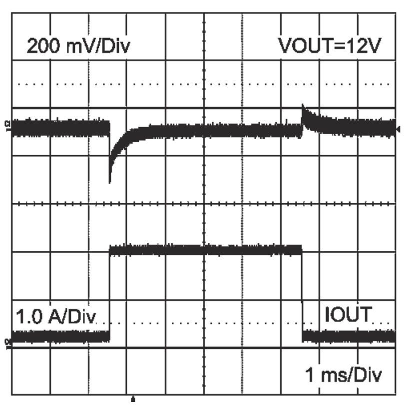


图 6-35. Load Transient Response V_{IN} = 24 V V_{OUT} = 12 V Load Step from 10% to 100%

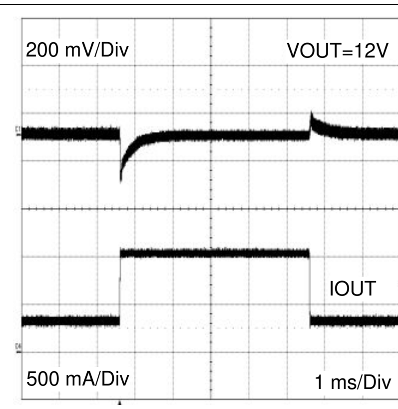


图 6-36. Load Transient Response V_{IN} = 24 V V_{OUT} = 12 V Load Step From 30% to 100%

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

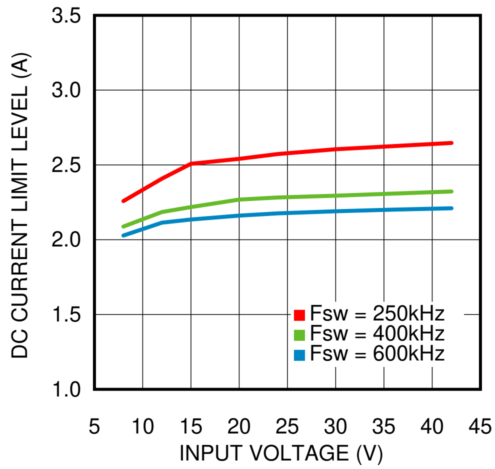


图 6-37. Current Limit vs. Input Voltage V_{OUT} = 5 V

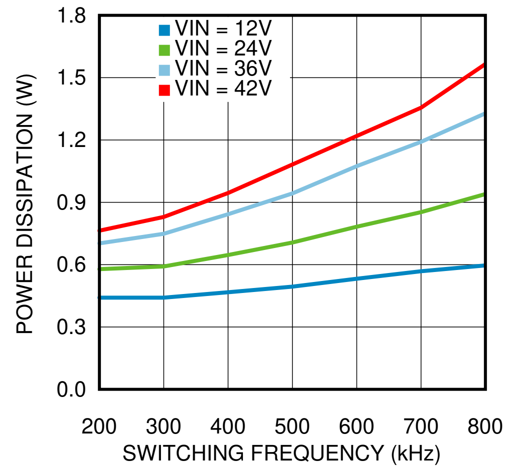


图 6-38. Switching Frequency vs. Power Dissipation V_{OUT} = 5 V

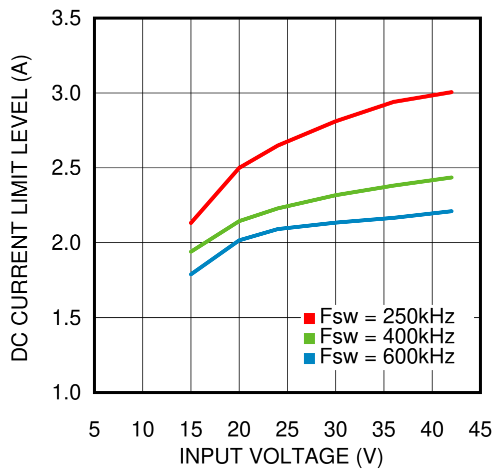


图 6-39. Current Limit vs. Input Voltage V_{OUT} = 12 V

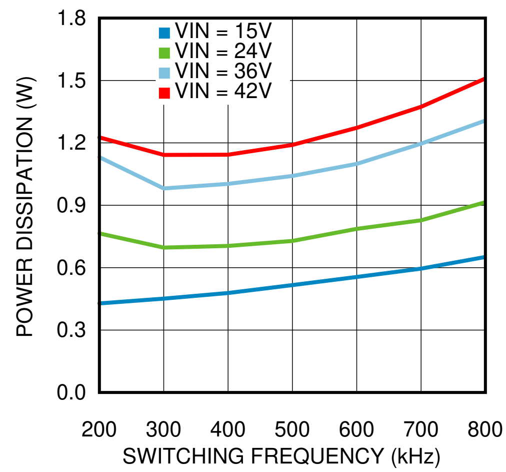


图 6-40. Switching Frequency vs. Power Dissipation V_{OUT} = 12 V

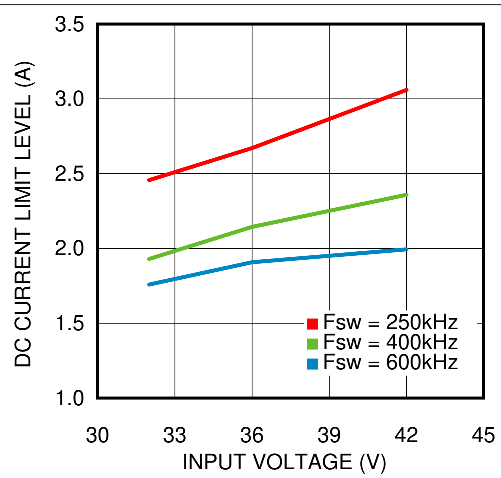


图 6-41. Current Limit vs. Input Voltage V_{OUT} = 24 V

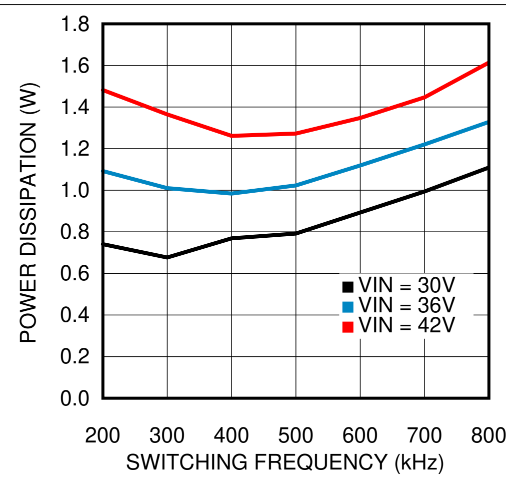


图 6-42. Switching Frequency vs. Power Dissipation V_{OUT} = 24 V

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

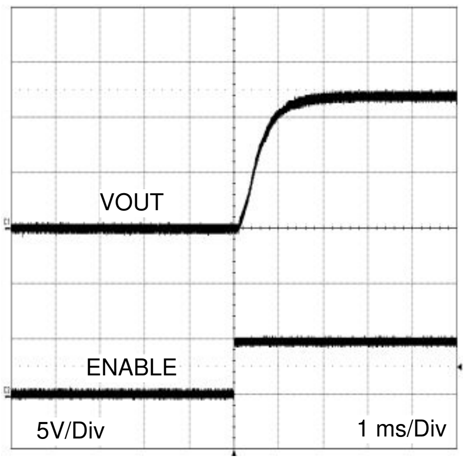


图 6-43. Start-Up V_{IN} = 24 V, I_{OUT} = 1 A

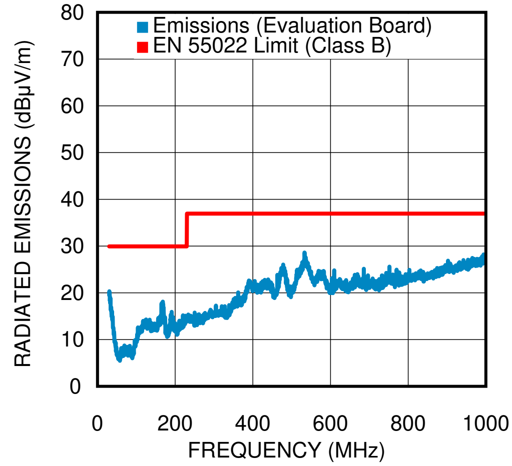


图 6-44. Radiated EMI of Evaluation Board, V_{OUT} = 12 V

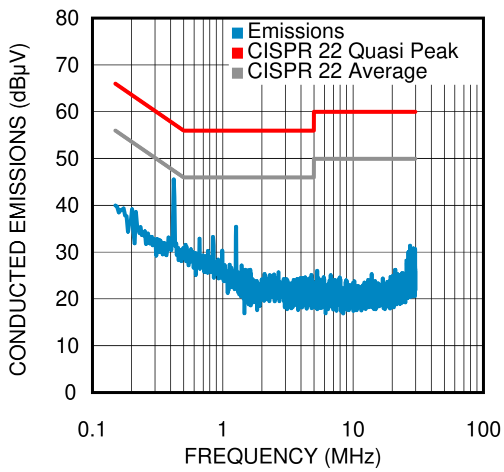


图 6-45. Conducted EMI, V_{OUT} = 12 V Evaluation Board BOM and 3.3-µH, 1-µF LC Line Filter

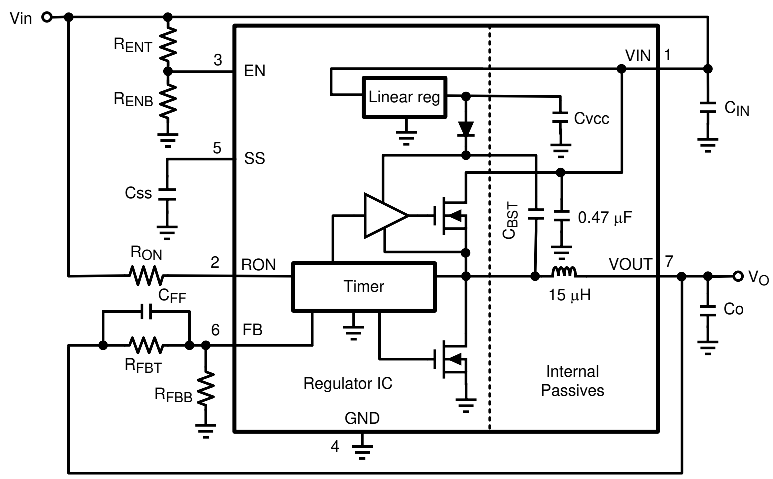
7 Detailed Description

7.1 Overview

7.1.1 COT Control Circuit Overview

Constant ON-Time control is based on a comparator and an ON-time one-shot, with the output voltage feedback compared to an internal 0.8V reference. If the feedback voltage is below the reference, the high-side MOSFET is turned on for a fixed ON-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the high-side MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Overvoltage Comparator

The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

7.3.2 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the 节 *7.2*, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds the I_{CL} value, the current limit comparator disables the start of the next ON-time period. The next switching cycle will occur only if the FB input is less than 0.8 V and the inductor current has decreased below I_{CL}. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds I_{CL}, further ON-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer OFF-time.

Note

The DC current limit varies with duty cycle, switching frequency, and temperature.

7.3.3 Thermal Protection

The junction temperature of the LMZ14201H should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145 °C (typical Hyst = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

7.3.4 Zero Coil Current Detection

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

7.3.5 Prebiased Start-Up

The LMZ14201H will properly start up into a prebiased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The prebias level of the output voltage must be less than the input UVLO set point. This will prevent the output prebias from enabling the regulator through the high-side MOSFET body diode.

7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light-load, the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. During the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained because conduction and switching losses are reduced with the smaller load and lower switching frequency.

8 Application and Implementation

Note

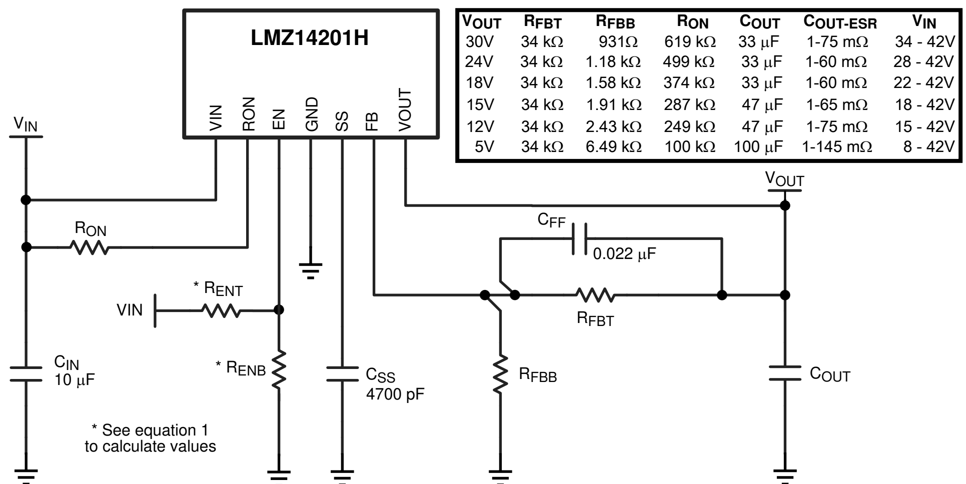
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The LMZ14201H is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMZ14201H. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software utilizes iterative design procedure and accesses comprehensive databases of components. Please go to www.ti.com for more details.

8.2 Typical Application



VOUT	RFBT	RFBB	RON	COUT	COUT-ESR	VIN
30V	34 kΩ	931Ω	619 kΩ	33 µF	1-75 mΩ	34 - 42V
24V	34 kΩ	1.18 kΩ	499 kΩ	33 µF	1-60 mΩ	28 - 42V
18V	34 kΩ	1.58 kΩ	374 kΩ	33 µF	1-60 mΩ	22 - 42V
15V	34 kΩ	1.91 kΩ	287 kΩ	47 µF	1-65 mΩ	18 - 42V
12V	34 kΩ	2.43 kΩ	249 kΩ	47 µF	1-75 mΩ	15 - 42V
5V	34 kΩ	6.49 kΩ	100 kΩ	100 µF	1-145 mΩ	8 - 42V

图 8-1. Simplified Application Schematic

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = Up to 42 V
- V_{OUT} = 5 V to 30 V
- I_{OUT} = 1 A

Refer to the table in 图 8-1 for more information.

8.2.2 Detailed Design Procedure

8.2.2.1 Design Steps for the LMZ14201H Application

The LMZ14201H is fully supported by WEBENCH which offers the following: component selection, electrical simulation, thermal simulation, as well as a build-it prototype board for a reduction in design time. The following list of steps can be used to manually design the LMZ14201H application.

1. Select minimum operating V_{IN} with enable divider resistors.
2. Program V_O with divider resistor selection.
3. Program turnon time with soft-start capacitor selection.
4. Select C_O.
5. Select C_{IN}.
6. Set operating frequency with R_{ON}.

7. Determine module dissipation.
8. Lay out PCB for required thermal performance.

8.2.2.1.1 Enable Divider, R_{ENT} and R_{ENB} Selection

The enable input provides a precise 1.18-V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider shown in the 节 7.2 is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable undervoltage lockout. This is often used in battery-powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14201H output rail. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\text{-}ENABLE} / 1.18\ V) - 1 \tag{1}$$

The EN pin is internally pulled up to VIN and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will ensure smooth start-up and will prevent overloading the input supply.

8.2.2.1.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The high-side MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8\ V \times (1 + R_{FBT} / R_{FBB}) \tag{2}$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8\ V) - 1 \tag{3}$$

These resistors should be chosen from values in the range of 1 kΩ to 50 kΩ.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , and R_{ON} is included in the simplified applications schematic.

8.2.2.1.3 Soft-Start Capacitor, C_{SS}, Selection

Programmable soft-start permits the regulator to slowly ramp to its steady-state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turnon, after all UVLO conditions have been passed, an internal 8uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady-state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / I_{ss} = 0.8\ V \times C_{SS} / 8\ uA \tag{4}$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8\ \mu A / 0.8\ V \quad (5)$$

Use of a 4700-pF capacitor results in 0.5-ms soft-start duration. This is a recommended value. Note that high values of C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use 方程式 18 below to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the soft-start capacitor value should be less than 0.018 µF.

Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200-µA current sink:

- The enable input being “pulled low”
- Thermal shutdown condition
- Overcurrent fault
- Internal V_{IN} UVLO

8.2.2.1.4 Output Capacitor, C_O, Selection

None of the required output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst-case RMS current rating of 0.5 × $I_{LR\ P\text{-}P}$, as calculated in 方程式 19. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Low-ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

8.2.2.1.4.1 Capacitance

方程式 6 provides a good first pass approximation of C_O for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} - V_O) \times V_{OUT\text{-}TRAN}) \quad (6)$$

As an example, for 1A load step, V_{IN} = 24 V, V_{OUT} = 12 V, $V_{OUT\text{-}TRAN}$ = 50 mV:

$C_O \geq 1\ A \times 0.8\ V \times 15\ \mu H \times 24\ V / (4 \times 12\ V \times (24\ V - 12\ V) \times 50\ mV)$

$C_O \geq 10.05\ \mu F$

8.2.2.1.4.2 ESR

The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the overvoltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid overvoltage protection during normal operation. The following equations can be used:

$$ESR_{MAX\text{-}RIPPLE} \leq V_{OUT\text{-}RIPPLE} / I_{LR\ P\text{-}P} \quad (7)$$

where

- $I_{LR\ P\text{-}P}$ is calculated using 方程式 19 below.

$$ESR_{MAX\text{-}OVP} < (V_{FB\text{-}OVP} - V_{FB}) / (I_{LR\ P\text{-}P} \times A_{FB}) \quad (8)$$

where

- A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency.

As worst-case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.

The selected capacitor should have sufficient voltage and RMS current rating. The RMS current through the output capacitor is:

$$I(C_{OUT(RMS)}) = I_{LR\ P\text{-}P} / \sqrt{12} \quad (9)$$

8.2.2.1.5 Input Capacitor, C_{IN}, Selection

The LMZ14201H module contains an internal 0.47 μF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be as close as possible to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value.

Worst-case input ripple current rating is dictated by 方程式 10:

$$I(C_{IN(RMS)}) \cong 1 / 2 \times I_O \times \sqrt{(D / 1\text{-}D)} \quad (10)$$

where

- $D \cong V_O / V_{IN}$

(As a point of reference, the worst-case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10-uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI also recommends to pay attention to the voltage and temperature deratings of the capacitor selected. Also note ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then 方程式 11 may be used.

$$C_{IN} \geq I_O \times D \times (1 - D) / f_{SW\text{-}CCM} \times \Delta V_{IN} \quad (11)$$

If ΔV_{IN} is 1% of V_{IN} for a 24-V input to 12-V output application this equals 240 mV and f_{SW} = 400 kHz.

$C_{IN} \geq$ 1 A × 12 V/24 V × (1 – 12 V/24 V) / (400000 × 0.240 V)

$C_{IN} \geq$ 2.6 μF

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

8.2.2.1.6 ON-Time, R_{ON}, Resistor Selection

Many designs will begin with a desired switching frequency in mind. As seen in the *Typical Characteristics* section, the best efficiency is achieved in the 300 kHz to 400 kHz switching frequency range. 方程式 12 can be used to calculate the R_{ON} value.

$$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \text{ x } R_{ON}) \quad (12)$$

This can be rearranged as

$$R_{ON} \cong V_O / (1.3 \times 10^{-10} \text{ x } f_{SW(CCM)} \quad (13)$$

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the ON-time and OFF-time for the *COT Control Circuit Overview* section.

The ON-time of the LMZ14201H timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN} \quad (14)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the ON-time at maximum V_{IN} is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by 方程式 15:

$$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150 \text{ nsec}) \quad (15)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum ON-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geqslant V_{IN(MAX)} \times 150 \text{ nsec} / (1.3 \times 10^{-10}) \quad (16)$$

If R_{ON} calculated in 方程式 13 is less than the minimum value determined in 方程式 16 a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

Additionally, the minimum OFF-time of 260 ns (typical) limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

8.2.2.1.6.1 Discontinuous Conduction and Continuous Conduction Mode Selection

Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \approxeq V_O \times (V_{IN}-1) \times 15 \text{ µH} \times 1.18 \times 10^{20} \times I_O / ((V_{IN} - V_O) \times R_{ON}{}^2) \quad (17)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using 方程式 12 above.

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \approxeq V_O \times (V_{IN} - V_O) / (2 \times 15 \text{ µH} \times f_{SW(CCM)} \times V_{IN}) \quad (18)$$

The inductor internal to the module is 15 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN}- V_O) / (15 \text{ µH} \times f_{SW} \times V_{IN}) \quad (19)$$

where

- V_{IN} is the maximum input voltage and f_{SW} is determined from 方程式 12.

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

8.2.3 Application Curve

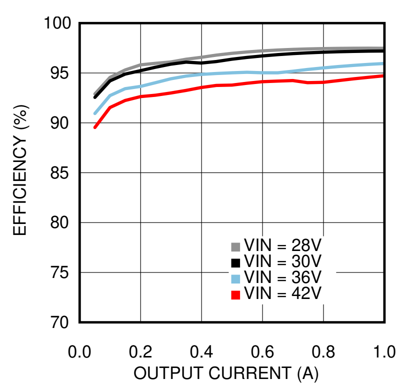


图 8-2. Efficiency V_{OUT} = 24 V, T_A = 25°C

9 Power Supply Recommendations

The LMZ14201H device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ14201H supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ14201H, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PCB layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14203. Therefore place C_{IN1} as close as possible to the LMZ14203 VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).
2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.
3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The trace are from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14203 to minimize noise.
4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.
5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

10.1.1 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness – 0.125 mm to 0.15 mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to AN *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* (SNAA214) for Reflow information
- Maximum number of reflows allowed is one

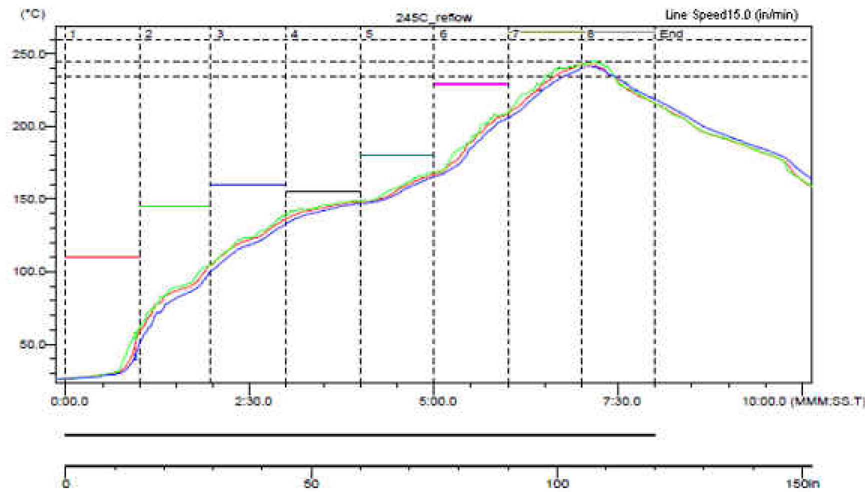


图 10-1. Sample Reflow Profile

表 10-1. Sample Reflow Profile Table

PROBE	MAX TEMP (°C)	REACHED MAX TEMP	TIME ABOVE 235°C	REACHED 235°C	TIME ABOVE 245°C	REACHED 245°C	TIME ABOVE 260°C	REACHED 260°C
1	242.5	6.58	0.49	6.39	0	–	0	–
2	242.5	7.1	0.55	6.31	0	7.1	0	–
3	241	7.09	0.42	6.44	0	–	0	–

10.2 Layout Example

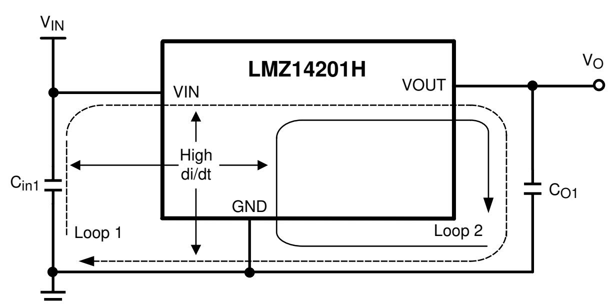


图 10-2. Critical Current Loops to Minimize

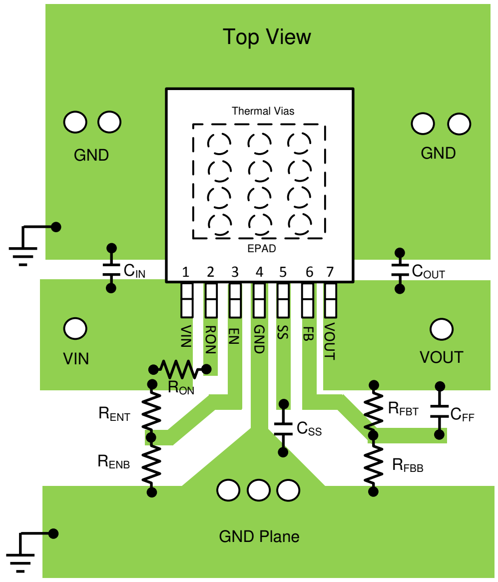


图 10-3. PCB Layout Guide

10.2.1 Power Dissipation and Board Thermal Requirements

For a design case of V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 1 A, T_A (MAX) = 85°C , and $T_{JUNCTION}$ = 125°C, the device must see a maximum junction-to-ambient thermal resistance of:

$$R_{\theta JA\text{-}MAX} < (T_{J\text{-}MAX} - T_{A(MAX)}) / P_D \quad (20)$$

This $R_{\theta JA\text{-}MAX}$ will ensure that the junction temperature of the regulator does not exceed $T_{J\text{-}MAX}$ in the particular application ambient temperature.

To calculate the required $R_{\theta JA\text{-}MAX}$ we need to get an estimate for the power losses in the IC. 图 10-4 is taken from the *Typical Characteristics* section and shows the power dissipation of the LMZ14201H for V_{OUT} = 12 V at 85°C T_A.

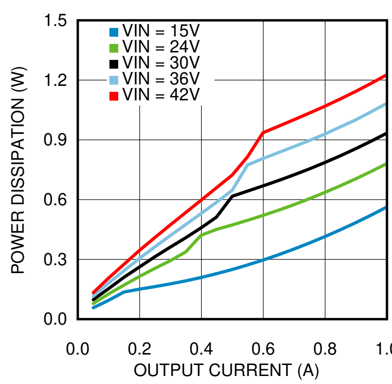


图 10-4. Power Dissipation V_{OUT} = 12 V, T_A = 85°C

Using the 85°C T_A power dissipation data as a conservative starting point, the power dissipation P_D for V_{IN} = 24 V and V_{OUT} = 12 V is estimated to be 0.75 W. The necessary $R_{\theta JA\text{-}MAX}$ can now be calculated.

$$R_{\theta JA\text{-}MAX} < (125°C - 85°C) / 0.75 W \quad (21)$$

$$R_{\theta JA\text{-}MAX} < 53.3°C/W \quad (22)$$

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to 图 10-5. This graph is taken from the *Typical Characteristics* section and shows how the $R_{\theta JA}$ varies with the PCB area.

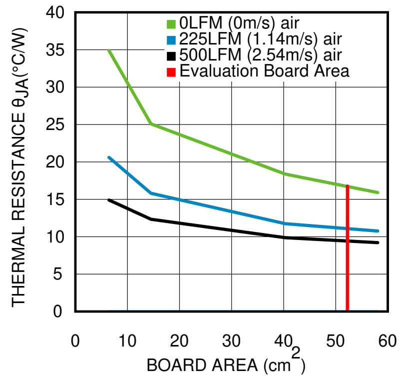


图 10-5. Package Thermal Resistance $R_{\theta JA}$ 4-Layer PCB With 1-oz Copper

For $R_{\theta JA\text{-}MAX} < 53.3$°C/W and only natural convection (that is. no air flow), the PCB area can be smaller than 9 cm^2. This corresponds to a square board with 3 cm × 3 cm (1.18 in × 1.18 in) copper area, 4 layers, and 1 oz copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

For more guidelines and insight on PCB copper area, thermal vias placement, and general thermal design practices, refer to Application Note AN-2020 (SNVA419).

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *AN-2027 Inverting Application for the LMZ14203 SIMPLE SWITCHER Power Module*, SNVA425
- *Evaluation Board Application Note AN-2024*, SNVA422
- *AN-2026 Effect of PCB Design on Thermal Performance of SIMPLE SWITCHER Power Modules*, SNVA424
- *AN-2020 Thermal Design By Insight, Not Hindsight*, SNVA419
- *AN Design Summary LMZ1xxx and LMZ2xxx Power Modules Family*, SNAA214

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ14201HTZ/NOPB	ACTIVE	TO-PMOD	NDW	7	250	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ	Samples
LMZ14201HTZE/NOPB	ACTIVE	TO-PMOD	NDW	7	45	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ	Samples
LMZ14201HTZX/NOPB	ACTIVE	TO-PMOD	NDW	7	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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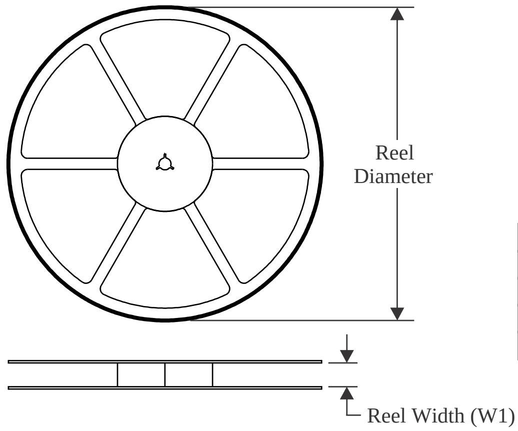
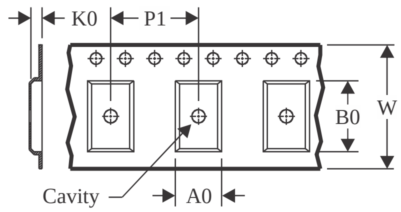
TAPE AND REEL INFORMATION

REEL DIMENSIONS

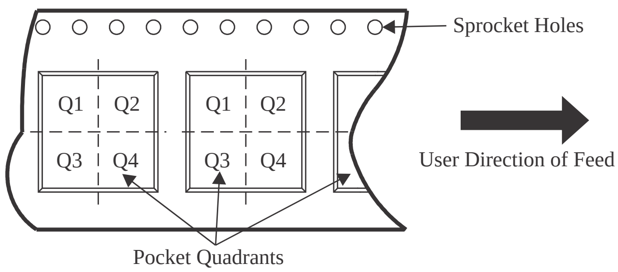


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

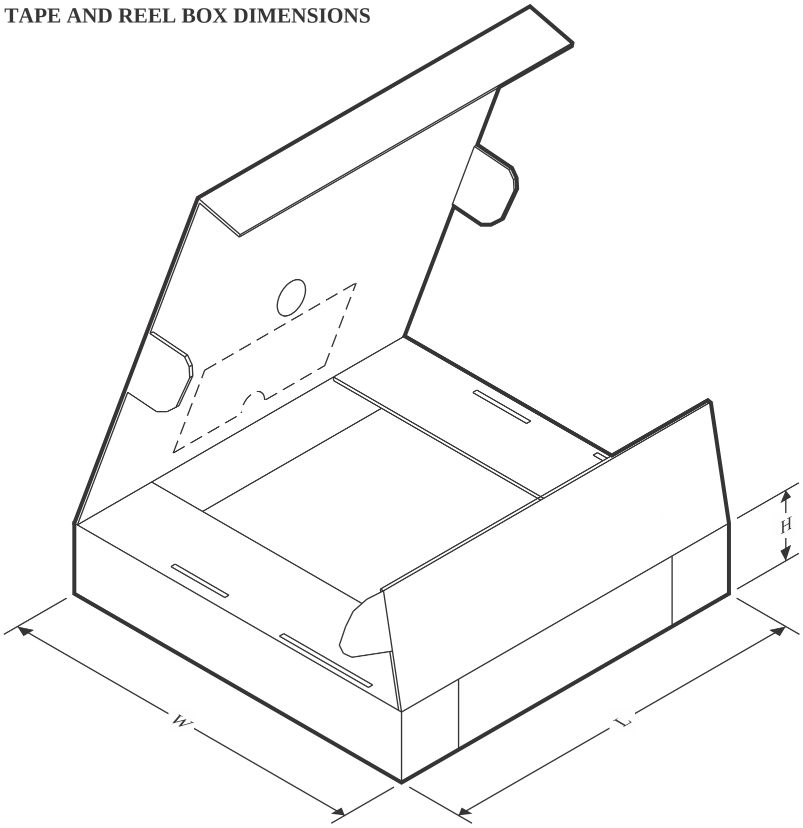
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ14201HTZ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ14201HTZX/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

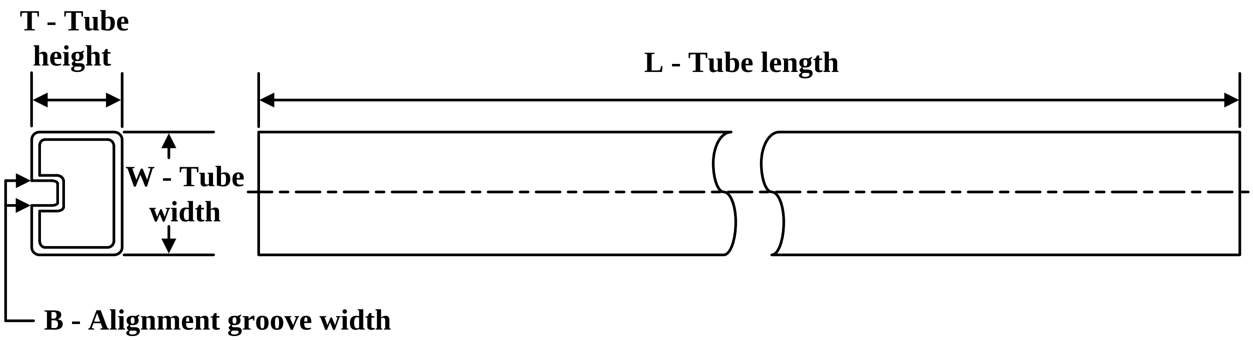
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ14201HTZ/NOPB	TO-PMOD	NDW	7	250	356.0	356.0	45.0
LMZ14201HTZX/NOPB	TO-PMOD	NDW	7	500	356.0	356.0	45.0

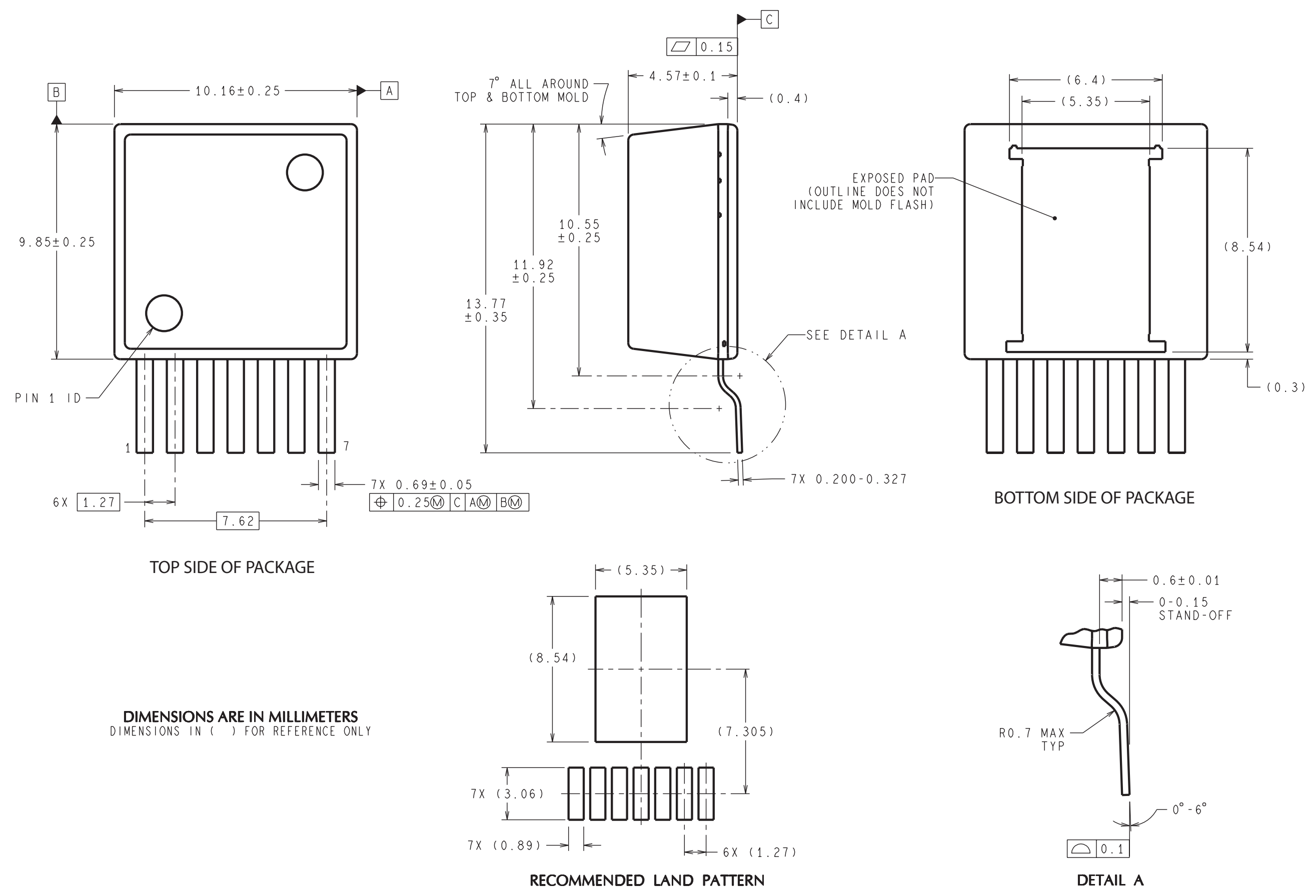
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMZ14201HTZE/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4

NDW0007A



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