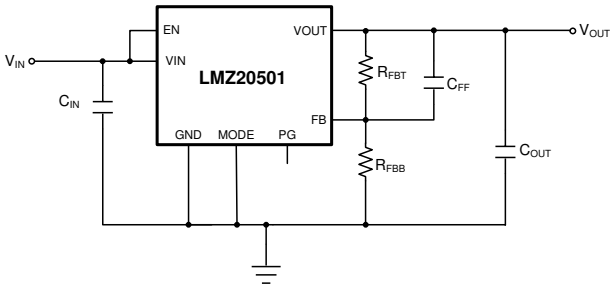
LMZ20501 1A 纳米模块

1 特性

- 集成电感器
- 微型 3.5mm × 3.5mm × 1.75mm 封装
- 最大负载电流为 1A
- 输入电压范围为 2.7 V 至 5.5V
- 可调输出电压范围为 0.8V 至 3.6V
- 温度范围内的反馈容差为 ±1%
- 关断模式下静态电流为 2.4μA（最大值）
- 3MHz 固定 PWM 开关频率
- -40°C 至 125°C 的结温范围
- 电源正常状态标志功能
- 引脚可选开关模式
- 内部补偿和软启动
- 电流限制、热关断和 UVLO 保护
- 使用 LMZ20501 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 负载点调节
- 空间受限型应用



简化版原理图

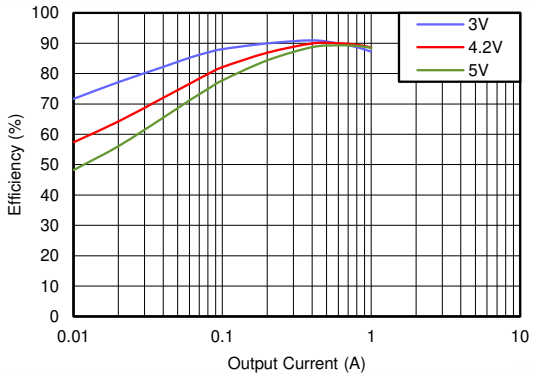
3 说明

LMZ20501 纳米模块稳压器是一款易于使用的同步降压直流/直流转换器，能够从最高 5.5V 的输入电压驱动高达 1A 的负载电流，以极小的解决方案尺寸提供优异的效率和输出精度。这种创新型封装将稳压器和电感器包含在 3.5mm × 3.5mm × 1.75mm 的小体积中，节省了布板空间以及电容器选型所需的时间和开销。LMZ20501 仅需要五个外部组件，其引脚设计可实现简单、最优的 PCB 布局。该器件使用很少数量的外部元件和 TI WEBENCH® 设计工具，提供一个易于使用的完整设计。TI 的 WEBENCH 工具包含诸如外部元件计算、电气模拟和 WebTherm® 等特性。有关焊接信息，请参阅 SNOA401。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LMZ20501	USIP (8)	3.50mm × 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



V_{OUT} = 1.8V 时自动模式下的典型效率

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (August 2018) to Revision E (September 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated 图 7-3 title	10

Changes from Revision C (April 2015) to Revision D (August 2018)	Page
• 删除了 Simple Switcher 品牌；添加了 WEBENCH 链接	1

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5 Pin Configuration and Functions

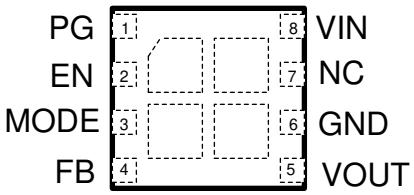


图 5-1. 8-Pins USIP Package (SIL) (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
1	PG	O	Power-good flag; open drain. Connect to logic supply through a resistor. High = power good; low = power bad. If not used, leave unconnected.
2	EN	I	Enable input. High = On, Low = Off. A valid input voltage, on pin 8, must be present before EN is asserted. Do not float.
3	MODE	I	Mode selection input. High = forced PWM. Low = AUTO mode with PFM at light load. Do not float.
4	FB	I	Feedback input to controller. Connect to output through feedback divider.
5	VOUT	P	Regulated output voltage. Connect to C_{OUT}.
6	GND	G	Ground for all circuitry. Reference point for all voltages
7	NC	—	This pin must be left floating. Do not connect to ground or any other node.
8	VIN	P	Input supply to regulator. Connect to input capacitor(s) as close as possible to the VIN pin and GND pin of the module.
EP	EP	G	Ground and heat-sink connection. See 节 10.1 for more information.

(1) G = Ground, I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

Under the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted) (1)

	MIN	MAX	UNIT
VIN to GND	–0.2	6	V
EN, MODE, FB, PG, to GND(2)	–0.2	V_{IN}+0.2	
VOUT to GND(2)	–0.2	V_{IN}+0.2	
Junction temperature		150	°C
Peak soldering reflow temperature for Pb(3)		240	°C
Peak soldering reflow temperature for No-Pb(3)		260	
Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum voltage on this pin must not exceed 6 V with respect to ground. Do not allow the voltage on the output pin to exceed the voltage on the input pin by more than 0.2 V.
(3) For soldering information, please refer to the following document: SNOA401.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Under the recommended operating junction temperature range of -40°C to 125°C (unless otherwise noted) (1)

	MIN	NOM	MAX	UNIT
Input voltage	2.7		5.5	V
Output voltage programming	0.8		3.6	V
Output voltage range (2)	0		3.6	V
Load current	0		1	A
Power good flag current	0		4	mA
Junction temperature	-40		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Under no conditions should the output voltage be allowed to fall below zero volts.

6.4 Thermal Information

THERMAL METRIC(1)		LMZ20501 USIP (SIL) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W

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THERMAL METRIC(1)		LMZ20501 USIP (SIL) 8 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	°C/W

(1) The values given in this table are only valid for comparison with other packages and can not be used for design purposes. For design information please see the 节 8.2.1.5 section. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to 125°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 3.6 V

PARAMETER		TEST CONDITIONS	MIN (1)	TYP	MAX(1)	UNIT
V_{FB}	Feedback voltage	V_{IN} = 3.6 V	0.594	0.6	0.606	V
I_{Q_AUTO}	Operating quiescent current in AUTO mode	AUTO mode, V_{FB} = 0.8 V		72	90	µA
I_{Q_PWM}	Operating quiescent current in forced PWM mode	PWM mode, V_{FB} = 0.8 V		490	620	µA
I_{Q_off}	Shutdown quiescent current(2)	V_{IN} = 3.6 V, V_{EN} = 0.0 V		0.7	1.5	µA
		V_{IN} = 5.5 V, V_{EN} = 0.0 V		1.0	2.4	
V_{UVLO}	Input supply undervoltage lockout thresholds	Rising		2.5		V
		Falling		2.3		
V_{EN}	High level input voltage	V_{IH}	1.4			V
	Low level input voltage	V_{IL}			0.4	
V_{MODE}	High level input voltage	V_{IH}	1.2			V
	Low level input voltage	V_{IL}			0.4	
I_{LIM}	Peak switch current limit(3)		1.3	1.7		A
F_{osc}	Internal oscillator frequency		2.5	3.0	3.2	MHz
T_{ON}	Minimum switch on time(5)			50		ns
T_{ss}	Soft-start time(5)			800		µs
R_{PG}	Power-good flag pulldown R_{dson}		40	70	110	Ω
V_{PG1}	Power good flag, undervoltage trip(4)	% of feedback voltage, rising		92%		
V_{PG2}	Power good flag, undervoltage trip(4)	% of feedback voltage, falling		88%		
V_{PG3}	Power good flag, overvoltage trip(4)	% of feedback voltage, rising		112%		
V_{PG4}	Power good flag, overvoltage trip(4)	% of feedback voltage, falling		108%		
T_{SD}	Thermal shutdown(5)	Rising threshold		159		°C
	Thermal shutdown hysteresis(5)			15		°C

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Shutdown current includes leakage current of the switching transistors.
(3) This is the peak switch current limit measured with a slow current ramp. Due to inherent delays in the current limit comparator, the peak current limit measured at 3MHz will be larger.
(4) See 节 7.3.6 for explanation of voltage levels.
(5) This parameter is not tested in production.

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6.6 System Characteristics

The following specifications apply to the circuit found in 图 8-1 with the appropriate modifications from 表 8-1. **These parameters are not tested in production and represent typical performance only.** Unless otherwise stated the following conditions apply: T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load Regulation	Percent output voltage change for the given load current change	V_{OUT} = 1.2 V, V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, PWM		0.14%		
		V_{OUT} = 1.8 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, PWM		0.15%		
		V_{OUT} = 3.3 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, PWM		0.11%		
Line Regulation	Percent output voltage change for the given change in input voltage	V_{OUT} = 1.2 V I_{OUT} = 1 A, V_{IN} = 3 V to 5 V, PWM		0.16%		
		V_{OUT} = 1.8 V I_{OUT} = 1 A, V_{IN} = 3 V to 5 V, PWM		0.12%		
		V_{OUT} = 3.3 V I_{OUT} = 1 A,V_{IN} = 4 V to 5 V, PWM		0.1%		
V_{R-PWM}	Output voltage ripple in PWM	V_{OUT} = 1.2 V I_{OUT} = 1 A, V_{IN} = 5 V, PWM		3.3		mV pk-pk
		V_{OUT} = 1.8 V I_{OUT} = 1 A, V_{IN} = 5 V, PWM		3.3		
		V_{OUT} = 3.3V I_{OUT}= 1 A, V_{IN} = 5 V, PWM		4.2		
V_{R-PFM}	Output voltage ripple in PFM	V_{OUT} = 1.2V I_{OUT}= 1 mA, V_{IN} = 3 V, PFM		22		mV pk-pk
		V_{OUT} = 1.8 V I_{OUT}= 1 mA, V_{IN}=3 V, PFM		22		
		V_{OUT} = 3.3 V I_{OUT} = 1 mA, V_{IN} = 5 V, PFM		40		
Load Transient	Output voltage deviation from nominal due to a load current step	V_{OUT} = 1.2 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, Tr = Tf = 2 µs, PWM		±60		mV
		V_{OUT} = 1.8 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, Tr = Tf = 2 µs, PWM		±50		
		V_{OUT} = 3.3 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, Tr = Tf = 2 µs, PWM		±60		
Line Transient	Output voltage deviation due to an input voltage step	V_{OUT} = 1.2V I_{OUT} = 1 A, V_{IN} = 3 V to 5 V, Tr = Tf = 50 µs, PWM		25		mV pk-pk
		V_{OUT} = 1.8 V I_{OUT} = 1 A, V_{IN} = 3 V to 5 V, Tr = Tf = 50 µs, PWM		30		
		V_{OUT} = 3.3 V I_{OUT} = 1 A, V_{IN} = 4 V to 5 V, Tr = Tf = 50 µs, PWM		20		

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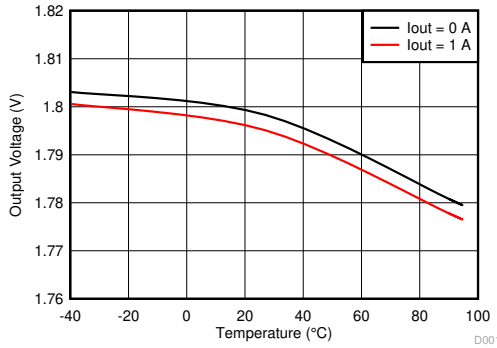
The following specifications apply to the circuit found in 图 8-1 with the appropriate modifications from 表 8-1. **These parameters are not tested in production and represent typical performance only.** Unless otherwise stated the following conditions apply: T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
η	Peak efficiency	V_{OUT} = 1.2 V V_{IN} = 3 V		87%		
		V_{OUT} = 1.8 V V_{IN} = 3 V		91%		
		V_{OUT} = 3.3 V V_{IN} = 4.2 V		94%		
	Full load efficiency	V_{OUT} = 1.2 V V_{IN} = 3 V, I_{OUT} = 1 A		83%		
		V_{OUT} = 1.8 V V_{IN} = 3 V, I_{OUT} = 1 A		87%		
		V_{OUT} = 3.3 V V_{IN} = 4.2 V, I_{OUT} = 1 A		93%		

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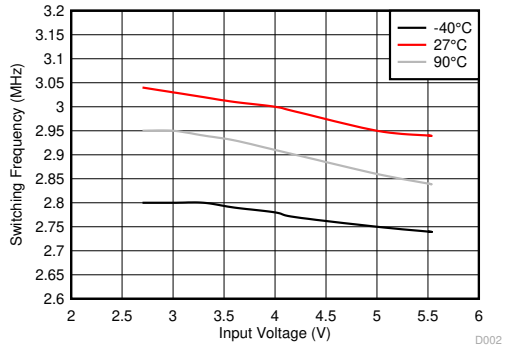
6.7 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 3.6 V, T_A = 25°C.



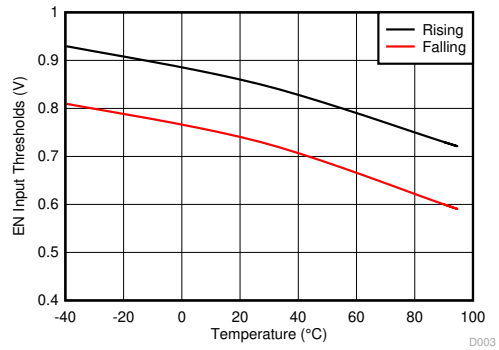
V_{IN} = 3.6 V PWM Mode V_{OUT} = 1.8 V

图 6-1. Typical Output Voltage vs Temperature



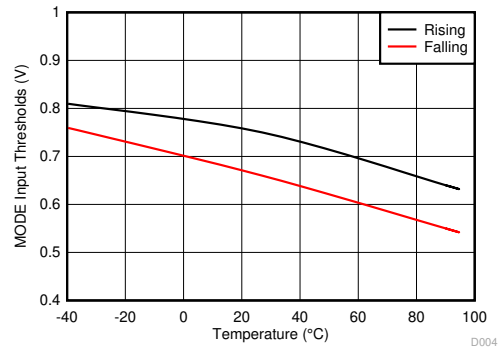
V_{IN} = 3.6 V I_{OUT} = 0 A PWM Mode

图 6-2. Switching Frequency in PWM Mode



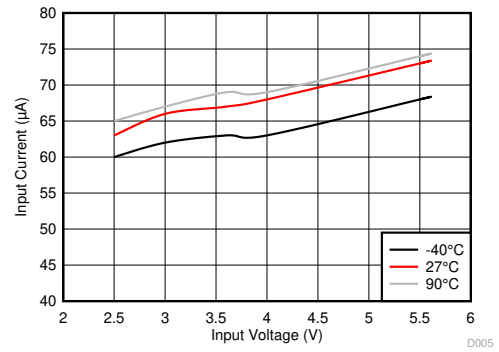
V_{IN} = 3.6 V

图 6-3. EN Input Thresholds



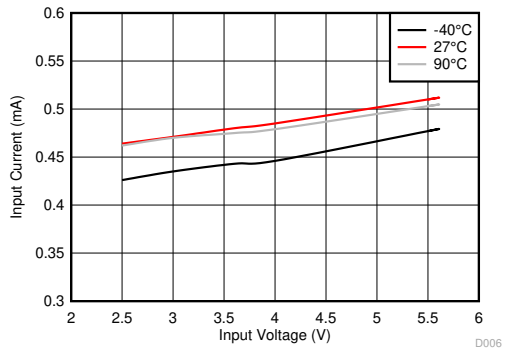
V_{IN} = 3.6 V

图 6-4. MODE Input Thresholds



V_{FB} = 0.8 V AUTO Mode

图 6-5. Non-Switching Input Current in AUTO Mode



V_{FB} = 0.8 V PWM Mode

图 6-6. Non-Switching Input Current in PWM Mode

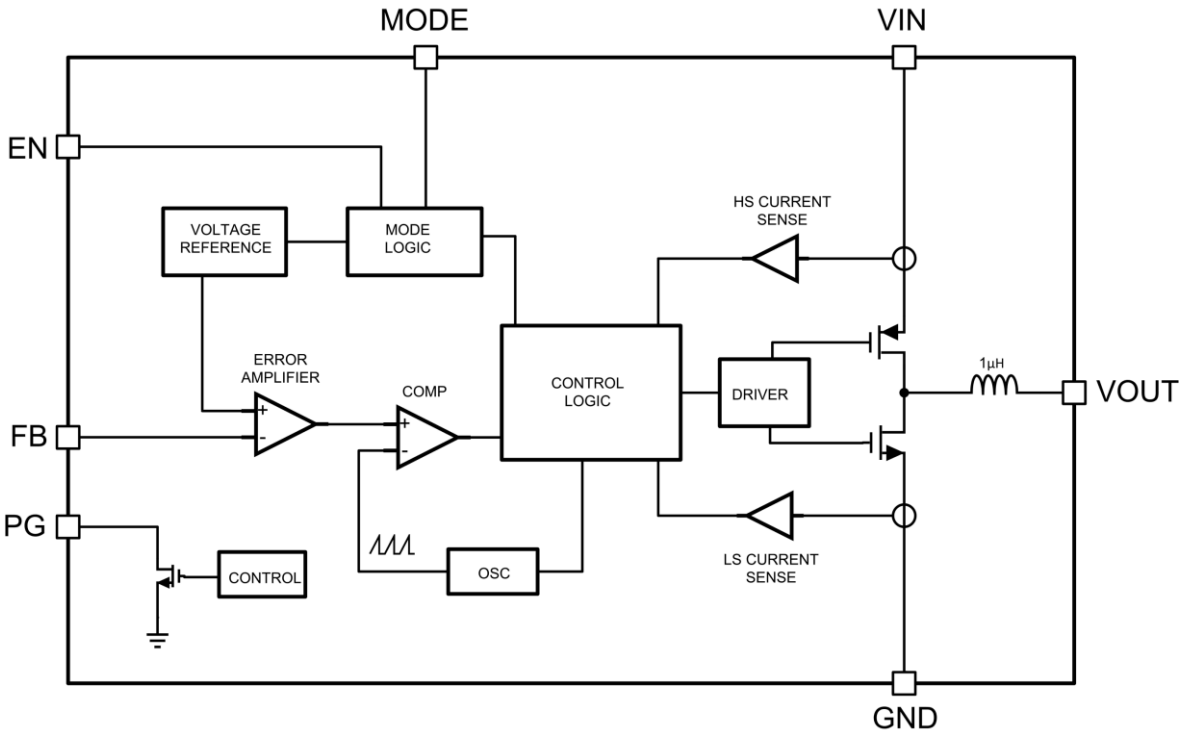
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7 Detailed Description

7.1 Overview

The LMZ20501 nano module is a voltage mode buck regulator with an integrated inductor. Input voltage feedforward is used to compensate for loop gain variation with input voltage. Two operating modes allow the user to tailor the regulator to their specific requirements. In forced PWM mode, the regulator operates as a full synchronous device with a 3 MHz (typical) switching frequency and very low output voltage ripple. In AUTO mode, the regulator moves into PFM when the load current drops below the mode change threshold (see 节 8.2.2). In PFM, the device regulates the output voltage between wider ripple limits than in PWM. This results in much smaller supply current than in PWM, at light loads, and high efficiency. A simplified block diagram is shown in 节 7.2.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Nano Scale Package

The LMZ20501 incorporates world class package technology to provide a 1-A power supply with a total volume of only 21 mm^3 (excluding external components). All that is required for a complete power supply is the addition of feedback resistors to set the output voltage and the input and output filter capacitors. 图 7-1 and 图 7-2 show the LMZ20501 package. The regulator die is embedded into a PCB substrate while the power inductor is mounted on top. Vias and copper clad are used to make the connections to the die, inductor, and the external components. This package is MSL3-compliant.

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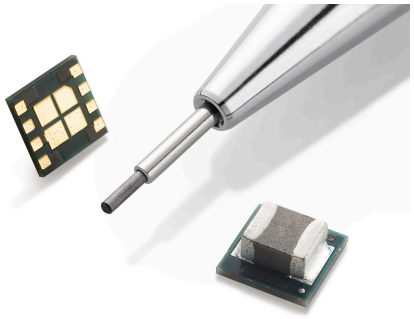


图 7-1. Package Photo

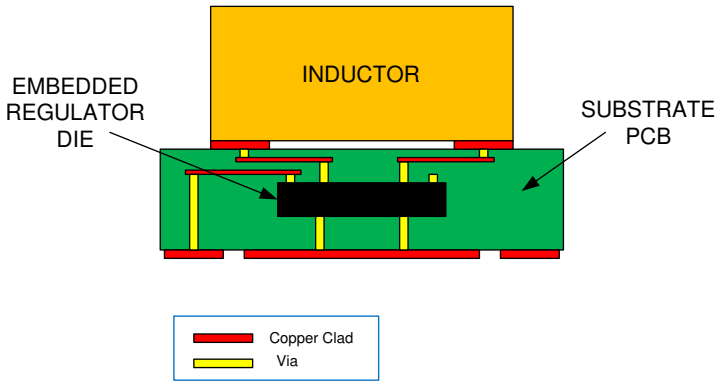


图 7-2. Package Side View Drawing

7.3.2 Internal Synchronous Rectifier

The LMZ20501 uses an internal NMOS FET as a synchronous rectifier to minimize switch voltage drop and increase efficiency. The NMOS is designed to conduct through its body diode during switch dead time. This dead time is imposed to prevent supply current "shoot-through".

7.3.3 Current Limit Protection

The LMZ20501 incorporates cycle-by-cycle peak current limit on both the high- and low-side MOSFETs. This feature limits the output current in case the output is overloaded. During the overload, the peak inductor current is limited to that value found in 节 6.5 under the heading of "I_{LIM}".

In addition to current limit, a short circuit protection mode is also implemented. When the feedback voltage is brought down to less than 300 mV, but greater than 150 mV, by a short circuit, the synchronous rectifier is turned off. This provides more voltage across the inductor to help maintain the required volt-second balance. If a "harder" short brings the feedback voltage to below 150 mV, the current limit and switching frequency are both reduced to approximately one half of the nominal values. In addition, when the current limit is tripped, the device stops switching for approximately 85 µs. At the end of the time-out, switching resumes and the cycle repeats until the short is removed.

The effect of both overload and short circuit protection can be seen in 图 7-3. This graph demonstrates that the device will supply slightly more than 1 A to the load when in overload and much less current during fold-back mode. This is typical behavior for any regulator with this type of current limit protection.

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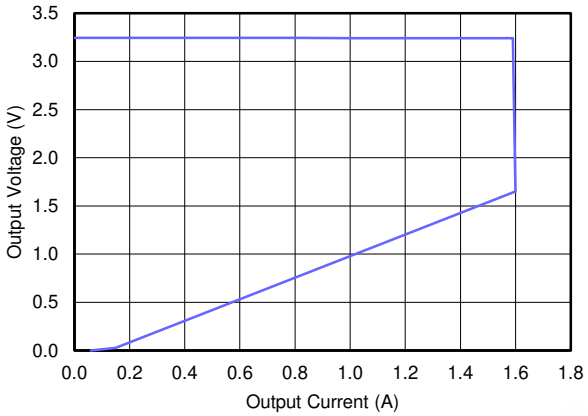


图 7-3. Typical Current Limit Profile V_{IN} = 5 V, V_{OUT} = 3.3 V

7.3.4 Start-Up

Start-up and shutdown of the LMZ20501 is controlled by the EN input. The characteristics of this input are found in 节 6.5. A valid input voltage must be present on VIN before the enable control is asserted. The maximum voltage on the EN pin is 5.5 V or V_{IN}, whichever is smaller. Do not allow this input to float.

The LMZ20501 features a current limit based soft start that prevents large inrush currents and output overshoots as the regulator is starting up. The peak inductor current is stepped-up in a staircase fashion during the soft start period. A typical start-up event is shown in 图 7-4:

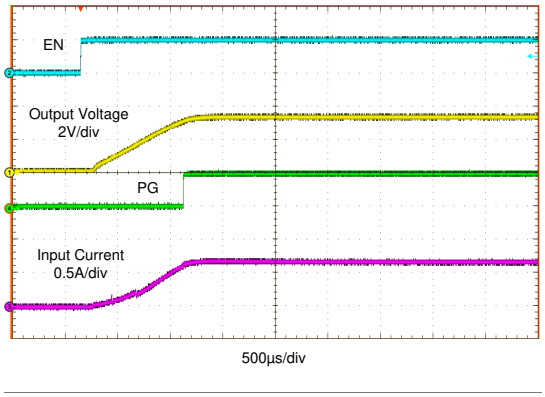


图 7-4. Typical Start-Up Waveforms, V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A

7.3.5 Dropout Behavior

When the input voltage is close to the output voltage, the regulator will operate at very large duty cycles. Normal time delays of the internal circuits prevents the attainment of controlled duty cycles near 100%. In this condition, the LMZ20501 will skip switching cycles to maintain regulation with the highest possible input-to-output ratio. Some increase in output voltage ripple can appear as the regulator skips cycles. As the input voltage gets closer to the output voltage, the regulator will eventually reach 100% duty cycle, with the high side switch turned on. The output will then follow the input voltage minus the drop across the high-side switch and inductor resistance. 图 7-5 and 图 7-6 show typical dropout behavior for output voltages of 2.5 V and 3.3 V.

Since the internal gate drive levels of the LMZ20501 are dependent on input voltage, the R_{dson} of the power FETs will increase at low input voltages. This will result in degraded efficiency at input voltages below approximately 2.9 V. Also, combinations of low input voltage and high output voltage increase the effective switch duty cycle, which can result in increased output voltage ripple.

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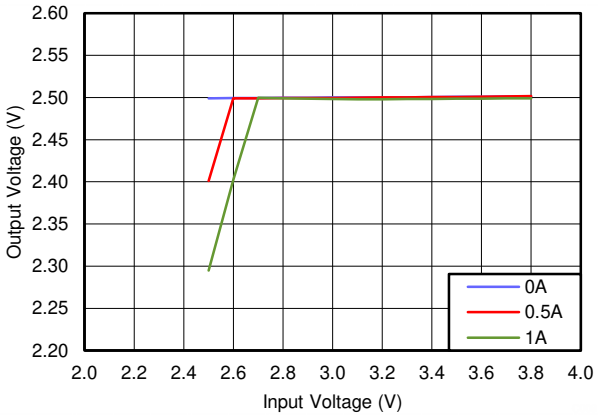


图 7-5. Typical Dropout Behavior, V_{OUT} = 2.5 V

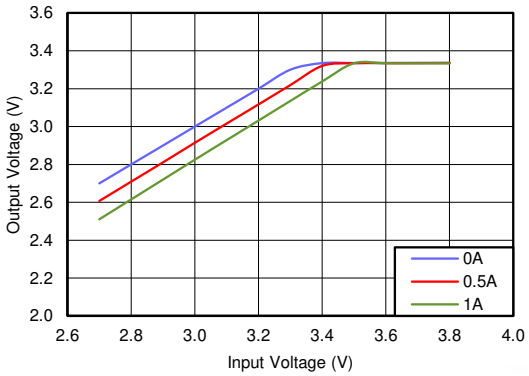


图 7-6. Typical Dropout Behavior, V_{OUT} = 3.3 V

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7.3.6 Power Good Flag Function

The operation of the power good flag function is described in the diagram shown in 图 7-7.

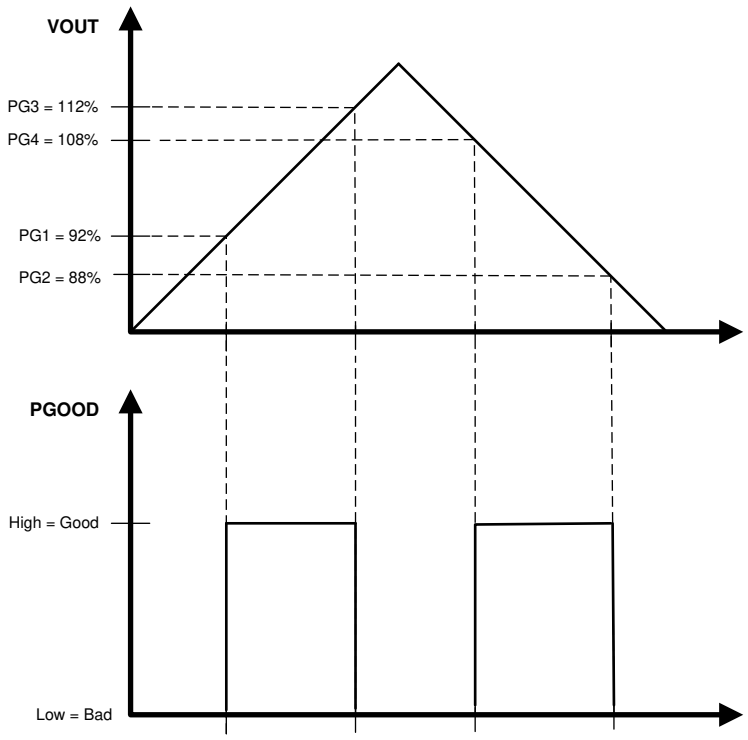


图 7-7. Typical Power Good-Flag Operation

This output consists of an open-drain NMOS with an R_{dson} of approximately 70 Ω. When used, the power-good flag should be connected to a logic supply through a pullup resistor. It can also be pulled up to either V_{IN} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PG output should be left floating. The current through this flag pin should be limited to less than 4 mA. A pullup resistor of greater than or equal to 1.5 kΩ will satisfy this requirement. When the EN input is pulled low, the PG flag output will also be forced low, assuming a valid input voltage is present at the VIN pin.

7.3.7 Thermal Shutdown

The LMZ20501 incorporates a thermal shutdown feature to protect the device from excessive die temperatures. The device will stop switching when the internal die temperature reaches about 159°C. Switching will resume when the die temperature drops to about 144°C.

7.4 Device Functional Modes

Please refer to 表 7-1 and the following paragraphs for a detailed description of the functional modes of the LMZ20501. These modes are controlled by the MODE input as shown in 表 7-1. The maximum voltage on the MODE pin is 5.5 V or V_{IN}, whichever is smaller. This input must not be allowed to float.

表 7-1. Mode Selection

MODE PIN VOLTAGE	OPERATION
> 1.2 V	Forced PWM: The regulator operates in constant frequency, PWM mode for all loads from no-load to full load; no diode emulation is used.
< 0.4 V	AUTO Mode: The regulator operates in constant frequency mode for loads greater than the mode change threshold. For loads less than the mode change threshold, the regulator operates in PFM with diode emulation.

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7.4.1 PWM Operation

In forced PWM mode, the converter operates as a constant frequency voltage mode regulator with input voltage feedforward. This provides excellent line and load regulation and low output voltage ripple. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. While in PWM mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This mode trades off reduced light load efficiency for low output voltage ripple and constant switching frequency. In this mode, a negative current limit of approximately 750 mA is imposed to prevent damage to the regulator power FETs.

7.4.2 PFM Operation

When in AUTO mode and at light loads, the device enters PFM. The regulator estimates the load current by measuring both the high-side and low-side switch currents. This estimate is only approximate, and the exact load current threshold, to trigger PFM, can vary greatly with input and output voltage. 节 8.2.2 shows mode change thresholds for several typical operating points. When the regulator detects this threshold, the reference voltage is increased by approximately 10 mV. This causes the output voltage to rise to meet the new regulation point. When this point is reached, the converter stops switching and much of the internal circuitry is shut off, while the reference is returned to the PWM value. This saves supply current while the output voltage naturally starts to fall under the influence of the load current. When the output voltage reaches the PWM regulation point, switching is again started and the reference voltage is again increased by approximately 10 mV, starting the next cycle. Typical waveforms are shown in 图 7-8.

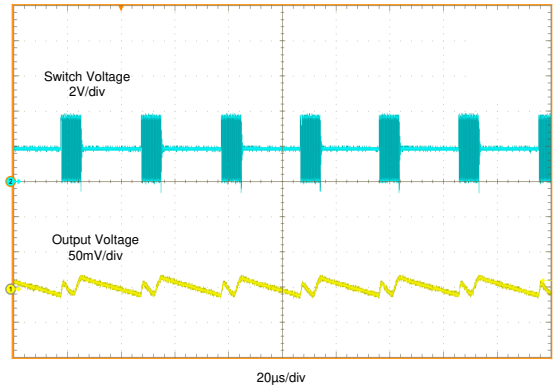


图 7-8. Typical PFM Mode Waveforms: V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA

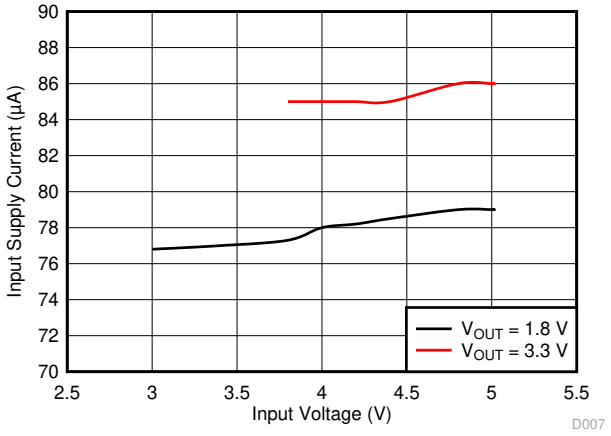


图 7-9. Typical No Load Input Supply Current

The actual output voltage ripple will depend on the feedback divider ratio and on the delay in the PFM comparator. The frequency of the PFM "bursts" will depend on the input voltage, output voltage, load, and output

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capacitor. Within each "burst", the device switches at 3 MHz (typical). If the load current increases above the threshold, normal PWM operation is resumed. This mode provides high light load efficiency by reducing the amount of supply current required to regulate the output at small load currents. This mode trades off very good light load efficiency for larger output voltage ripple and variable switching frequency. An example of the typical input supply current while regulating with no load is shown in 图 7-9.

Because of normal part-to-part variation, the LMZ20501 may not switch into PFM mode at high input voltages. This can be seen with output voltages of approximately 1.2 V and below, and at input voltages of approximately 4.2 V and above.

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8 Application and Implementation

Note

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8.1 Application Information

The LMZ20501 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMZ20501. Alternately, the WEBENCH design tool may be used to generate a complete design. WEBENCH utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

8.2 Typical Application

图 8-1 shows the minimum required application circuit for a 1.8-V output. 图 8-2 shows a full featured application circuit. Please refer to 图 8-1 and 图 8-2 during the following design procedures.

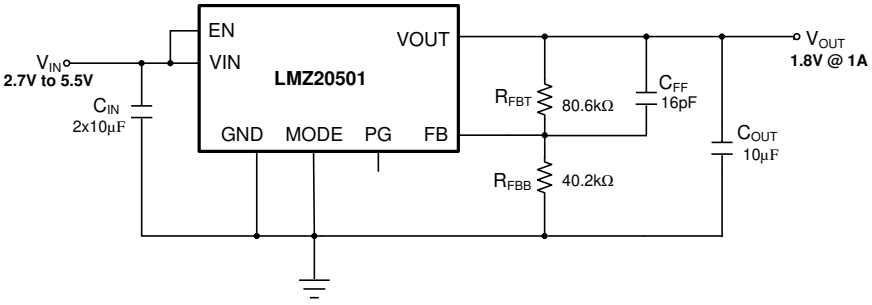


图 8-1. LMZ20501 Typical Application V_{OUT} = 1.8 V

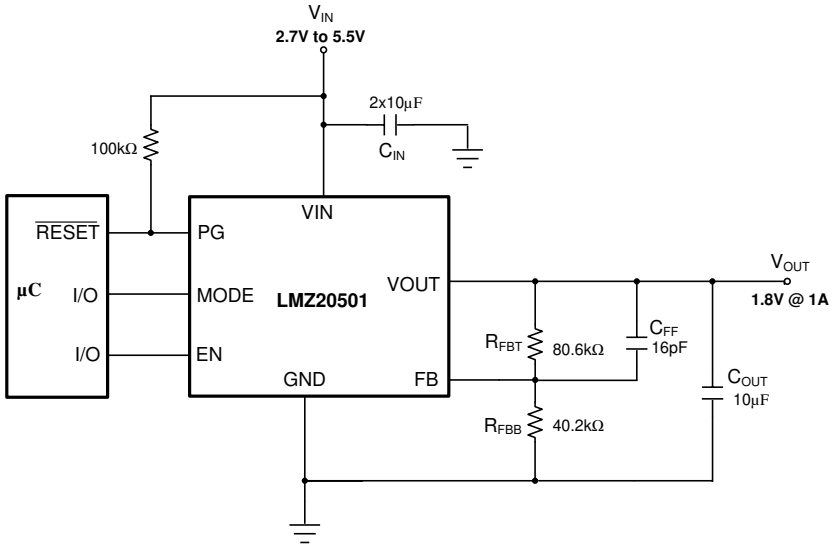


图 8-2. LMZ20501 Full Featured Application

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8.2.1 Detailed Design Procedure

Please refer to 表 8-1 while following the detailed design procedure. This procedure applies to both 图 8-1 and to 图 8-2. Also, the *Application Curves* apply to both schematics.

表 8-1. Recommended Component Values

V_{OUT} (V)	R_{FBB} (kΩ)	R_{FBT} (kΩ)	C_{OUT} (µF)	EFFECTIVE C_{OUT} (µF)(2)	C_{FF} (pF)	C_{IN} (µF)(1)	EFFECTIVE C_{IN} (µF)(2)
0.8	121	40.2	2 x 10	18 µF	39	2 x 10	14
1.2	30.1	30.1	10	8.8 µF	20	2 x 10	14
1.8	40.2	80.6	10	8.4 µF	16	2 x 10	14
2.5	47.5	150	10	7.8 µF	12	2 x 10	14
3.3	53.2	237	10	7.1 µF	82	2 x 10	14
3.6	53.2	267	10	6.8 µF	82	2 x 10	14

(1) C_{IN} = C_{OUT} = 10 µF, 16 V, 0805, X7R, Samsung CL21B106KOQNNNE. C_{OUT} measured at V_{OUT}; C_{IN} measured at 3.3 V.
(2) The effective value takes into account the capacitor voltage coefficient.

8.2.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ20501 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2 Setting The Output Voltage

The LMZ20501 regulates its feedback voltage to 0.6 V (typical). A feedback divider, shown in 图 8-1, is used to set the desired output voltage. 方程式 1 can be used to select R_{FBB}.

$$R_{FBB} = \frac{0.6}{(V_{OUT} - 0.6)} \cdot R_{FBT} \quad (1)$$

For the best results, R_{FBT} should be chosen between 30 kΩ and 300 kΩ. See 表 8-1 for recommended values for typical output voltages.

8.2.1.3 Output and Feedforward Capacitors

The LMZ20501 is designed to work with low-ESR ceramic capacitors. The **effective** value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have large voltage coefficients, in addition to normal tolerances and temperature coefficients. Under D.C. bias, the capacitance value drops considerably. Larger case sizes, higher voltage capacitors, or both are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum **effective** capacitance up to the desired value. This can also ease the RMS current requirements on a single capacitor. Typically, 10-V, X5R, 0805 capacitors are adequate for the output, while 16-V capacitors can be used on the input. Some recommended component values are provided in 表 8-1. Also, shown are the measured values of **effective** input and output capacitance for the given capacitor. If smaller values of output capacitance are used,

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C_{FF} must be adjusted to give good phase margin. In any case, load transient response will be compromised with lower values of output capacitance. Values much lower than those found in 表 8-1 should be avoided.

In practice, the output capacitor and C_{FF} are adjusted for the best transient response and highest loop phase margin. Load transient testing and Bode plots are the best way to validate any given design. The *Optimizing Transient Response of Internally Compensated DC-DC Converters Application Report* should prove helpful when optimizing the feedforward capacitor. Also, the *AN-1889 How to Measure the Loop Transfer Function of Power Supplies Application Report* details a simple method of creating a Bode plot with basic laboratory equipment. The values of C_{FF} found in 表 8-1 provide a good starting point.

A careful study of the temperature and bias voltage variation of any candidate ceramic capacitor should be made in order to make sure that the minimum values of **effective** capacitance are provided. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH tool.

The maximum value of total output capacitance should be limited to between 100 µF and 200 µF. Large values of output capacitance can prevent the regulator from starting-up correctly and adversely affect the loop stability. If values in the range given above, or larger, are to be used, then a careful study of start-up at full load and loop stability must be performed.

8.2.1.4 Input Capacitors

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. An **effective** value of at least 14 µF is normally sufficient for the input capacitor. If the main input capacitor or capacitors cannot be placed close to the module, then a small 10 nF to 100 nF capacitor should be placed directly at the module across the supply and ground pins.

Many times, it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by long power leads. This method can also help to reduce voltage spikes that can exceed the maximum input voltage rating of the LMZ20501. The use of this additional capacitor will also help with voltage dips caused by input supplies with unusually high impedance.

Most of the switching current passes through the input ceramic capacitor or capacitors. The approximate RMS value of this current can be calculated with 方程式 2 and should be checked against the manufactures maximum ratings.

$$I_{RMS} \approx \frac{I_{OUT}}{2} \tag{2}$$

8.2.1.5 Maximum Ambient Temperature

As with any power conversion device, the LMZ20501 will dissipate internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature is a function of the ambient temperature, the power loss, and the effective thermal resistance $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMZ20501 is 125°C, thus establishing a limit on the maximum device power dissipation and, therefore, load current at high ambient temperatures. 方程式 3 shows the relationships between the important parameters.

$$I_{OUT} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \tag{3}$$

It is easy to see that larger ambient temperatures and larger values of $R_{\theta JA}$ will reduce the maximum available output current. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the values given in the *Thermal Information* table are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that never obtain in an actual application. The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation

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- Air temperature
- PCB area
- Copper heatsink area
- Air flow
- Adjacent component placement

The resources found in 表 11-1 can be used as a guide to estimate the $R_{\theta JA}$ for a given application environment. A typical example of $R_{\theta JA}$ versus copper board area is shown in 图 8-3. The copper area in this graph is that for each layer; the inner layers are 1 oz (35µm). An $R_{\theta JA}$ of 44°C/W is the approximate value for the LMZ20501 evaluation board. The efficiency found in 方程式 3, η, should be taken at the elevated ambient temperature. For the LMZ20501, the efficiency is approximately two to three percent lower at high temperatures. Therefore, a slightly lower value than the typical efficiency can be used in the calculation. In this way, 方程式 3 can be used to estimate the maximum output current for a given ambient, or to estimate the maximum ambient for a given load current.

A typical curve of maximum load current versus ambient temperature is shown in 图 8-4. This graph assumes a $R_{\theta JA}$ of 44°C/W and an input voltage of 5 V.

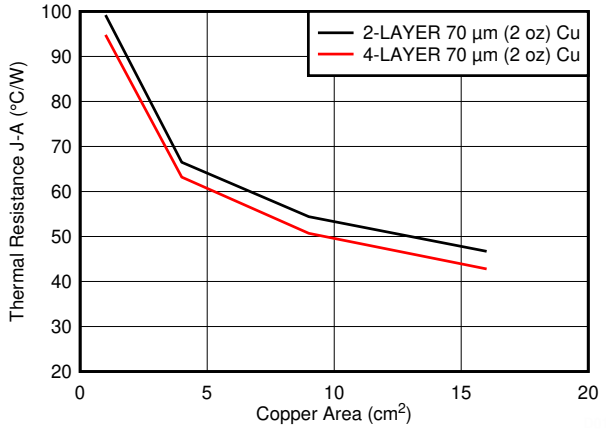


图 8-3. $R_{\theta JA}$ Versus Copper Board Area

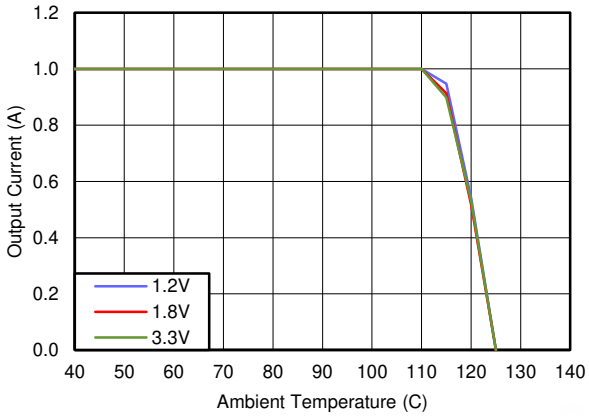


图 8-4. Maximum Output Current Versus Ambient Temperature, $R_{\theta JA}$ = 44°C/W, V_{IN} = 5 V

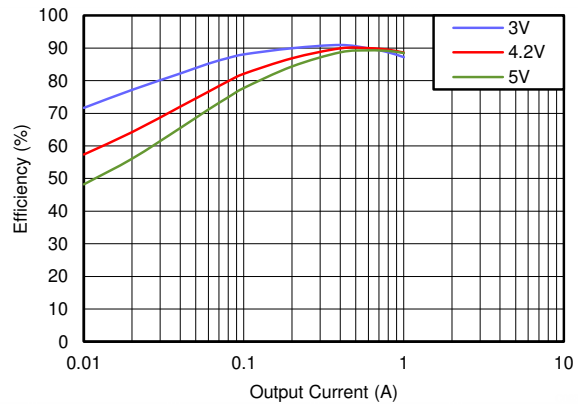
8.2.1.6 Options

The circuit in 图 8-2 highlights the use of the features of the LMZ20501. The PG output is open drain, and requires a pullup resistor to a logic supply that is commensurate with the system logic voltage levels. If a reset function is not needed, the PG pin should be left open. The EN and MODE inputs are digital inputs, requiring only simple logic levels for proper operation. If the system does not need to control these features, the inputs should be connected to either VIN or GND, as appropriate. See 节 7.3 for details.

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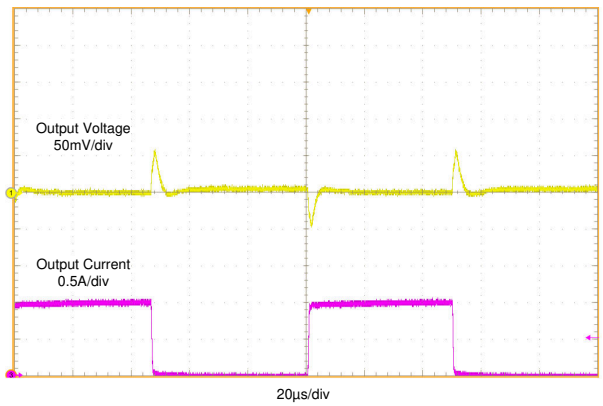
8.2.2 Application Curves

The following specifications apply to the circuit found in 图 8-1 or 图 8-2 with the appropriate modifications from 表 8-1. **These parameters are not tested and represent typical performance only.** Unless otherwise stated the following conditions apply: T_A = 25°C.



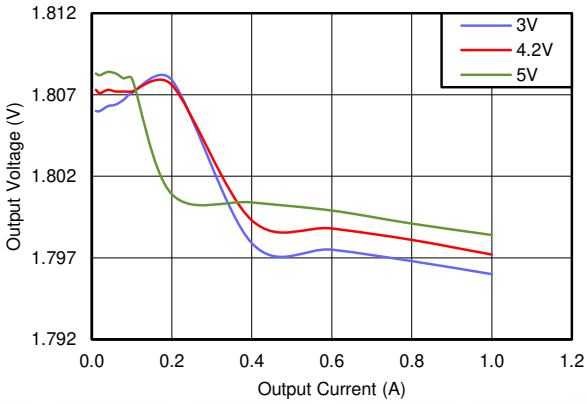
V_{OUT} = 1.8 V

图 8-5. Efficiency



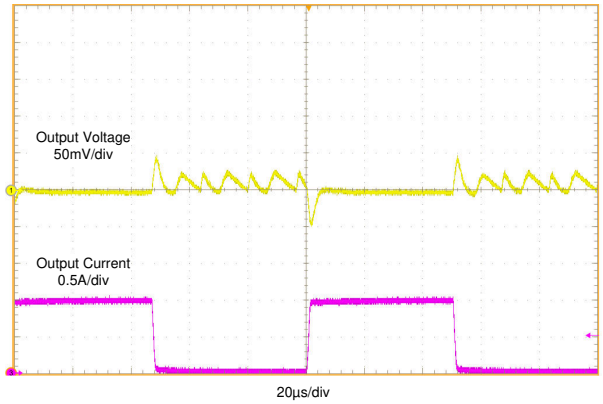
V_{OUT} = 1.8 V V_{IN} = 4.2 V

图 8-6. Load Transient In PWM



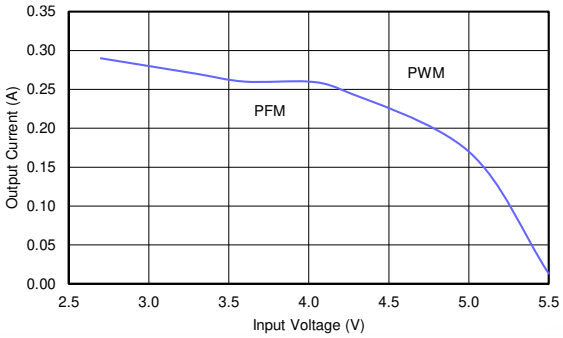
V_{OUT} = 1.8 V

图 8-7. Regulation, AUTO Mode



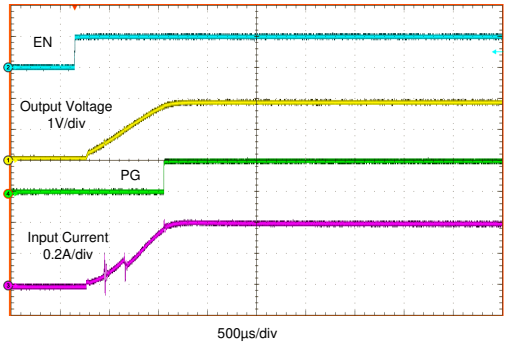
V_{OUT} = 1.8 V V_{IN} = 4.2 V

图 8-8. Load Transient In AUTO Mode



V_{OUT} = 1.8 V

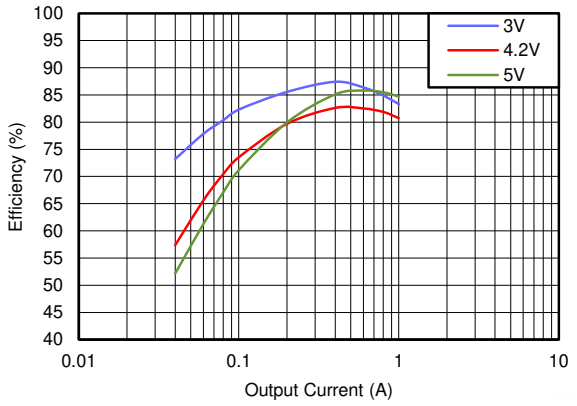
图 8-9. AUTO Mode Thresholds



V_{OUT} = 1.8 V V_{IN} = 5 V I_{OUT} = 1 A

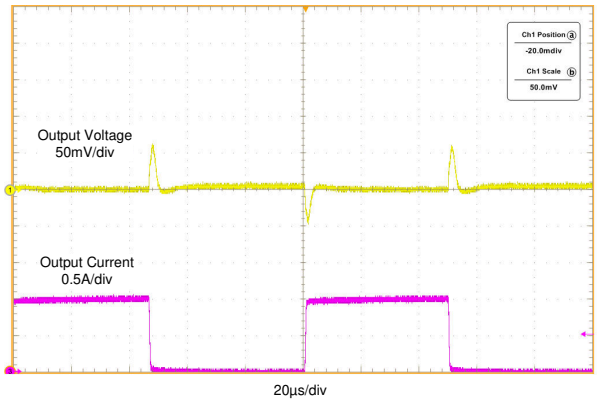
图 8-10. Start-Up

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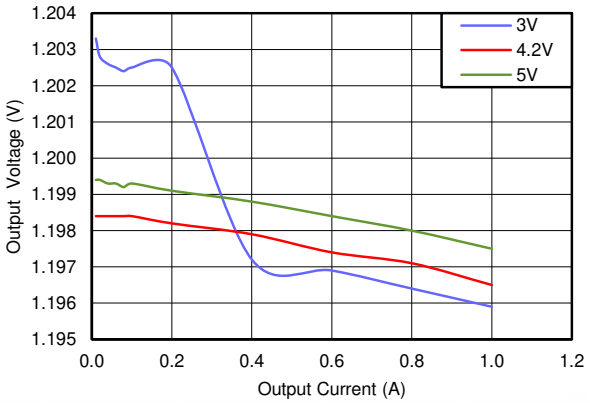
V_{OUT} = 1.2 V

图 8-11. Efficiency



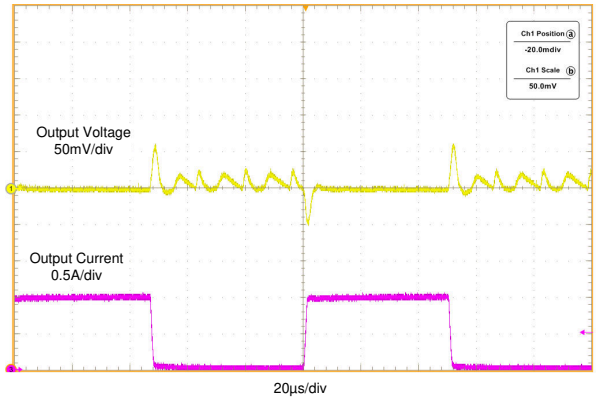
V_{OUT} = 1.2 V V_{IN} = 4.2 V

图 8-12. Load Transients In PWM



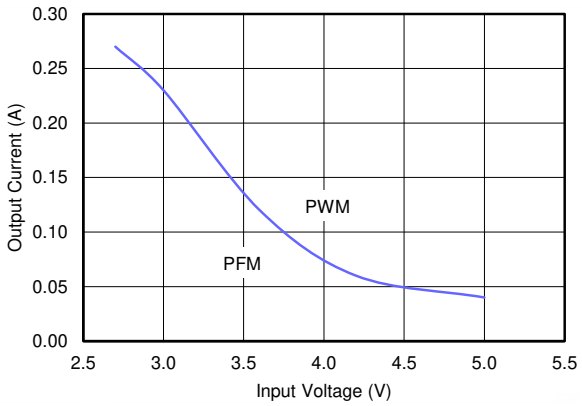
V_{OUT} = 1.2 V

图 8-13. Regulation, AUTO Mode



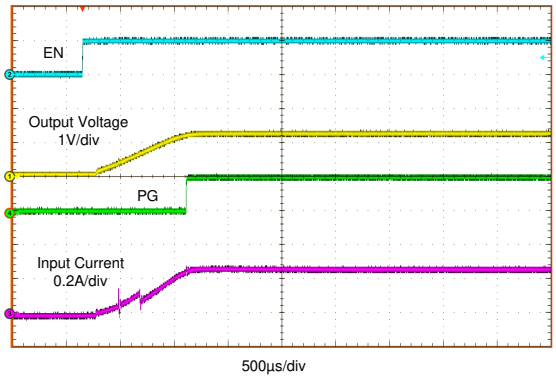
V_{OUT} = 1.2 V V_{IN} = 4.2 V

图 8-14. Load Transients In AUTO Mode



V_{OUT} = 1.2 V

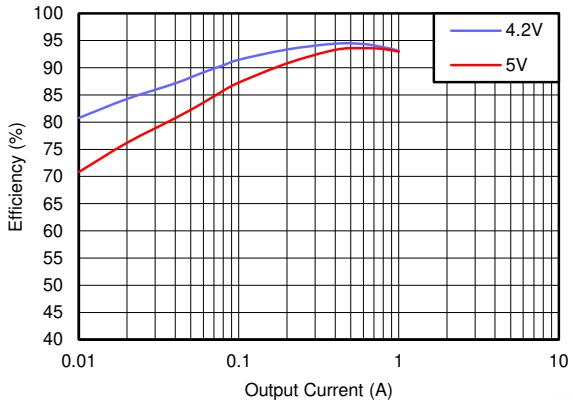
图 8-15. AUTO Mode Thresholds



V_{OUT} = 1.2 V V_{IN} = 5 V I_{OUT} = 1 A

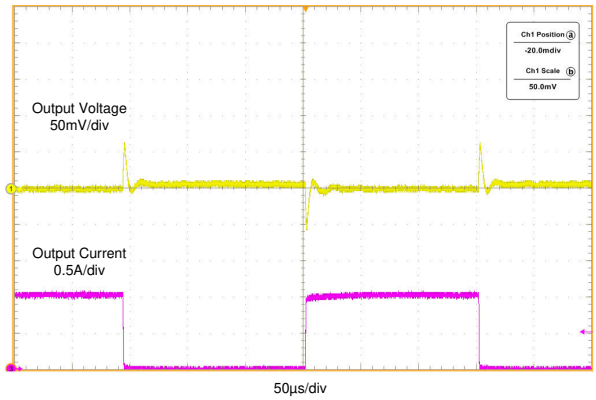
图 8-16. Start-Up

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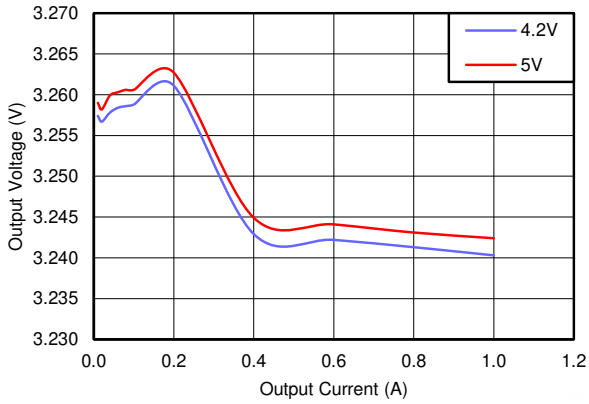
V_{OUT} = 3.3 V

图 8-17. Efficiency



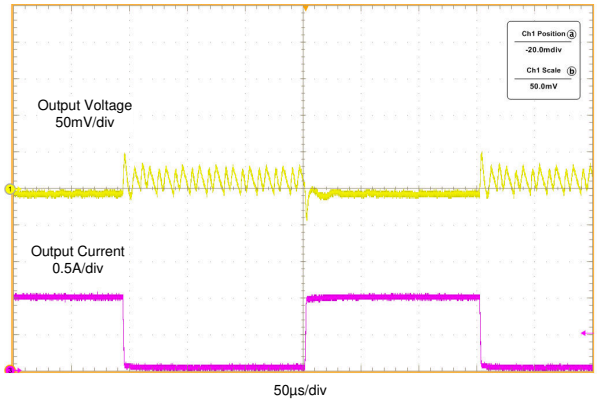
V_{OUT} = 3.3 V V_{IN} = 5 V

图 8-18. Load Transients In PWM Mode



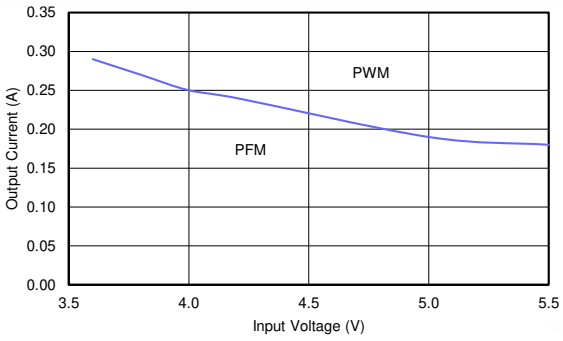
V_{OUT} = 3.3 V

图 8-19. Regulation, AUTO Mode



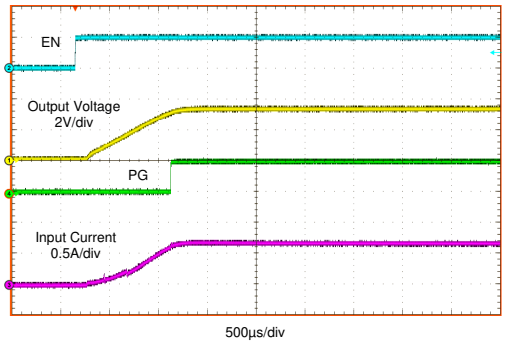
V_{OUT} = 3.3 V V_{IN} = 5 V

图 8-20. Load Transients In AUTO Mode



V_{OUT} = 3.3 V

图 8-21. AUTO Mode Thresholds



V_{OUT} = 3.3 V V_{IN} = 5 V I_{OUT} = 1 A

图 8-22. Start-Up

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8.3 Do's and Don'ts

- **Don't:** Exceed the *Absolute Maximum Ratings*.
- **Don't:** Exceed the *ESD Ratings*.
- **Don't:** Exceed the *Recommended Operating Conditions*.
- **Don't:** Allow the EN or MODE input to float.
- **Don't:** Allow the voltage on the EN or MODE input to exceed the voltage on the VIN pin.
- **Don't:** Allow the output voltage to exceed the input voltage.
- **Don't:** Use the thermal data given in the *Thermal Information* table to design your application.
- **Do:** Follow all of the guidelines and suggestions found in this data sheet before committing your design to production. TI Application Engineers are ready to help critique your design and PCB layout to help make your project a success.
- **Do:** Refer to the helpful documents found in 表 11-1 and 表 11-2

.

9 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 方程式 4

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{4}$$

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit can cause overvoltage transients at the VIN pin, each time the input supply is cycled on and off. The parasitic resistance will cause the voltage at the VIN pin to dip when the load on the regulator is switched on, or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip can cause the device to shutdown, reset, or both. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator, use an aluminum or tantalum input capacitor in parallel with the ceramics, or both. The moderate ESR of these types of capacitors will help to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator module. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The following user guide provides helpful suggestions when designing an input filter for any switching regulator: *AN-2162 Simple Success With Conducted EMI From DC-DC Converters Application Report*.

In some cases, a Transient Voltage Suppressor (TVS) is used on the input of regulators. One class of this device has a "snap-back" V-I characteristic (thyristor type). The use of a device with this type of characteristic is not recommend. When the TVS "fires", the clamping voltage drops to a very low value. If this holding voltage is less than the output voltage of the regulator, the output capacitors will be discharged through the regulator back to the input. This uncontrolled current flow could damage the regulator.

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10 Layout

10.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor and the module ground, as shown in 图 10-1. This loop carries fast transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop should be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 图 10-2 shows a recommended layout for the critical components of the LMZ20501; the top side metal is shown in red. This PCB layout is a good guide for any specific application. The following important guidelines should also be followed:

1. **Place the input capacitor CIN as close as possible to the VIN and GND terminals.** VIN (pin 8) and GND (pin 6) are on the same side of the module, simplifying the input capacitor placement.
2. **Place the feedback divider as close as possible to the FB pin on the module.** The divider and C_{FF} should be close to the module, while the length of the trace from VOUT to the divider can be somewhat longer. However, this latter trace should not be routed near any noise sources that can capacitively couple to the FB input.
3. **Connect the EP pad to the GND plane.** This pad acts as a heat-sink connection and a ground connection for the module. It must be solidly connected to a ground plane. The integrity of this connection has a direct bearing on the effective $R_{\theta JA}$.
4. **Provide enough PCB area for proper heat-sinking.** As stated in 节 8.2.1.5, enough copper area must be used to provide a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers should be made with two ounce copper; and no less than one ounce.
5. **The resources in 表 11-2 provide additional important guidelines.**

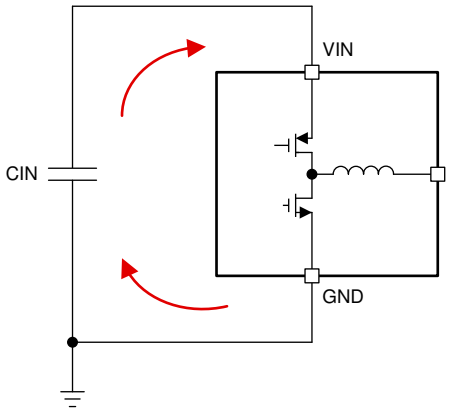


图 10-1. Current Loops With Fast Transient Currents

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10.2 Layout Example

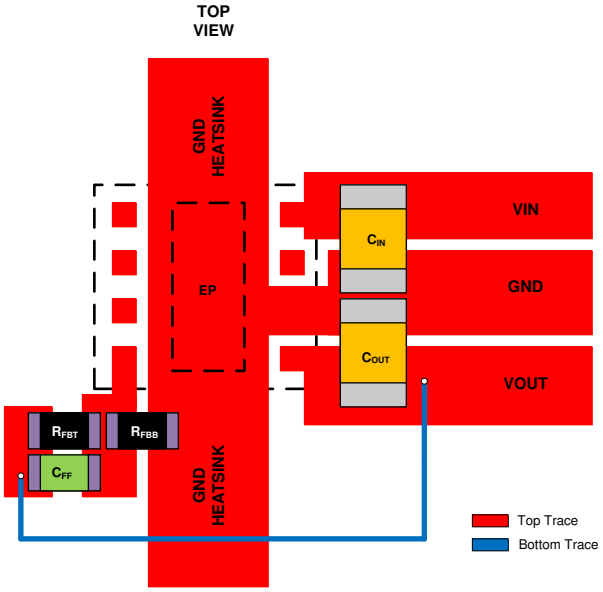


图 10-2. Example PCB Layout

10.2.1 Soldering Information

Proper operation of the LMZ20501 requires that it be correctly soldered to the PCB. This is especially true regarding the EP. This pad acts as a quiet ground reference for the device and a heatsink connection. Use the following recommendations when utilizing machine placement of the device:

- Dimension of area for pickup: 2 mm × 2.5 mm
- Use a nozzle size of less than 1.3 mm in diameter, so that the head does not touch the outer area of the package.
- Use a soft tip pick-and-place head.
- Add 0.05 mm to the component thickness so that the device will be released 0.05 mm into the solder paste without putting pressure or splashing the solder paste.
- Slow the pick arm when picking the part from the tape and reel carrier and when depositing the device on the board.
- If the machine releases the component by force, use the minimum force and no more than 3 N.
- For PCBs with surface mount components on both sides, it is suggested to put the LMZ20501 on the top side. In case the application requires bottom side placement, a re-flow fixture can be required to protect the module during the second reflow.

In addition, please follow the important guidelines found in the *AN-1187 Leadless Leadframe Package (LLP) Application Report*. The curves in 图 10-3 and 图 10-4 show typical soldering temperature profiles.

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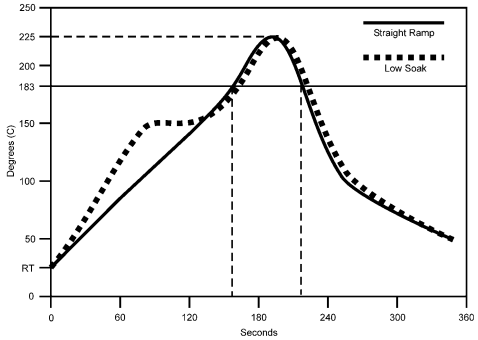


图 10-3. Typical Re-flow Profile Eutectic (63sn/37pb) Solder Paste

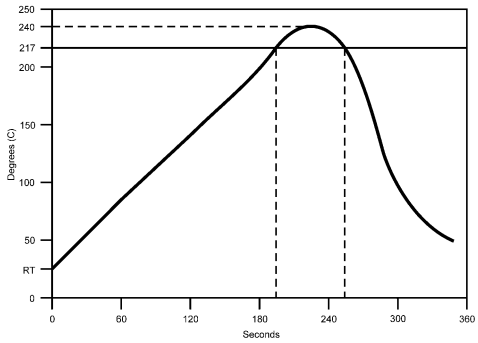


图 10-4. Typical Re-flow Profile Lead-Free (Sca305 Or Sac405) Solder Paste

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11 Device and Documentation Support

11.1 Device Support

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ20501 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

表 11-1. Resources For Estimating $R_{\theta JA}$

TITLE	LINK
AN-2020 *Thermal Design By Insight, Not Hindsight*	SNVA419
AN-2026 *The Effect of PCB Design on the Thermal Performance of SIMPLE SWITCHER Power Modules*	SNVA424
AN-1520 *A Guide to Board Layout for Best Thermal Resistance for Exposed Packages*	SNVA183
AN-1187 *Leadless Lead-frame Package (LLP)*	SNOA401
SPRA953B *Semiconductor and IC Package Thermal Metrics*	SPRA953

表 11-2. PCB Layout Resources

TITLE	LINK
AN-1149 *Layout Guidelines for Switching Power Supplies*	SNVA021
AN-1229 *SIMPLE SWITCHER PCB Layout Guidelines*	SNVA054
Constructing Your Power Supply- Layout Considerations	SLUP230

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11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

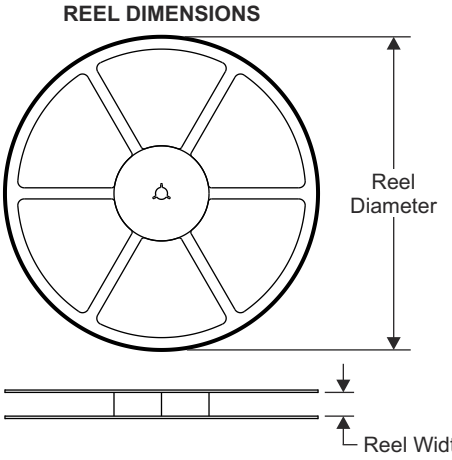
TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

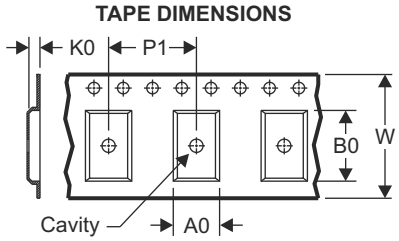
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12 Mechanical, Packaging, and Orderable Information

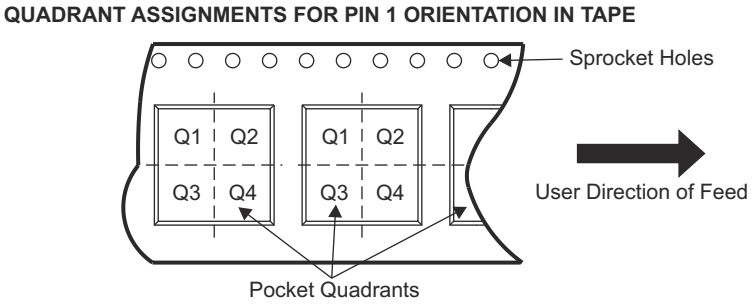
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information





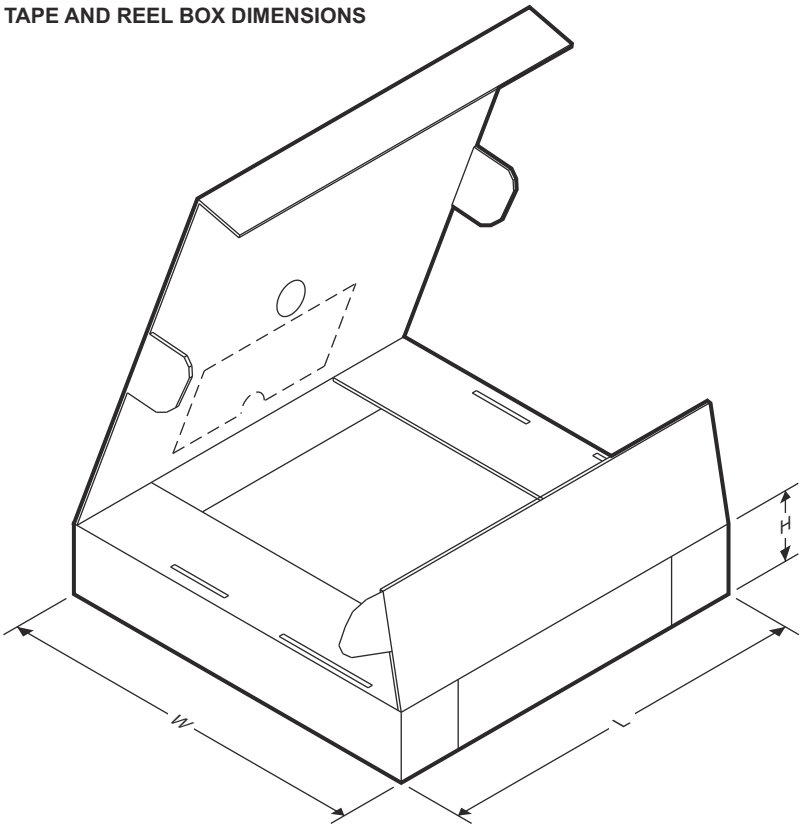
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ20501SILR	uSiP	SIL	8	3000	330.0	12.4	3.75	3.75	2.2	8.0	12.0	Q2
LMZ20501SILT	uSiP	SIL	8	250	178.0	13.2	3.75	3.75	2.2	8.0	12.0	Q2

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ20501SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
LMZ20501SILT	uSiP	SIL	8	250	223.0	194.0	35.0

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZ20501SILR	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	1501 7543 EB
LMZ20501SILR.A	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	1501 7543 EB
LMZ20501SILT	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	1501 7543 EB
LMZ20501SILT.A	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	1501 7543 EB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

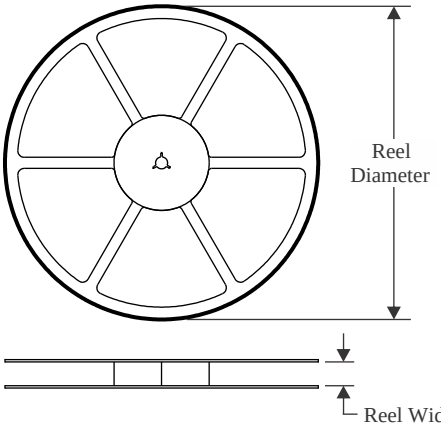
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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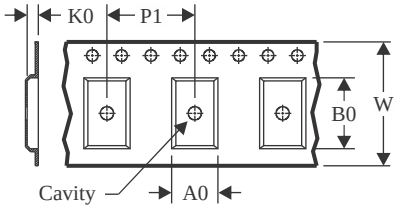
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TAPE AND REEL INFORMATION

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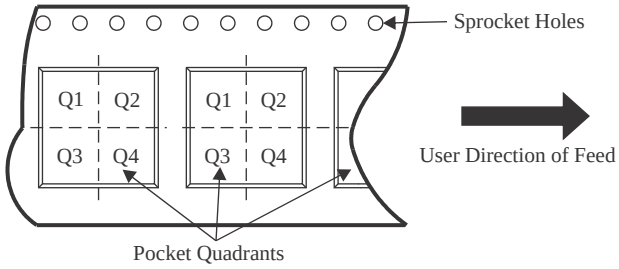


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

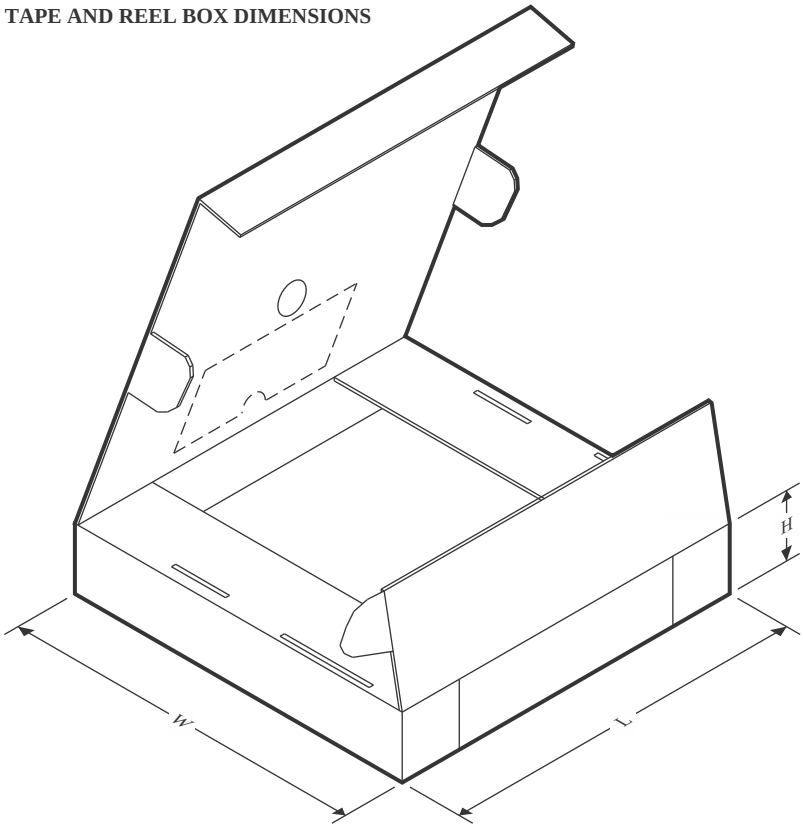
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ20501SILR	uSiP	SIL	8	3000	330.0	12.4	3.75	3.75	2.2	8.0	12.0	Q2
LMZ20501SILT	uSiP	SIL	8	250	178.0	13.2	3.75	3.75	2.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ20501SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
LMZ20501SILT	uSiP	SIL	8	250	223.0	194.0	35.0

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