LMZM33606 3.5V 至 36V 输入、1V 至 20V 输出、6A 电源模块

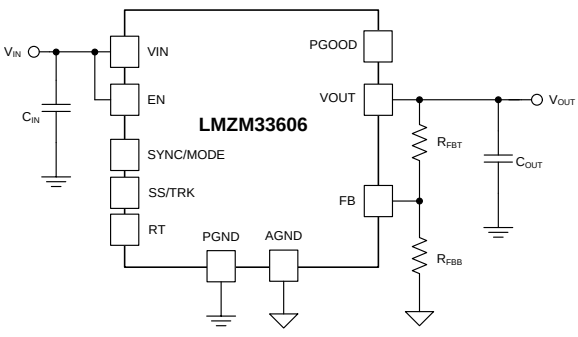
1 特性

- 较小的总体解决方案尺寸：< 250mm^2
  - 所需的外部组件数低至 4 个
  - 16mm × 10mm × 4mm QFN 封装
- 支持 5V、12V、24V、28V 输入电源轨
  - 1V 至 20V 输出电压范围
  - 引脚与 4A LMZM33604 兼容
- 符合 EN55011 辐射发射标准
- 可配置为负输出电压
- 用于实现 设计灵活性的 可调节功能
  - 开关频率（350kHz 至 2.2MHz）
  - 可与外部时钟保持同步
  - 可选自动模式或 FPWM 模式
    - 自动：提升轻负载下的效率
    - FPWM：在整个负载上具有固定频率
  - 可调软启动和跟踪输入
  - 精密使能功能，用于对系统 UVLO 进行编程
- 保护 特性
  - 断续模式电流限制
  - 过热保护
  - 电源正常输出
- 可在恶劣环境中运行
  - 在 85°C 且无气流的情况下具有高达 50W 的输出功率
  - 工作结温范围：–40°C 至 +125°C
  - 工作环境温度范围：–40°C 至 +105°C
  - 通过了 Mil-STD-883D 冲击和振动测试

2 应用

- 工业、医疗和测试设备
- 通用宽输入电压稳压
- 反相输出 应用

简化电路原理图



3 说明

LMZM33606 电源模块是一款易于使用的集成式电源解决方案，它在一个低厚度的封装内整合了一个带有功率 MOSFET 的 6A 直流/直流转换器、一个屏蔽式电感器和多个无源器件。此电源解决方案仅需四个外部组件，并且省去了设计流程中的环路补偿和电感器元件选择过程。

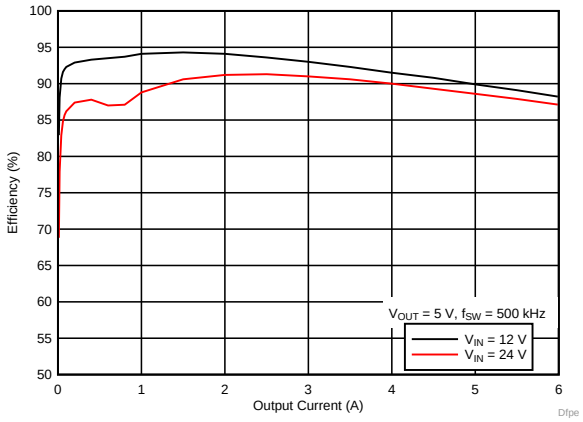
该器件采用 16mm × 10mm × 4mm、41 引脚 QFN 封装，可轻松焊接到印刷电路板上，并可实现紧凑的低厚度负载点设计。LMZM33606 的全套功能包括电源正常指示、可调节软启动、跟踪、同步、可编程 UVLO、预偏置启动、可选自动或 FPWM 模式以及过流和过热保护。可针对反相应用将 LMZM33606 配置为负输出电压。

器件信息

器件型号	封装	封装尺寸（标称值）
LMZM33606	QFN (41)	16.00mm × 10.00mm

最小解决方案尺寸

典型效率（自动模式）



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (October 2018) to Revision B **Page**

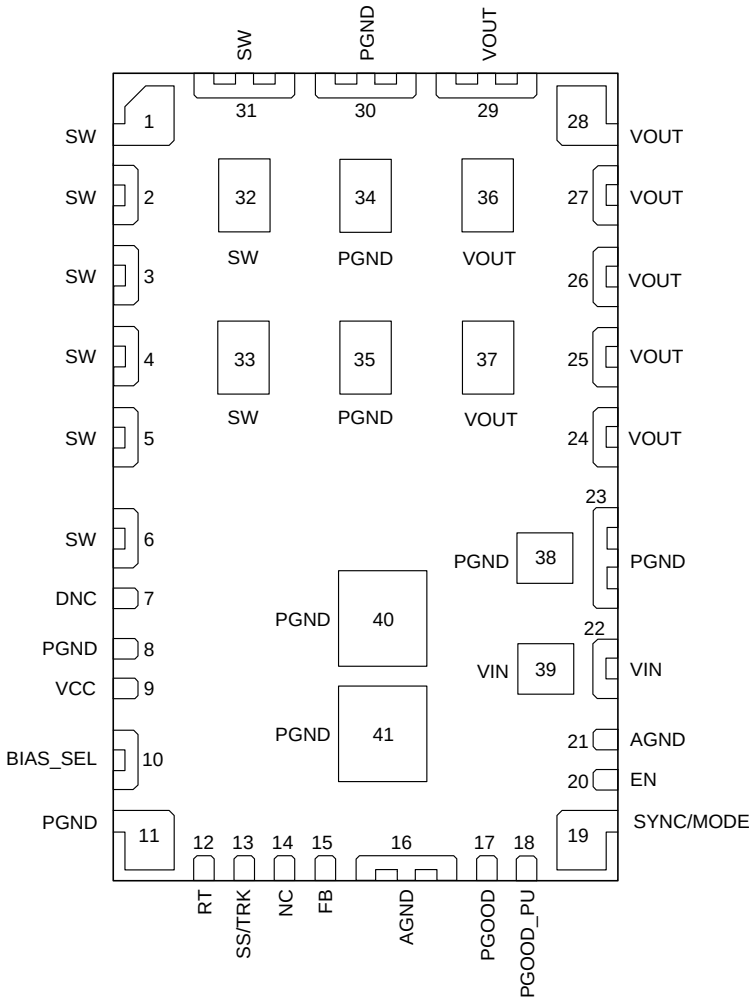
- 已添加 information on internal LDO and BIAS_SEL ... 22

Changes from Original (June 2018) to Revision A **Page**

- 首次发布生产数据数据表 ... 1

5 Pin Configuration and Functions

RLX Package
41-Pin QFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	16, 21	G	Analog ground. Zero voltage reference for internal references and logic. These pins are not connected to one another internal to the device and must be connected to one another externally. Do not connect these pins to PGND; the AGND to PGND connection is made internal to the device. See the *Layout* section of the datasheet for a recommended layout.
BIAS_SEL	10	I	Optional BIAS LDO supply input. An internal 470 nF capacitor is placed between this pin and PGND. Do not float; tie to PGND if not used. Tie to VOUT if 3.3 V ≤ VOUT ≤ 18 V, or tie to an external 3.3-V or 5-V rail if available to improve efficiency.
DNC	7	—	Do not connect. This pin is connected to internal circuitry. Do not connect this pin to AGND, PGND, or any other voltage. **This pin must be soldered to an isolated pad.**.
EN	20	I	Precision enable input to regulator. Do not float. High = ON, Low = OFF. Can be tied to VIN. Precision enable input allows adjustable system UVLO using external resistor divider.
FB	15	I	Feedback input. Connect the center point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND.
NC	14	—	Not internally connected.
PGND	8, 11, 23, 30, 34, 35, 38, 40, 41	G	Power ground. This is the return current path for the power stage of the device. Connect these pins to the low side of the input source, load, and bypass capacitors associated with VIN and VOUT using power ground planes on the PCB. Not all pins are connected to PGND internal to the device; connections must be made externally. Connect pad 40 and 41 to the ground planes using multiple vias for good thermal performance.
PGOOD	17	O	Open drain output for power-good flag. Internal to the device, a 100-kΩ pullup resistor is placed between this pin and the PGOOD_PU pin.
PGOOD_PU	18	I	Power-good pull-up supply. Connect to logic rail or other DC voltage no higher than 20 V.
RT	12	I	An external timing resistor connected between this pin and AGND adjusts the switching frequency of the device. If floating, the default switching frequency is 500 kHz. Do not short to ground.
SS/TRK	13	I	Soft start / tracking control pin. Leave this pin floating to use the 5-ms internal soft-start ramp.To increase the internal soft start ramp time, simply connect a capacitor between this pin and AGND. This pin sources 2-μA of current to charge this external capacitor. Connect to external voltage ramp for tracking. Do not connect to ground.
SW	1, 2, 3, 4, 5, 6, 31, 32, 33	O	Switch node. Connect these pins to a small copper island under the device for thermal relief. Do not place any external components on these pins or tie them to a pin of another function.
SYNC/MODE	19	I	Synchronization input and Mode setting pin. Do not float; tie to AGND or logic high if not used. Connect to an external clock to synchronize (see *Synchronization (SYNC/MODE)*). Connect to AGND to select Auto mode or connect to logic high to select FPWM mode. (see *Mode Select (Auto or FPWM)*).
VCC	9	O	Output of internal bias supply. Used to supply internal control circuits and drivers. Do not place any external component on this pin or tie it to a pin of another function.
VIN	22, 39	I	Input supply voltage. Connect external input capacitors between these pins and PGND.
VOUT	24, 25, 26, 27, 28, 29, 36, 37	O	Output voltage. These pins are connected to the output of the internal inductor. Connect these pins to the output VOUT load and connect external bypass capacitors between these pins and PGND.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	-0.3	42	V
	EN to AGND	-0.3	V_{IN} + 0.3	V
	FB, RT, SS/TRK to AGND	-0.3	5	V
	PGOOD to AGND	-0.1	20	V
	SYNC/MODE to AGND	-0.3	5.5	V
	BIAS_SEL to AGND	-0.3	Lower of (V_{IN}+0.3) and 20	V
	AGND to PGND	-0.3	0.3	V
Output voltage	VOUT to PGND	-0.3	V_{IN}	V
	SW to PGND	-0.3	V_{IN} + 0.3	V
	SW to PGND (<10 ns transients)	-3.5	42	V
	VCC to PGND	-0.3	5	V
Peak Reflow Case Temperature			240	°C
Maximum Number of Reflows Allowed			1	
Temperature	Maximum junction temperature, T_J (2)	-40	125	°C
	Storage temperature, T_{stg}	-55	150	°C
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under the recommended operating conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_{IN}	3.5 (1)	36	V
Output voltage, V_{OUT}	1	20	V
EN voltage, V_{EN}	0	VIN	V
PGOOD pullup voltage, V_{PGOOD}	0	18	V
PGOOD sink current	0	5	mA
BIAS_SEL	3.3	Lower of VIN and 18	V
Output current, I_{OUT}	0	6	A
Switching frequency, F_{SW}	350	1200	kHz
Operating ambient temperature, T_A	–40	105	°C
Input Capacitance, C_{IN}	20 (2)		µF
Output Capacitance, C_{OUT}	min (3)	700	µF

(1) For output voltages ≤ 5 V, the recommended minimum V_{IN} is 3.5 V or (VOUT + 1 V), whichever is greater. For output voltages > 5 V, the recommended minimum V_{IN} is (1.1 × VOUT). See *Voltage Dropout* for more information.
(2) A minimum of 20 µF ceramic input capacitance is required for proper operation. An additional 100 µF of bulk capacitance is recommended for applications with transient load requirements. (see *Input Capacitor Selection*).
(3) The minimum amount of required output capacitance varies depending on the output voltage (see *Output Capacitor Selection*).

6.4 Thermal Information

THERMAL METRIC (1)		LMZM33606 RLX(B2QFN) 41 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	13.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)	6.2	°C/W
T_{SHDN}	Thermal Shutdown Temperature	160	°C
	Thermal Shutdown Hysteresis	25	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 75 mm x 75 mm double-sided PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +105°C, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = I_{OUT} maximum, f_{sw} = 500 kHz, FPWM mode (unless otherwise noted); C_{IN1} = 3x 10 µF, 50-V, 1210 ceramic; C_{IN2} = 2x 4.7 µF, 50-V, 1210 ceramic; C_{OUT} = 6x 22 µF, 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN}	Input voltage range	Over I_{OUT} range, V_{OUT} = 2.5 V, f_{SW} = 350 kHz	3.5(1)		36	V
	V_{IN} turn on	V_{IN} increasing, V_{OUT} = 2.5 V, I_{OUT} = 0 A		3.12		V
	V_{IN} turn off	V_{IN} decreasing, V_{OUT} = 2.5 V, I_{OUT} = 0 A		2.62		V
I_{SHDN}	Shutdown supply current	V_{IN} = 12 V, V_{EN} = 0 V, I_{OUT} = 0 A		0.8	10	µA
INTERNAL LDO (VCC, BIAS_SEL)						
V_{CC}	Internal V_{CC} voltage	PWM operation		3.27		V
		PFM operation		3.1		V
I_{BIAS_SEL}	BIAS_SEL quiescent current (non-switching)	V_{IN} = 12 V, V_{FB} = 1.5 V, V_{EN} = 2 V, V_{BIAS_SEL} = 3.3 V		21	50	µA
FEEDBACK						
V_{FB}	Feedback voltage(2)	–40°C ≤ T_J = T_A ≤ 125°C, I_{OUT} = 0 A, Over V_{IN} range, V_{OUT} = 2.5 V, f_{SW} = 350 kHz	0.987	1.006	1.017	V
	Load regulation	Over I_{OUT} range, T_A = 25 °C		0.1%		
I_{FB}	Feedback leakage current	V_{FB} = 1 V		0.2	65	nA
CURRENT						
I_{OUT}	Output current	Natural convection, T_A = 25 °C	0		6	A
	Overcurrent threshold			9		A
PERFORMANCE						
η	Efficiency	I_{OUT} = 3 A, T_A = 25 °C		91%		
SOFT START						
T_{SS}	Internal soft start time	SS pin open		5		ms
I_{SSC}	Soft-start charge current	V_{IN} = 12 V, V_{FB} = 1.5 V, V_{EN} = 2 V, $V_{SS/TRK}$ = 0.5 V	1.8	2	2.2	µA
ENABLE (EN)						
V_{EN-H}	EN rising threshold		1.14	1.2	1.25	V
V_{EN-HYS}	EN hysteresis voltage			-100		mV
I_{EN}	EN Input leakage current	V_{IN} = 12 V, V_{FB} = 1.5 V, V_{EN} = 2 V		1.4	200	nA
POWER GOOD (PGOOD)						
V_{PGOOD}	PGOOD thresholds	Overvoltage	106%	110%	113%	
		Undervoltage	86%	90%	93%	
	PGOOD low voltage	0.5-mA pullup, V_{EN} = 0 V			0.3	V
V_{INPG}	Minimum V_{IN} for valid PGOOD	50-µA pullup, V_{EN} = 0 V, T_J = T_A = 25°C		1.3	2	V

(1) For output voltages ≤ 5 V, the recommended minimum V_{IN} is 3.5 V or (V_{OUT} + 1 V), whichever is greater. For output voltages > 5 V, the recommended minimum V_{IN} is (1.1 × V_{OUT}). See *Voltage Dropout* for more information.
(2) The overall output voltage tolerance will be affected by the tolerance of the external R_{FBT} and R_{FBB} resistors.

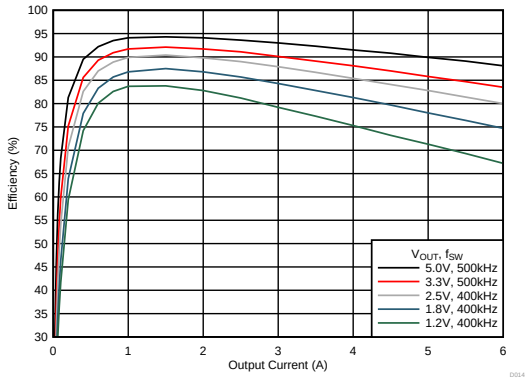
6.6 Switching Characteristics

Limits apply over T_A = –40°C to +105°C, V_{IN} = 24 V, V_{OUT} = 5 V, FPWM mode (unless otherwise noted);
Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm, and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY (RT) and SYNCHRONIZATION (SYNC)						
f_{SW}	Default switching frequency	RT pin = open, I_{OUT} = 0 A	440	500	560	kHz
	Switching frequency range	I_{OUT} = 0 A	350		2200	kHz
V_{SYNC}	High Threshold				2	V
	Low Threshold		0.4			V
T_{S-MIN}	Minimum SYNC ON/OFF time			80		ns

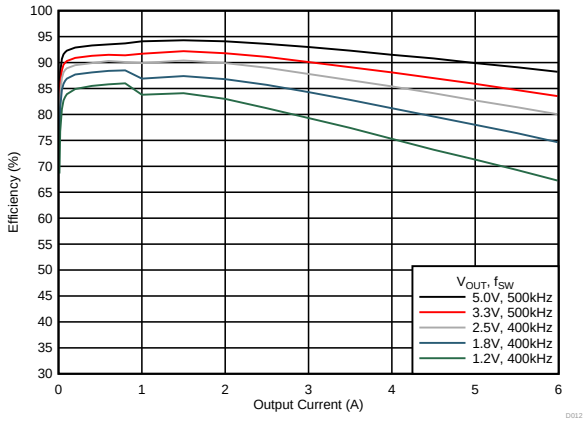
6.7 Typical Characteristics (V_{IN} = 12 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



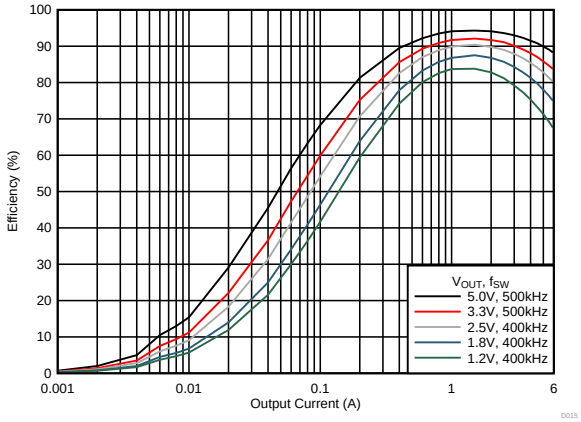
FPWM Mode Linear Scale

图 1. Efficiency vs Output Current



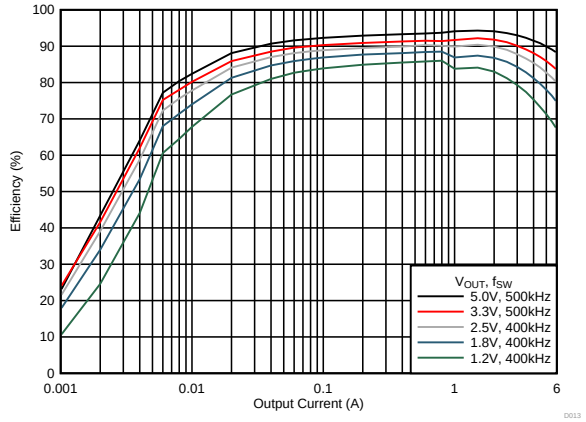
Auto Mode Linear Scale

图 2. Efficiency vs Output Current



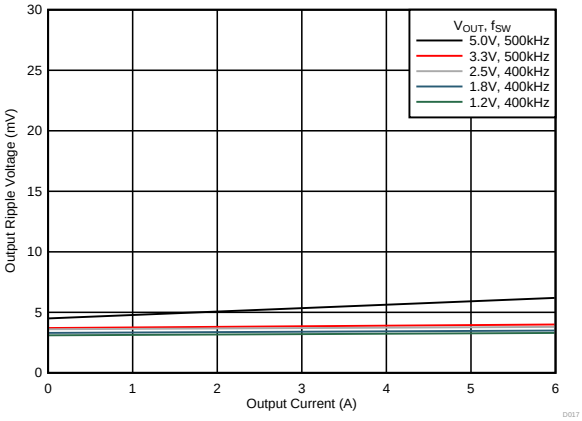
FPWM Mode Log Scale

图 3. Efficiency vs Output Current



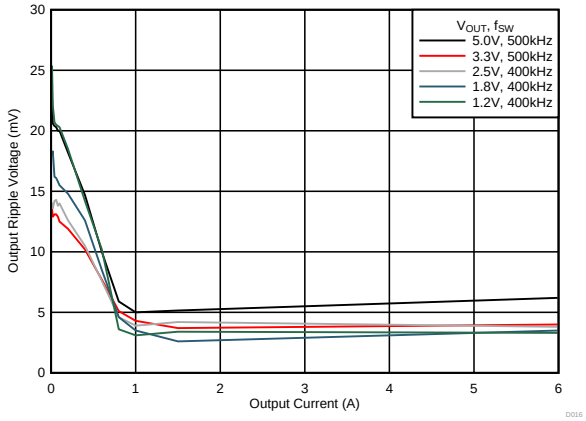
Auto Mode Log Scale

图 4. Efficiency vs Output Current



FPWM Mode C_{OUT} = 4 × 47 µF ceramic

图 5. Voltage Ripple vs Output Current



Auto Mode C_{OUT} = 4 × 47 µF ceramic

图 6. Voltage Ripple vs Output Current

Typical Characteristics (V_{IN} = 12 V) (接下页)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.

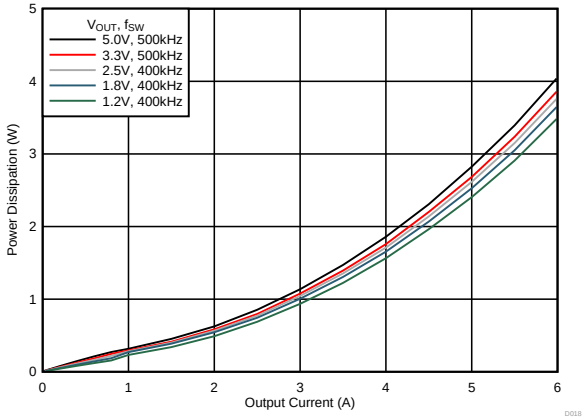
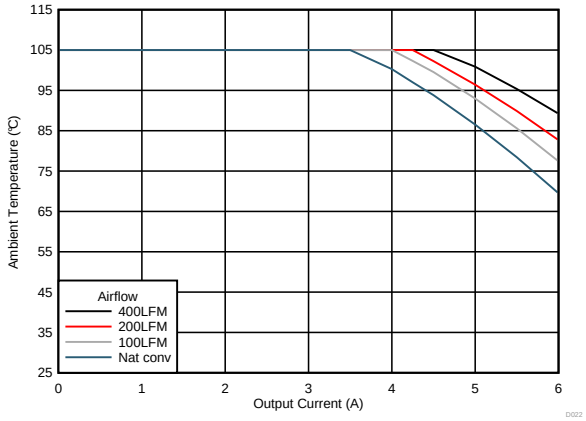
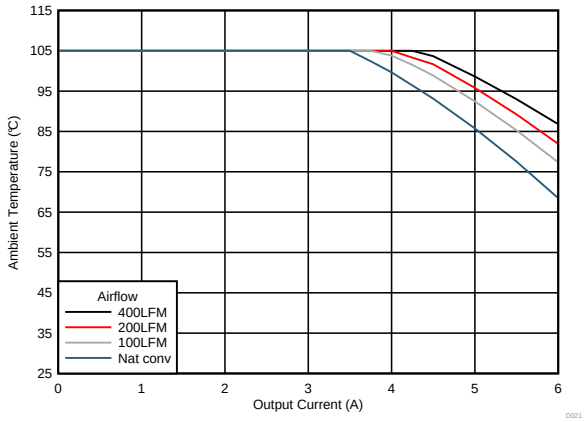


图 7. Power Dissipation vs Output Current



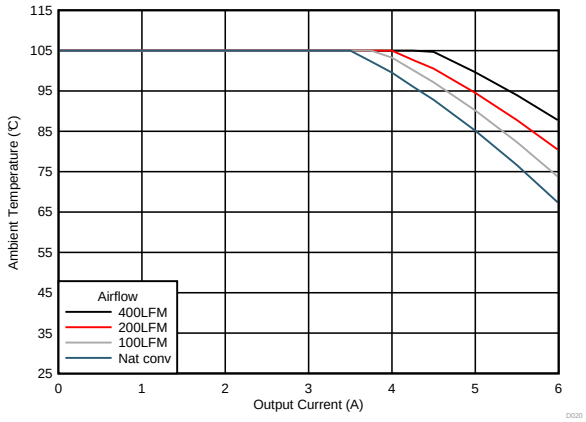
V_{OUT} = 1.8 V f_{SW} = 400 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 8. Safe Operating Area



V_{OUT} = 3.3 V f_{SW} = 500 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 9. Safe Operating Area

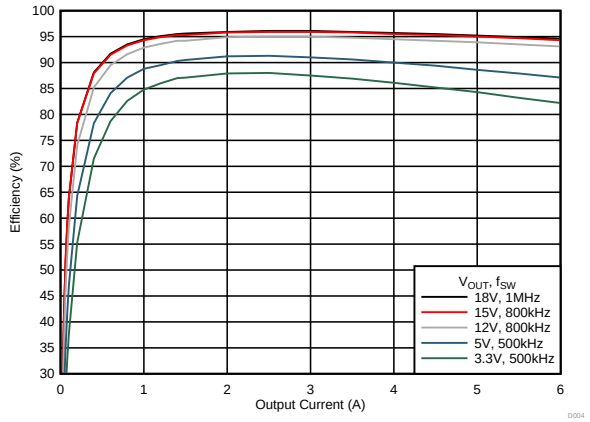


V_{OUT} = 5 V f_{SW} = 500 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 10. Safe Operating Area

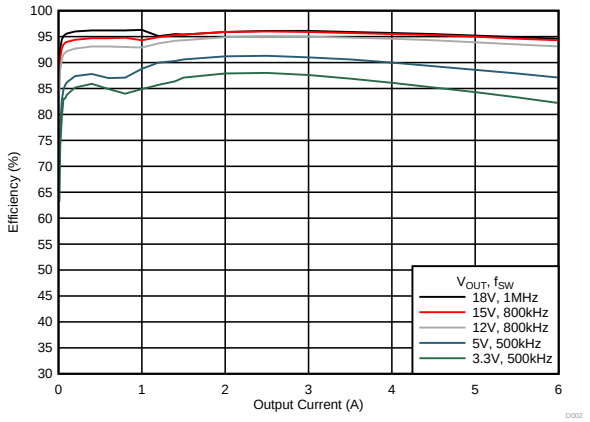
6.8 Typical Characteristics (V_{IN} = 24 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



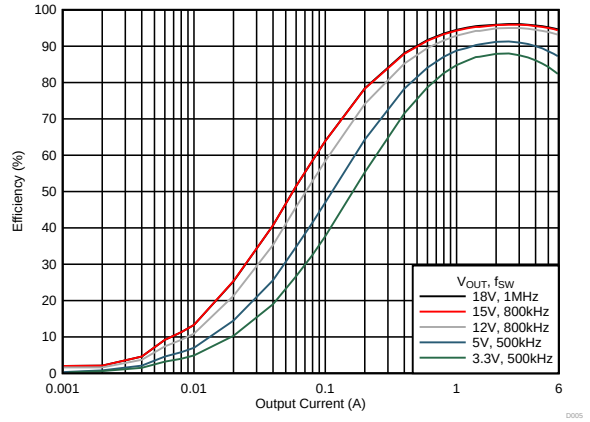
FPWM Mode Linear Scale

图 11. Efficiency vs Output Current



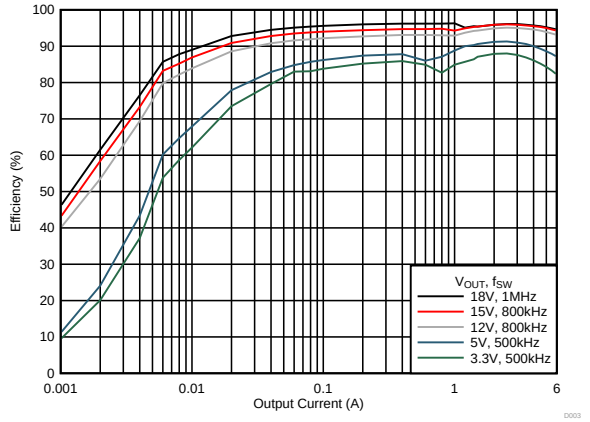
Auto Mode Linear Scale

图 12. Efficiency vs Output Current



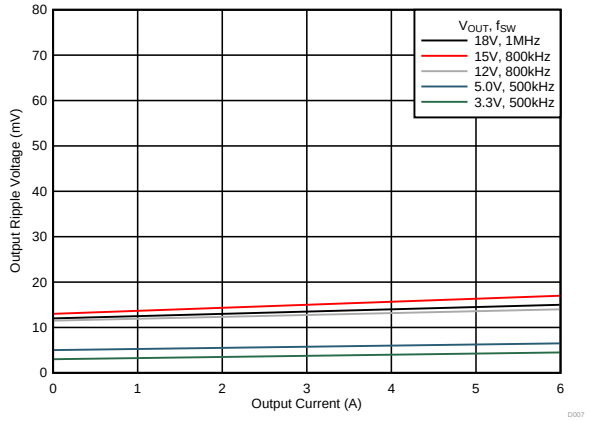
FPWM Mode Log Scale

图 13. Efficiency vs Output Current



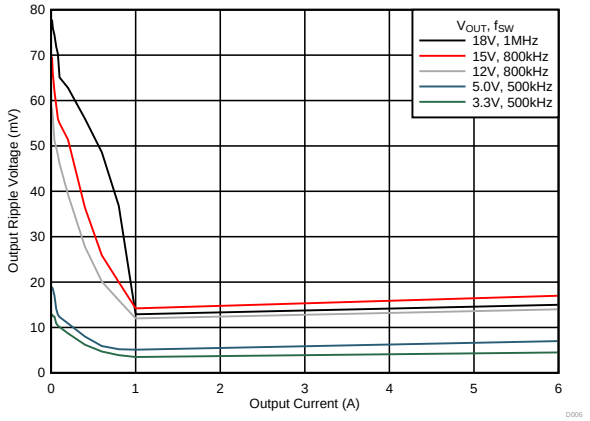
Auto Mode Log Scale

图 14. Efficiency vs Output Current



FPWM Mode C_{OUT} = 4 × 47 µF ceramic

图 15. Output Voltage Ripple



Auto Mode C_{OUT} = 4 × 47 µF ceramic

图 16. Output Voltage Ripple

Typical Characteristics (V_{IN} = 24 V) (接下页)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.

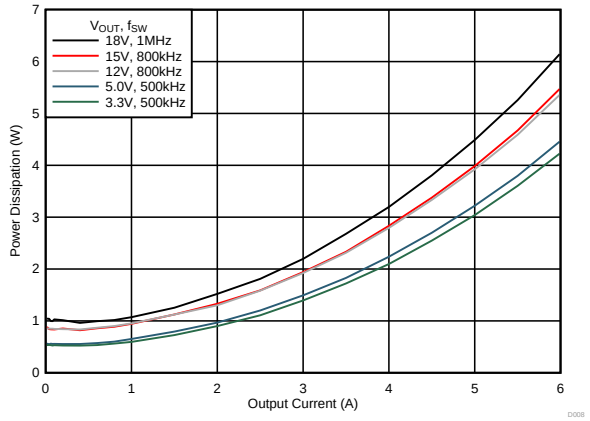
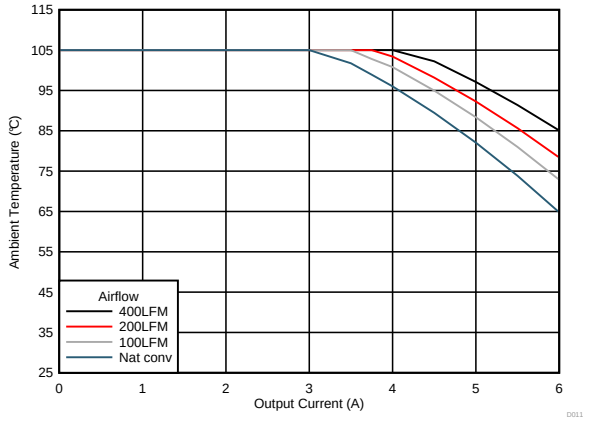
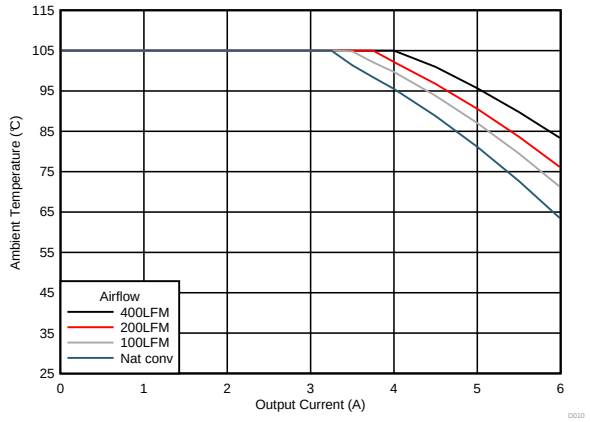


图 17. Power Dissipation



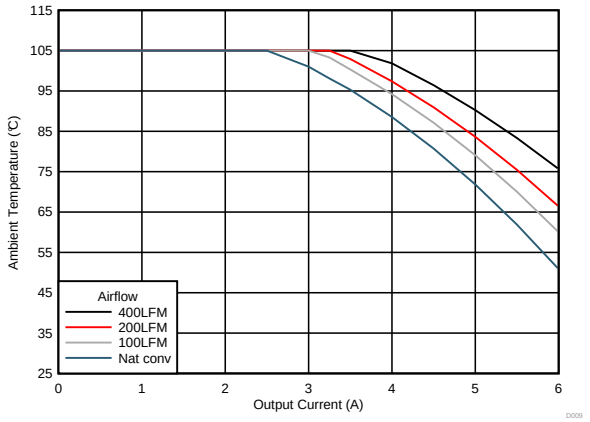
V_{OUT} = 3.3 V f_{SW} = 500 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 18. Safe Operating Area



V_{OUT} = 5 V f_{SW} = 500 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 19. Safe Operating Area

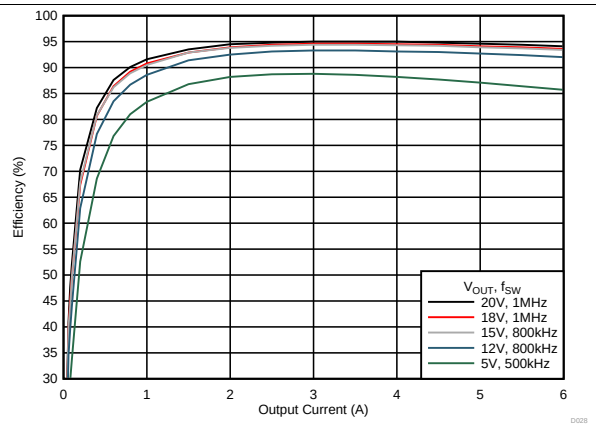


V_{OUT} = 12 V f_{SW} = 800 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 20. Safe Operating Area

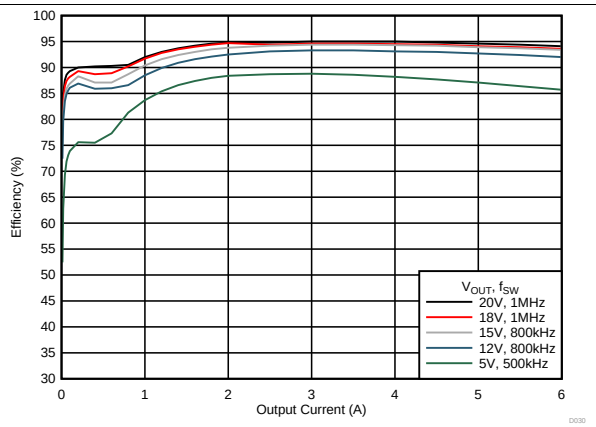
6.9 Typical Characteristics (V_{IN} = 36 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



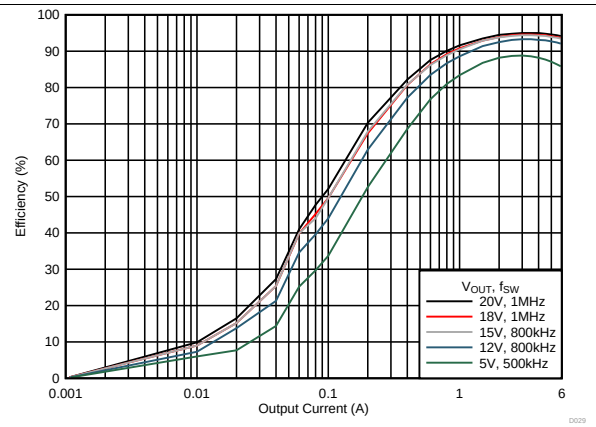
FPWM Mode Linear Scale

图 21. Efficiency vs Output Current



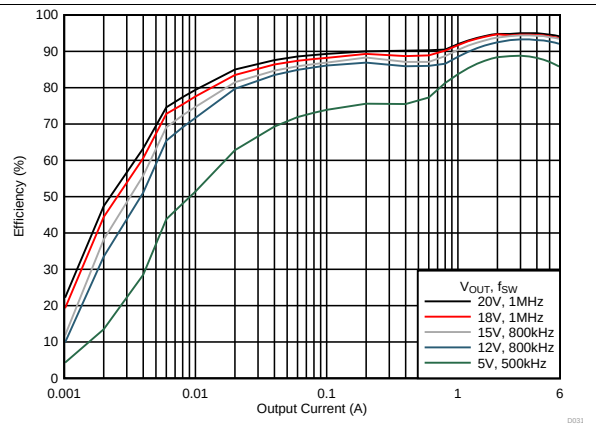
Auto Mode Linear Scale

图 22. Efficiency vs Output Current



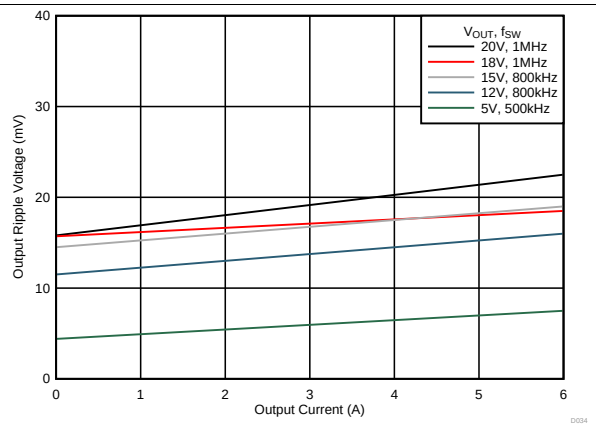
FPWM Mode Log Scale

图 23. Efficiency vs Output Current



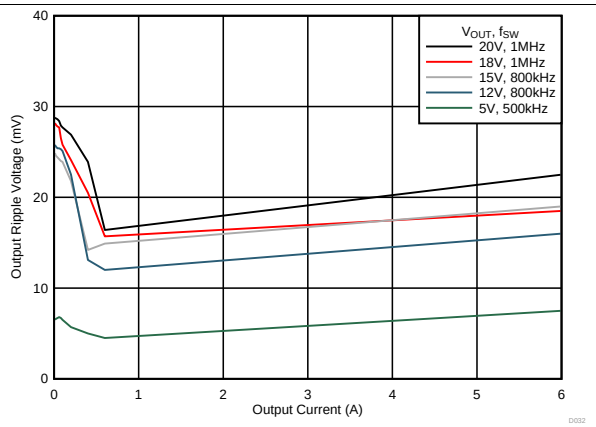
Auto Mode Log Scale

图 24. Efficiency vs Output Current



FPWM Mode C_{OUT} = 4 × 47 µF ceramic

图 25. Voltage Ripple vs Output Current



Auto Mode C_{OUT} = 4 × 47 µF ceramic

图 26. Voltage Ripple vs Output Current

Typical Characteristics (V_{IN} = 36 V) (接下页)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.

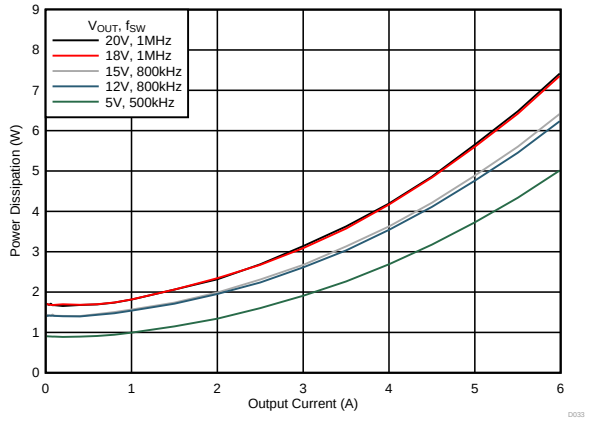
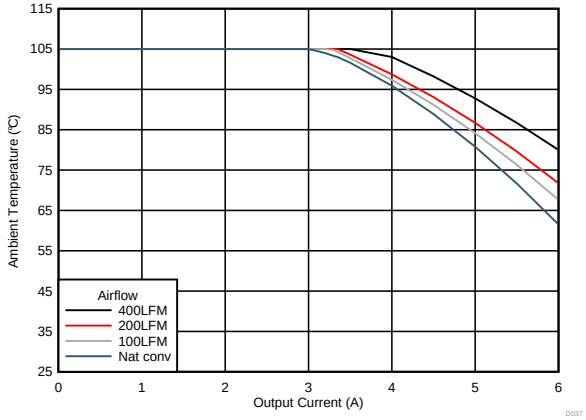
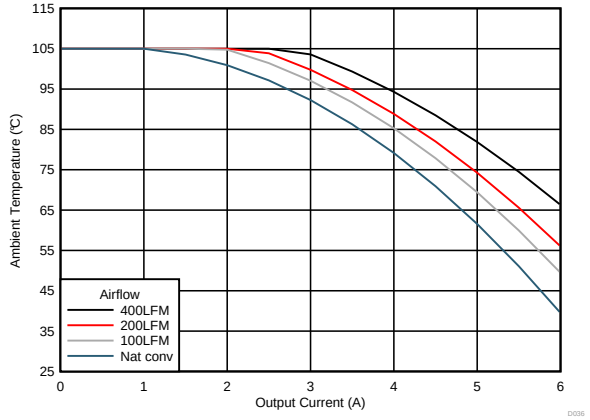


图 27. Power Dissipation vs Output Current



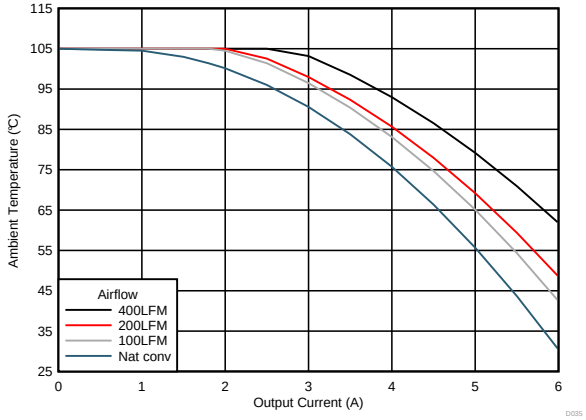
V_{OUT} = 5 V f_{SW} = 500 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 28. Safe Operating Area



V_{OUT} = 12 V f_{SW} = 800 kHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

图 29. Safe Operating Area



V_{OUT} = 20 V f_{SW} = 1 MHz
PCB = 75 mm × 75 mm, 4-layer, 2 oz. copper

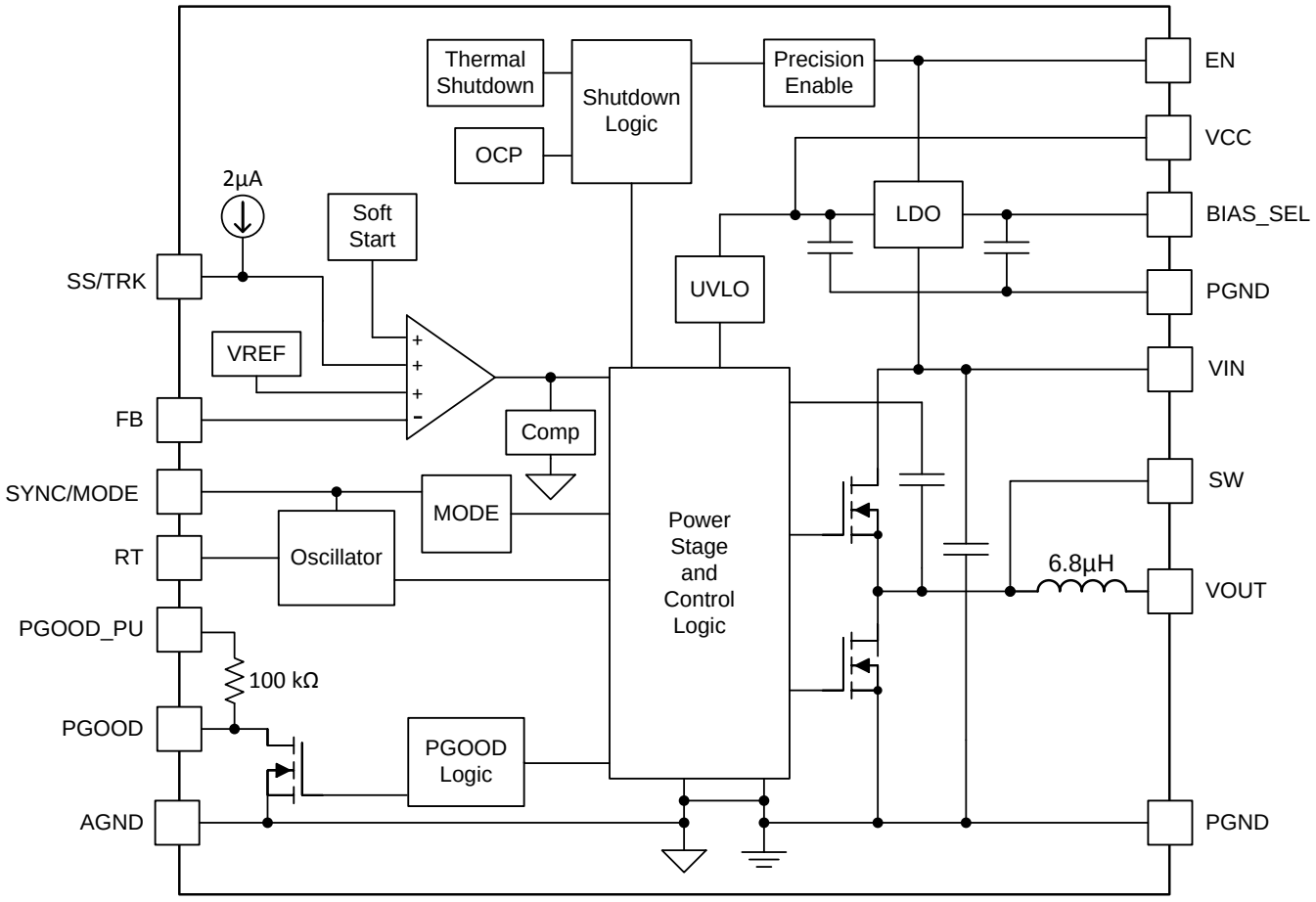
图 30. Safe Operating Area

7 Detailed Description

7.1 Overview

The LMZM33606 is a full-featured 36-V input, 6-A, synchronous step-down converter with controller, MOSFETs, shielded inductor, and control circuitry integrated into a low-profile, overmolded package. The device integration enables small designs, while providing the ability to adjust key parameters to meet specific design requirements. The LMZM33606 provides an output voltage range of 1 V to 20 V. An external resistor divider is used to adjust the output voltage to the desired value. The switching frequency can also be adjusted, by either an external resistor or a sync signal, which allows the LMZM33606 to optimize efficiency for a wide variety of input and output voltage conditions. The device provides accurate voltage regulation over a wide load range by using a precision internal voltage reference. The EN pin can be pulled low to put the device into standby mode to reduce input quiescent current. The system undervoltage lockout can be adjusted using a resistor divider on the EN pin. A power-good signal is provided to indicate when the output is within its nominal voltage range. Thermal shutdown and current limit features protect the device during an overload condition. A 41-pin, QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjusting the Output Voltage

A resistor divider connected to the FB pin (pin 15) programs the output voltage of the LMZM33606. The output voltage adjustment range is from 1 V to 20 V. 图 31 shows the feedback resistor connection for setting the output voltage. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using 公式 1.

表 1 lists the standard external R_{FBT} values for several standard output voltages along with the recommended switching frequency (F_{SW}) and the frequency setting resistor (R_{RT}) for each of the output voltages listed. (See *Voltage Dropout* for the allowable output voltage as a function of input voltage.)

$$R_{FBT} = 10 \times \left(V_{OUT} - V_{FB} \right) (k\Omega) \quad (1)$$

where

- V_{FB} (typical) = 1.006 V

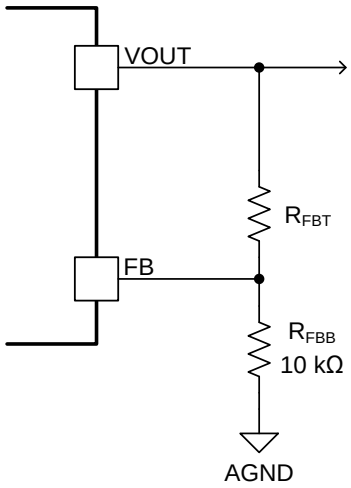


图 31. Setting the Output Voltage

表 1. Standard Component Values

V_{OUT} (V)	R_{FBT} (kΩ)(1)	f_{SW} (kHz)	R_{RT} (kΩ)
1.2	1.96	400	100
1.8	7.87	400	100
2.5	15.0	400	100
3.3	22.6	500	78.7 or open
5	40.2	500	78.7 or open
7.5	64.9	500	78.7 or open
12	110	800	47.5
15	140	800	47.5
18	169	1000	38.3
20	191	1000	38.3

(1) R_{FBB} = 10 kΩ.

7.3.2 Input Capacitor Selection

The LMZM33606 requires a minimum of 20 µF of ceramic type input capacitance. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. TI recommends an additional 33 µF of non-ceramic capacitance for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 3 A_{RMS}. 表 2 includes a preferred list of capacitors by vendor.

表 2. Recommended Input Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)	ESR (3) (mΩ)
TDK	X5R	C3225X5R1H106K	50	10	3
Murata	X7R	GRM32ER71H106K	50	10	2
Murata	X7R	GRM32ER71J106K	63	10	2
Panasonic	ZA	EEHZA1H101P	50	100	28
Panasonic	ZA	EEHZA1J560P	63	56	30

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR at 100 kHz, 25°C.

7.3.3 Output Capacitor Selection

The minimum amount of required output capacitance for the LMZM33606 varies depending on the output voltage. 表 3 lists the minimum output capacitance for several output voltage ranges. The required output capacitance must be comprised of all ceramic capacitors.

When adding additional output capacitance, ceramic capacitors or a combination of ceramic and polymer-type capacitors can be used. The required capacitance above the minimum is determined by actual transient deviation requirements. See 表 4 for a preferred list of output capacitors by vendor.

表 3. Minimum Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (1)	
MIN	MAX	CAPACITANCE VALUE	VOLTAGE RATING
1	1	400 µF	≥ 6.3 V
> 1	1.8	300 µF	
> 1.8	2.5	200 µF	
> 2.5	3.3	150 µF	
> 3.3	5	100 µF	
> 5.0	12	100 µF	≥ 16 V
> 12	20	50 µF	≥ 25 V

(1) The minimum required output capacitance must be made up of ceramic type capacitors. Additional capacitance above the minimum can be either ceramic or low-ESR polymer type.

表 4. Recommended Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			VOLTAGE (V)	CAPACITANCE (µF)(2)	ESR (mΩ)(3)
TDK	X5R	C3225X5R1C106K	16	10	2
Murata	X5R	GRM32ER61C106K	16	10	2
TDK	X5R	C3225X5R1C226M	16	22	2
Murata	X5R	GRM32ER61C226K	16	22	2
Murata	X6S	GRM31CC81E226K	25	22	2
Murata	X7R	GRM32ER71E226M	25	22	2
TDK	X5R	C3225X5R1A476M	10	47	2
Murata	X5R	GRM32ER61C476K	16	47	2
Murata	X5R	GRM31CR61E476M	25	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR at 100 kHz, 25°C.

7.3.4 Transient Response

表 5 shows the voltage deviation for several transient conditions.

表 5. Output Voltage Transient Response

C_{IN} = 2× 10 µF, 50-V Ceramic, 33 µF, 50-V Polymer Electrolytic		
V_{OUT} (V)	C_{OUT}	VOLTAGE (1) DEVIATION (mV)
1.8	300 µF	55
	500 µF	45
3.3	150 µF	65
	400 µF	55
5	100 µF	80
	250 µF	70
12	100 µF	260
	200 µF	220

(1) 50% load step at 1 A/µs.

7.3.5 Feed-Forward Capacitor

The LMZM33606 is internally compensated to be stable over the operating range of the device. However, depending on the output voltage and amount of output capacitance, a feed-forward capacitor, C_{FF}, may be added for optimum performance. The feed-forward capacitor should be placed in parallel with the top resistor divider, R_{FBT} as shown in 图 32. The value for C_{FF} can be calculated using 公式 2. For output voltages < 1.2 V, C_{FF} is ineffective and is not recommended.

$$C_{FF} = 4.3 \times \frac{V_{OUT} \times C_{OUT}}{R_{FBT}} \quad (pF) \tag{2}$$

where

- C_{OUT} is in µF
- R_{FBT} is in kΩ

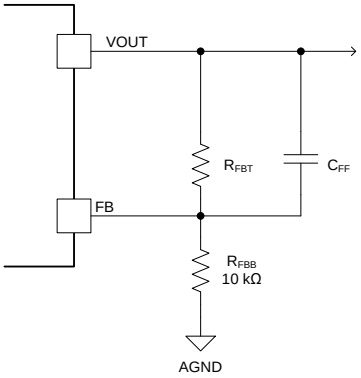


图 32. Feed-Forward Capacitor

7.3.6 Switching Frequency (RT)

The recommended switching frequency range of the LMZM33606 is 350 kHz to 1.2 MHz. 表 6 shows the allowable output voltage range for several switching frequency settings for three common input voltages. Under some operating conditions, the device can operate at higher switching frequencies (up to 2.2 MHz), however, this will reduce efficiency and thermal performance. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Additionally, the RT pin can be left floating, and the LMZM33606 operates at 500 kHz default switching frequency. Use 公式 3 to calculate the R_{RT} value for a desired frequency or simply select from 表 6.

The switching frequency must be selected based on the output voltage setting of the device. See 表 6 for R_{RT} values and the allowable output voltage range at a given switching frequency for several common input voltages. For the most efficient solution, always select the lowest allowable frequency.

$$R_{RT} = \frac{1}{f_{SW}(\text{kHz}) \times (2.675 \times 10^{-5}) - 0.0007} \quad (\text{k}\Omega) \tag{3}$$

表 6. Switching Frequency vs Output Voltage

SWITCHING FREQUENCY (kHz)	R_{RT} RESISTOR (kΩ)	V_{IN} = 5 V (±10%)		V_{IN} = 12 V (±10%)		V_{IN} = 24 V (±10%)	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX
350	115	1	4	1	8.2	1	8.4
400	100	1	4	1	8.8	1	9.9
500	78.7 or open	1	4	1	9.9	1.1	13.9
600	64.9	1	4	1	9.9	1.3	15.6
700	54.9	1	3.5	1	9.7	1.5	16.9
800	47.5	1	3.4	1	9.6	1.7	18
1000	38.3	1	3.4	1.1	9.3	2.1	20
1200	31.6	1	3.3	1.3	9.1	2.5	19.1
1500	25.5	1	2.9	1.8	8.1	3.2	18.1
1800	21.0	1.1	2.7	2.1	7.7	3.9	17.2
2000	19.1	1.2	2.5	2.5	7.5	4.4	16.5
2200	17.4	1.3	2.4	2.7	7.2	4.8	15.9

7.3.7 Synchronization (SYNC/MODE)

The LMZM33606 switching frequency can also be synchronized to an external clock from 350 kHz to 2.2 MHz. Before the external clock is present, the device switches at the frequency programmed by the R_{RT} resistor. Select R_{RT} to set the frequency to be the same as the external synchronization frequency. Once the external clock is present, the device transitions to SYNC mode within 1 ms (typical) and overrides the RT mode. If the external clock is removed, the device continues to switch at the SYNC frequency for 10 µs (typ) before returning to the switching frequency set by the RT resistor, resulting in minimal disturbance to the output voltage during the transitions.

Recommendations for the external clock include a high level no lower than 2 V, low level no higher than 0.4 V, duty cycle between 10% and 90%, and both positive and negative pulse width no shorter than 80 ns.

When synchronizing to an external clock, the device operation mode is FPWM. If synchronization is not needed, connect this pin to AGND or logic high to select either Auto mode or FPWM mode. Do not leave this pin open.

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. 表 6 and show the allowable frequencies for a given range of output voltages. For the most efficient solution, always select the lowest allowable frequency.

7.3.8 Output Enable (EN)

The voltage on the EN pin provides electrical ON/OFF control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The EN pin cannot be open circuit or floating. The simplest way to enable the operation of the LMZM33606 is to connect the EN pin to VIN directly as shown in 图 33. This allows self-start-up of the LMZM33606 when VIN reaches the turn-on threshold.

If an application requires controlling the EN pin, an external logic signal can be used to drive EN pin as shown in 图 34. Applications using an open drain/collector device to interface with this pin require a pull-up resistor to a voltage above the enable threshold.

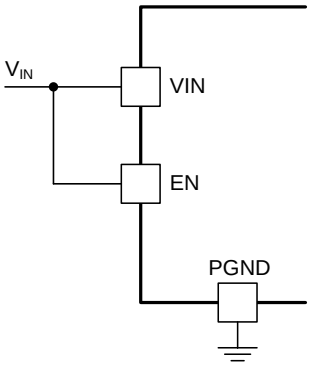


图 33. Enabling the Device

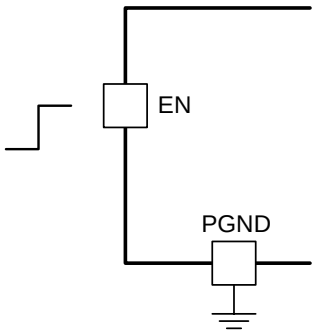


图 34. Typical Enable Control

7.3.9 Programmable System UVLO (EN)

Many applications benefit from employing an enable divider to establish a customized system UVLO. This can be used for sequencing, to satisfy a system timing requirement, or to reduce the occurrence of deep discharge of a battery power source. 图 35 shows how to use a resistor divider to set a system UVLO level. An external logic output can also be used to drive the EN pin for system sequencing.

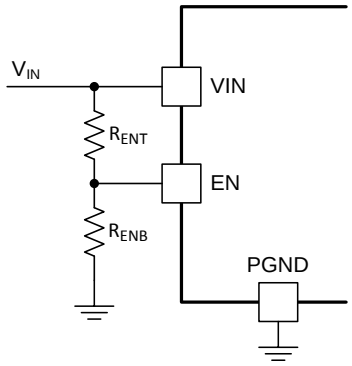


图 35. System UVLO

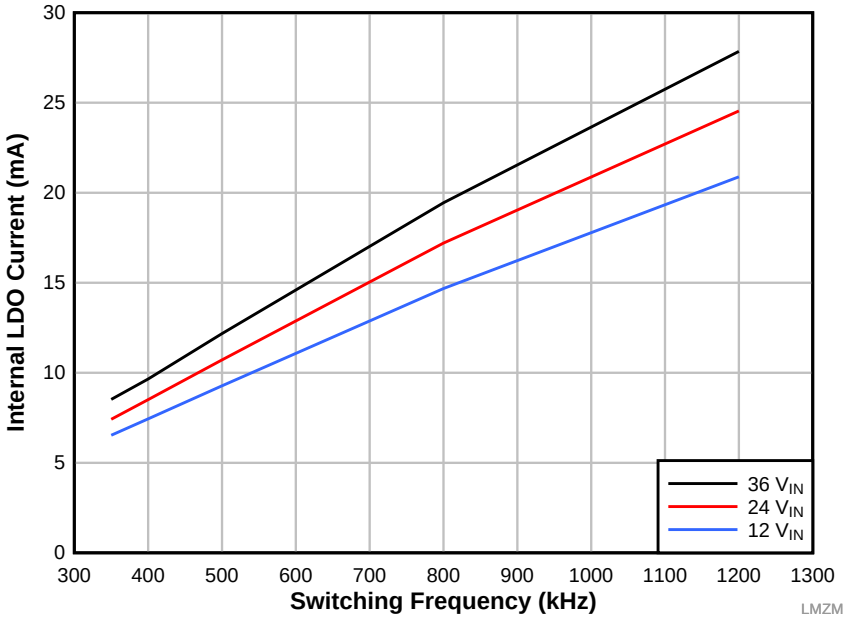
表 7 lists recommended resistor values for R_{ENT} and R_{ENB} to adjust the system UVLO voltage. TI recommends to set the system UVLO turn-on threshold to approximately 80% to 85% of the minimum expected input voltage.

表 7. Resistor Values for Setting System UVLO

UVLO (V)	6.5	10	15	20	25
R_{ENT} (kΩ)	100	100	100	100	100
R_{ENB} (kΩ)	22.6	13.7	8.66	6.34	4.99

7.3.10 Internal LDO and BIAS_SEL

The LMZM33606 integrates an internal LDO, generating a typical V_{CC} voltage (3.27 V) for control circuitry and MOSFET drivers. The LDO generates V_{CC} voltage from V_{IN} unless a sufficient bias voltage, V_{BIAS}, is applied to BIAS_SEL pin. The BIAS_SEL input provides an option to supply the LDO with a lower voltage than V_{IN} to reduce the LDO power loss. The smaller the difference between the input applied to the LDO, V_{IN_LDO}, and the LDO output voltage, V_{CC}, the more efficiently the device will perform. The amount of current supplied through the LDO will change based on operating conditions. 图 36 demonstrates the typical LDO current, I_{LDO}, for common input voltages over the recommended switching frequency range.



V_{OUT} = 5 V

图 36. LDO Current vs Switching Frequency

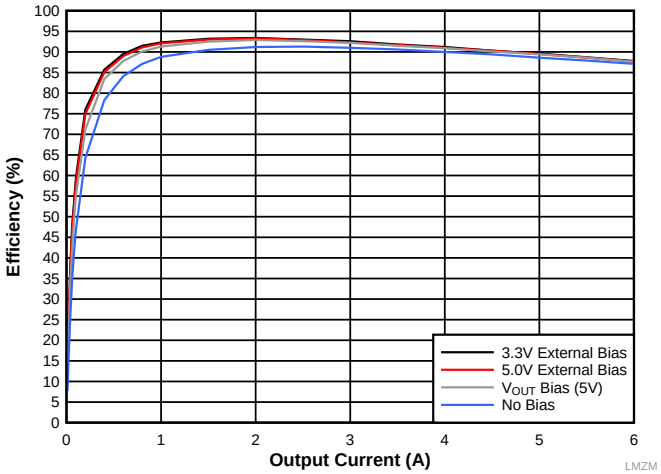
The amount of power loss in the LDO can be calculated by 公式 4.

$$P_{LOSS\_LDO} = I_{LDO} \times (V_{IN\_LDO} - V_{CC}) \quad (4)$$

For example, when the device is operating at V_{IN} = 24 V, V_{OUT} = 5 V, f_{sw} = 500 kHz, BIAS_SEL = PGND, the I_{LDO} is typical 11 mA, therefore, the P_{LOSS_LDO} = 11 mA × (24 V – 3.27 V) = 228.03 mW. For the same operating conditions with BIAS_SEL = 5 V, the power loss is equal to 11 mA × (5 V – 3.27 V) = 19.03 mW. The benefits of applying a bias voltage to reduce power loss are most notable in applications when V_{IN} » V_{CC} or when the device is operating at a higher switching frequency. The power savings can be calculated by 公式 5.

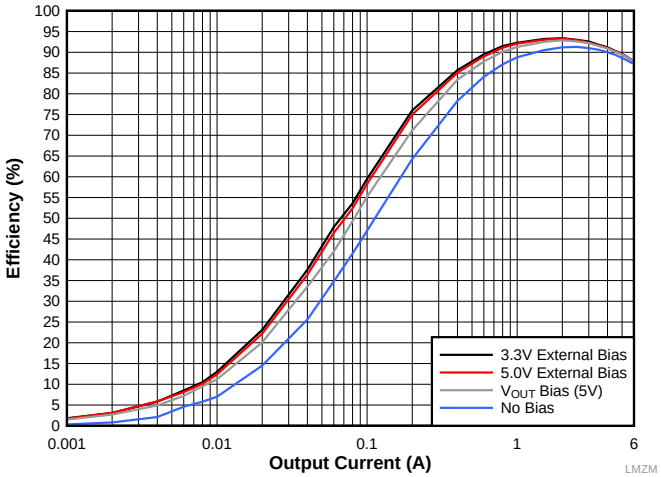
$$\text{Power Savings} = I_{LDO} \times (V_{IN} - V_{BIAS\_SEL}) \quad (5)$$

图 37 and 图 38 show efficiency plots of the LMZM33606 operating with different source voltages applied to the BIAS_SEL pin. 图 39 demonstrates the power dissipation of the device with various source voltages at BIAS_SEL pin. The plots include BIAS_SEL tied to a 3.3 V external bias, 5 V external bias, VOUT (5 V) and no bias voltage applied. The efficiency improvements are more significant when the device is operating at light loads because the LDO loss is a higher percentage of the total loss.



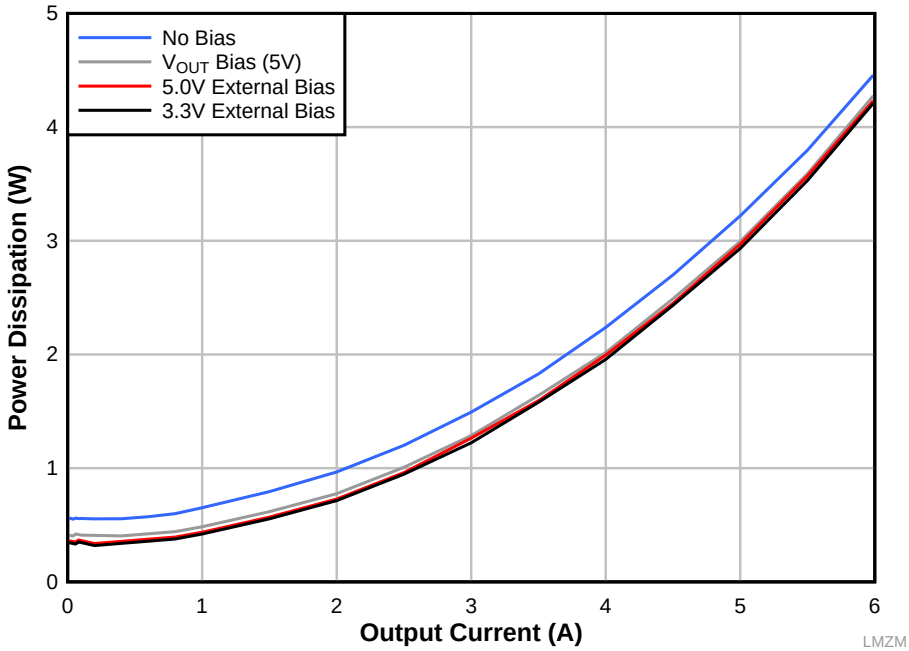
V_{IN} = 24 V f_{SW} = 500 kHz FPWM Mode

图 37. Efficiency Comparison with BIAS_SEL vs Output Current



V_{IN} = 24 V f_{SW} = 500 kHz FPWM Mode

图 38. Efficiency Comparison with BIAS_SEL vs Output Current



V_{IN} = 24 V f_{SW} = 500 kHz FPWM Mode

图 39. Power Dissipation Comparison with BIAS_SEL

7.3.11 Power Good (PGOOD) and Power Good Pull-Up (PGOOD_PU)

The LMZM33606 has a built-in power-good signal (PGOOD) that indicates whether the output voltage is within its regulation range. The PGOOD pin is an open-drain output that requires a pull-up resistor to a nominal voltage source of 15 V or less. The maximum recommended PGOOD sink current is 5 mA. A typical pull-up resistor value is between 10 kΩ and 100 kΩ.

Once the output voltage rises above 90% (typical) of the set voltage, the PGOOD pin rises to the pull-up voltage level. The PGOOD pin is pulled low when the output voltage drops lower than 90% (typical) or rises higher than 110% (typ) of the nominal set voltage.

Internal to the device, a 100-kΩ pull-up resistor is placed between the PGOOD pin and the PGOOD_PU pin. Applying a pull-up voltage directly to the PGOOD_PU pin, eliminates the need for an external pull-up resistor.

7.3.12 Mode Select (Auto or FPWM)

The LMZM33606 has configurable Auto mode or FPWM mode options. To select Auto mode, connect the SYNC/MODE pin (pin 19) to AGND, or a logic signal lower than 0.3 V. To select FPWM mode, connect the SYNC/MODE pin to a bias voltage or logic signal greater than 0.6 V. When synchronizing to an external clock, the device inherently operates in FPWM mode.

In Auto mode, the device operates in discontinuous conduction mode (DCM) at light loads. In DCM, the inductor current stops flowing when it reaches 0 A. Additionally, at very light loads, the switching frequency reduces (PFM operation) to regulate the required load current, thus improving efficiency by reducing switching losses. At heavier loads, when the inductor current valley is above 0 A, the device operates in continuous conduction mode (CCM), where the switching frequency is fixed and set by the RT pin.

In forced PWM (FPWM) mode, the device operates in CCM (at a fixed frequency) regardless of load. In this mode, inductor current can go negative. At light loads, the efficiency in FPWM mode is lower than in Auto mode, due to higher conduction losses and higher switching losses. The fact that the switching frequency is fixed over the entire load range is beneficial in noise sensitive applications.

7.3.13 Soft Start and Voltage Tracking

The soft-start and tracking features control the output voltage ramp during start-up. The soft-start feature reduces inrush current during start-up and improves system performance and reliability. If the SS/TRK pin is floating, the LMZM33606 starts up following the fixed, 5-ms internal soft-start ramp. Use C_{SS} to extend soft-start time when there are a large amount of output capacitors, or the output voltage is high, or the output is heavily loaded during start-up.

If longer soft-start time is desired, an external capacitor can be added from SS/TRK pin to AGND. There is a 2 µA (typical) internal current source, I_{SSC}, to charge the external capacitor. For a desired soft-start time t_{SS}, capacitance of C_{SS} can be found by 公式 6.

$$C_{SS} = I_{SSC} \times t_{SS} \quad (6)$$

where

- C_{SS} = soft-start capacitor value (F)
- I_{SSC} = soft-start charging current (A)
- t_{SS} = desired soft-start time(s)

LMZM33606 can track an external voltage ramp applied to the SS/TRK pin, if the ramp is slower than the internal soft-start ramp. The external ramp final voltage after start-up must be greater than 1.5 V to avoid noise interfering with the reference voltage. 图 40 shows how to use resistor divider to set V_{OUT} to follow an external ramp.

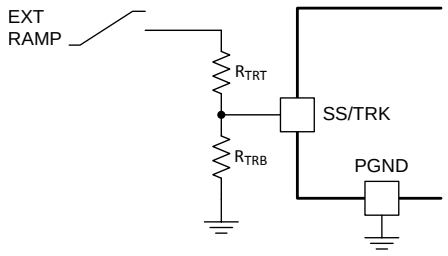


图 40. Soft-Start Tracking External Ramp

7.3.14 Voltage Dropout

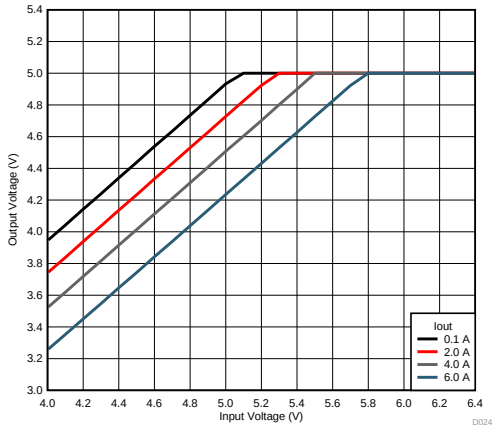
Voltage dropout is the minimum difference between the input voltage and output voltage that is required to maintain output voltage regulation while providing the rated output current.

To ensure the LMZM33606 maintains output voltage regulation at the recommended switching frequency, over the operating temperature range, the following requirements apply:

For output voltages ≤ 5 V, the minimum V_{IN} is 3.5 V or (V_{OUT} + 1 V), whichever is greater.

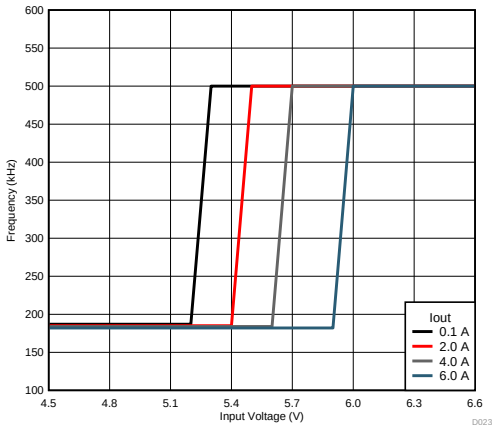
For output voltages > 5 V, the minimum V_{IN} is (1.1 × V_{OUT}).

However, if fixed switching frequency operation is not required, the LMZM33606 operates in a frequency foldback mode when the dropout voltage is less than the recommendations above. Frequency foldback reduces the switching frequency to allow the output voltage to maintain regulation as input voltage decreases. 图 41 through 图 44 show typical dropout voltage and frequency foldback curves for 5 V and 12 V outputs at T_A = 25°C. (As ambient temperature increases, dropout voltage and frequency foldback occur at higher input voltages.)



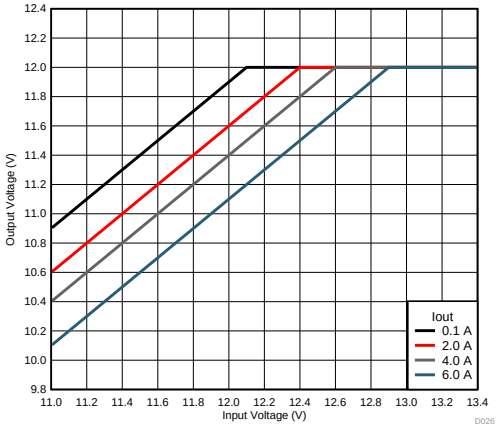
V_{OUT} = 5 V f_{SW} = 500 kHz

图 41. Voltage Dropout



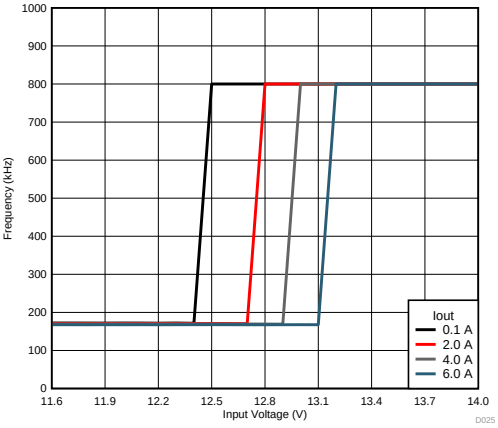
V_{OUT} = 5 V f_{SW} = 500 kHz

图 42. Frequency Foldback



V_{OUT} = 12 V f_{SW} = 800 kHz

图 43. Voltage Dropout



V_{OUT} = 12 V f_{SW} = 800 kHz

图 44. Frequency Foldback

7.3.15 Overcurrent Protection (OCP)

The LMZM33606 is protected from overcurrent conditions. Hiccup mode is activated if a fault condition persists to prevent overheating. In hiccup mode, the regulator is shut down and kept off for 10 ms (typical) before the LMZM33606 tries to start again. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

7.3.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 135°C (typical).

7.4 Device Functional Modes

7.4.1 Active Mode

The LMZM33606 is in active mode when VIN is above the turn-on threshold and the EN pin voltage is above the EN high threshold. The simplest way to enable the LMZM33606 is to connect the EN pin to VIN. This allows self start-up of the LMZM33606 when the input voltage is in the operation range of 3.5 V to 36 V.

7.4.2 Auto Mode

In Auto mode, the LMZM33606 operates in discontinuous conduction mode (DCM) at light loads. In DCM, the inductor current stops flowing when it reaches 0 A. Additionally, at very light loads, the switching frequency reduces (PFM operation) to regulate the required load current, thus improving efficiency by reducing switching losses. At heavier loads, when the inductor current valley is above 0 A, the device operates in continuous conduction mode (CCM), where the switching frequency is fixed and set by the RT pin.

7.4.3 FPWM Mode

In forced PWM (FPWM) mode, the LMZM33606 operates in CCM (at a fixed frequency) regardless of load. In this mode, inductor current can go negative. At light loads, the efficiency in FPWM mode is lower than in Auto mode, due to higher conduction losses and higher switching losses.

7.4.4 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMZM33606. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode the standby current is 0.8 μA typical. If V_{IN} falls below the turn-off threshold, the output of the regulator is turned off.

8 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZM33606 is a synchronous, step-down, DC/DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 6 A. The following design procedure can be used to select components for the LMZM33606. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH® software utilizes an iterative design procedure and accesses comprehensive databases of components. See www.ti.com for more details.

8.2 Typical Application

The LMZM33606 only requires a few external components to convert from a wide input-voltage-supply range to a wide range of output voltages. 图 45 shows a typical LMZM33606 schematic.

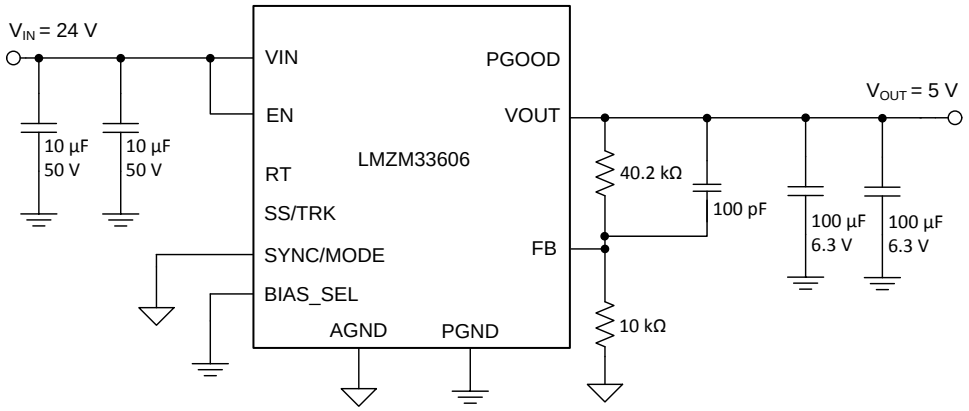


图 45. LMZM33606 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8 as the input parameters and follow the design procedures in *Detailed Design Procedure*.

表 8. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	6 A
Operating frequency	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Setpoint

The output voltage of the LMZM33606 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be selected from 表 1 or calculated using the 公式 7:

$$R_{FBT} = 10 \times \left(V_{OUT} - V_{FB} \right) \text{ (k}\Omega\text{)} \quad (7)$$

For the desired output voltage of 5 V, the formula yields a value of 40 kΩ. Choose the closest available value of 40.2 kΩ for R_{FBT}.

8.2.2.2 Setting the Switching Frequency

The recommended switching frequency for a 5-V application is 500 kHz. To set the switching frequency to 500 kHz, the RT pin can be left open to operate at the default 500-kHz switching frequency.

8.2.2.3 Input Capacitors

The LMZM33606 requires a minimum input capacitance of 20-µF ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, 2x 10-µF, 50-V ceramic capacitors are selected.

8.2.2.4 Output Capacitor Selection

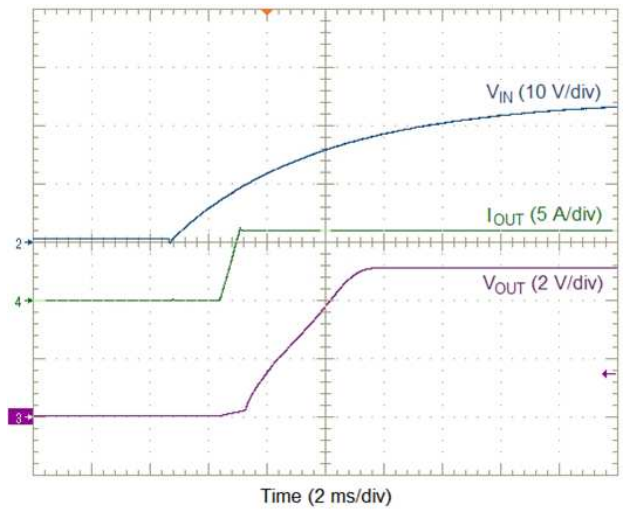
The LMZM33606 requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See *表 3* for the required output capacitance.

For this design example, 2 × 100-µF, 6.3-V ceramic capacitors are used.

8.2.2.5 Feed-Forward Capacitor (C_{FF})

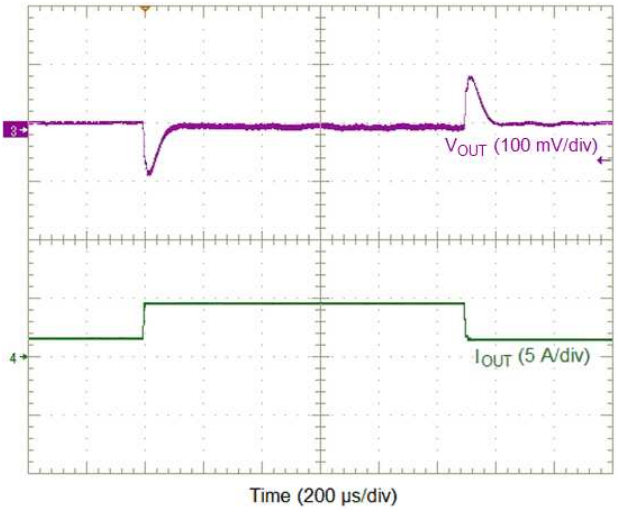
For typical applications, an external feed-forward capacitor, C_{FF} is not required. Applications requiring optimum transient performance can benefit from placing a C_{FF} capacitor in parallel with the top resistor divider, R_{FBT}. The value for C_{FF} can be calculated using 公式 2. The recommended C_{FF} value for 5-V application is 100 pF.

8.2.2.6 Application Curves



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 6 A

图 46. Start-up Waveforms



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 1.5 A to 4.5 A
C_{OUT} = 200 µF Slew rate: 1 A/µs

图 47. Transient Response

9 Power Supply Recommendations

The LMZM33606 is designed to operate from an input voltage supply range between 3.5 V and 36 V. This input supply must be able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMZM33606 supply voltage that can cause a turn-off and system reset.

If the input supply is located more than a few inches from the LMZM33606 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is a 100-µF electrolytic capacitor.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 图 48 thru 图 51, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- **Connect all PGND pins together using copper plane or thick copper traces.**
- Connect the SW pins together using a small copper island under the device for thermal relief.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. AGND and PGND are connected internal to the device.
- Place R_{FBT}, R_{FBB}, R_{RT}, and C_{FF} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

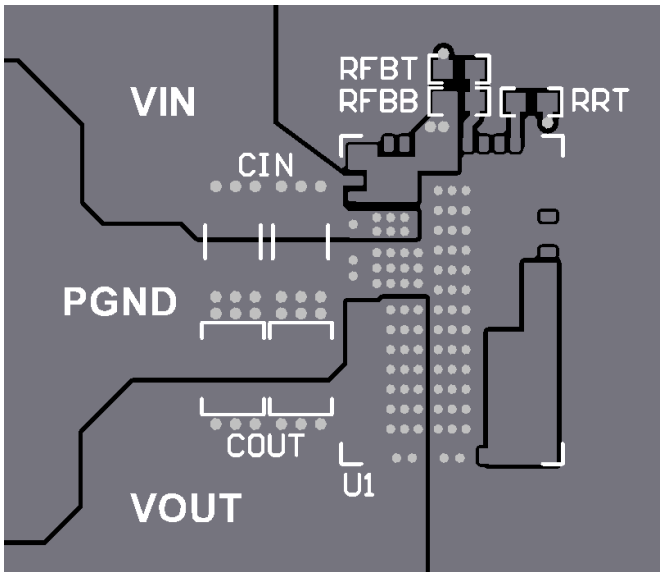


图 48. Typical Top-Layer Layout

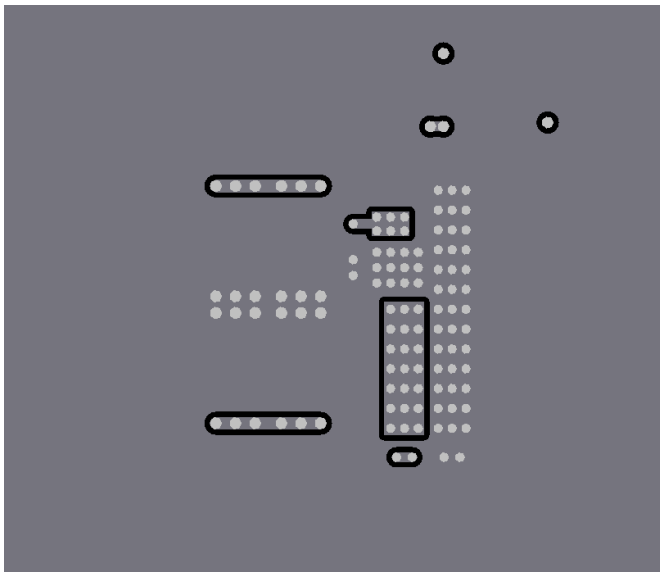


图 49. Typical Layer-2 Layout

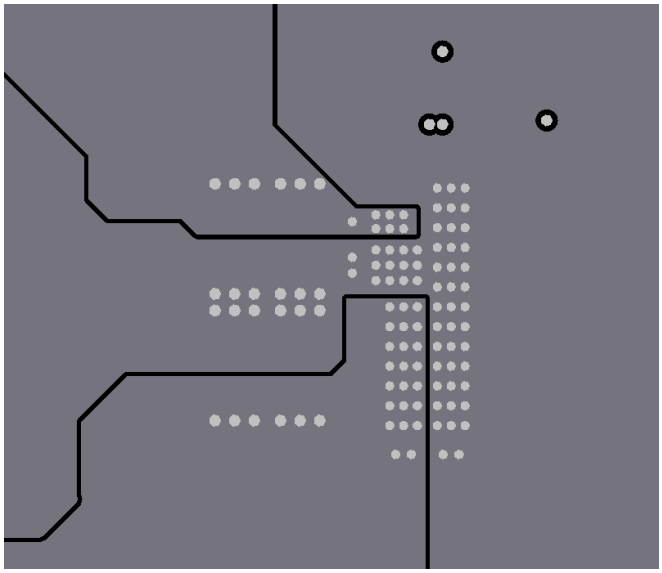


图 50. Typical Layer 3 Layout

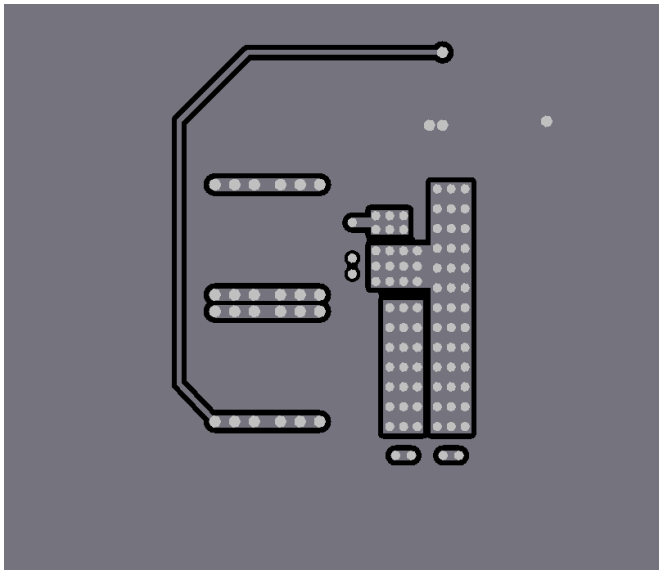


图 51. Typical Bottom-Layer Layout

10.3 Theta JA vs PCB Area

The amount of PCB copper effects the thermal performance of the device. 图 52 shows the effects of copper area on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the LMZM33606. The junction-to-ambient thermal resistance is plotted for a 4-layer PCB and a 6-layer PCB with PCB area from 16 cm^2 to 100 cm^2.

To determine the required copper area for an application:

1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in the *Typical Characteristics* section.
2. Calculate the maximum θ_{JA} using 公式 8 and the maximum ambient temperature of the application.

$$\theta_{JA} = \frac{(125^{\circ}C - T_{A(max)})}{P_{D(max)}} \ (^{\circ}C/W) \tag{8}$$

3. Reference 图 52 to determine the minimum required PCB area for the application conditions.

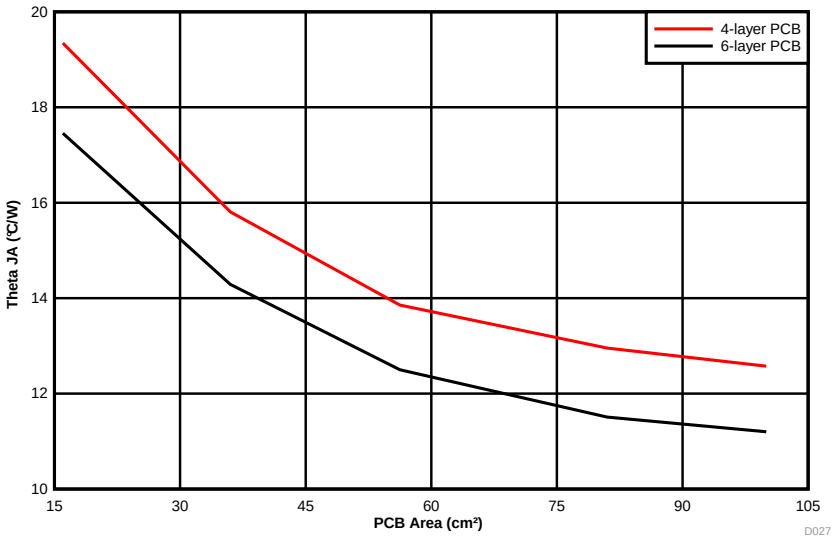


图 52. θ_{JA} vs PCB Area

10.4 Package Specifications

表 9. Package Specifications Table

LMZM33606		VALUE	UNIT
Weight		2.0	grams
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	85.5	MHrs

10.5 EMI

The LMZM33606 is compliant with EN55011 radiated emissions. 图 53, 图 54, and 图 55 show typical examples of radiated emissions plots for the LMZM33606. The graphs include the plots of the antenna in the horizontal and vertical positions.

10.5.1 EMI Plots

EMI plots were measured using the standard LMZM33606EVM with no input filter.

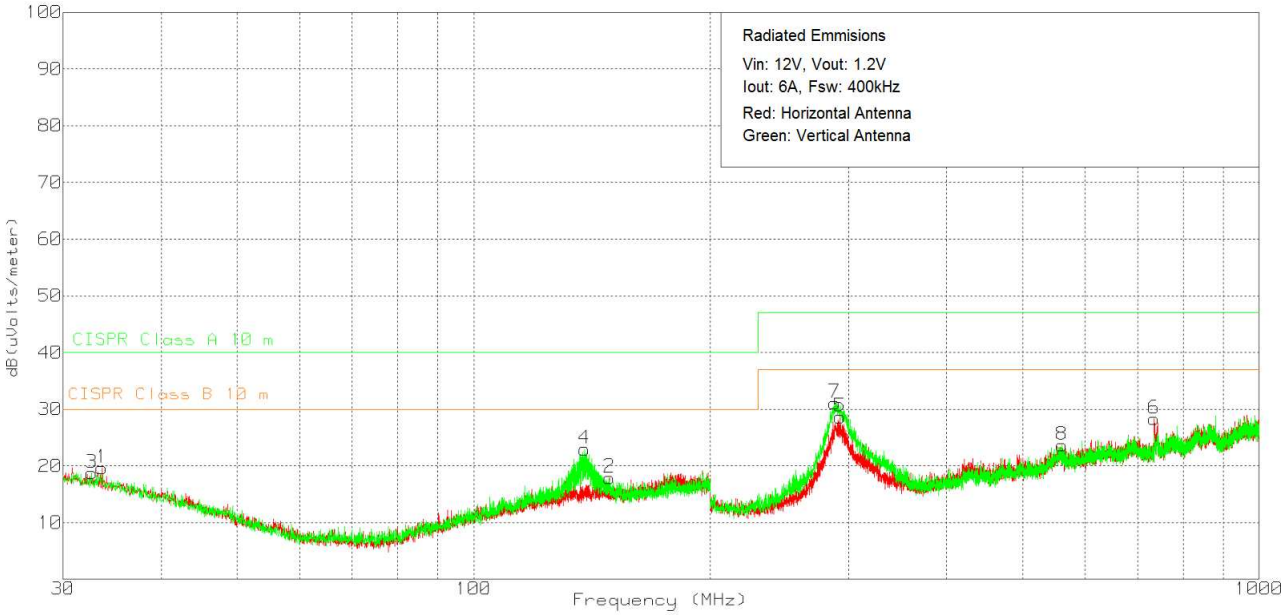


图 53. Radiated Emissions 12-V Input, 1.2-V Output, 6-A Load

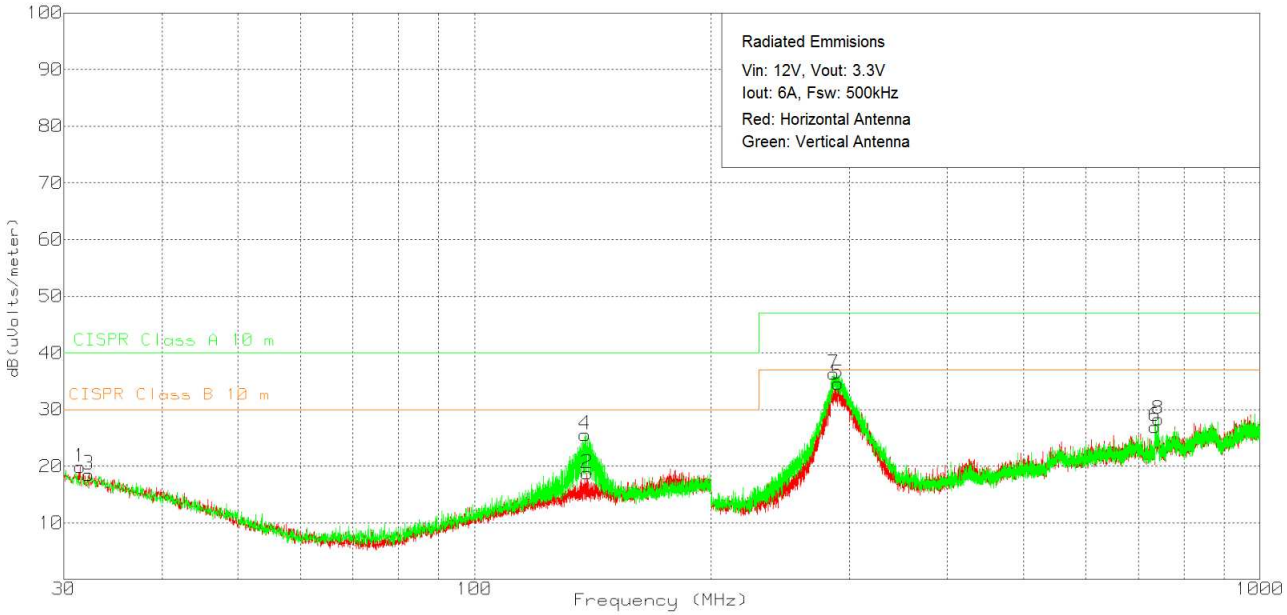


图 54. Radiated Emissions 12-V Input, 3.3-V Output, 6-A Load

EMI (接下页)

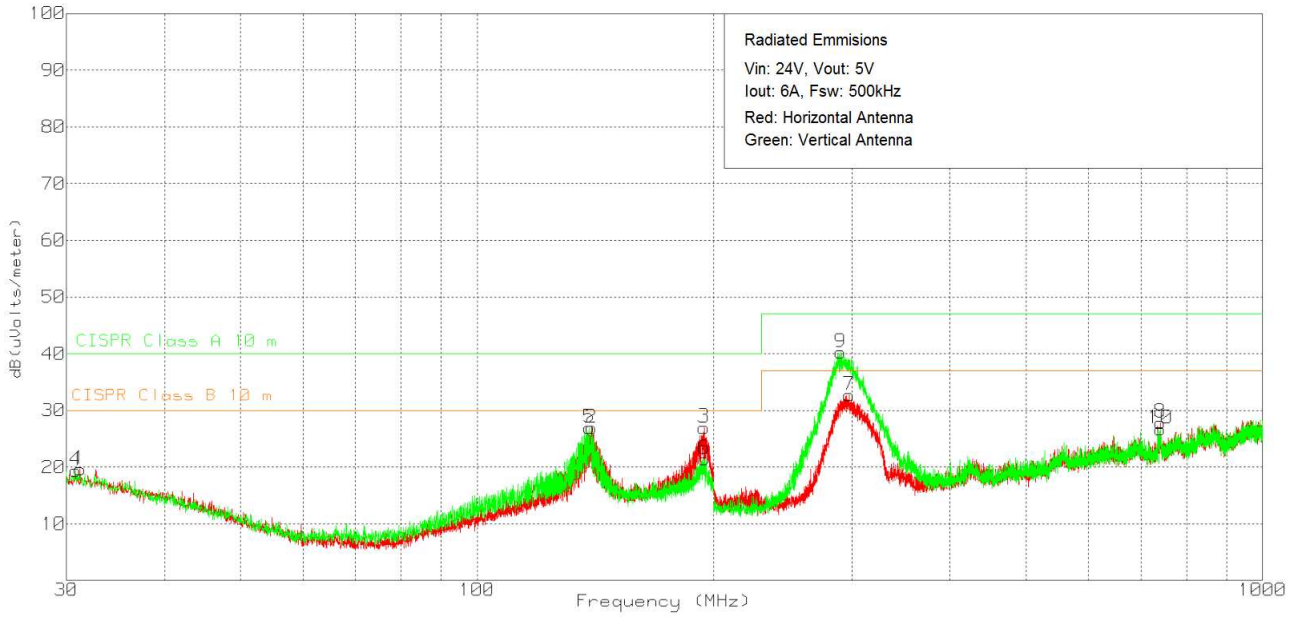


图 55. Radiated Emissions 24-V Input, 5-V Output, 6-A Load

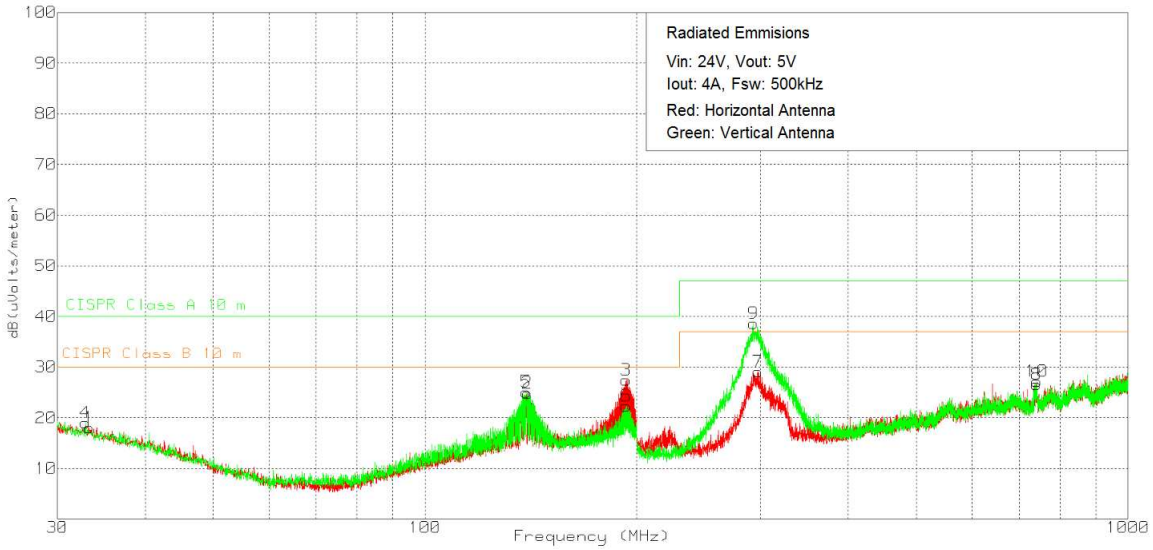


图 56. Radiated Emissions 24-V Input, 5-V Output, 4-A Load

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

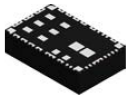
11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

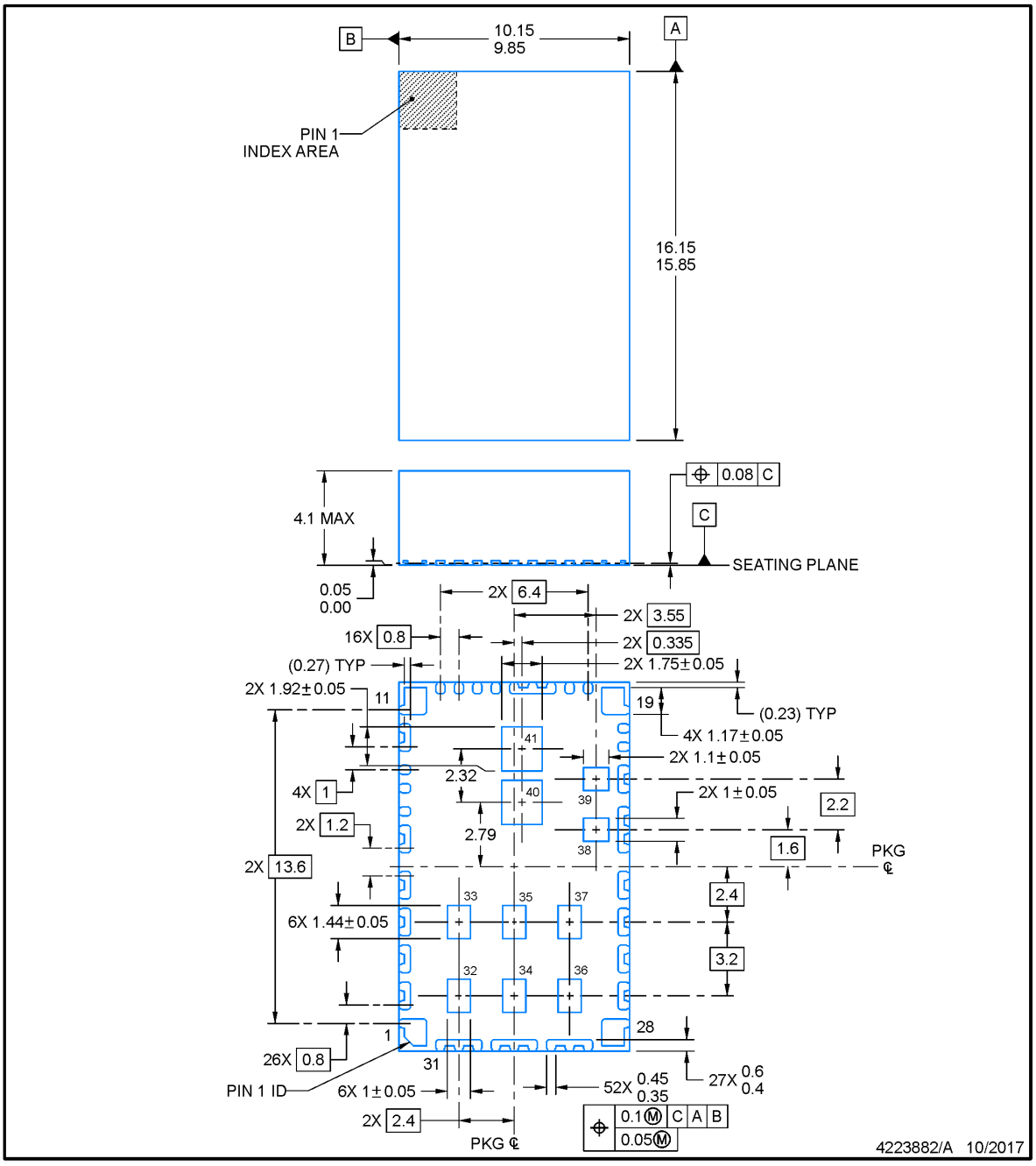


PACKAGE OUTLINE

RLX0041A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

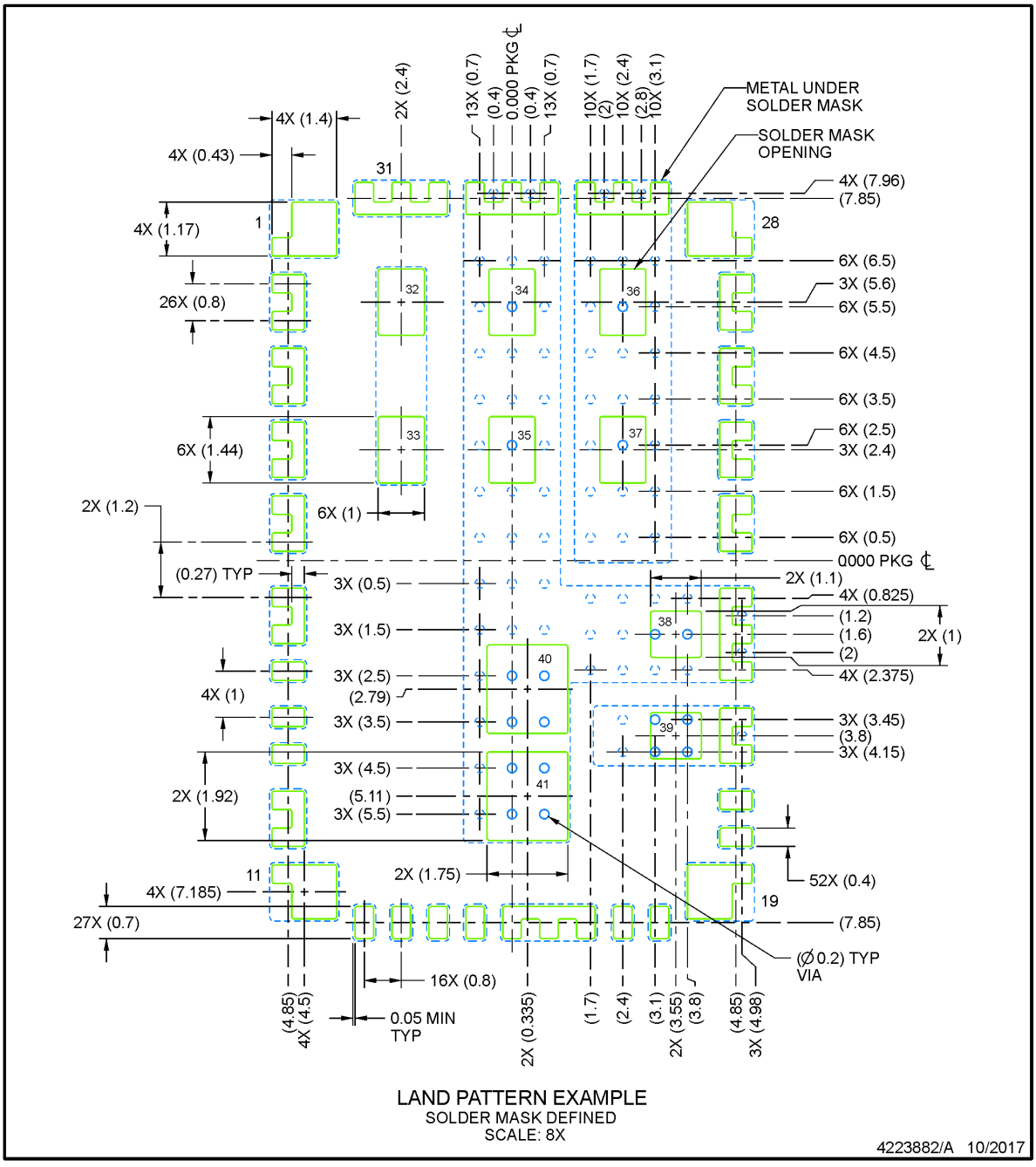
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RLX0041A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 8X

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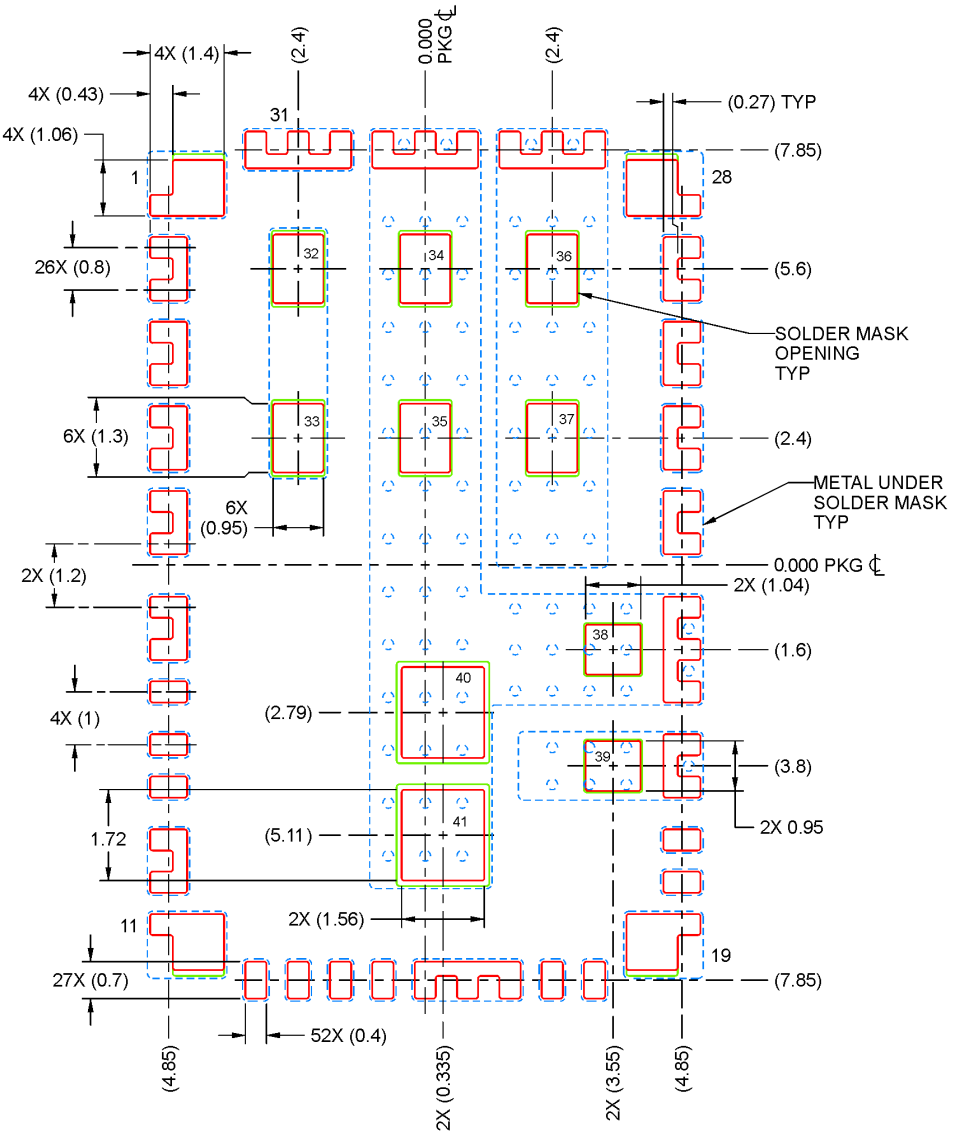
NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RLX0041A — **B3QFN - 4.1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PADS 1,11,19,28,38 & 39: 90%; PADS 32-37: 86%; PADS 40 & 41: 80%
SCALE: 8X

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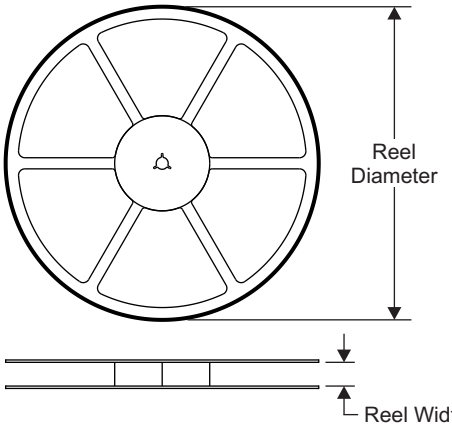
NOTES: (continued)

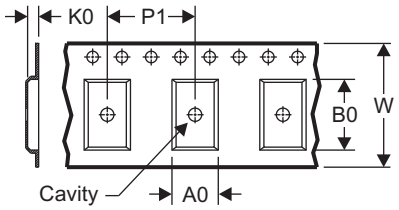
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Tape and Reel Information

REEL DIMENSIONS

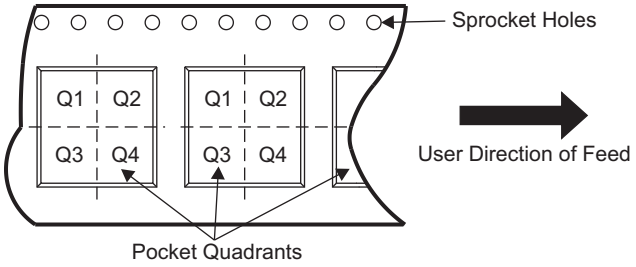


TAPE DIMENSIONS



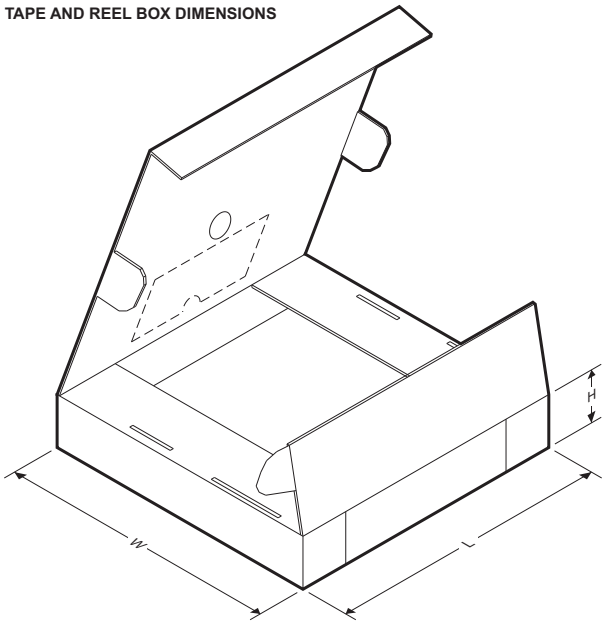
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZM33606RLXR	B2QFN	RLX	41	500	330.0	32.4	10.45	16.45	4.4	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZM33606RLXR	B2QFN	RLX	41	500	383.0	353.0	58.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZM33606RLXR	Active	Production	B3QFN (RLX) | 41	500 | LARGE T&R	Exempt	NIPDAU	Level-3-240C-168 HR	-40 to 105	LMZM33606
LMZM33606RLXRG4	Active	Production	B3QFN (RLX) | 41	500 | LARGE T&R	Yes	NIPDAU	Level-3-240C-168 HR	-40 to 105	LMZM33606
LMZM33606RLXRG4.B	Active	Production	B3QFN (RLX) | 41	500 | LARGE T&R	Yes	NIPDAU	Level-3-240C-168 HR	-40 to 105	LMZM33606

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

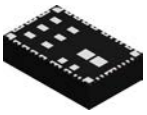
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

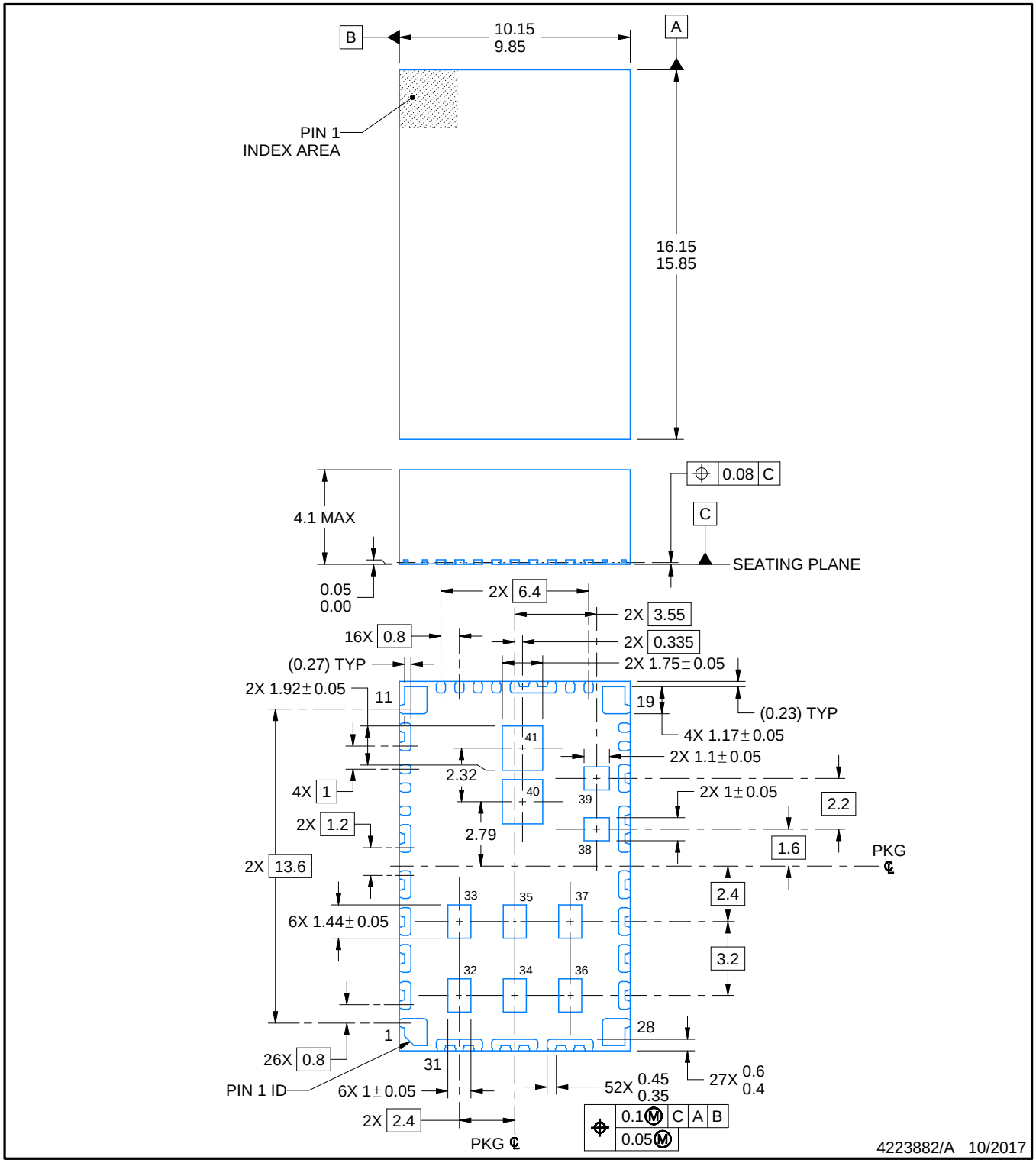
RLX0041A



PACKAGE OUTLINE

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

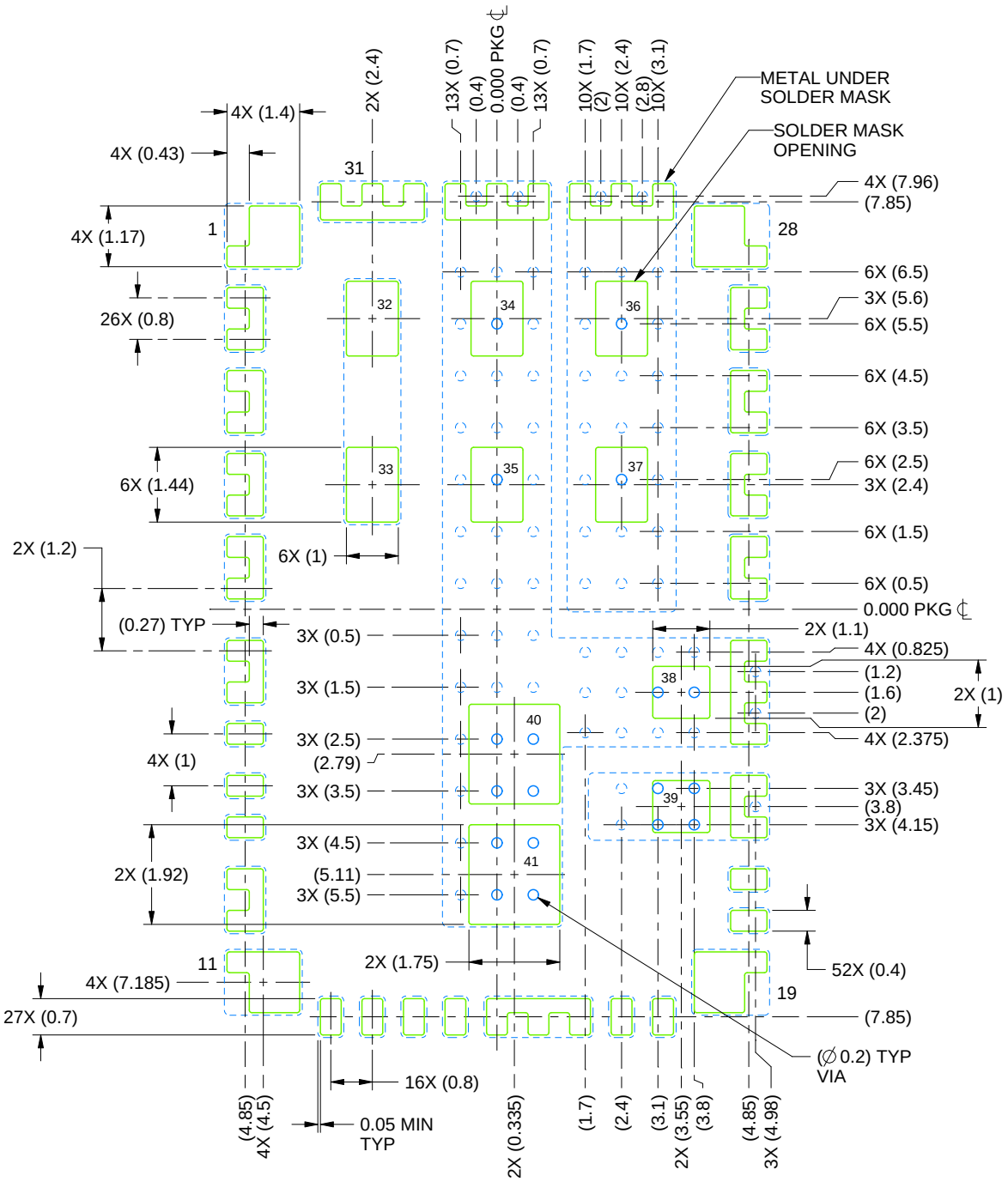
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RLX0041A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 8X

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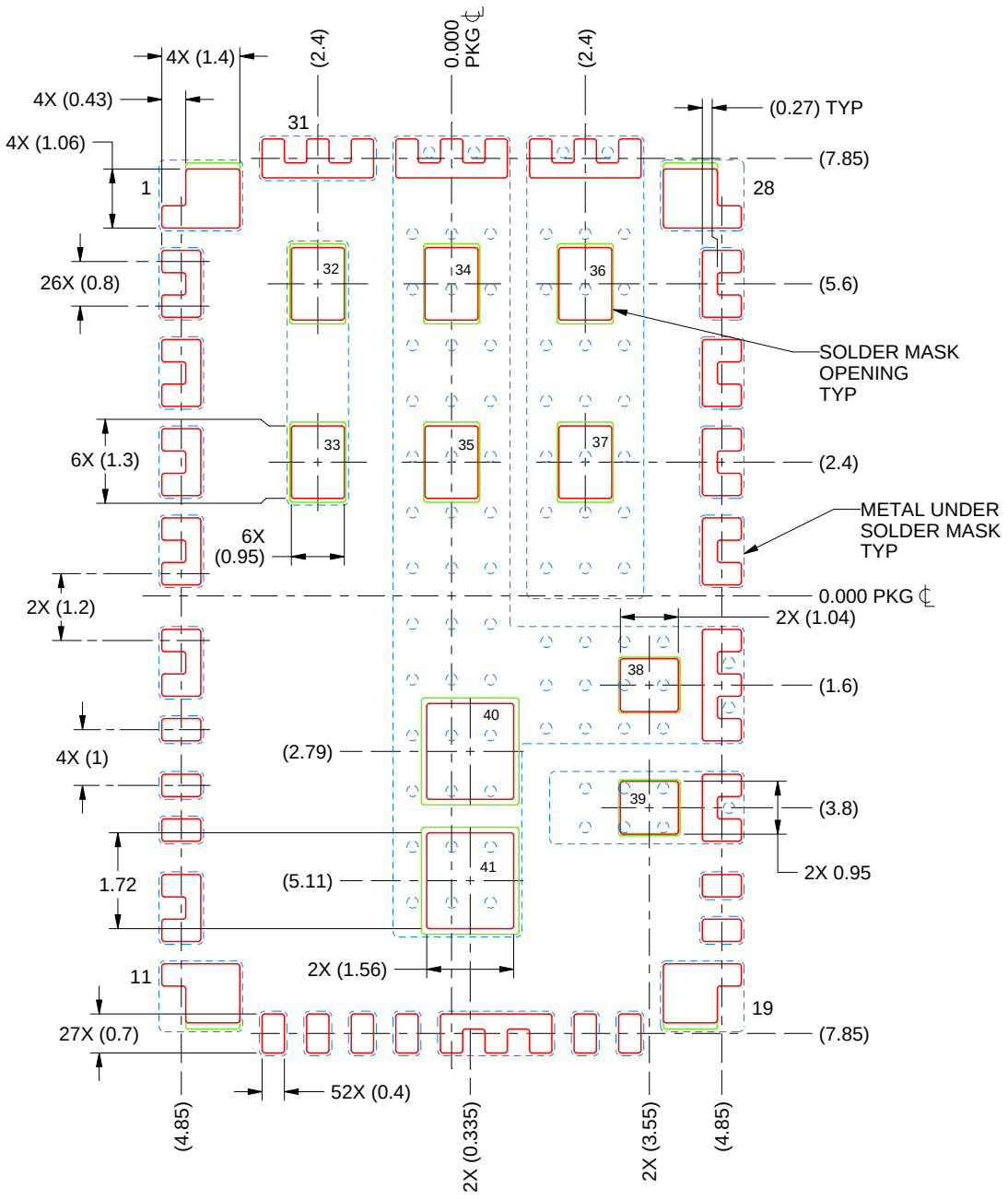
NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PADS 1,11,19,28,38 & 39: 90%; PADS 32-37: 86%; PADS 40 & 41: 80%
SCALE: 8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月