LP3983 Micropower, Low Quiescent Current, CMOS Voltage Regulator in DSBGA Package

Check for Samples: LP3983

FEATURES

- **Miniature 5 Pin Package**
- **Logic Controlled Enable**
- **No Noise Bypass Capacitor Required**
- **Stable with Low ESR Ceramic Capacitors**
- **Fast Turn ON**
- **Short Circuit Protection**

APPLICATIONS

- **GSM Portable Phones**
- **CDMA Cellular Handsets**
- **Bluetooth Devices**
- **Portable Information Appliances**

KEY SPECIFICATIONS

- **Input Voltage Range: 2.5V to 6.0V**
- **Output Voltages: 1.6V, 1.8V, and 2.5V**
- **Output Current: 5 mA**
- **Output Capacitors: 1µF Low ESR**
- **Virtually Zero I_Q (Disabled): 1.0 µA**
- **Low I_Q (Enabled): 14 µA**
- **PSRR: 10 dB**
- **Fast Start Up: 170 µs**

DESCRIPTION

The LP3983 is a fixed voltage low current regulator.

The LP3983 is ideally suited to standby type applications in battery powered equipment, it allows the lifetime of the battery to be maximized. The device can be controlled via an Enable(disable) control and can thus be used by the system to further extend the battery lifetime by reducing the power consumption to virtually zero.

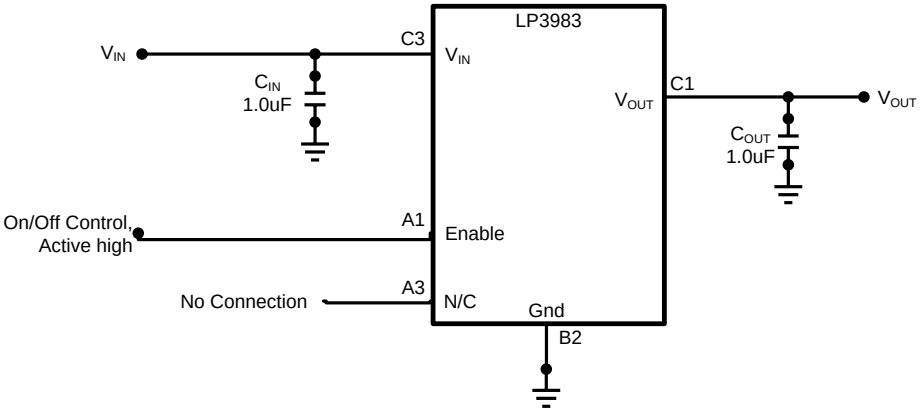
Performance is specified for a -40°C to 125°C temperature range.

For output voltages other than those stated and alternative package options, please contact your local NSC sales office.

Package

- 5 Bump Thin DSBGA Package

Typical Application Circuit



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Block Diagram

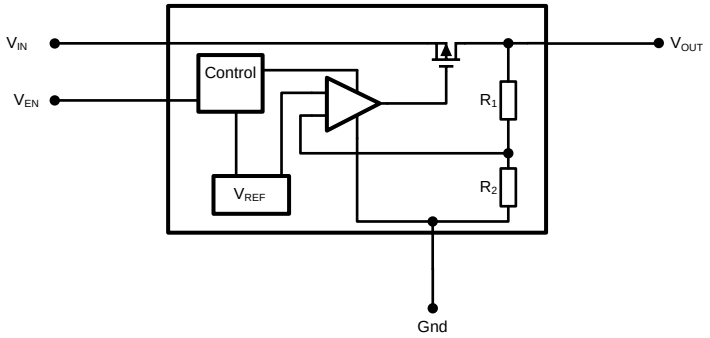


Figure 1. LP3983

Connection Diagrams

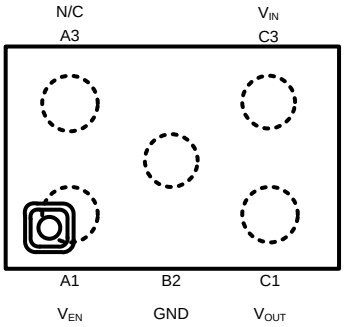


Figure 2. 5 Pin DSBGA Package Top View
See Package Number YZR0005ADA

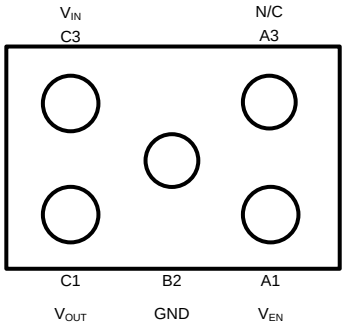


Figure 3. 5 Pin DSBGA Package Bottom View
See Package Number YZR0005ADA

PIN DESCRIPTIONS

Name	Pin No.	Name and Function
V_{EN}	A1	Enable Input Logic, Enables regulator when ≥ 1.2V. Disables regulator when ≤ 0.5V
GND	B2	Common Ground
V_{OUT}	C1	Voltage Output. Connect this Output to the Load Circuit.
V_{IN}	C3	Unregulated supply Input.
N/C	A3	No Connection. There should be no electrical connection made to this pin.

ORDERING INFORMATION (1) (2)

OUTPUT VOLTAGE (V)	GRADE	MINIMUM QUANTITY	OUTPUT MEDIA	ORDERABLE NUMBER
1.6	STD	250	Mini-Reel	LP3983ITL-1.6
		3000	Tape and Reel	LP3983ITLX-1.6
1.8		250	Mini-Reel	LP3983ITL-1.8
		3000	Tape and Reel	LP3983ITLX-1.8
2.5		250	Mini-Reel	LP3983ITL-2.5
		3000	Tape and Reel	LP3983ITLX-2.5

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

V_{IN}	−0.3 to 6.5V
V_{EN}	−0.3 to (V_{IN} + 0.3V) to 6.5V(max)
V_{OUT}	−0.3V to(V_{IN} + 0.3V) to 6.5V(max)
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Pad Temperature (Soldering, 10 sec.)	265°C
ESD (4)	
Human Body Model	2KV
Machine Model	100V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Ratings(1)(2)

V_{IN}(3)	$V_{IN(MIN)}$to 6V
V_{EN},	0 to 6.0V
Recommended Load Current	0 to 5mA
Junction Temperature	−40°C to +125°C
Ambient Temperature (4)	−40°C to +119°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) The minimum V_{IN} is dependant on the device output option.For $V_{OUT(NOM)} \leq 2.7V$, $V_{IN(MIN)}$ will equal 2.5V. For $V_{OUT(NOM)} > 2.7V$, $V_{IN(MIN)}$ will equal $V_{OUT(NOM)}$ + 200mV.
(4) The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Thermal Properties(1)

Junction to Ambient Thermal Resistance (θ_{JA})(2)	255°C/W

(1) The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.
(2) Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.8V,V_{IN} = $V_{OUT(nom)}$ + 1.0V, C_{IN} = 1.0 µF, I_{OUT} = 1.0mA, C_{OUT} = 1.0 µF.
Typical values and limits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 0mA to 5mA		-55	+55	mV from $V_{OUT(nom)}$
				-96	**+96**	
				− 6	**+6**	% of $V_{OUT(nom)}$
PSRR	Power Supply Rejection Ratio	V_{IN} = $V_{OUT(nom)}$ + 1V, f ≤10 kHz, I_{OUT} = 1mA	10			dB
I_Q	Quiescent Current	I_{OUT} = 50µA, V_{IN} = 4.2V	14		**21**	µA
		V_{EN} = 0.4V, V_{IN} = 4.2V	1		**3**	
I_{SC}	Short Circuit Current Limit (3)	Output Grounded	28		**35**	mA
I_{OUT}	Maximum Output Current	(4)		**5**		mA
Logic Control Characteristics						
I_{EN}	Maximum Input Current at V_{EN} input	V_{EN} = 0.4 and V_{IN}= 6.0V	0.02			µA
V_{IL}	Logic Low Input Threshold	V_{IN} = $V_{IN(MIN)}$ to 6.0V			**0.5**	V
V_{IH}	Logic High Input Threshold	V_{IN} = $V_{IN(MIN)}$ to 6.0V		**1.2**		V
Timing Characteristics						
T_{ON}	Turn on Time (3)	(5)	170		**250**	µs

(1) All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage which is labelled $V_{OUT(NOM)}$ is the desired voltage option.
(3) This electrical specification is guaranteed by design.
(4) The device maintains the regulated output voltage without load.
(5) Time from V_{EN} = 1.2V to V_{OUT} = 95% of $V_{OUT(NOM)}$

Electrical Characteristics Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Value	Limit		Units
				Min	Max	
C_o	Output Capacitor	Capacitance (1)	1.0	0.75		µF
		ESR		5	500	mΩ

(1) The capacitor tolerance should be ±25% or better over the temperature range. Capacitor types recommended are X7R, Y5V, and Z5U.

Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Ceramic, $V_{IN} = V_{OUT(nom)} + 1.0V$, $T_A = 25°C$, Enable pin is tied to V_{IN}.

Ground Current @ T_A = 25°C

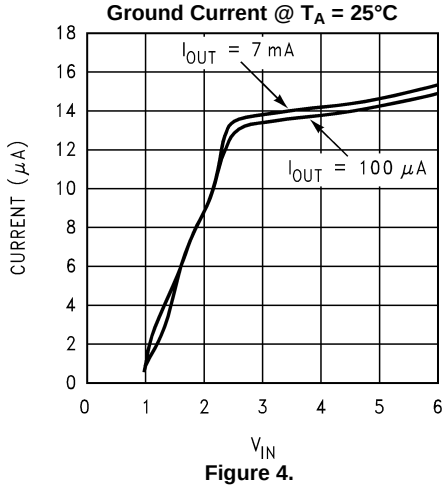


Figure 4.

Ground Current vs V_{IN}. I_{OUT} = 7mA

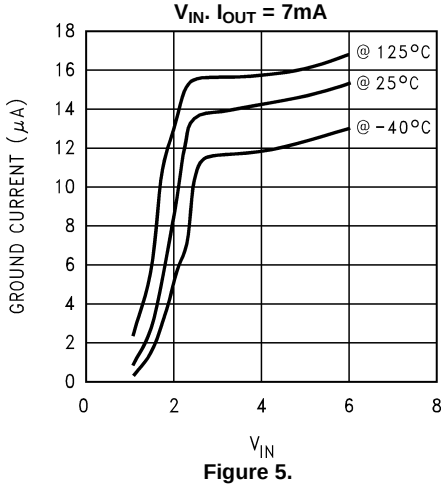


Figure 5.

Ripple Rejection ($C_{IN} = C_{OUT}$ = 1μF, I_L = 100μA)

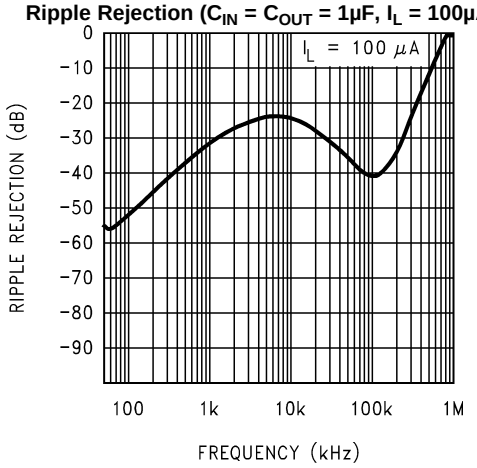


Figure 6.

Start Up Time. V_{OUT} = 1.8V

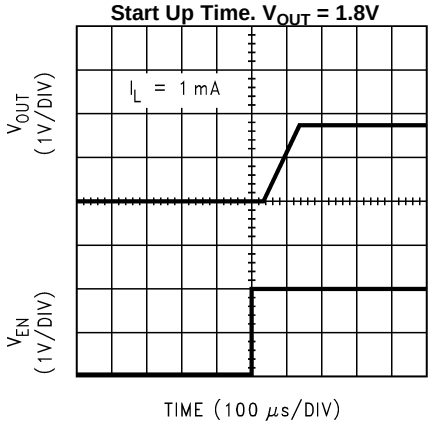


Figure 7.

Turn-Off Time. V_{OUT} = 1.8V

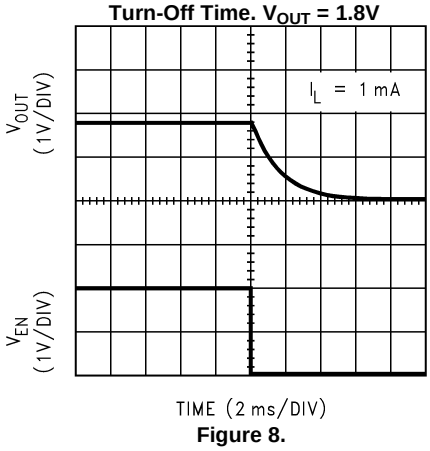


Figure 8.

Load Transient Response. V_{OUt} = 1.8V

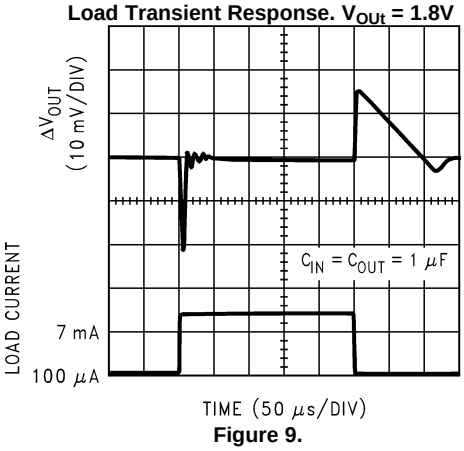


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT(nom)} + 1.0V$, $T_A = 25°C$, Enable pin is tied to V_{IN}.

Line Transient Response

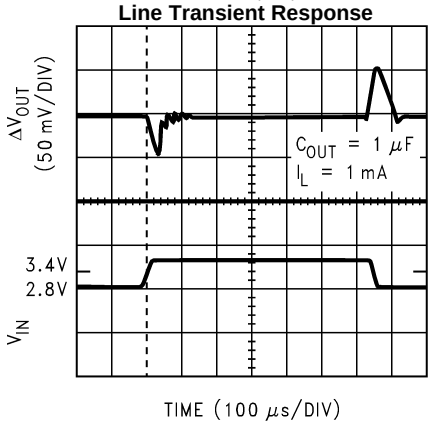


Figure 10.

APPLICATION HINTS

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in the Electrical Characteristics section, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = (T_J - T_A)/\theta_{JA} \quad (1)$$

With a θ_{JA} = 255°C/W, the device in the DSBGA package returns a value of 392mW with a maximum junction temperature of 125°C and an ambient temperature of 25°C. The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal considerations, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

In common with most low-dropout regulators, the LP3983 requires external capacitors to ensure stable operation. The LP3983 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0uF capacitor be connected between the LP3983 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the **ESR** (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3983 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R), recommended value 2.2µF and with ESR between 5mΩ to 500mΩ, is suitable in the LP3983 application circuit.

For this device the output capacitor should be connected between the VOUT pin and ground.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see the section CAPACITOR CHARACTERISTICS).

NO-LOAD STABILITY

The LP3983 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3983 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1µF to 4.7µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3983.

The temperature performance of ceramic capacitors varies by type. Larger value ceramic capacitors may be manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

ENABLE OPERATION

The LP3983 may be switched ON or OFF by a logic input at the ENABLE pin, V_{EN}. A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes < 1µA. If the application does not require the shutdown feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in Application Note AN-1112, (SNVA009).

Referring to the section *PCB Layout*, it should be noted that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight may cause mis-operation of the device. Light sources such as Halogen lamps can effect electrical performance if brought near to the device.

Light with wavelengths in the red and infra-red part of the spectrum have the most detrimental effect thus the fluorescent lighting used inside most buildings has very little effect on the output voltage of the device. Tests carried out on a DSBGA test board showed a negligible effect on the regulated output voltage when brought within 1cm of a fluorescent lamp. A deviation of less than 0.1% from nominal output voltage was observed.

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3983ITL-2.5/NOPB	Active	Production	DSBGA (YZR) | 5	250 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3
LP3983ITL-2.5/NOPB.A	Active	Production	DSBGA (YZR) | 5	250 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

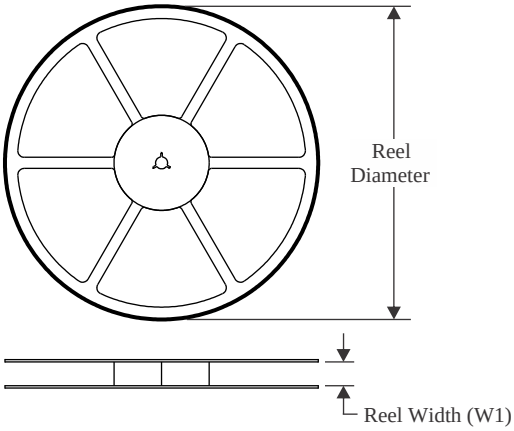
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

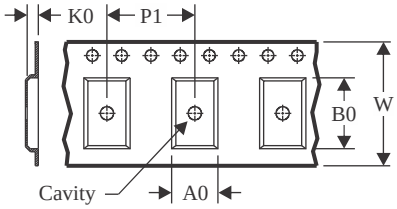
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

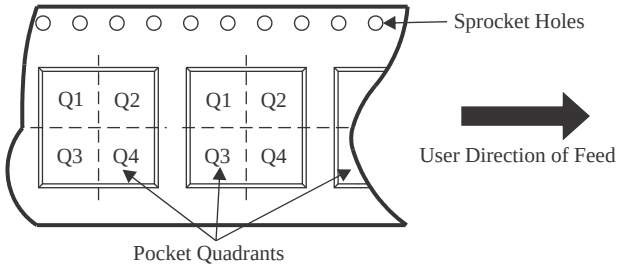


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

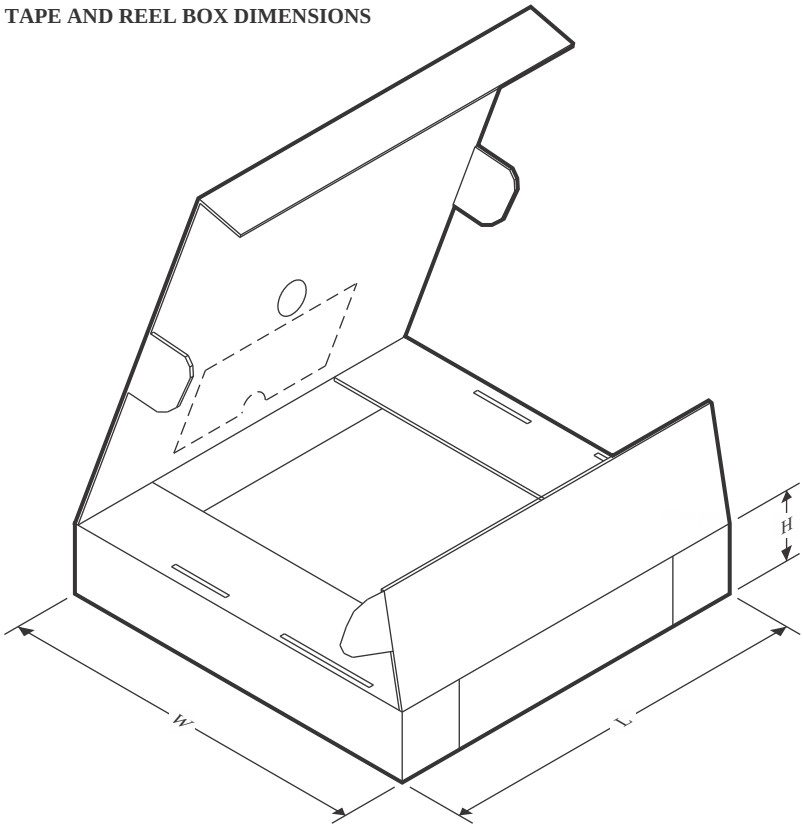
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3983ITL-2.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1

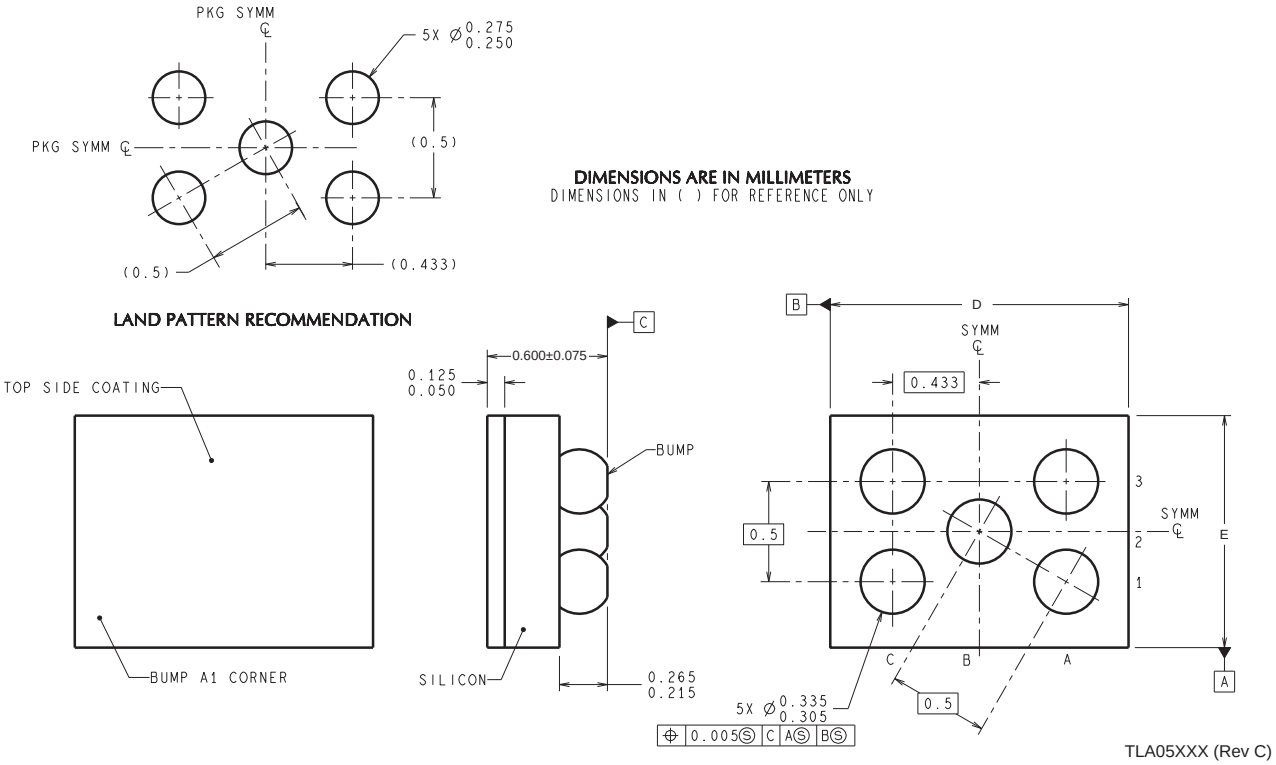
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3983ITL-2.5/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0

YZR0005



D: Max = 1.502 mm, Min =1.441 mm

E: Max = 1.045 mm, Min =0.984 mm

4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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