具有电源正常指示功能的微功耗，150mA 超低压降 CMOS 电压稳压器

查询样品: LP3988-Q1

特性

- 符合汽车应用要求
- 具有下列结果的 **AEC-Q100** 测试指南：
  - 器件温度 **1** 级：**-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C4B**
- 小外形尺寸晶体管 **(SOT)23-5** 封装
- 电源正常标志输出
- 逻辑控制使能
- 与陶瓷电容器和高品质钽电容器一起工作时保持稳定
- 快速接通
- 热关断和短路电流限制

应用范围

- 汽车用
- **CDMA** 手机
- 宽带 **CDMA** 手机
- **GSM** 手机
- 便携式信息设备
- 微型 **3.3V ± 5%** 至 **2.85V**，**150mA** 转换器

说明

LP3988-Q1 是一款 150mA 低压降稳压器，此款稳压器被专门设计成满足便携式电池供电类应用的要求。 LP3988-Q1 与节省空间的，1µF 陶瓷电容器一同工作。 LP3988-Q1 特有一个指示故障输出情况的错误标志输出。

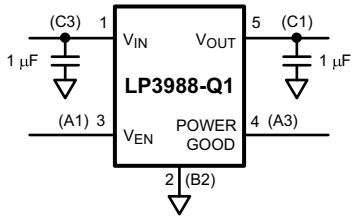
LP3988-Q1 的性能针对电池供电类系统进行了优化以传送低噪声、极低压降电压和低静态电流。 稳压器接地电流只是轻微地增加了压降，这样进一步延长了电池使用寿命。

低频时电源抑制比好于 60dB，并且在 10kHz 时开始下降。 此器件将高电源抑制比保持在低水平，以降低到电池供电类电路的共同输入电压电平。

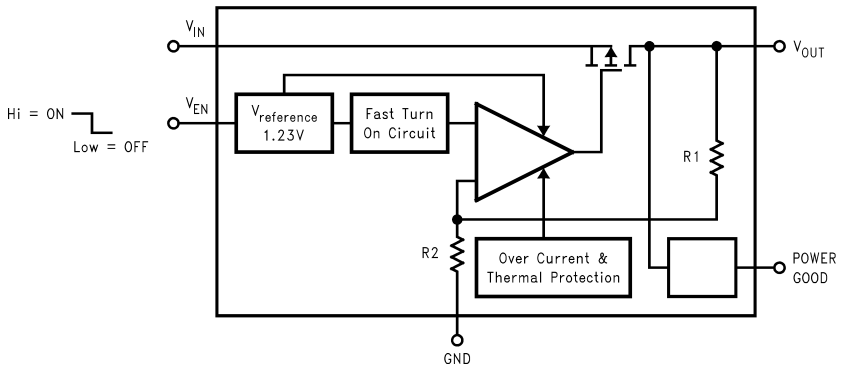
此器件是手机和相类似的电池供电类无线应用的理想选择。 它在由 2.5V 至 6V 输入电压供电时，可提供高达 150mA 的电流，在禁用模式中流耗少于 1µA，并且快速接通时间小于 200µs。

LP3988-Q1 采用 5 引脚 SOT-23 封装，额定运行温度范围为 -40°C 至 125°C，并且可提供 2.85V 输出电压。 **请注意：**对于其它电压选项，请与 TI 销售商取得联系。

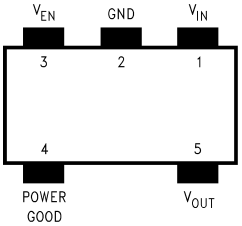
Typical Application Circuit



Block Diagram



SOT-23-5 PACKAGE
TOP VIEW



Pin Descriptions

Name	SOT-23	Function
V_{EN}	3	Enable Input Logic, Enable High
GND	2	Common Ground
V_{OUT}	5	Output Voltage of the LDO
V_{IN}	1	Input Voltage of the LDO
Power Good	4	Power Good Flag (output): open-drain output, connected to an external pull-up resistor. Active low indicates an output voltage out of tolerance condition.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage		−0.3	6.5	V
Power good	V_{OUT}, V_{EN}	−0.3 V to (V_{IN} + 0.3 V)	6	V
Junction temperature			150	°C
Storage Temperature		−65	150	°C
Power dissipation (1)	SOT-23-5		364	mW
ESD rating (2)	Human-body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C4B		750	V

(1) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A) / \theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 364-mW rating appearing under *Absolute Maximum Ratings* for the SOT-23-5 package results from substituting the absolute-maximum junction temperature, 150°C, for T_J, 70°C for T_A, and 175°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C . Less power can be dissipated safely at ambient temperatures above 70°C. The absolute-maximum power dissipation can be increased by 4.5 mW for each degree below 70°C, and it must be derated by 4.5 mW for each degree above 70°C.

(2) The human-body model is 100 pF discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN} (2)	2.5		6	V
V_{OUT}, V_{EN}	0		V_{IN}	V
Operating temperature	−40		125	°C

(1) All voltages are with respect to the potential at the GND pin.

(2) The minimum V_{IN} depends on the device output option. For $Vout_{(NOM)} < 2.5V$, $V_{IN(MIN)}$ will equal 2.5V. For $Vout_{(NOM)} \geq 2.5V$, $V_{IN(MIN)}$ will equal $Vout_{(NOM)}$ + 200mV.

Thermal Information

THERMAL METRIC(1)		SOT-23 Package DBV-5	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	175	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	78	°C/W
θ_{JB}	Junction-to-board thermal resistance	31.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_A = 25°C. Limits appearing in **boldface type** apply over the entire operating temperature range for operation, −40°C to 125°C. (1) (2)

Symbol	Parameter	Conditions	Limit			Units
			Min	Typ	Max	
ΔV_{OUT}	Output voltage tolerance	−40°C ≤ T_A ≤ 125°C, SOT-23-5	−2 **−3.5**		2 **3.5**	% of $V_{OUT(nom)}$
	Line-regulation error	V_{IN} = $V_{OUT\ (NOM)}$ + 0.5 V to 6 V	−0.15 **−0.2**		0.15 **0.2**	%/V
	Load-regulation error (3)	I_{OUT} = 1 mA to 150 mA			0.005 **0.007**	%/mA
PSRR	Power-supply rejection ratio	V_{IN} = $V_{OUT(nom)}$ + 1 V, f = 1 kHz, I_{OUT} = 50 mA (Figure 3)		65		dB
		V_{IN} = $V_{OUT(nom)}$ + 1 V, f = 10 kHz, I_{OUT} = 50 mA (Figure 3)		45		
I_Q	Quiescent current	V_{EN} = 1.4 V, I_{OUT} = 0 mA		85	120	µA
		V_{EN} = 1.4 V, I_{OUT} = 0 to 150 mA		140	**200**	
		V_{EN} = 0.4V		0.003	**1.0**	
	Dropout Voltage (4)	I_{OUT} = 1 mA		1	**5**	mV
		I_{OUT} = 150 mA		80	115 **150**	
I_{SC}	Short Circuit Current Limit	See (5)		600		mA
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1 µF		220		µVrms
C_{OUT}	Output Capacitor	Capacitance (6)	**1**		**20**	µF
		ESR (6)	**5**		**500**	mΩ
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			20		°C
Enable Control Characteristics (7)						
I_{EN}	Maximum Input Current at EN	V_{EN} = 0 and V_{IN} = 6 V			**0.1**	µA
V_{IL}	Logic Low Input threshold	V_{IN} = 2.5 V to 6 V			**0.5**	V
V_{IH}	Logic High Input threshold	V_{IN} = 2.5 V to 6 V	**1.2**			V
Power Good						
V_{THL} V_{THH}	Power Good Low threshold High Threshold	% of V_{OUT} (PG ON) Figure 2 % of V_{OUT} (PG OFF) Figure 2 (8)	90 92	93 95	95 98	%
V_{OL}	PG Output Logic Low Voltage	$I_{PULL-UP}$ = 100 µA, fault condition		0.02	**0.1**	V
I_{PGL}	PG Output Leakage Current	PG off, V_{PG} = 6 V		0.02		µA
t_{ON}	Power Good Turn On time, (4)	V_{IN} = 4.2V		10		µs
t_{OFF}	Power Good Turn Off time, (4)	V_{IN} = 4.2V		10		µs

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_A = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
(3) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(5) Short-circuit current is measured on input supply line after pulling down V_{OUT} to 95% $V_{OUT(nom)}$.
(6) Specified by design. The capacitor tolerance should be ±30% or better over the full temperature range. The full range of operating conditions such as temperature, dc bias and even capacitor case size for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitor types are recommended to meet the full device temperature range.
(7) Turnon time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.
(8) The low and high thresholds are generated together. Typically a 2.6% difference is seen between these thresholds.

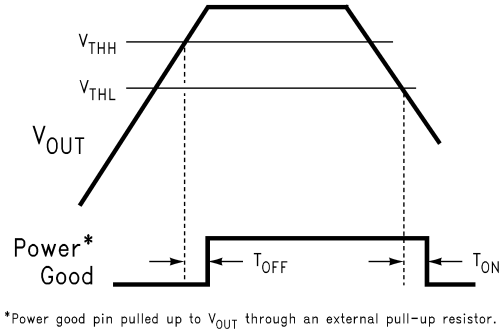


Figure 1. Power Good Flag Timing

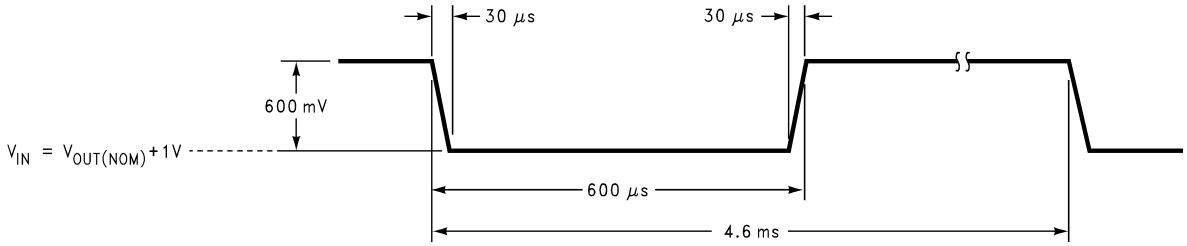


Figure 2. Line Transient Response Input Perturbation

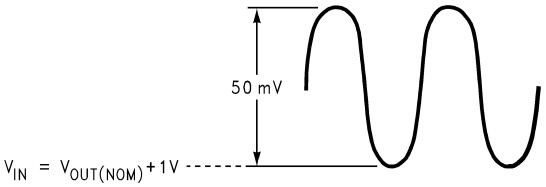


Figure 3. PSRR Input Perturbation

Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, enable pin is tied to V_{IN}.

RIPPLE REJECTION RATIO (LP3988-Q1-2.85)

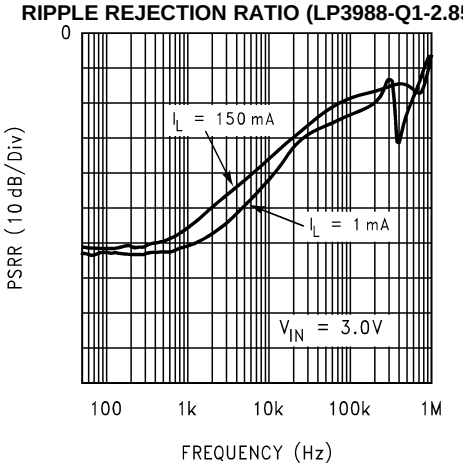


Figure 4.

RIPPLE REJECTION RATIO (LM3988-2.85)

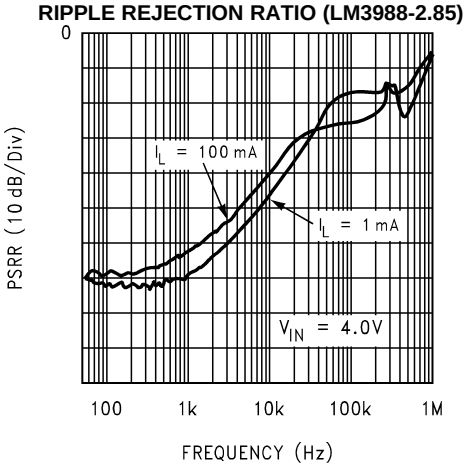


Figure 5.

POWER-GOOD RESPONSE TIME (LP3988-Q1-2.85) (flag pin pulled to V_{OUT} through a 100-kΩ resistor)

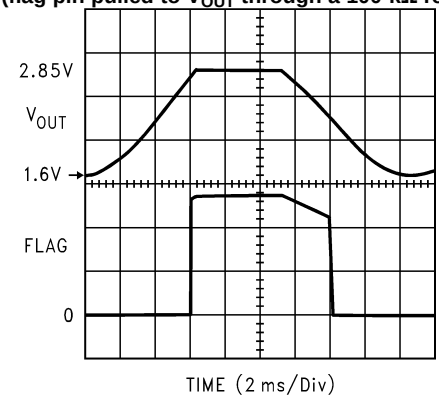


Figure 6.

POWER-GOOD RESPONSE TIME (LP3988-Q1-2.85) (flag pin pulled to V_{IN} through a 100-kΩ resistor)

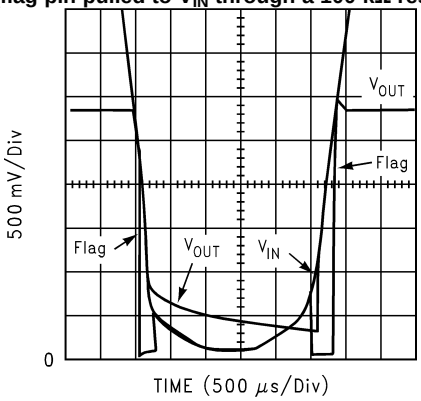


Figure 7.

POWER-GOOD RESPONSE TIME (LP3988-Q1-2.85) (flag pin pulled to V_{OUT} through a 100-kΩ resistor)

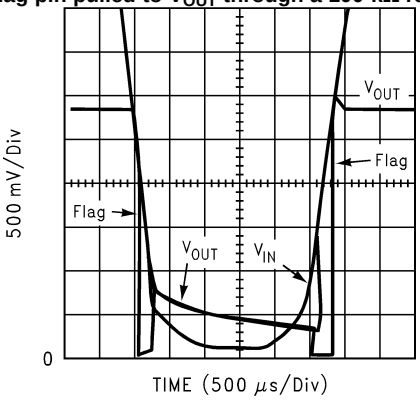


Figure 8.

LINE TRANSIENT RESPONSE (LP3988-Q1-2.85)

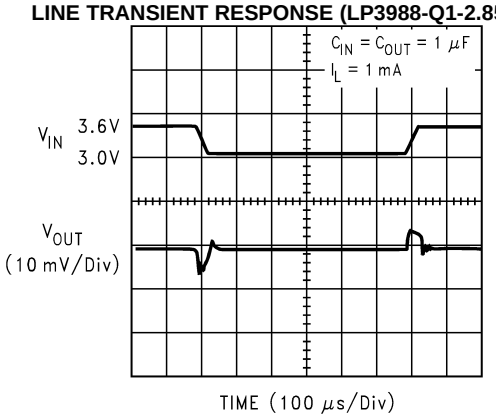


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, enable pin is tied to V_{IN}.

LINE TRANSIENT RESPONSE (LP3988-Q1-2.85)

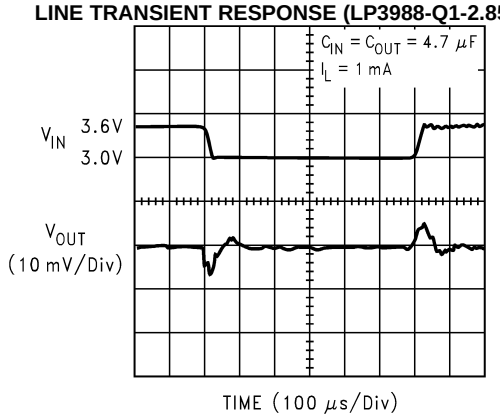


Figure 10.

POWER-UP RESPONSE

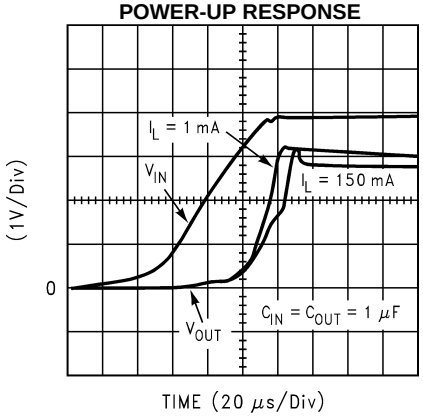


Figure 11.

ENABLE RESPONSE

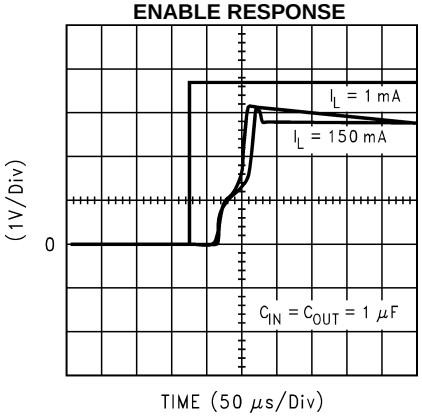


Figure 12.

ENABLE RESPONSE

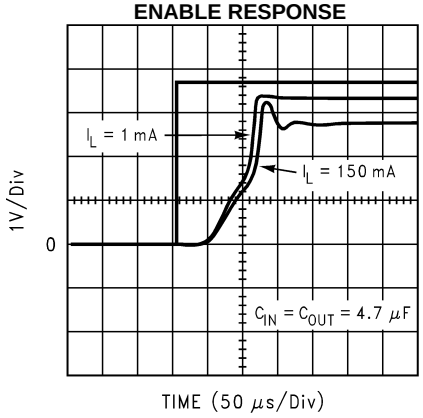


Figure 13.

LOAD-TRANSIENT RESPONSE

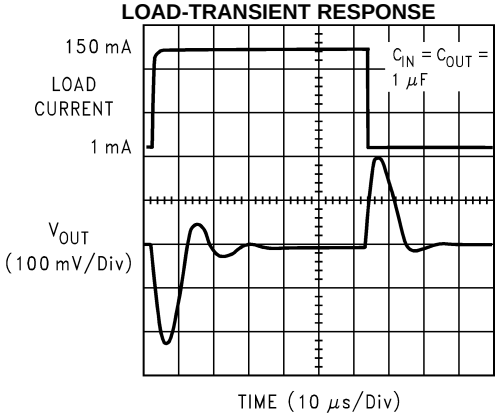


Figure 14.

LOAD-TRANSIENT RESPONSE

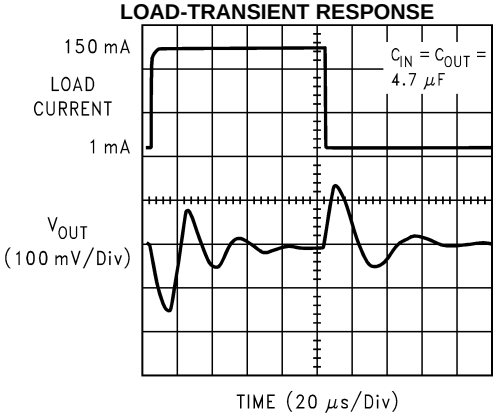


Figure 15.

APPLICATION INFORMATION

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3988-Q1 requires external capacitors for regulator stability. The LP3988-Q1 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 1µF is required between the LP3988-Q1 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge-current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance is ≅ 1 µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3988-Q1 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in the 1-µF to 22-µF range with a 5-mΩ to 500-mΩ ESR range is suitable in the LP3988-Q1 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see the *CAPACITOR CHARACTERISTICS* section).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an Equivalent Series Resistance (ESR) value which is within a stable range (5 mΩ to 500 mΩ).

NO-LOAD STABILITY

The LP3988-Q1 remains stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3988-Q1 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3988-Q1.

The ceramic capacitor's capacitance can vary with temperature. Most large-value ceramic capacitors (≅ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent-size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

ON/OFF INPUT OPERATION

The LP3988-Q1 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turnon/turnoff voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST ON-TIME

The LP3988-Q1 utilizes a speed-up circuit to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turnon time.

REVISION HISTORY

Changes from Original (March 2013) to Revision A **Page**

- Deleted 其它电压，剩下的只用 2.5V 1
- Added TI 销售商对于额外电压的说明 1
- Changed θ_{JA} temp from 220°C/W to 175°C/W in *Absolute Maxium Ratings* table note 3
- Changed voltage in the title of the first two Typical Characteristics graphs (*Ripple Rejection Ratio*) from 2.6 to 2.85 6
- Changed LP3988Q to correct device name of LP3988-Q1 9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3988QMFX-2P85	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RABQ
LP3988QMFX-2P85.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RABQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LP3988-Q1 :

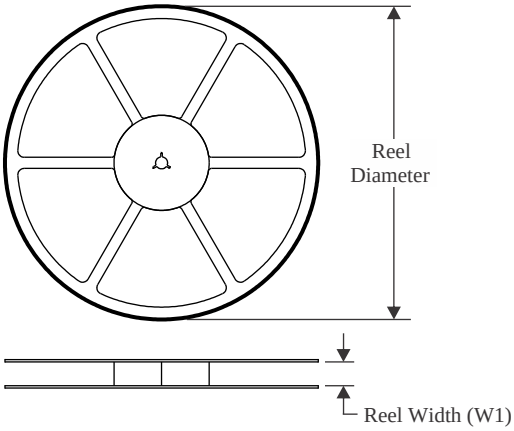
- Catalog : LP3988

NOTE: Qualified Version Definitions:

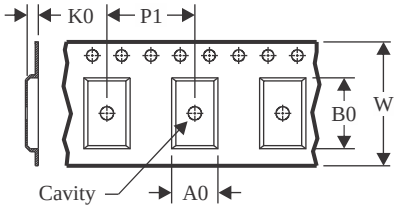
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

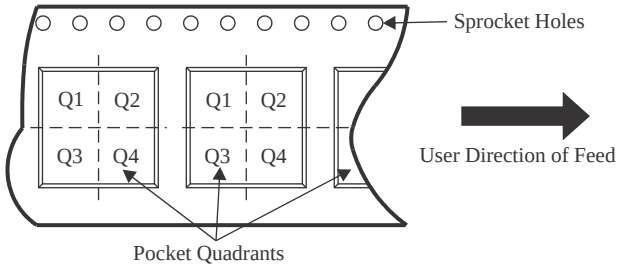


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

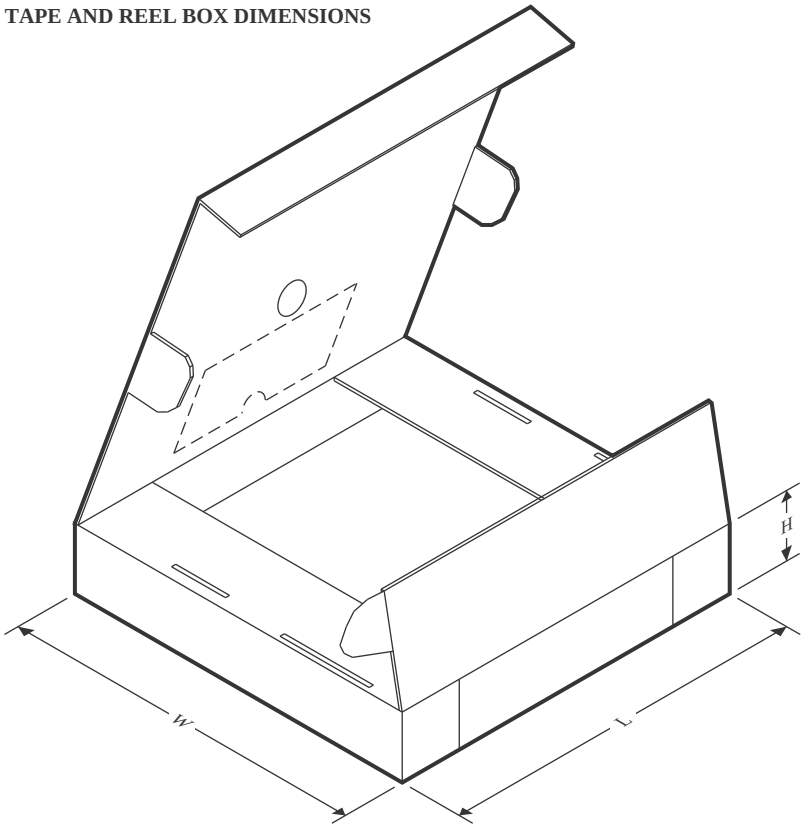
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3988QMFX-2P85	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

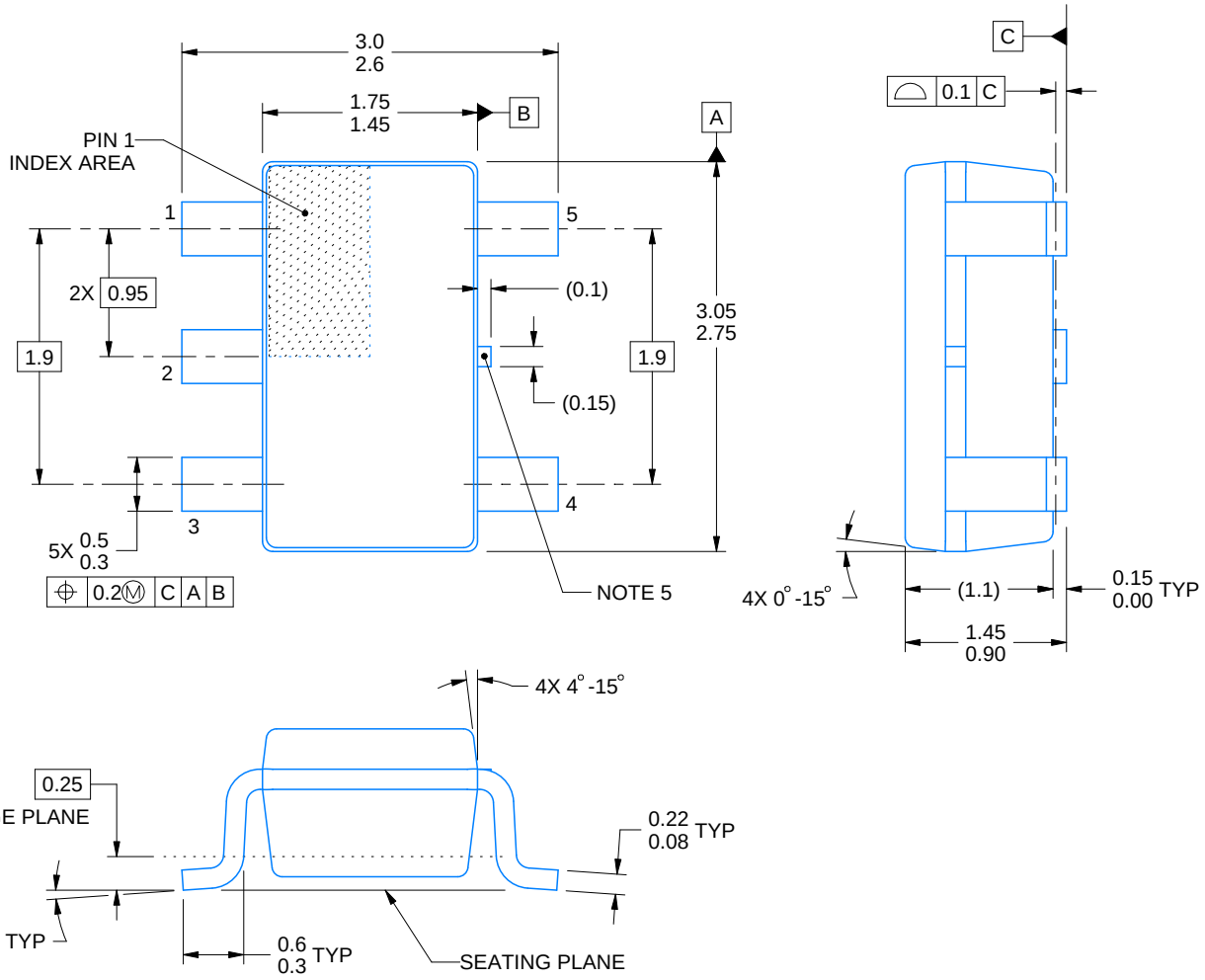
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3988QMFX-2P85	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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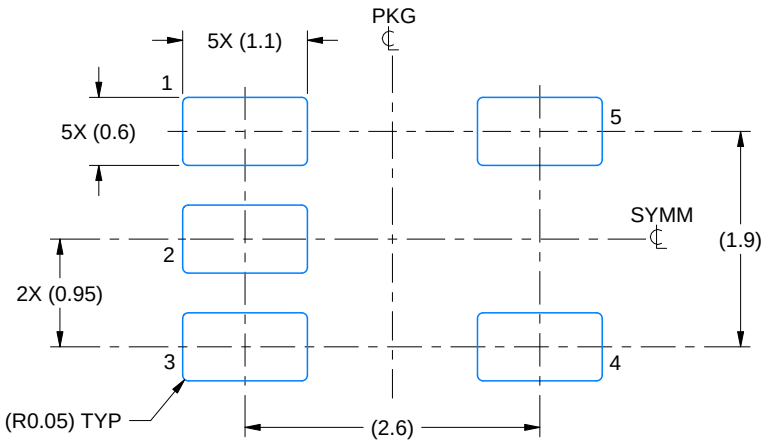
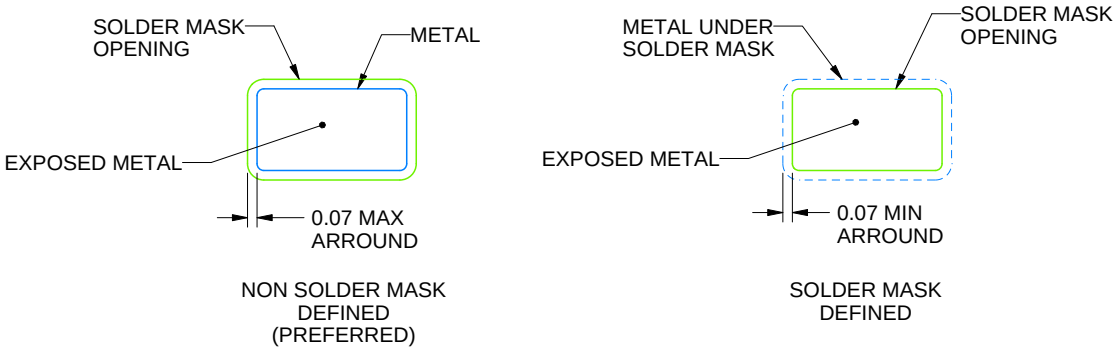
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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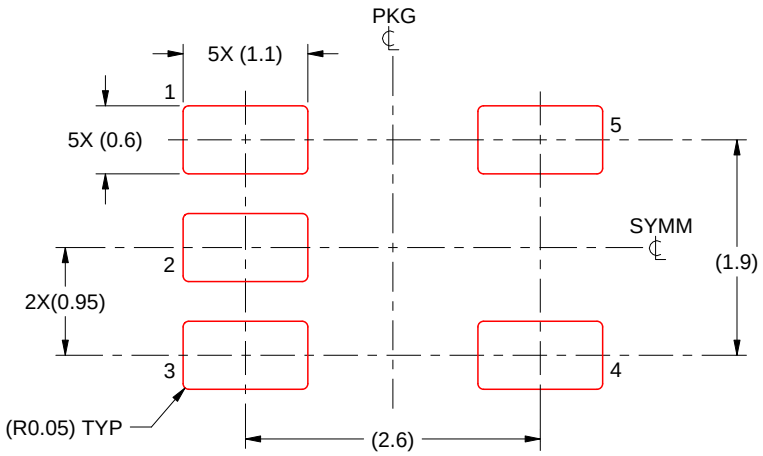
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月