LPV542 双路毫微功耗 1.8V、490nA、RRIO CMOS 运算放大器

1 特性

- 宽电源电压范围：1.6V 至 5.5V
- 低电源电流：490nA（典型值/通道）
- 低偏移电压：3mV（最大值/室温）
- 低 TcVos：1µV/°C（典型值）
- 增益带宽：8kHz（典型值）
- 轨到轨输入和输出
- 单位增益稳定
- 低输入偏置电流：1pA（最大值/室温）
- 强化的电磁干扰 (EMI) 保护
- 温度范围：-40℃ 至 125℃
- 3mm x 3mm x 0.45mm 薄型 X1SON 封装

2 应用

- 可穿戴产品
- 个人健康监视器
- 电池组
- 手机和平板电脑
- 太阳能或能量采集系统
- PIR、烟雾、燃气和火灾检测系统
- 电池供电物联网 (IoT) 设备
- 远程传感器
- 微功耗参考缓冲器

3 说明

LPV542 是一款超低功耗双路运算放大器，带宽 8kHz，静态电流 490nA，是电池供电应用的理想选择，如医疗和健身可穿戴设备、楼宇自动化和遥感节点。

每个放大器的 CMOS 输入级偏置电流仅为皮安级，可以减少光电二极管和充电感测应用等兆欧级反馈电阻拓扑中引入的常见误差。 此外，输入共模范围扩展到电源轨，输出摆幅扩展到电源轨的 ±3mV 范围内，从而保持了最宽的动态范围。 同样，LPV542 设有 EMI 保护，可降低来自手机、WiFi、无线电发射器和标签阅读器的无用射频信号对系统造成的影响。

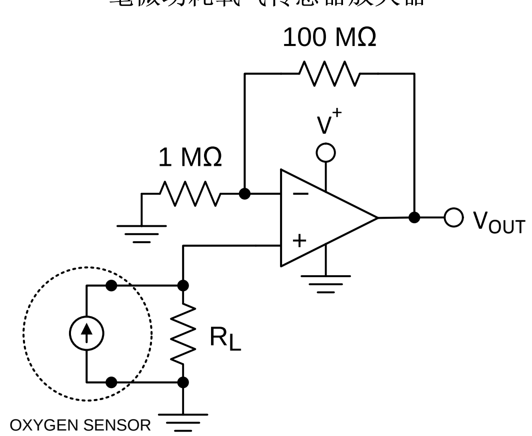
LPV542 可在 1.6V 的低电源电压下运行，确保在电池低电量的情况下保持出色性能。 该器件采用 8 焊盘 3mm x 3mm x 0.45mm 薄型无铅 X1SON 封装和标准 8 引脚 VSSOP 封装。

器件信息[(1)]

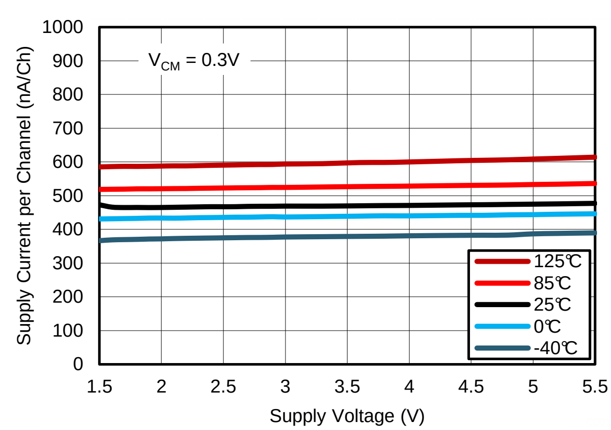
器件型号	封装	封装尺寸（标称值）
LPV542	X1SON (8)	3.00mm x 3.00mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

毫微功耗氧气传感器放大器



电源电流与 电源电压间的关系



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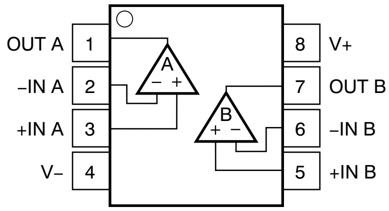
4 修订历史记录

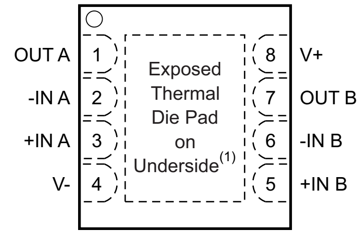
日期	修订版本	注释
2015 年 3 月	*	最初发布。

5 Pin Configuration and Functions

8-Pin VSSOP
DGK Package
Top View



8-Pad X1SON
DNX Package
Top View



(1) Connect thermal die pad to V-.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DGK	DNX		
OUT A	1	1	O	Channel A Output
-IN A	2	2	I	Channel A Inverting Input
+IN A	3	3	I	Channel A Non-Inverting Input
V-	4	4	P	Negative (lowest) power supply
+IN B	5	5	I	Channel B Non-Inverting Input
-IN B	6	6	I	Channel B Inverting Input
OUT B	7	7	O	Channel B Output
V+	8	8	P	Positive (highest) power supply
Die Pad	--	DAP	P	Die Attach Pad. Connect to V- (DNX package only)

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)(2)(3)]

		MIN	MAX	UNIT
Supply voltage, V+ to V–		-0.3	6	V
Signal input pins	Voltage[(2)]	(V-) - 0.3	(V+) + 0.3	V
	Current[(2)]	-10	10	mA
Output short current		Continuous[(4)]		
Junction temperature		-40	150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Short-circuit to V-.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

	MIN	NOM	MAX	UNIT
Supply Voltage ($V^+ – V^-$)	1.6		5.5	V
Specified Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		DGK (VSSOP) 8 PINS	DNX (X1SON) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance		46.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance		33.3	
$R_{θJB}$	Junction-to-board thermal resistance		21	
$ψ_{JT}$	Junction-to-top characterization parameter		0.2	
$ψ_{JB}$	Junction-to-board characterization parameter		21.2	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance		7	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics 1.8 V

T_A = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage (V_{OS})	V_{CM} = 0.3 V		±1	±2	mV
	V_{CM} = 1.5 V		±1	±3	
Over temperature	V_{CM} = 0.3 V and 1.5 V			±4	
Drift (dV_{OS}/dT)			1		µV/°C
Power-Supply Rejection Ratio (PSRR)	V_S = 1.6 V to 5.5 V, V_{CM} = 0.3 V	83	109		dB
INPUT VOLTAGE RANGE					
Common-mode voltage range (V_{CM})	CMRR ≥ 60 dB	0		1.8	V
Common-Mode Rejection Ratio (CMRR)	0 V < V_{CM} < 1.8 V	63	92		dB
	0 V < V_{CM} < 0.7 V	87	92		
	1.3 V < V_{CM} < 1.8 V	63	98		
INPUT BIAS CURRENT					
Input bias current (I_B)	T_A = 25°C		±0.1	±1	pA
	T_A = –40°C to 125°C			±100	
Input offset current (I_{OS})			±0.1	±1	
INPUT IMPEDANCE					
Differential			10^{13} || 2.5		Ω || pF
Common mode			10^{13} || 2.5		
NOISE					
Input voltage noise density, f = 1 kHz (e_n)			250		nV/√Hz
Current noise density, f = 1 kHz (i_n)			80		fA√Hz
OPEN-LOOP GAIN					
Open-loop voltage gain (A_{OL})	R_L = 100 kΩ to V^+/2, 0.5 V < V_O < 1.3 V	91	101		dB
OUTPUT					
Voltage output swing from positive rail	R_L = 100 kΩ to V^+/2		3	20	mV
Voltage output swing from negative rail	R_L = 100 kΩ to V^+/2		2	20	
Output current sourcing	Sourcing, V_O to V^-, V_{IN}(diff) = 100 mV	1	3		mA
Output current sinking	Sinking, V_O to V^+, V_{IN}(diff) = –100 mV	1	5		
FREQUENCY RESPONSE					
Gain-bandwidth product (GBWP)	C_L = 20 pF		7		kHz
Slew rate (SR)	G = +1, Rising edge, $1V_{p-p}$, C_L = 20 pF		3.4		V/ms
	G = +1, Falling edge, $1V_{p-p}$, C_L = 20 pF		3.7		
POWER SUPPLY					
Specified voltage range (V_S)		1.6		5.5	V
Quiescent current per channel (I_Q)	V_{CM} = 0.3 V, I_O = 0		490	800	nA
Over temperature				1100	
Quiescent current per channel (I_Q)	V_{CM} = 1.5 V, I_O = 0		680	1100	
Over temperature				1500	

(1) Refer to *Typical Characteristics*.

6.6 Electrical Characteristics 3.3 V

T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage (V_{OS})	V_{CM} = 0.3		±1	±2	
	V_{CM} = 3 V		±1	±3	mV
Over temperature	V_{CM} = 0.3 V and 3 V			±4	
Drift (dV_{OS}/dT)			1		µV/°C
Power-Supply Rejection Ratio (PSRR)	V_S = 1.6 V to 5.5 V, V_{CM} = 0.3 V	83	109		dB
INPUT VOLTAGE RANGE					
Common-mode voltage range (V_{CM})	CMRR ≥ 60 dB	0		3.3	V
Common-Mode Rejection Ratio (CMRR)	0 V < V_{CM} < 3.3 V	64	98		
	0 V < V_{CM} < 2.2V	88	98		dB
	2.7 V < V_{CM} < 3.3 V	64	105		
INPUT BIAS CURRENT					
Input bias current (I_B)	T_A = 25°C		±0.1	±1	
	T_A = –40°C to 125°C			±100	pA
Input offset current (I_{OS})			±0.1	±1	
INPUT IMPEDANCE					
Differential			10^{13} || 2.5		Ω || pF
Common mode			10^{13} || 2.5		
NOISE					
Input voltage noise density, f = 1 kHz (e_n)			250		nV/√Hz
Current noise density, f = 1 kHz (i_n)			60		fA√Hz
OPEN-LOOP GAIN					
Open-loop voltage gain (A_{OL})	R_L = 100 kΩ to V^+/2, 0.5 V < V_O < 2.8 V	91	101		dB
OUTPUT					
Voltage output swing from positive Rail	R_L = 100 kΩ to V^+/2		3	20	mV
Voltage output swing from negative Rail	R_L = 100 kΩ to V^+/2		2	20	
Output current sourcing	Sourcing, V_O to V^-, V_{IN}(diff) = 100 mV	5	14		mA
Output current sinking	Sinking, V_O to V^+, V_{IN}(diff) = –100 mV	5	19		
FREQUENCY RESPONSE					
Gain-bandwidth product (GBWP)	C_L = 20 pF		8		kHz
Slew rate (SR)	G = +1, Rising edge, 1V_{p-p}, C_L = 20 pF		3.6		V/ms
	G = +1, Falling edge, 1V_{p-p}, C_L = 20 pF		3.7		
POWER SUPPLY					
Specified voltage range (V_S)		1.6		5.5	V
Quiescent current per channel (I_Q)	V_{CM} = 0.3 V, I_O = 0		480	800	
Over temperature				1200	
Quiescent current per channel (I_Q)	V_{CM} = 3 V, I_O = 0		650	1100	nA
Over temperature				1500	

(1) Refer to *Typical Characteristics*.

6.7 Electrical Characteristics 5 V

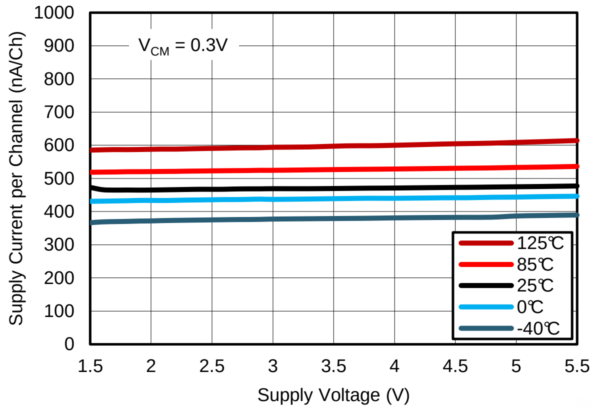
T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage (V_{OS})	V_{CM} = 0.3 V		±1	±2	mV
	V_{CM} = 4.7V		±1	±3	
Over temperature	V_{CM} = 0.3 V and 4.7V			±4	
Drift (dV_{OS}/dT)			1		µV/°C
Power-Supply Rejection Ratio (PSRR)	V_S = 1.6 V to 5.5 V, V_{CM} = 0.3 V	83	109		dB
INPUT VOLTAGE RANGE					
Common-Mode voltage range (V_{CM})	CMRR ≥ 60 dB	0		5	V
Common-Mode Rejection Ratio (CMRR)	0 V < V_{CM} < 5 V	73	101		dB
	0 V < V_{CM} < 3.9V	88	101		
	4.4 V < V_{CM} < 5 V	73	109		
INPUT BIAS CURRENT					
Input bias current (I_B)	T_A = 25°C		±0.1	±1	pA
	T_A = –40°C to 125°C			±100	
Input offset current (I_{OS})			±0.1	±1	
INPUT IMPEDANCE					
Differential			10^{13} || 2.5		Ω || pF
Common mode			10^{13} || 2.5		
NOISE					
Input voltage noise density, f = 1 kHz (e_n)			250		nV/√Hz
Current noise density, f = 1 kHz (i_n)			65		fA√Hz
OPEN-LOOP GAIN					
Open-loop voltage gain (A_{OL})	R_L = 100 kΩ to V^+/2, 0.5 V < V_O < 4.5 V	91	101		dB
OUTPUT					
Voltage output swing from positive rail	R_L = 100 kΩ to V^+/2		3	20	mV
Voltage output swing from negative rail	R_L = 100 kΩ to V^+/2		2	20	
Output current sourcing	Sourcing, V_O to V^-, V_{IN}(diff) = 100 mV	10	30		mA
Output current sinking	Sinking, V_O to V^+, V_{IN}(diff) = –100 mV	10	36		
FREQUENCY RESPONSE					
Gain-bandwidth product (GBWP)	C_L = 20 pF		8		kHz
Slew rate (SR)	G = +1, Rising edge, 1V_{p-p}, C_L = 20 pF		3.6		V/ms
	G = +1, Falling edge, 1V_{p-p}, C_L = 20 pF		3.7		
POWER SUPPLY					
Specified voltage range (V_S)		1.6		5.5	V
Quiescent current per channel (I_Q)	V_{CM} = 0.3 V, I_O = 0		480	850	nA
Over temperature				1300	
Quiescent current per channel (I_Q)	V_{CM} = 4.7 V, I_O = 0		680	1100	
Over temperature				1600	

(1) Refer to *Typical Characteristics*.

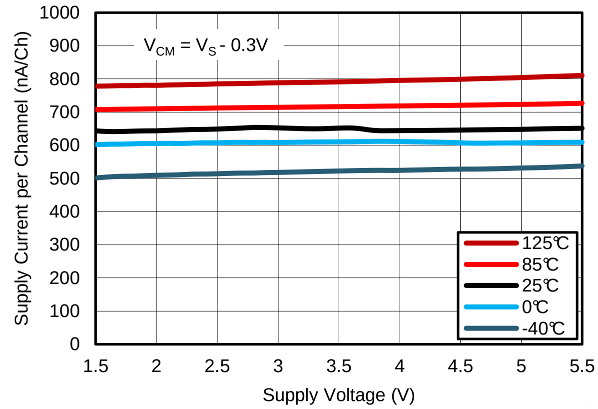
6.8 Typical Characteristics

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



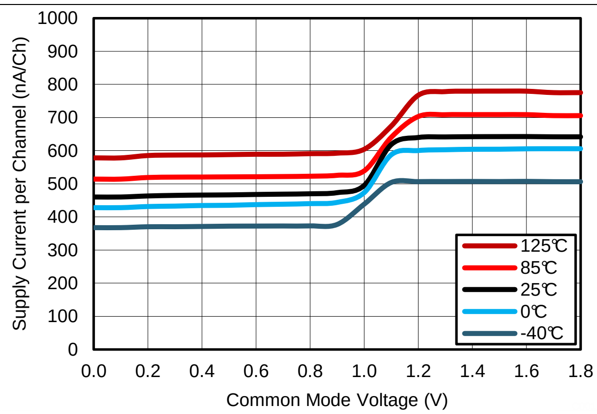
No Output Load V_{CM} = 0.3 V

Figure 1. Supply Voltage vs Supply Current per Channel, Low Vcm



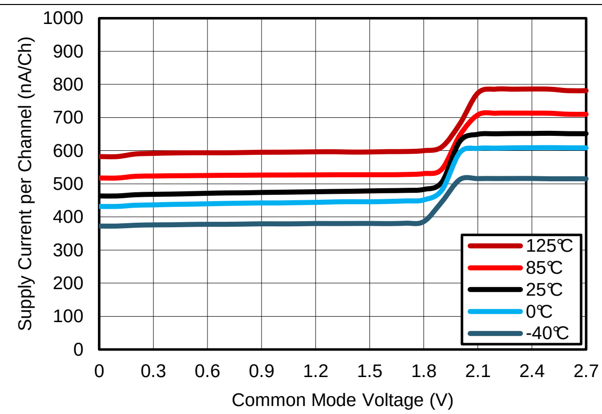
No Output Load V_{CM} = (V+) – 0.3 V

Figure 2. Supply Voltage vs Supply Current per Channel, High Vcm



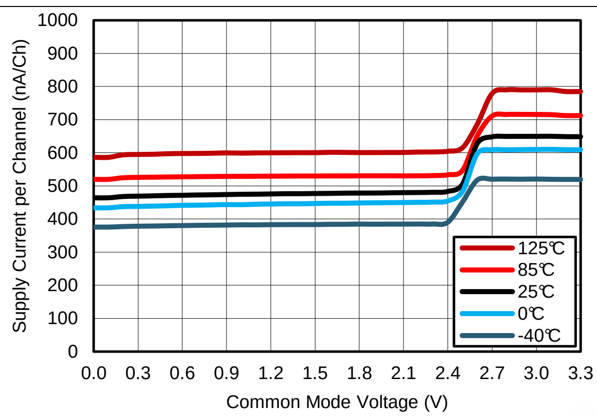
No Output Load

Figure 3. Supply Current vs Common Mode at 1.8 V



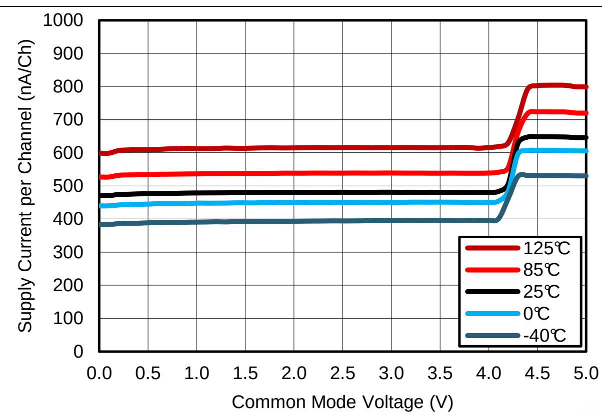
No Output Load

Figure 4. Supply Current vs Common Mode at 2.7 V



No Output Load

Figure 5. Supply Current vs Common Mode at 3.3 V



No Output Load

Figure 6. Supply Current vs Common Mode at 5 V

Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = $V_S/2$, R_{LOAD} = 1 MΩ connected to $V_S/2$, and C_L = 20 pF, unless otherwise noted.

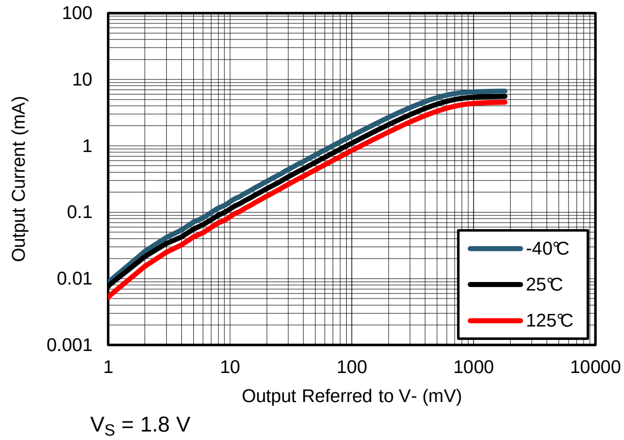


Figure 7. Output Sinking Current vs Output Swing at 1.8 V

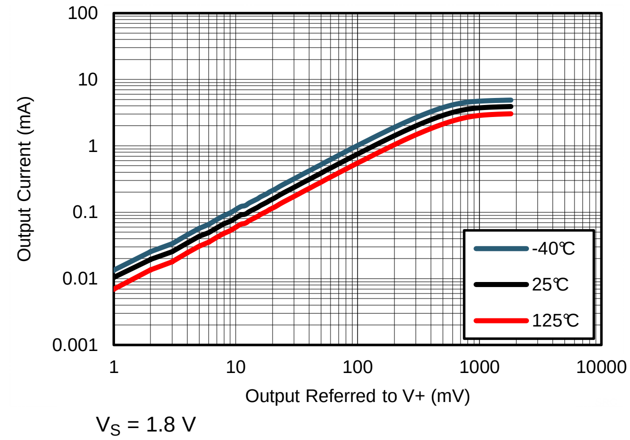


Figure 8. Output Sourcing Current vs Output Swing at 1.8 V

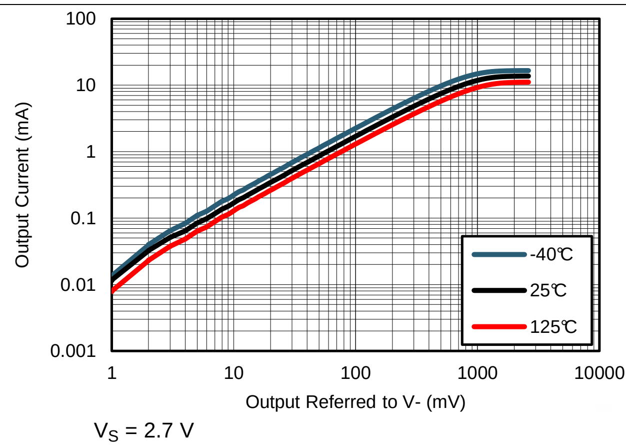


Figure 9. Output Sinking Current vs Output Swing at 2.7 V

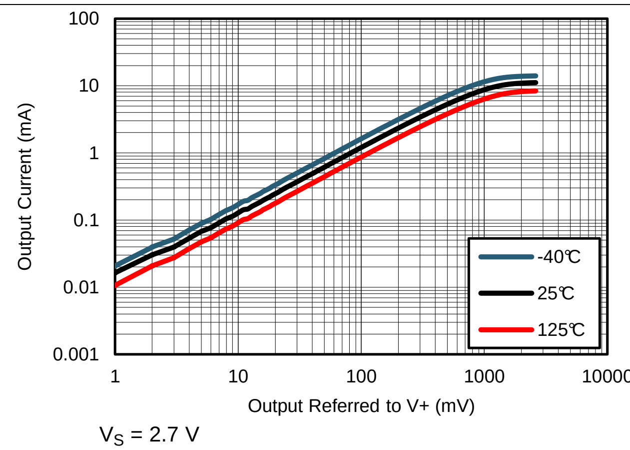


Figure 10. Output Sourcing Current vs Output Swing at 2.7 V

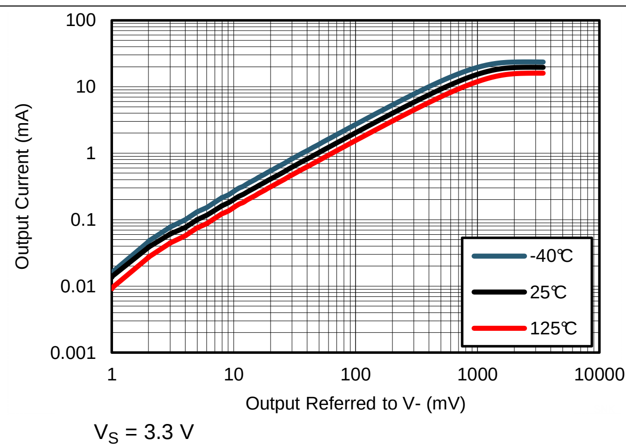


Figure 11. Output Sinking Current vs Output Swing at 3.3 V

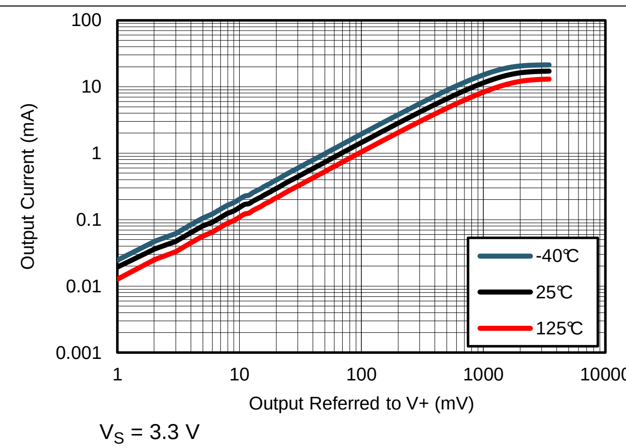
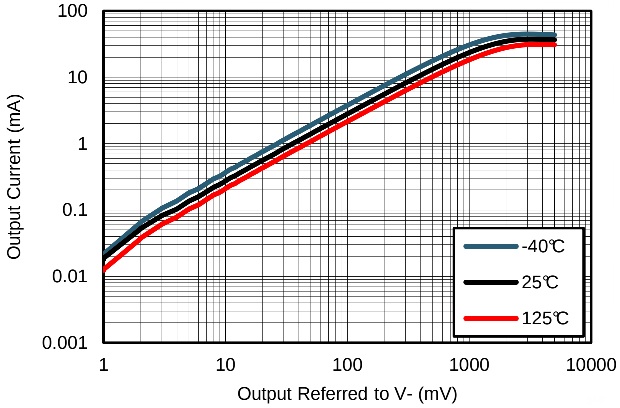


Figure 12. Output Sourcing Current vs Output Swing at 3.3 V

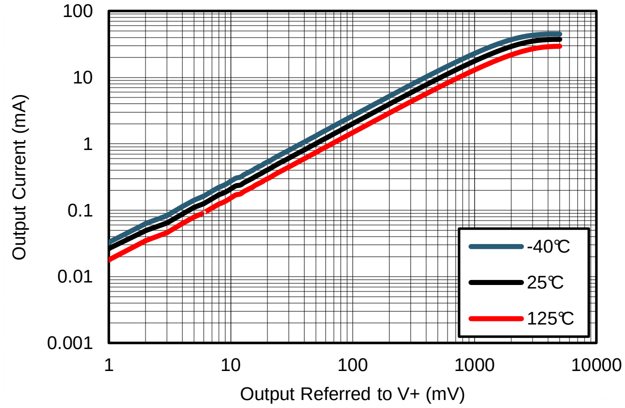
Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



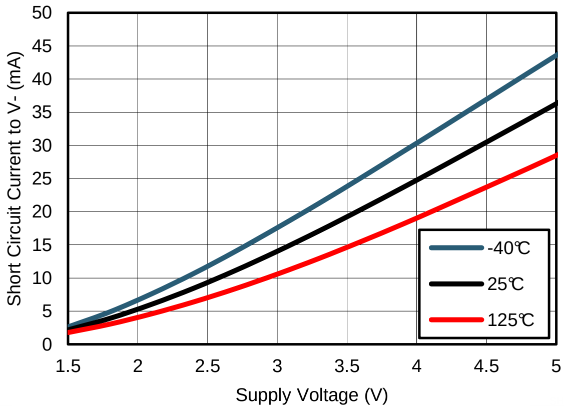
V_S = 5 V

Figure 13. Output Sinking Current vs Output Swing at 5 V



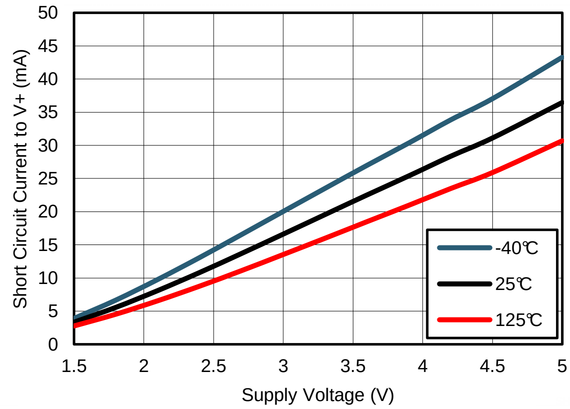
V_S = 5 V

Figure 14. Output Sourcing Current vs Output Swing at 5 V



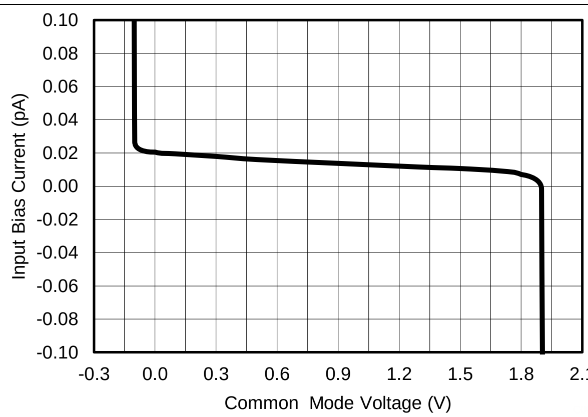
Output set high (sourcing), shorted to V–

Figure 15. Output Short Circuit Current to V- vs Supply Voltage



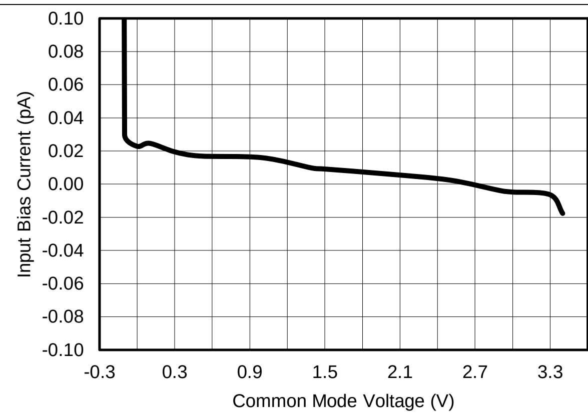
Ouput set low (sinking), shorted to V+

Figure 16. Output Short Circuit Current to V+ vs Supply Voltage



V_S = 1.8 V T_A = 25°C

Figure 17. Input Bias Current vs Common Mode Voltage at 1.8 V



V_S = 3.3 V T_A = 25°C

Figure 18. Input Bias Current vs Common Mode Voltage at 3.3V

Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.

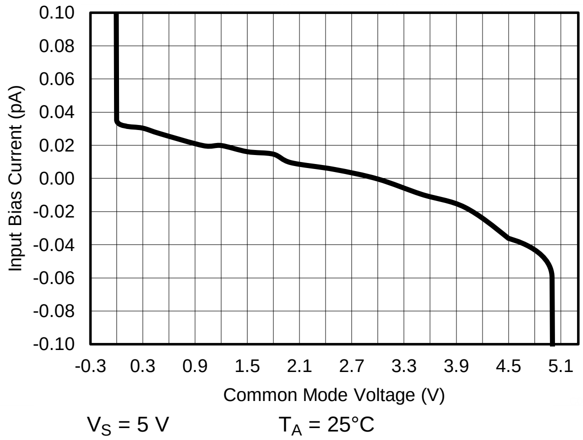


Figure 19. Input Bias Current vs Common Mode Voltage at 5V

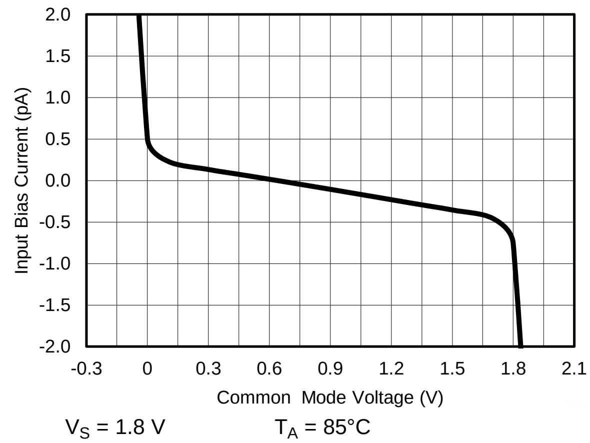


Figure 20. Input Bias Current vs Common Mode Voltage at 1.8V

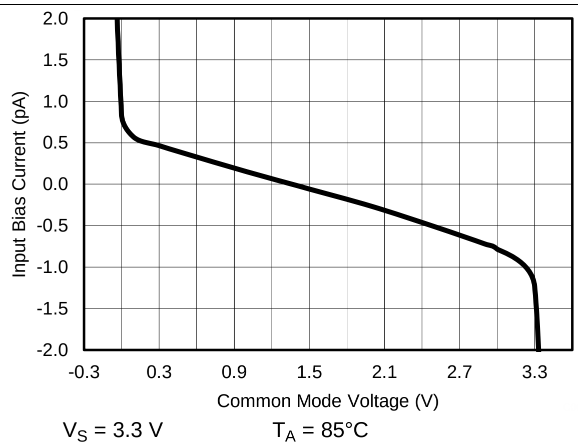


Figure 21. Input Bias Current vs Common Mode Voltage at 3.3 V

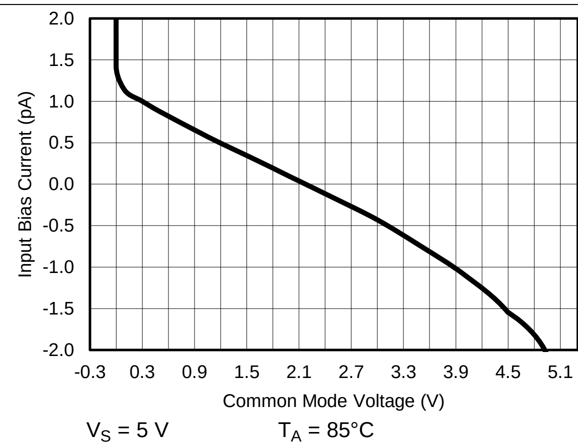


Figure 22. Input Bias Current vs Common Mode Voltage at 5 V

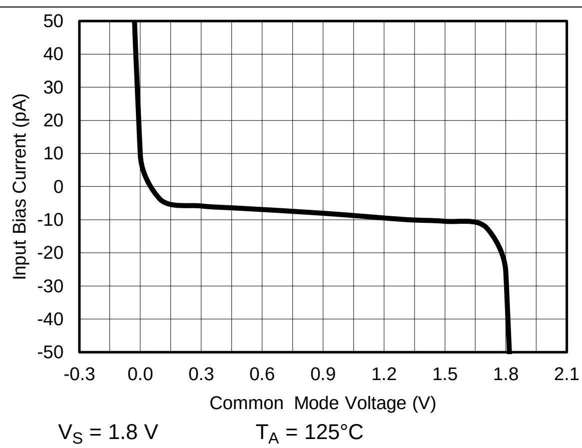


Figure 23. Input Bias Current vs Common Mode Voltage at 1.8 V

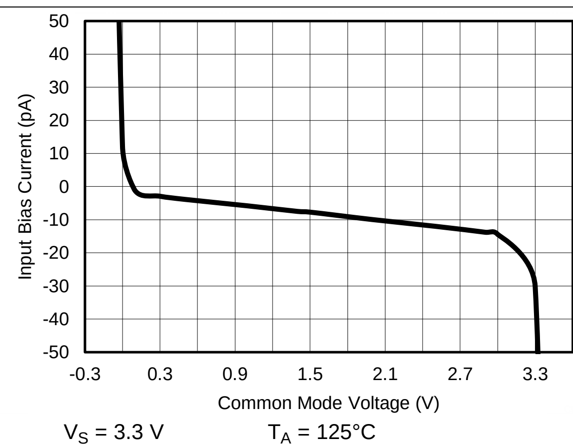
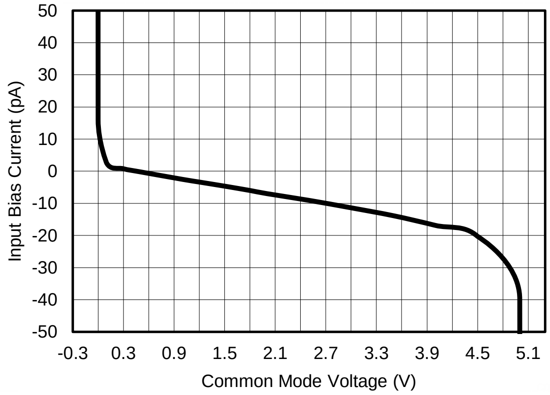


Figure 24. Input Bias Current vs Common Mode Voltage at 3.3 V

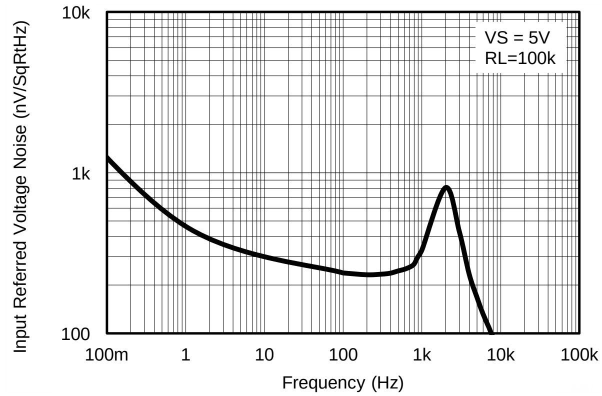
Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



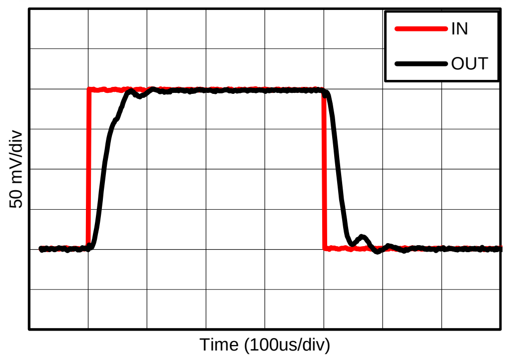
V_S = 5 V T_A = 125°C C_L = 20 pF

Figure 25. Input Bias Current vs Common Mode Voltage at 5 V



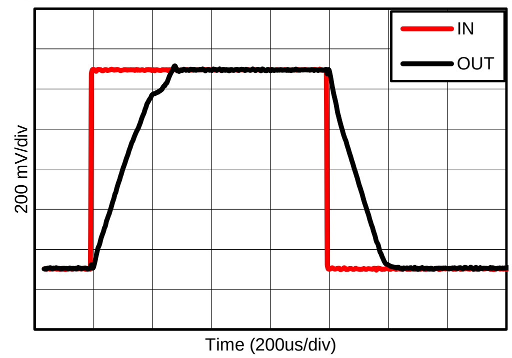
V_S = 5 V R_L = 100 kΩ C_L = 20 pF

Figure 26. Input Referred Voltage Noise



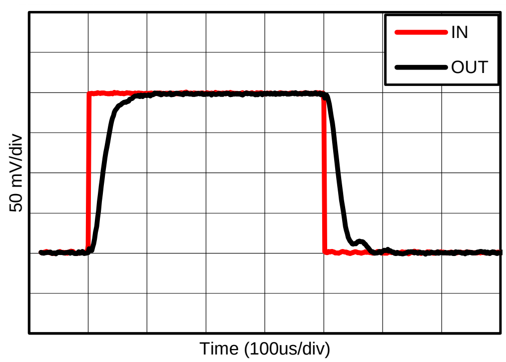
V_S = ±0.9 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±100 mV

Figure 27. Pulse Response, 200mVpp at 1.8 V



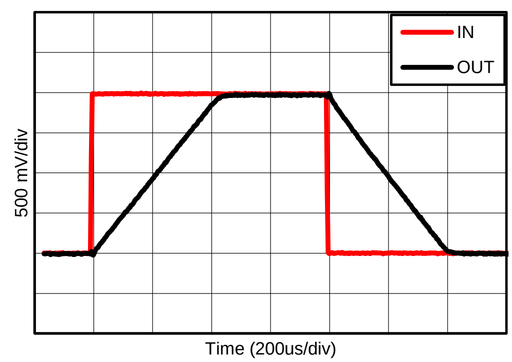
V_S = ±0.9 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±500mV

Figure 28. Pulse Response, 1Vpp at 1.8V



V_S = ±2.5 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±100 mV

Figure 29. Pulse Response, 200mVpp at 5V

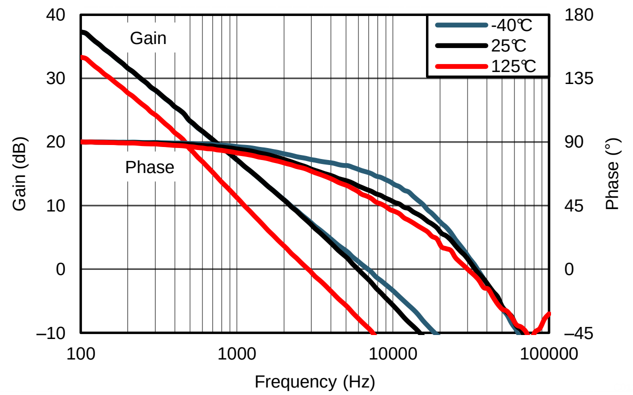


V_S = ±2.5 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±1V

Figure 30. Pulse Response, 2Vpp at 5V

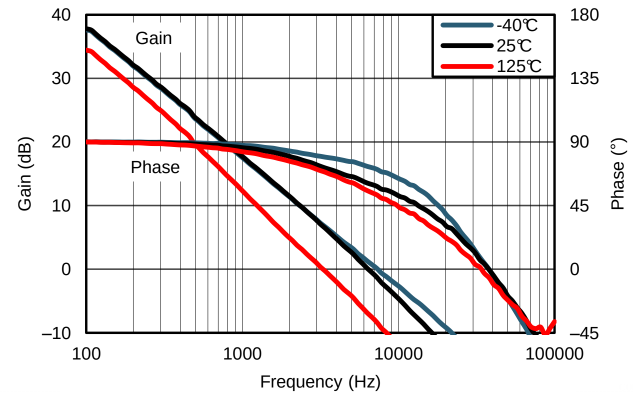
Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



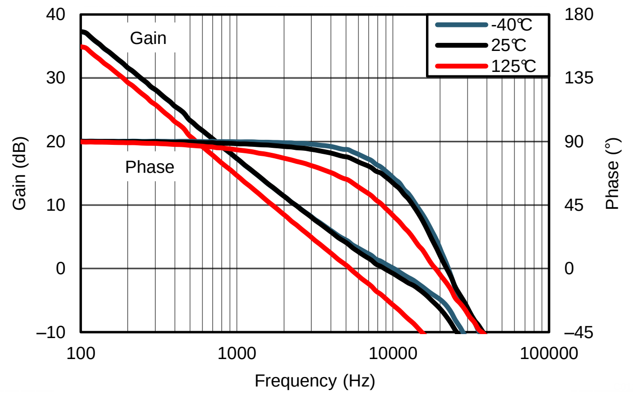
V_S = 1.8 V R_L = 100 kΩ C_L = 20 pF

Figure 31. Gain and Phase vs Temperature at 1.8 V



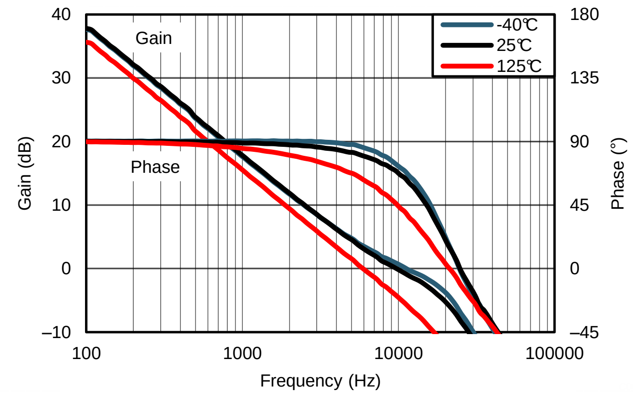
V_S = 5 V R_L = 100 kΩ C_L = 20 pF

Figure 32. Gain and Phase vs Temperature at 5 V



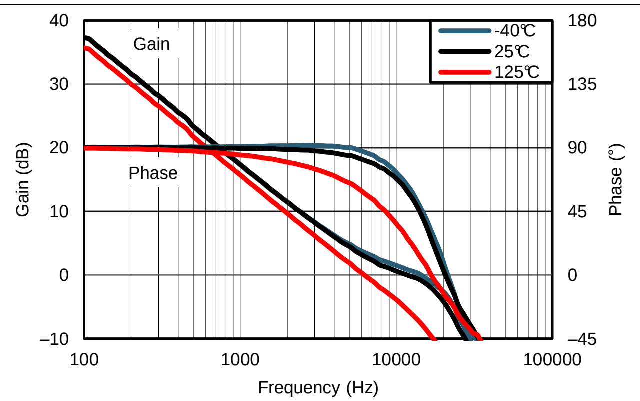
V_S = 1.8 V R_L = 1 MΩ C_L = 20 pF

Figure 33. Gain and Phase vs Temperature at 1.8 V



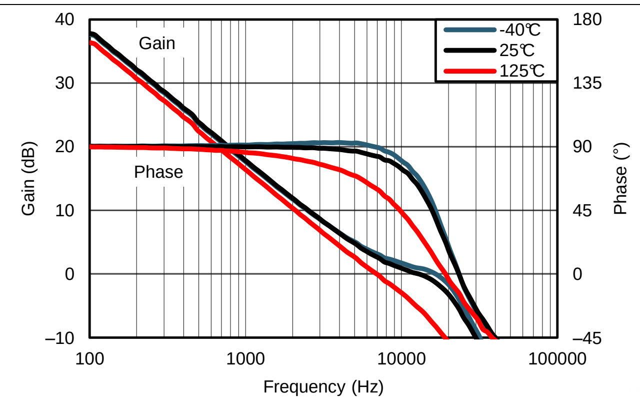
V_S = 5 V R_L = 1 MΩ C_L = 20 pF

Figure 34. Gain and Phase vs Temperature at 5 V



V_S = 1.8 V R_L = 10 MΩ C_L = 20 pF

Figure 35. Gain and Phase vs Temperature at 1.8 V



V_S = 5 V R_L = 10 MΩ C_L = 20 pF

Figure 36. Gain and Phase vs Temperature at 5 V

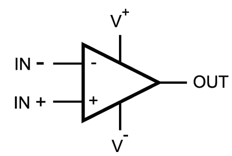
7 Detailed Description

7.1 Overview

The LPV542 dual op amplifier is unity-gain stable and can operate on a single supply, making it highly versatile and easy to use.

The LPV542 is fully specified and tested from 1.6 V to 5.5 V. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

7.2 Functional Block Diagram



7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ – IN^-) \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 100,000 Volts per microvolt).

7.4 Device Functional Modes

7.4.1 Rail-To-Rail Input

The input common-mode voltage range of the LPV542 extends to the supply rails. This is achieved with a complementary input stage — an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 800 mV to 200 mV above the positive supply, while the P-channel pair is on for inputs from 300 mV below the negative supply to approximately (V+) – 800 mV. There is a small transition region, typically (V+) – 1.2 V to (V+) – 0.8 V, in which both pairs are on. This 400 mV transition region can vary 200 mV with process variation. Within the 400 mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

7.4.2 Supply Current Changes over Common Mode

Because of the ultra-low supply current, changes in common mode voltages will cause a noticeable change in the supply current as the input stages transition through the transition region, as shown in Figure 37 below.

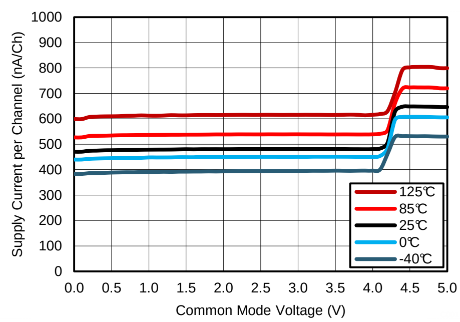


Figure 37. Supply Current Change over Common Mode at 5 V

Device Functional Modes (continued)

For the lowest supply current operation, keep the input common mode range between V- and 1 V below V+.

7.4.3 Design Optimization With Rail-To-Rail Input

In most applications, operation is within the range of only one differential pair. However, some applications can subject the amplifier to a common-mode signal in the transition region. Under this condition, the inherent mismatch between the two differential pairs may lead to degradation of the CMRR and THD. The unity-gain buffer configuration is the most problematic as it will traverse through the transition region if a sufficiently wide input swing is required.

7.4.4 Design Optimization for Nanopower Operation

When designing for ultralow power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electolytics may have static leakage currents in the tens to hundreds of nanoamps.

7.4.5 Common-Mode Rejection

The CMRR for the LPV542 is specified in two ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 0.9 V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at V_S = 5 V over the entire common-mode range is specified.

7.4.6 Output Stage

The LPV542 output voltage swings 3 mV from rails at 3.3 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV542 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load.

7.4.7 Driving Capacitive Load

The LPV542 is internally compensated for stable unity gain operation, with a 8 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (>50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 38. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

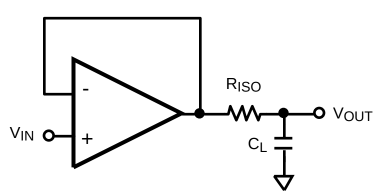


Figure 38. Resistive Isolation Of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV542 is a ultra-low power operational amplifier that provides 8 kHz bandwidth with only 490nA quiescent current, and near precision offset and drift specifications at a low cost. These rail-to-rail input and output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the power-supply rails and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

8.2 Typical Application: 60 Hz Twin "T" Notch Filter

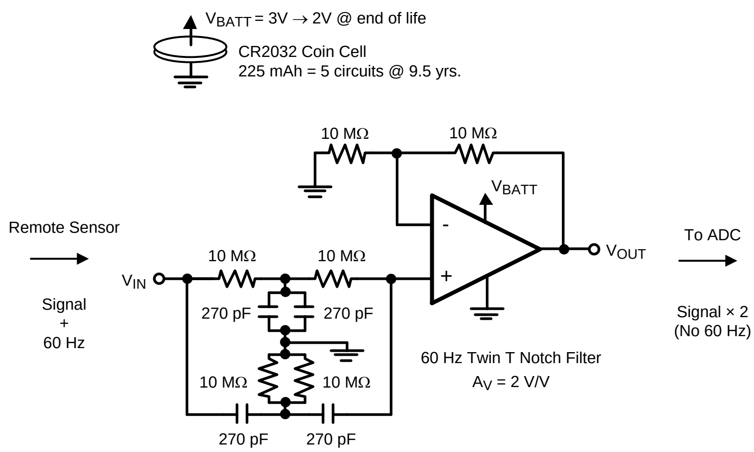


Figure 39. 60 Hz Notch Filter

8.2.1 Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60 Hz interference from AC power lines. The circuit of Figure 39 notches out the 60 Hz and provides a gain A_V = 2 for the sensor signal represented by a 1 kHz sine wave. Similar stages may be cascaded to remove 2nd and 3rd harmonics of 60 Hz. Thanks to the nA power consumption of the LPV542, even 5 such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3 V and an end of life voltage of 2 V. With an operating voltage from 1.6 V to 5.5 V the LPV542 can function over this voltage range.

8.2.2 Detailed Design Procedure

The notch frequency is set by:

$$F_0 = 1 / 2\pi RC. \quad (2)$$

To achieve a 60 Hz notch use R = 10 MΩ and C = 270 pF. If eliminating 50 Hz noise, which is common in European systems, use R = 11.8 MΩ and C = 270 pF.

The Twin T Notch Filter works by having two separate paths from V_{IN} to the amplifier's input. A low frequency path through the series input resistors and another separate high frequency path through the series input capacitors. However, at frequencies around the notch frequency, the two paths have opposing phase angles and the two signals will tend to cancel at the amplifier's input.

Typical Application: 60 Hz Twin "T" Notch Filter (continued)

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter needs to be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected clean board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in Figure 39 can be done over a bandwidth of 2 kHz, which takes the conservative approach of overestimating the bandwidth (LPV542 typical GBW/A_V is lower). The total noise at the output is approximately 800 µVpp, which is excellent considering the total consumption of the circuit is only 900 nA. The dominant noise terms are op amp voltage noise , current noise through the feedback network (430 µVpp), and current noise through the notch filter network (280 µVpp). Thus the total circuit's noise is below 1/2 LSB of a 10-bit system with a 2 V reference, which is 1 mV.

8.2.3 Application Curve

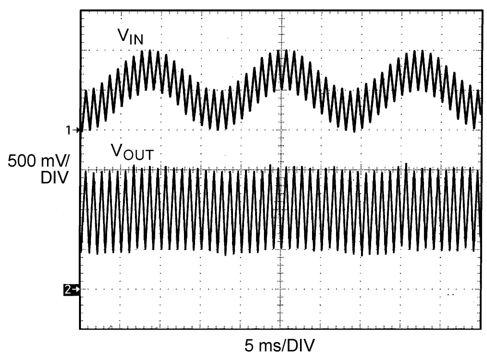


Figure 40. 60 Hz Notch Filter Waveform

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 KΩ per volt).

9 Power Supply Recommendations

The LPV542 is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

For proper operation, the power supplies bust be properly decoupled. For decoupling the supply lines it is suggested that 10 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and $V^–$ supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between $V^–$ and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize strays.

There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the V- pin. For best performance the DAP should be connected to the exact same potential as the V- pin. Do not use the DAP as the primary V- supply. Floating the DAP pad is not recommended. The DAP and V- pin should be joined directly as shown in the *Layout Example*.

10.2 Layout Example

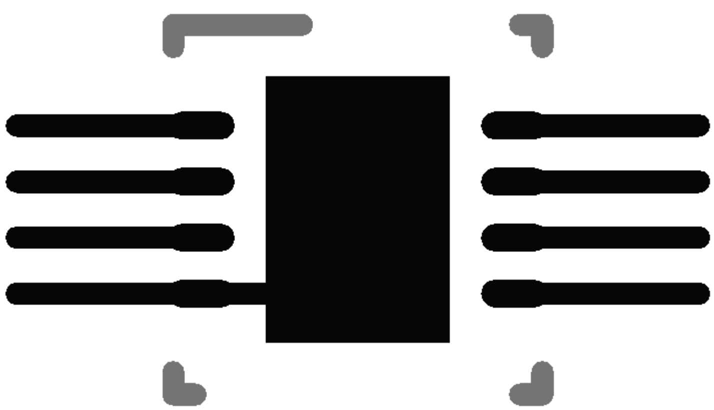


Figure 41. X1SON Layout Example (top view)

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

TINA-TI 基于 SPICE 的模拟仿真程序，http://www.ti.com.cn/tool/cn/tina-ti

DIP 适配器评估模块，http://www.ti.com.cn/tool/cn/dip-adapter-evm

TI 通用运行放大器评估模块，http://www.ti.com.cn/tool/cn/opampevm

TI FilterPro 滤波器设计软件，http://www.ti.com.cn/tool/cn/filterpro

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- AN-1798《设计电化学传感器》，SNOA514
- AN-1803《互阻抗放大器设计注意事项》，SNOA515
- AN-1852《设计 pH 电极》，SNOA529
- 《直观补偿互阻抗放大器》，SBOA055
- 《高速运算放大器互阻抗注意事项》，SBOA112
- 《FET 互阻抗放大器噪声分析》，SBOA060
- 《电路板布局布线技巧》，SLOA089
- 《运算放大器应用手册》，SBOA092

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LPV542DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(LP, V542)
LPV542DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LP, V542)
LPV542DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(LP, V542)
LPV542DGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LP, V542)
LPV542DNXR	Active	Production	X1SON (DNX) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV542
LPV542DNXR.B	Active	Production	X1SON (DNX) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV542
LPV542DNXT	Active	Production	X1SON (DNX) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV542
LPV542DNXT.B	Active	Production	X1SON (DNX) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV542

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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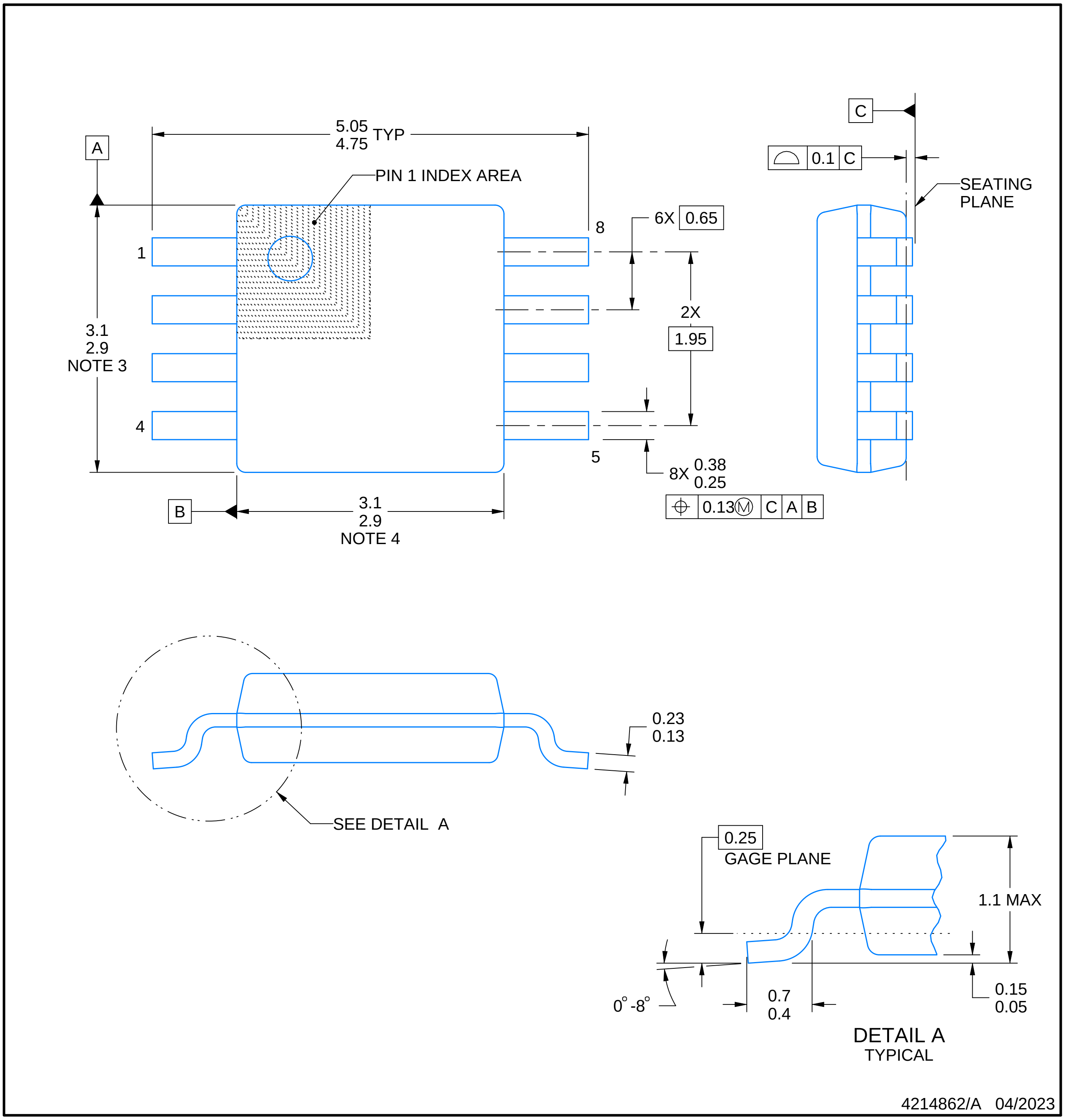
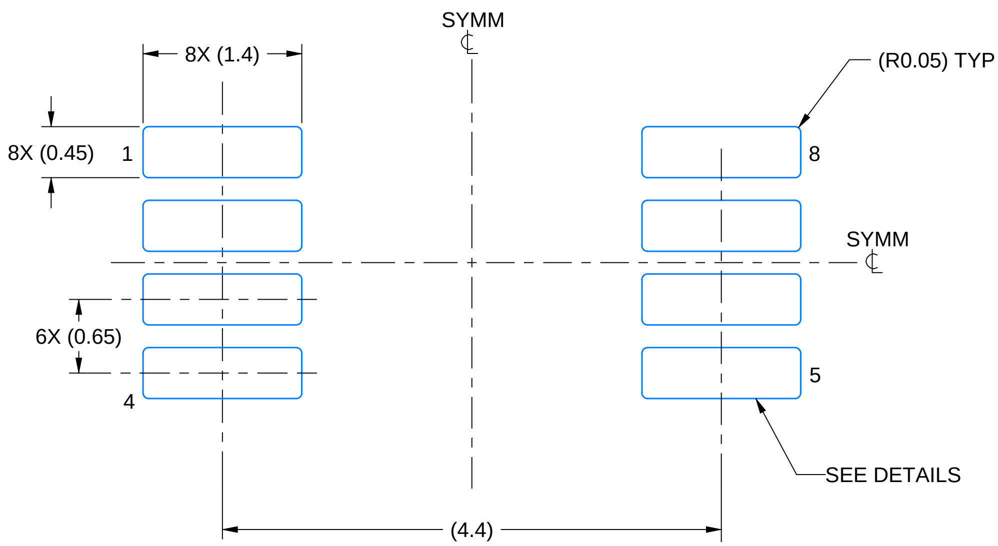
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



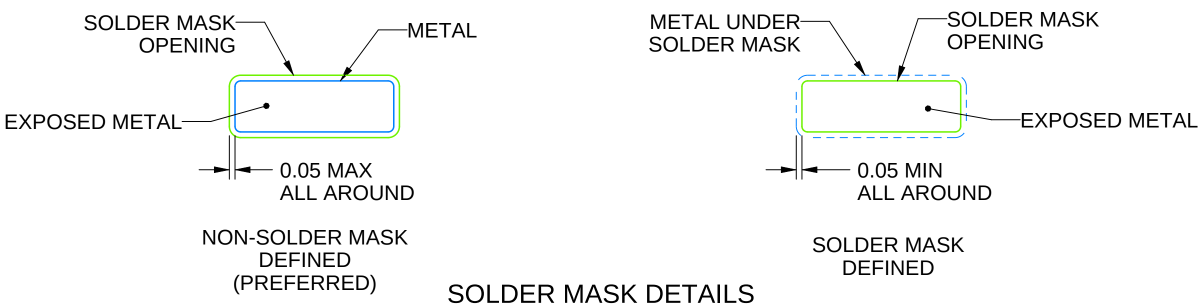
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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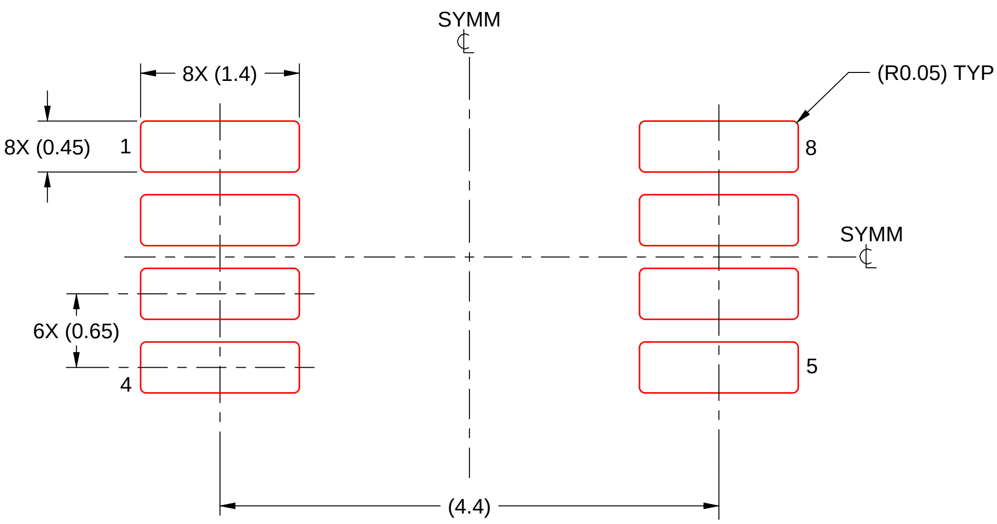
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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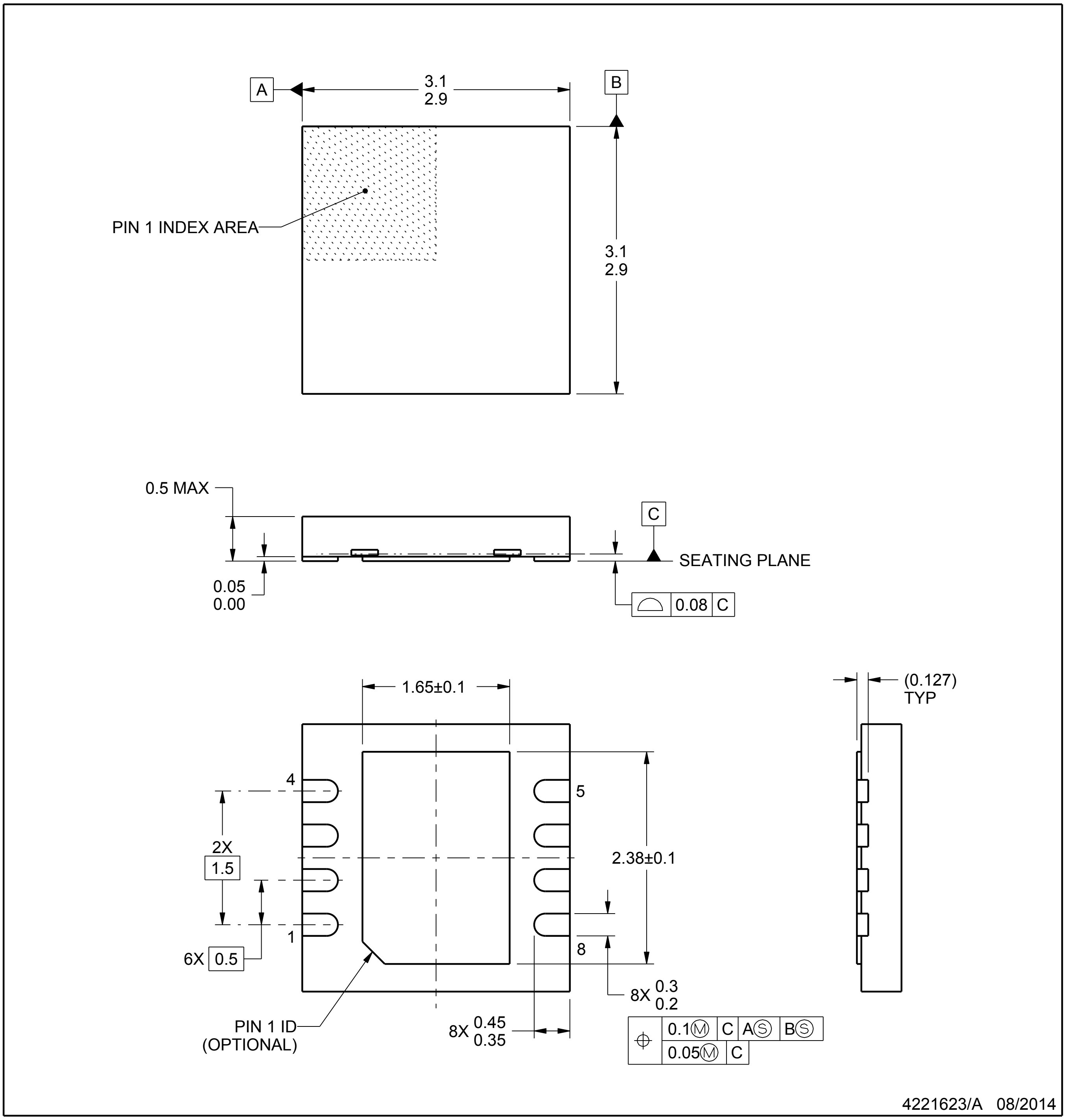
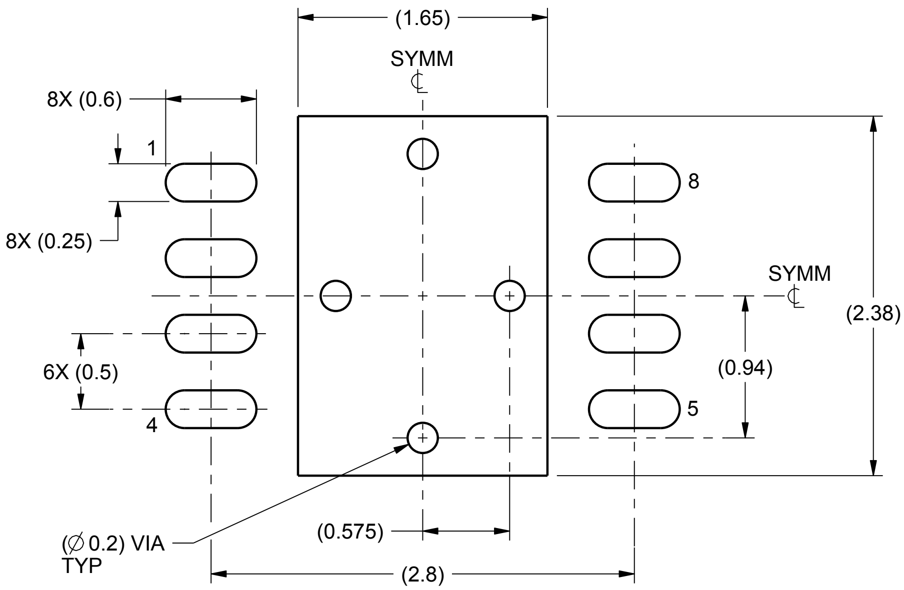
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

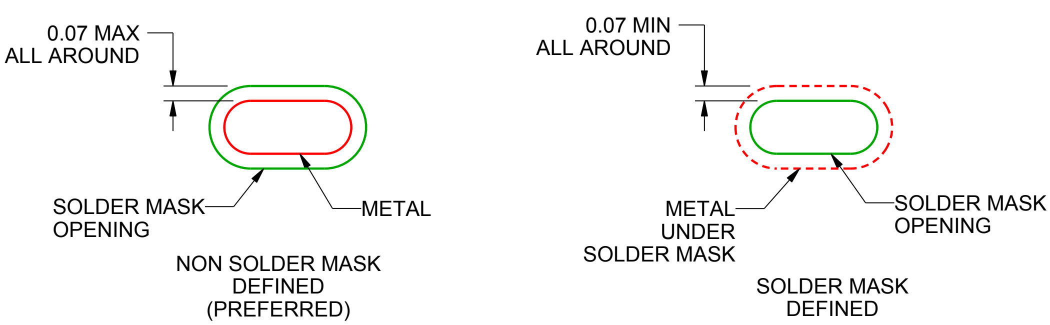


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

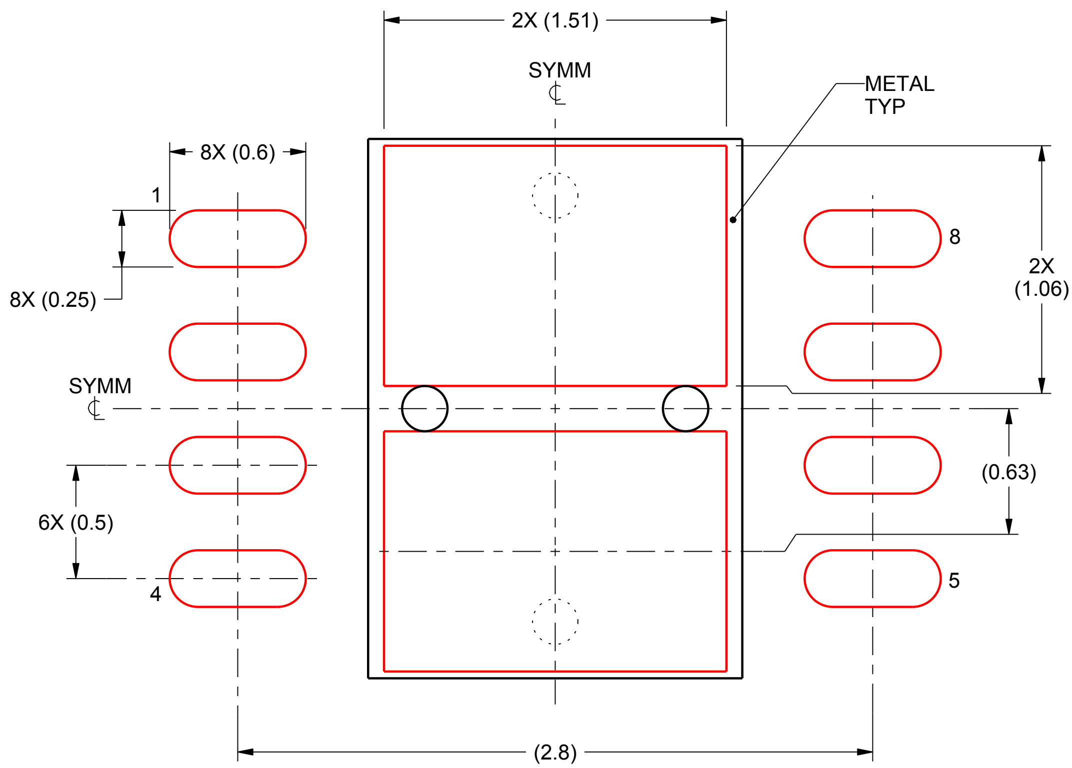


SOLDER MASK DETAILS

4221623/A 08/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4221623/A 08/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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