MAX211 具有 ±15kV ESD 保护的 5V 多通道 RS-232 线路驱动器和接收器

1 特性

- 使用人体放电模型 (HBM) 时，RS-232 总线引脚 ESD 保护大于 ±15kV
- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 由 5V V_{CC} 电源供电
- 四个驱动器和五个接收器
- 速率高达 120kbit/s
- 关断模式下的低电源电流：5μA（典型值）
- 外部电容器：4 × 0.1μF
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 电池供电型系统
- PDA
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

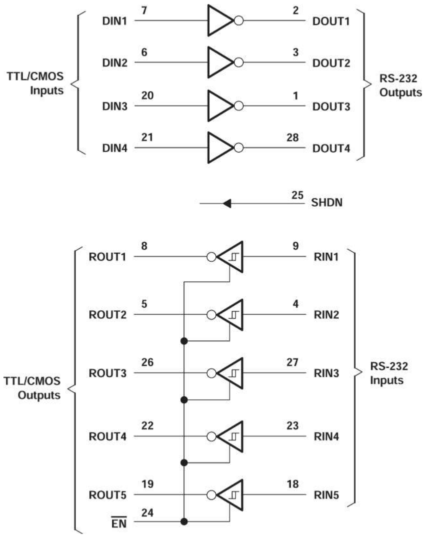
MAX211 器件由四个线路驱动器、五个线路接收器和一个双电荷泵电路组成，具有引脚对引脚（串行端口连接引脚，包括 GND）±15kV ESD 保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由单个 5V 电源供电。这些器件以高达 120kbit/s 的数据信号传输速率和最高 30V/μs 的驱动器输出压摆率运行。

MAX211 具有关断 (SHDN) 和使能控制 ($\overline{EN}$) 功能。在关断模式下，电荷泵会关闭，V+ 会下拉至 V_{CC}、V– 会下拉至 GND，且发送器输出被禁用。这通常会将电源电流降低至 1μA。$\overline{EN}$ 用于将接收器输出置于高阻抗状态，从而实现两个 RS-232 端口的有线 OR 连接。这对 RS-232 驱动器或电荷泵没有影响。

封装信息

器件型号	封装[1]	封装尺寸[2]
MAX211	DB（SSOP，28）	10.2mm × 7.8mm
	DW（SOIC，28）	17.9mm × 10.3mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

Table of Contents

4 Pin Configuration and Functions

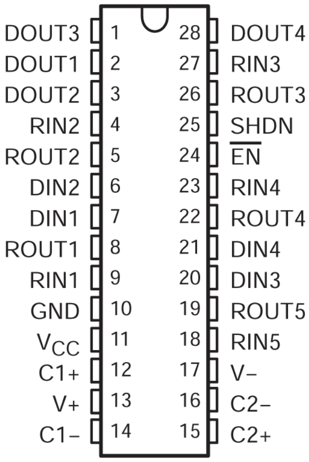


图 4-1. DB or DW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	DB or DW		
DOUT3	1	O	RS232 line data output (to remote RS232 system)
DOUT1	2	O	RS232 line data output (to remote RS232 system)
DOUT2	3	O	RS232 line data output (to remote RS232 system)
RIN2	4	I	RS232 line data input (from remote RS232 system)
ROUT2	5	O	Logic data output (to UART)
DIN2	6	I	Logic data input (from UART)
DIN1	7	I	Logic data input (from UART)
ROUT1	8	O	Logic data output (to UART)
RIN1	9	I	RS232 line data input (from remote RS232 system)
GND	10	-	Ground
V_{CC}	11	--	Supply Voltage, Connect to external 3V to 5.5V power supply
C1+	12	--	Positive lead of C1 capacitor
V+	13	O	Positive charge pump output for storage capacitor only
C1-	14	--	Negative lead of C1 capacitor
C2+	15	--	Positive lead of C2 capacitor
C2-	16	--	Negative lead of C2 capacitor
V-	17	O	Negative charge pump output for storage capacitor only
RIN5	18	I	RS232 line data input (from remote RS232 system)
ROUT5	19	O	Logic data output (to UART)
DIN3	20	I	Logic data input (from UART)
DIN4	21	I	Logic data input (from UART)
ROUT4	22	O	Logic data output (to UART)
RIN4	23	I	RS232 line data input (from remote RS232 system)
$\overline{EN}$	24	--	Active low enable
SHDN	25	--	Active high shutdown
ROUT3	26	O	Logic data output (to UART)
RIN3	27	I	RS232 line data input (from remote RS232 system)
DOUT4	28	O	RS232 line data output (to remote RS232 system)

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表 4-1. Pin Functions（续）

PIN		TYPE[1]	DESCRIPTION
NAME	**DB or DW**		
Thermal Pad	-	--	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (2)	Supply voltage range		−0.3	6	V
V+ (2)	Positive charge pump voltage range		V_{CC} − 0.3	14	V
V− (2)	Negative charge pump voltage range		0.3	−14	V
V_I	Input voltage range	Drivers	−0.3	V+ + 0.3	V
		Receivers (DW package)		±30	V
		Receivers (DB package)		±25	V
V_O	Output voltage range	Drivers	V− − 0.3V	V+ + 0.3	V
		Receivers	−0.3	V_{CC} + 0.3	V
	Short-circuit duration	DOUT	Continuous		
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

5.2 ESD Protection

PIN	TEST CONDITIONS	TYP	UNIT
D_{OUT}, R_{IN}	Human-Body Model	±15	kV

5.3 Recommended Operating Conditions

(see(1) and 图 6-4)

			MIN	NOM	MAX	UNIT
Supply voltage			1.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
	Control high-level input voltage	$\overline{EN}$, SHDN	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{EN}$, SHDN			0.8	V
V_I	Driver and control input voltage	DIN, $\overline{EN}$, SHDN	0		5.5	V
	Receiver input voltage	DW Package	−30		30	
		DB Package	-25		25	V
T_A	Operating free-air temperature	MAX211C	0		70	°C
		MAX211I	−40		85	

(1) Test conditions are C1−C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

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5.4 Thermal Information

THERMAL METRIC(1)		DB	DW	UNIT
		28-PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.1	46	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.2	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.0	37.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.6	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.5	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see (2))

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	No load,	See 图 8-1		14	20	mA
	Shutdown supply current (DB package)	T_A = 25°C	See 图 6-1		5	10	μA
	Shutdown supply current (DW package)	T_A = 25°C	See 图 6-1		1	20	μA

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Test conditions are C1−C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

5.6 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see (3) and 图 6-4)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3kΩ to GND		5	9		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3kΩ to GND		−5	−9		V
I_{IH}	Driver high-level input current	DIN = V_{CC}			15	200	μA
	Control high-level input current	$\overline{EN}$, SHDN = V_{CC}			3	10	
I_{IL}	Driver low-level input current	DIN = 0V			−15	−200	μA
	Control low-level input current	$\overline{EN}$, SHDN = 0V			−3	−10	
I_{OS} (2)	Short-circuit output current	V_{CC} = 5.5V,	V_O = 0V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, and V− = 0V,	V_O = ±2V	300			Ω

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1−C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

5.7 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see (3))

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
	Maximum data rate	C_L = 50pF to 1000pF, One DOUT switching,	R_L = 3kΩ to 7kΩ, See 图 6-2	120			kbit/s
$t_{PLH (D)}$	Propagation delay time, low- to high-level output	C_L = 2500pF, All drivers loaded,	R_L = 3kΩ, See 图 6-2		2		μs
$t_{PHL (D)}$	Propagation delay time, high- to low-level output	C_L = 2500pF, All drivers loaded,	R_L = 3kΩ, See 图 6-2		2		μs

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5.7 Switching Characteristics, Driver （续）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see (3))

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
$t_{sk(p)}$	Pulse skew(2)	C_L = 150pF to 2500pF,	R_L = 3kΩ to 7kΩ, See 图 6-3		300		ns
SR(tr)	Slew rate, transition region (see 图 6-2)	C_L = 50pF to 1000pF, V_{CC} = 5V	R_L = 3kΩ to 7kΩ,	3	6	30	V/μs

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} − t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1−C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

5.8 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see (2) and 图 8-1)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1mA		3.5	V_{CC}−0.	4 V	V
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA				0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5V,	T_A = 25°C		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} − V_{IT-})			0.2	0.5	1	V
r_i	Input resistance	V_{CC} = 5V,	T_A = 25°C	3	5	7	kΩ
	Output leakage current	$\overline{EN}$ = V_{CC},	0 ≤ ROUT ≤ V_{CC}		±0.05	±10	μA

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Test conditions are C1−C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

5.9 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see (3))

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$t_{PLH\ (R)}$	Propagation delay time, low- to high-level output	C_L= 150pF,	See 图 6-4		0.5	10	μs
$t_{PHL\ (R)}$	Propagation delay time, high- to low-level output	C_L= 150pF,	See 图 6-4		0.5	10	μs
t_{en}	Output enable time	C_L= 150pF, See 图 6-5	R_L = 1kΩ,		600		ns
t_{dis}	Output disable time	C_L= 150pF, See 图 6-5	R_L = 1kΩ,		200		ns
$t_{sk(p)}$	Pulse skew(2)	See 图 6-3			300		ns

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} − t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1−C4 = 0.1μF, at V_{CC} = 5V ± 0.5V.

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6 Parameter Measurement Information

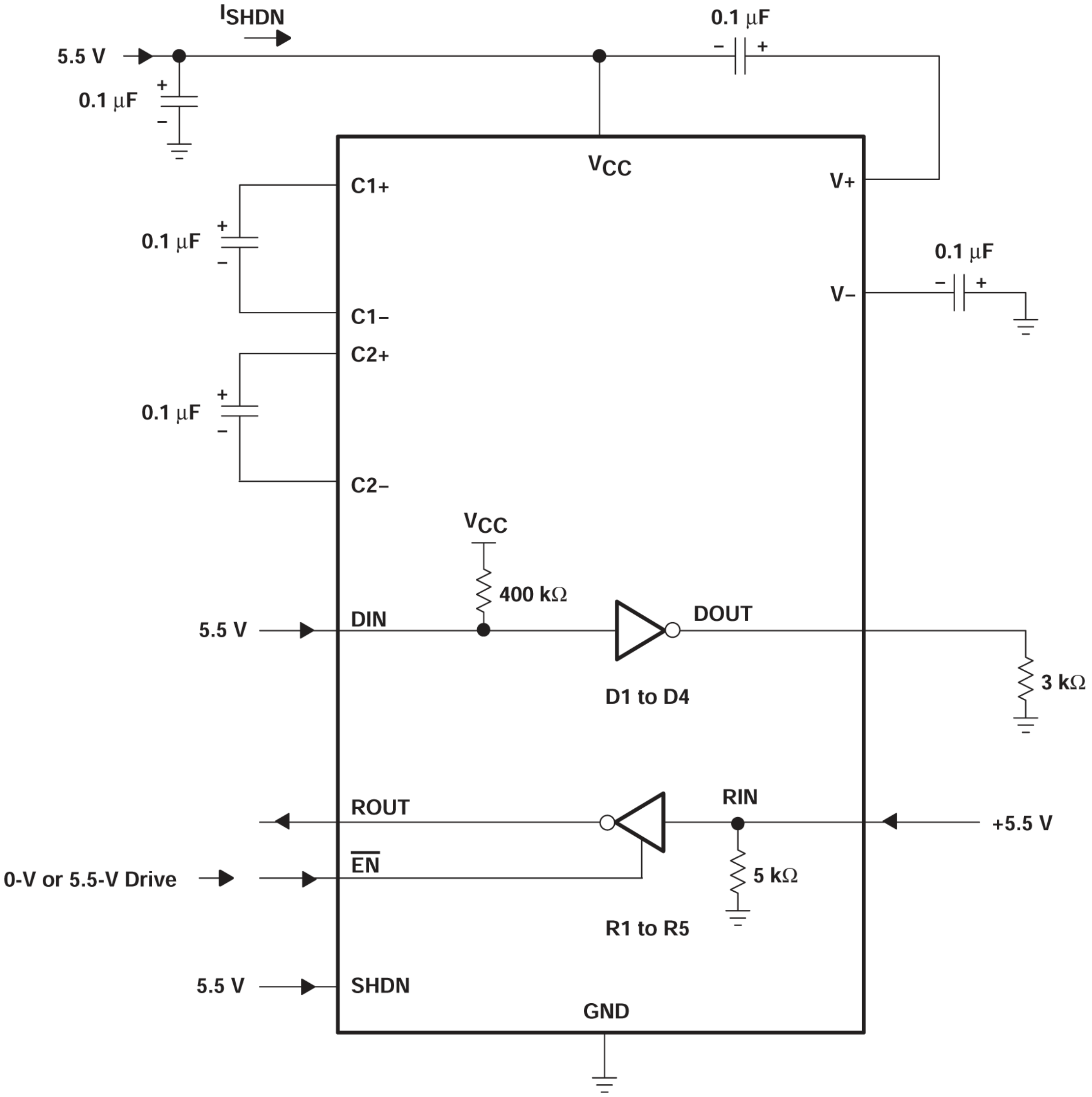
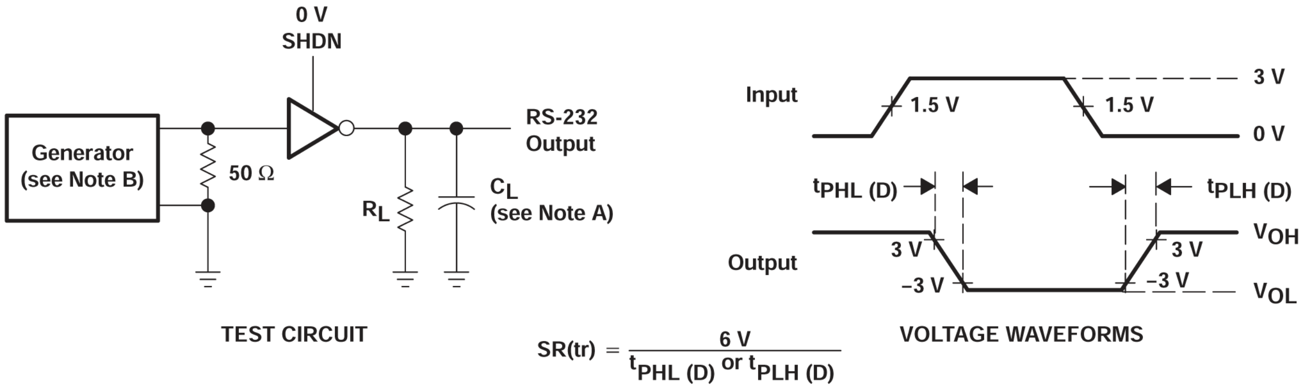


图 6-1. Shutdown Current Test Circuit



$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)}\ \text{or}\ t_{PLH\ (D)}}$$

A. C_L includes probe and jig capacitance.

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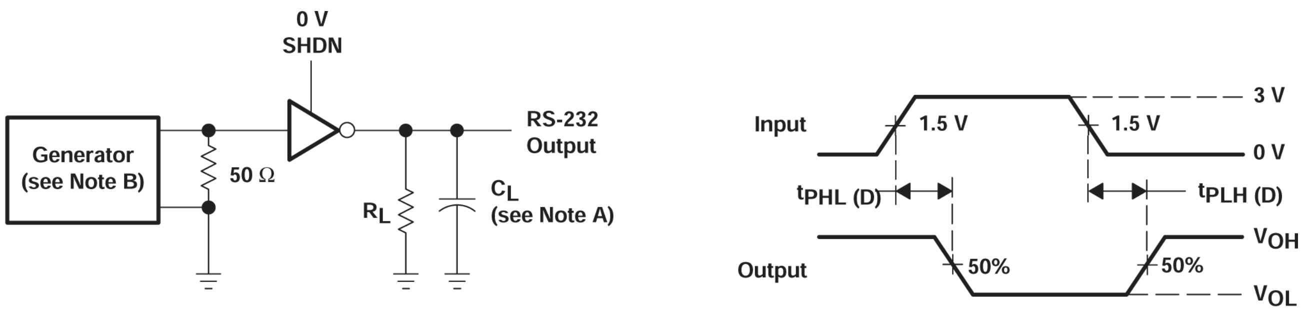
B. The pulse generator has the following characteristics: PRR = 120kbit/s, Z_O = 50Ω, 50% duty cycle, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns.

图 6-2. Driver Slew Rate and Propagation Delay Times



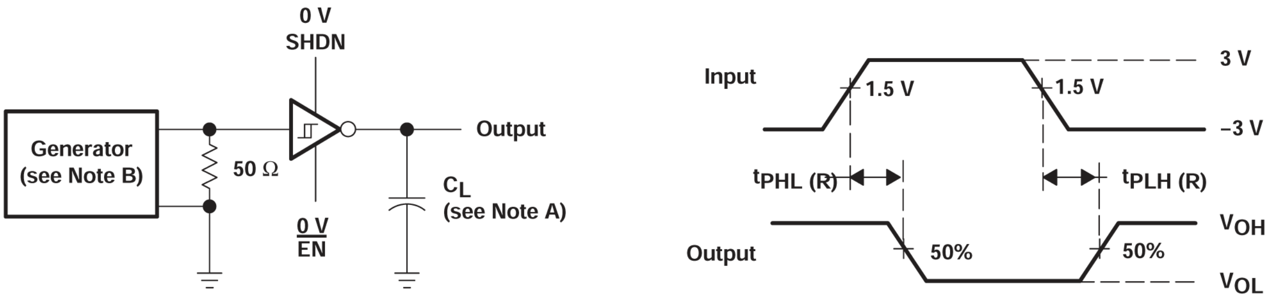
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120kbit/s, Z_O = 50Ω, 50% duty cycle, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns.

图 6-3. Driver Pulse Skew



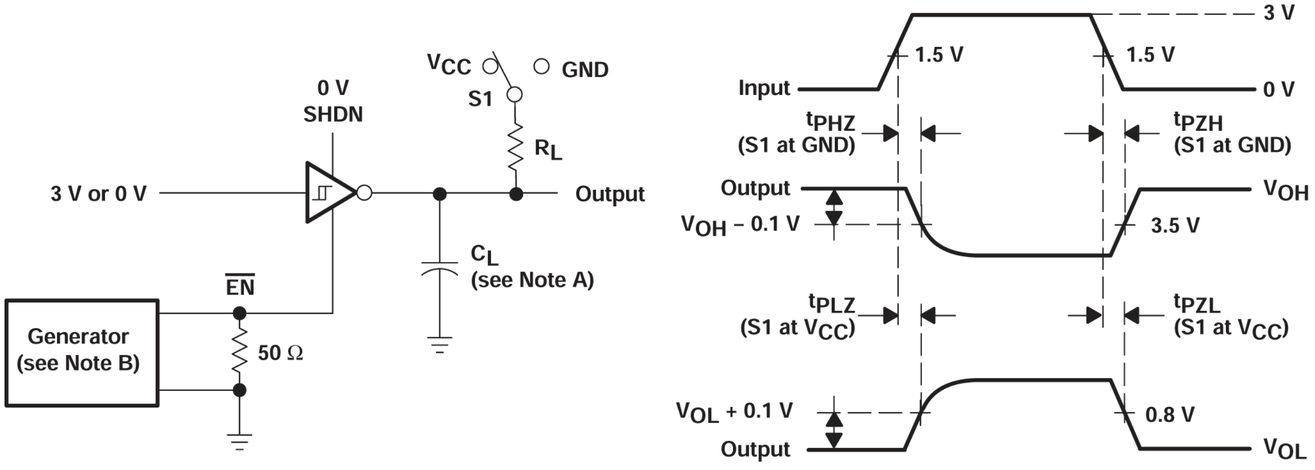
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns.

图 6-4. Receiver Propagation Delay Times



TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns.

C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

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D. t_{PZL} and t_{PZH} are the same as t_{en}.

图 6-5. Receiver Enable and Disable Times

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7 Device Functional Modes

表 7-1. Function Table

INPUTS(1)		DRIVER	RECEIVER	DEVICE STATUS
SHDN	$\overline{EN}$			
L	L	All active	All active	Normal operation
L	H	All active	Z	Normal operation
H	X	Z	Z	Shutdown

(1) X = don’t care, Z = high impedance

表 7-2. Function Table Each Driver

INPUTS(1)		OUTPUT DOUT	DRIVER STATUS
DIN	SHDN		
L	L	H	Normal operation
H	L	L	
X	H	Z	Powered off

(1) X = don’t care, Z = high impedance

表 7-3. Function Table Each Receiver

INPUTS(1)		OUTPUT ROUT	RECEIVER STATUS
RIN	$\overline{EN}$		
L	L	H	Normal operation
H	L	L	
X	H	Z	Powered off

(1) X = don’t care, Z = high impedance

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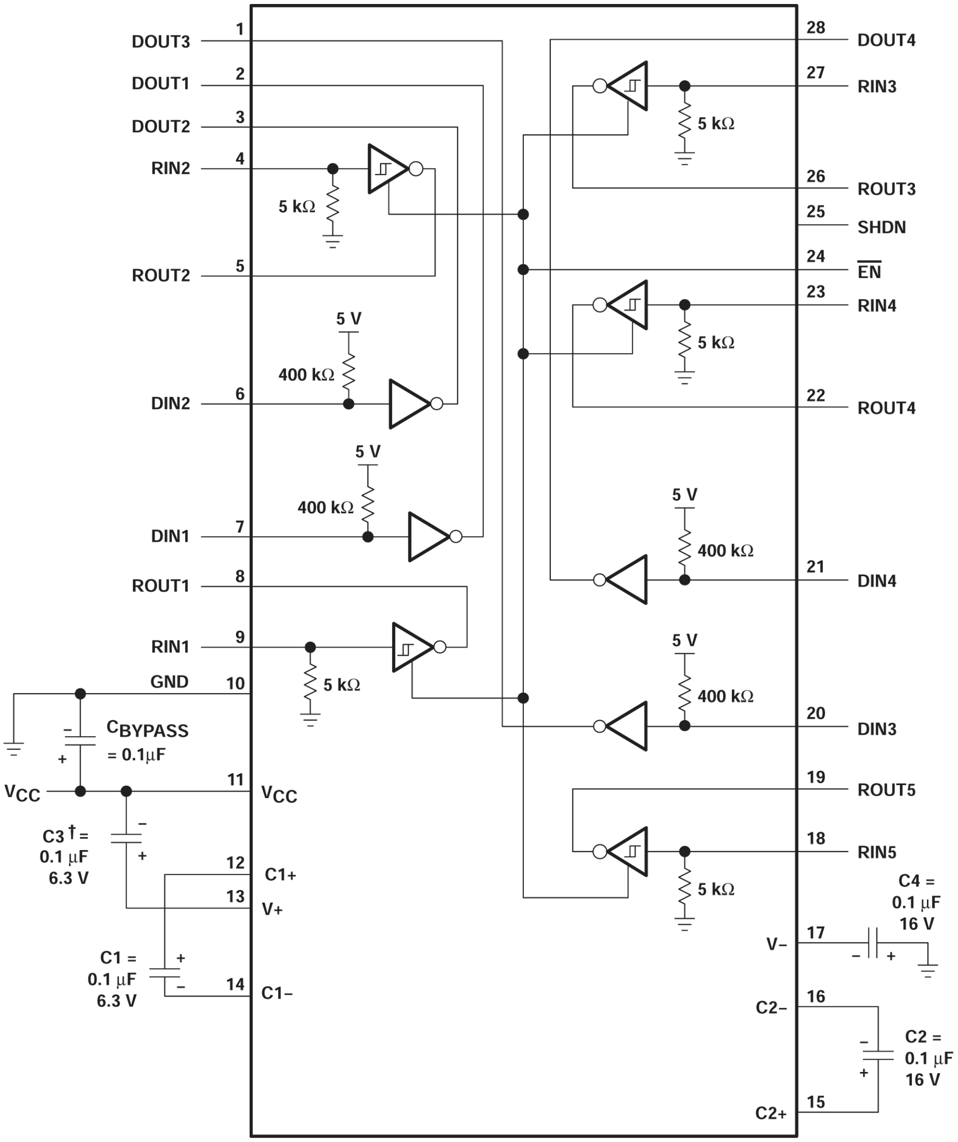
8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information



备注

C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, connect the capacitors as shown.

图 8-1. Typical Operating Circuit and Capacitor Values

8.1.1 Capacitor Selection

The capacitor type used for C1−C4 is not critical for proper operation. The MAX211 requires 0.1µF capacitors, although capacitors up to 10µF can be used without harm. Ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (2×) nominal value. The capacitors’ effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V−.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V−.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1−C4).

8.1.2 Electrostatic Discharge (ESD) Protection

Texas Instruments MAX211 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15kV when powered down.

8.1.3 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

8.1.4 Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in 图 8-2. 图 8-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100pF capacitor charged to the ESD voltage of concern and subsequently discharged into the DUT through a 1.5kΩ resistor.

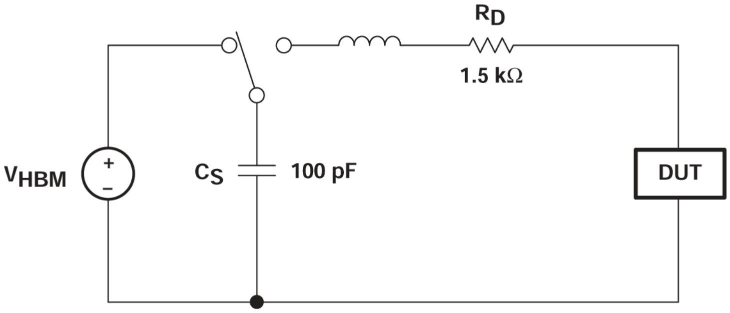


图 8-2. HBM ESD Test Circuit

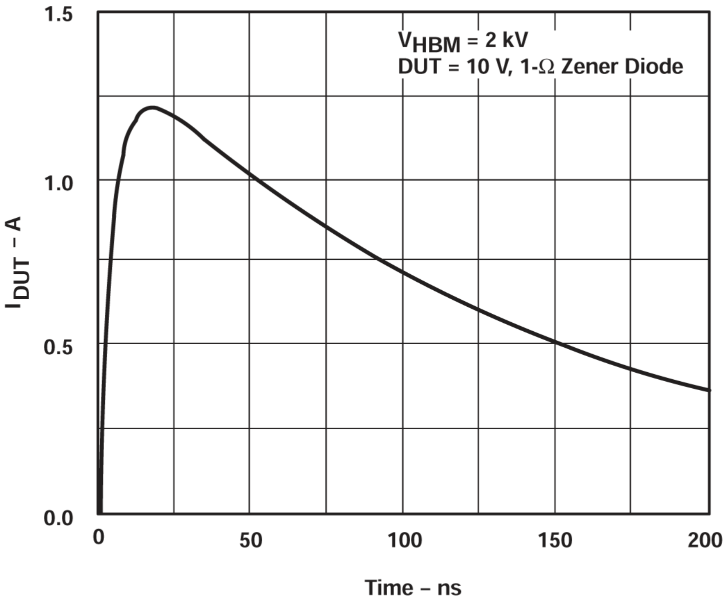


图 8-3. Typical HBM Current Waveform

8.1.5 Machine Model

The Machine Model (MM) ESD test applies to all pins, using a 200pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (January 2004) to Revision F (July 2024) **Page**

- 通篇更改了表格、图和交叉参考的编号格式 1
- Changed the Input voltage range for Receivers from ±30V to ±25V for the DB package in the *Absolute Maximum Ratings* and the *Recommended Operating Conditions* 5
- Changed the Shutdown supply current for DB package TYP value from 1μA to 5μA *Electrical Characteristics* 6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX211CDB	Obsolete	Production	SSOP (DB) | 28	-	-	Call TI	Call TI	0 to 70	MAX211C
MAX211CDBR	Obsolete	Production	SSOP (DB) | 28	-	-	Call TI	Call TI	0 to 70	MAX211C
MAX211CDW	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	0 to 70	MAX211C
MAX211CDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX211C
MAX211CDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX211C
MAX211IDB	Obsolete	Production	SSOP (DB) | 28	-	-	Call TI	Call TI	-40 to 85	MAX211I
MAX211IDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I
MAX211IDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I
MAX211IDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I
MAX211IDW	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	-40 to 85	MAX211I
MAX211IDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I
MAX211IDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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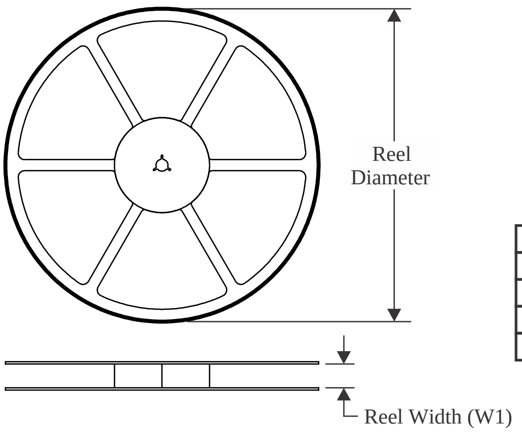
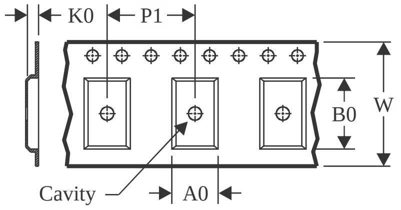
TAPE AND REEL INFORMATION

REEL DIMENSIONS

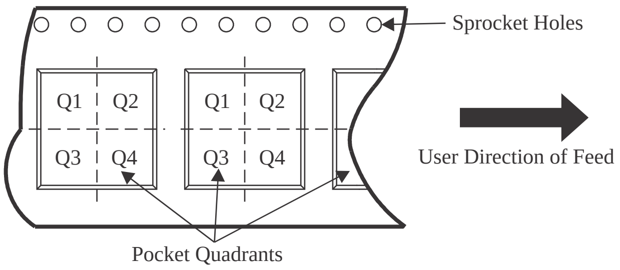


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

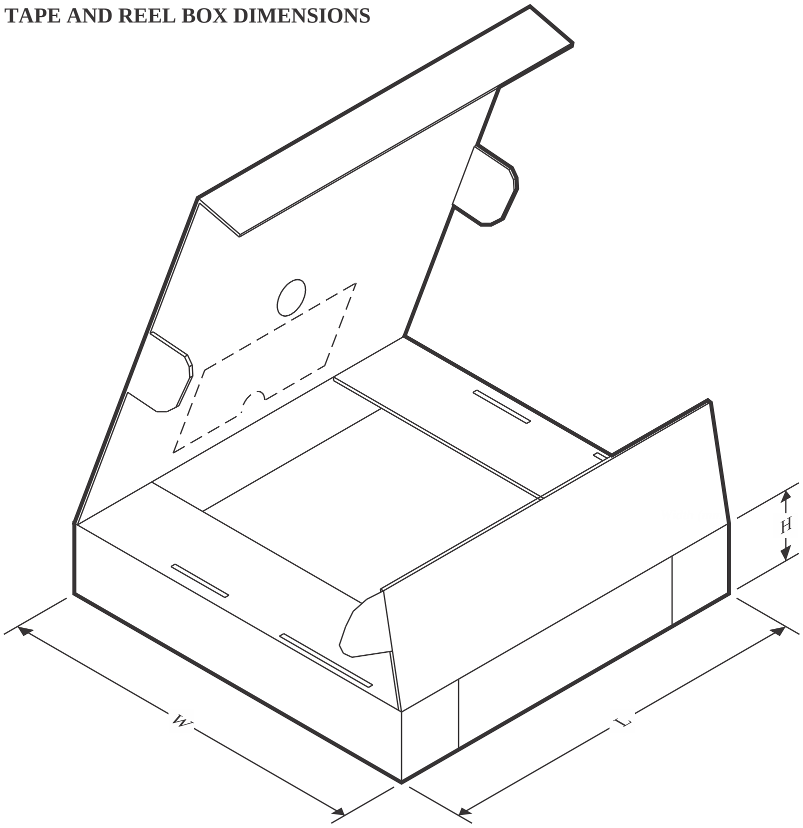
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX211CDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX211IDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
MAX211IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



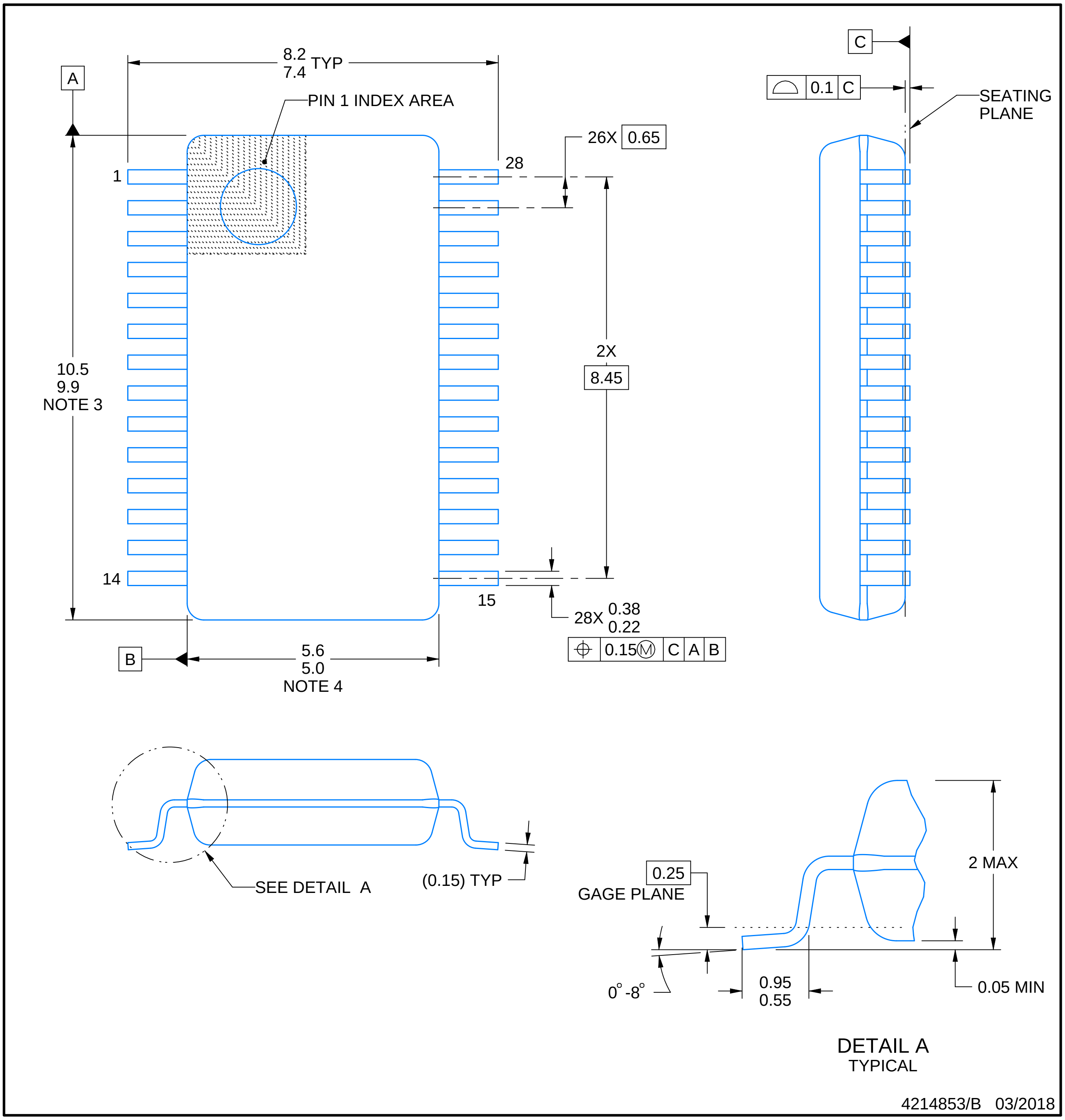
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX211CDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX211IDBR	SSOP	DB	28	2000	353.0	353.0	32.0
MAX211IDWR	SOIC	DW	28	1000	350.0	350.0	66.0

PACKAGE OUTLINE

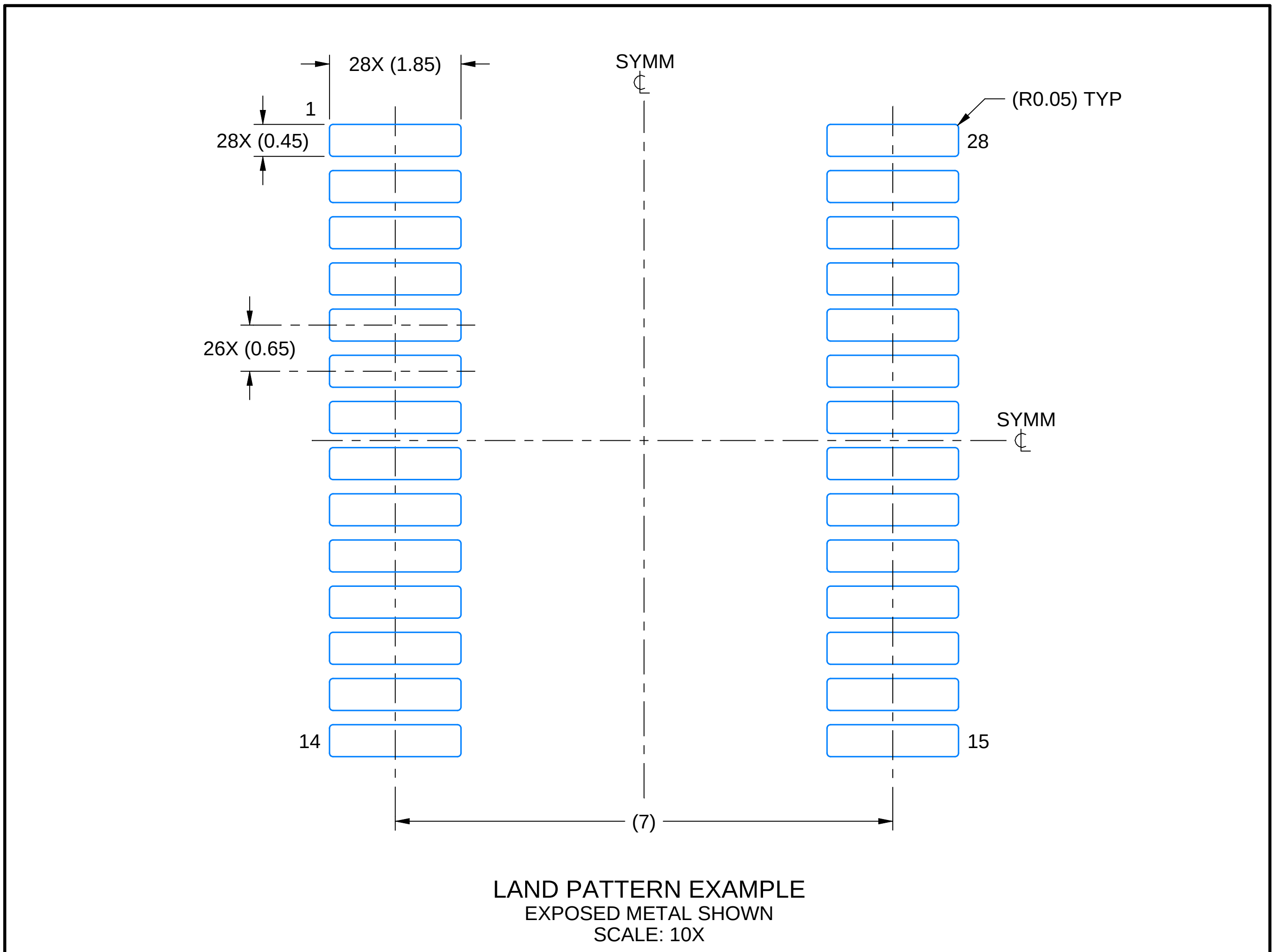
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

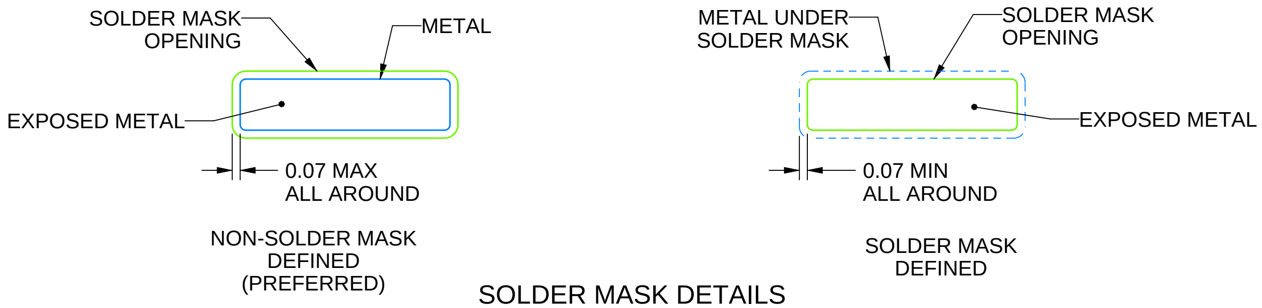


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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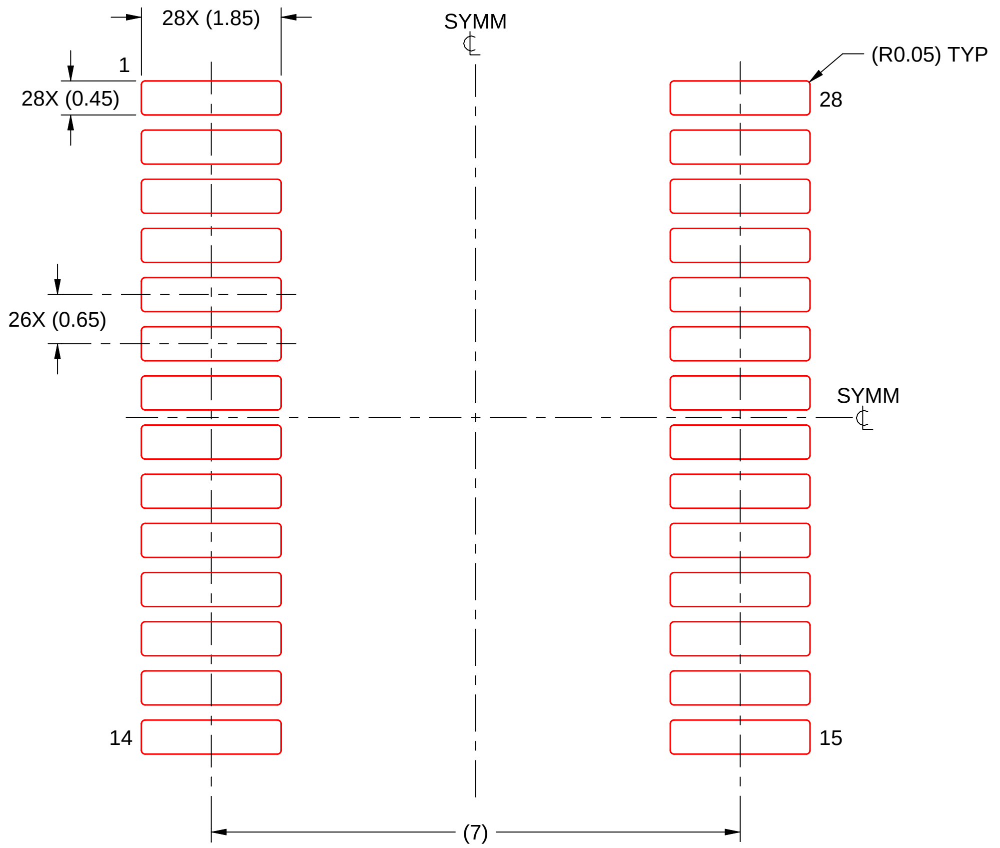
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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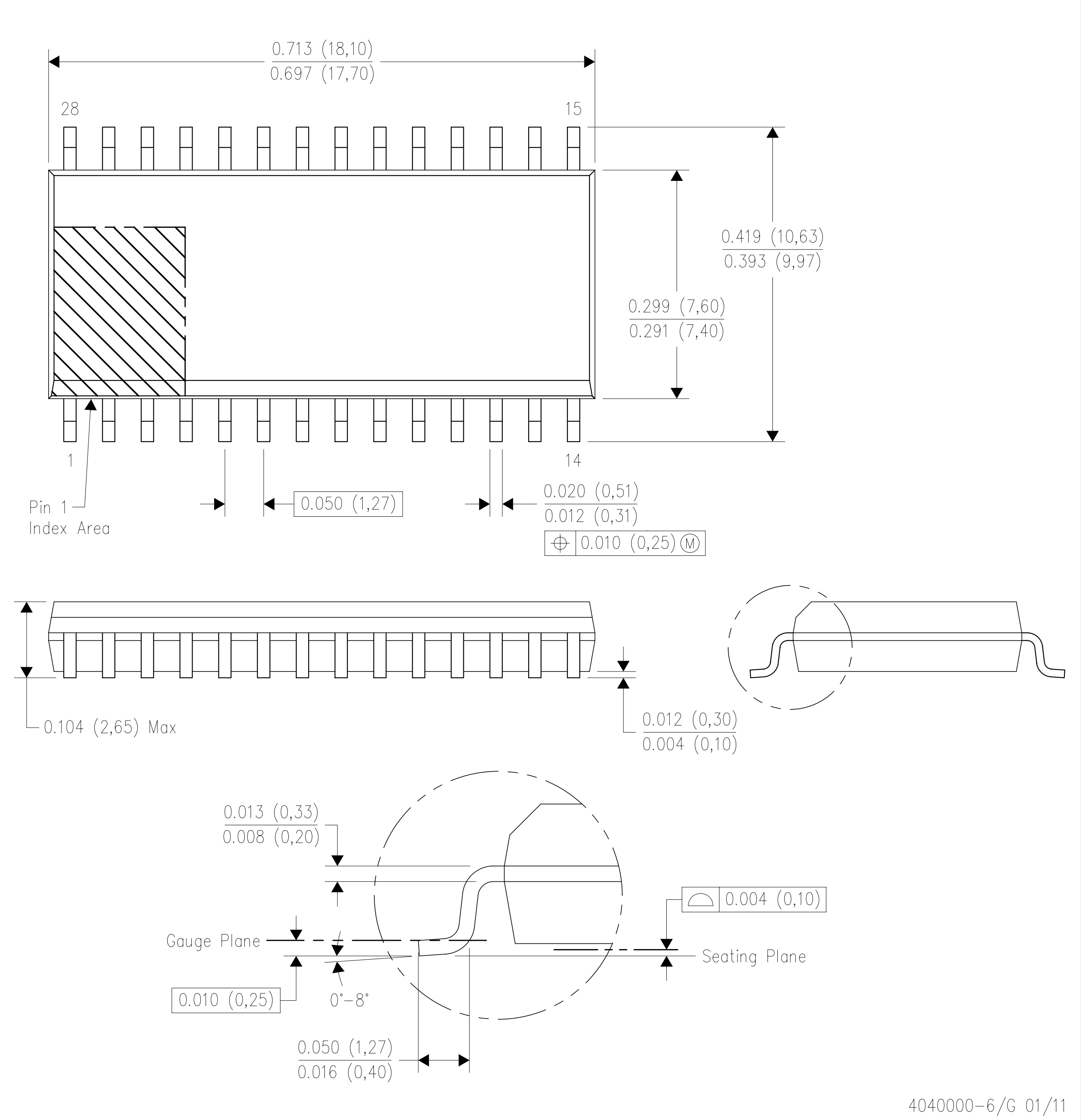
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AE.

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