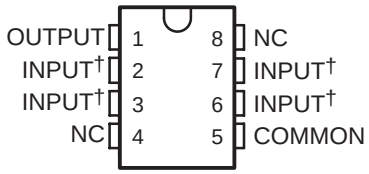
SLVS011D − OCTOBER 1982 − REVISED AUGUST 2003

- **3-Terminal Regulators**
- **Output Current Up To 100 mA**
- **No External Components Required**
- **Internal Thermal-Overload Protection**
- **Internal Short-Circuit Current Limiting**
- **Direct Replacement for Industry-Standard MC79L00 Series**
- **Available in 5% or 10% Selections**

D PACKAGE
(TOP VIEW)



† Internally connected
NC − No internal connection

LP PACKAGE
(TOP VIEW)



description/ordering information

This series of fixed negative-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used to control series pass elements to make high-current voltage-regulator circuits. One of these regulators can deliver up to 100 mA of output current. The internal current-limiting and thermal-shutdown features essentially make the regulators immune to overload. When used as a replacement for a Zener-diode and resistor combination, these devices can provide an effective improvement in output impedance of two orders of magnitude, with lower bias current.

ORDERING INFORMATION

T_J	OUTPUT VOLTAGE TOLERANCE	NOMINAL OUTPUT VOLTAGE (V)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5%	−5	SOIC (D)	Tube of 75	MC79L05ACD	79L05A
				Reel of 2500	MC79L05ACDR	
			TO-226 / TO-92 (LP)	Bulk of 1000	MC79L05ACLP	79L05AC
				Reel of 2000	MC79L05ACLPR	
		−12	SOIC (D)	Tube of 75	MC79L12ACD	79L12A
				Reel of 2500	MC79L12ACDR	
			TO-226 / TO-92 (LP)	Bulk of 1000	MC79L12ACLP	79L12AC
				Reel of 2000	MC79L12ACLPR	
		−15	TO-226 / TO-92 (LP)	Bulk of 1000	MC79L15ACLP	79L15AC
				Ammo of 2000	MC79L15ACLPM	
				Reel of 2000	MC79L15ACLPR	
	10%	−12	TO-226 / TO-92 (LP)	Bulk of 1000	MC79L12CLP	79L12C
		−15	SOIC (D)	Tube of 75	MC79L15CD	79L15C

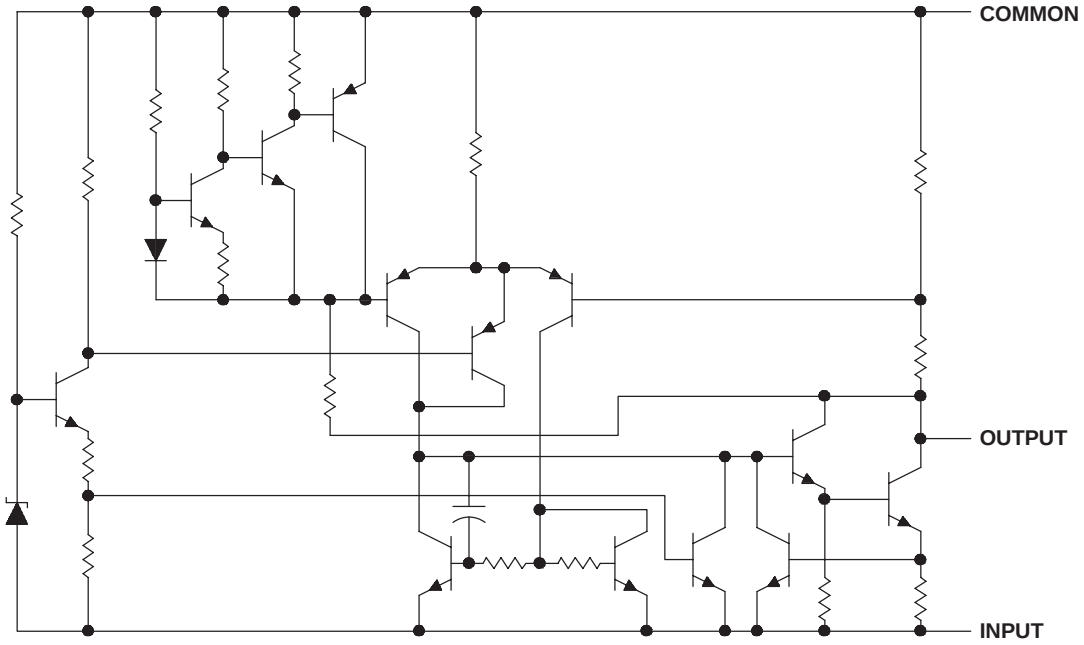
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage: MC79L05 . . . . . −30 V
MC79L12, MC79L15 . . . . . −35 V
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package . . . . . 97°C/W
LP package . . . . . 140°C/W
Operating free-air, case, or virtual junction temperature . . . . . 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_I	Input voltage	MC79L05	−7	−20	V
		MC79L12	−14.5	−27	
		MC79L15	−17.5	−30	
I_O	Output current			100	mA
T_J	Operating virtual junction temperature		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J	MC79L05C			MC79L05AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−4.6	−5	−5.4	−4.8	−5	−5.2	V
	V_I = −7 V to −20 V, I_O = 1 mA to 40 mA	0°C to 125°C	−4.5		−5.5	−4.75		−5.25	
	V_I = −10 V, I_O = 1 mA to 70 mA	0°C to 125°C	−4.5		−5.5	−4.75		−5.25	
Input regulation	V_I = −7 V to −20 V	25°C			200			150	mV
	V_I = −8 V to −20 V				150			100	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			60			60	mV
	I_O = 1 mA to 40 mA				30			30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40			40		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6			6	mA
		125°C			5.5			5.5	
Bias current change	V_I = −8 V to −20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J	MC79L12C			MC79L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−11.1	−12	−12.9	−11.5	−12	−12.5	V
	V_I = −14.5 V to −27 V, I_O = 1 mA to 40 mA	0°C to 125°C	−10.8		−13.2	−11.4		−12.6	
	V_I = −19 V, I_O = 1 mA to 70 mA	0°C to 125°C	−10.8		−13.2	−11.4		−12.6	
Input regulation	V_I = −14.5 V to −27 V	25°C			250			250	mV
	V_I = −16 V to −27 V				200			200	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			100			100	mV
	I_O = 1 mA to 40 mA				50			50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		80			80		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = −16 V to −27 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J	MC79L15C			MC79L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−13.8	−15	−16.2	−14.4	−15	−15.6	V
	V_I = −17.5 V to −30 V, I_O = 1 mA to 40 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
	V_I = −23 V, I_O = 1 mA to 70 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C			300			300	mV
	V_I = −17.5 V to −30 V				250			250	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			150			150	mV
	I_O = 1 mA to 40 mA				75			75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90			90		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = −20 V to −30 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC79L05ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	
MC79L05ACDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	
MC79L05ACDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	
MC79L05ACDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	
MC79L05ACDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	
MC79L05ACDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	
MC79L05ACLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L05AC	
MC79L05ACLPE3	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L05AC	
MC79L05ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L05AC	
MC79L12ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	
MC79L12ACDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	
MC79L12ACDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	
MC79L12ACLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L12AC	
MC79L12ACLPE3	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L12AC	
MC79L12ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L12AC	
MC79L12ACLPRE3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L12AC	
MC79L12CLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L12C	
MC79L15ACLP	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L15AC	
MC79L15ACLPE3	LIFEBUY	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L15AC	
MC79L15ACLPR	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L15AC	
MC79L15ACLPRE3	LIFEBUY	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	79L15AC	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

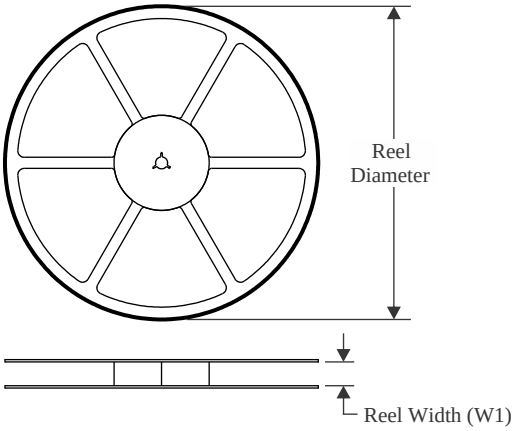
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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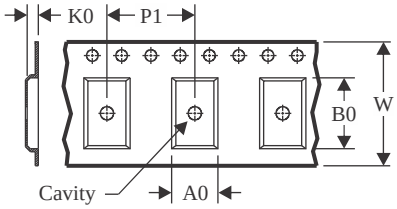
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

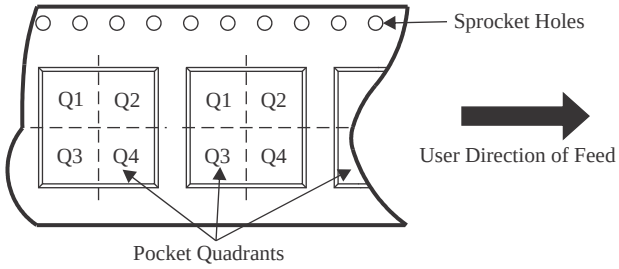


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

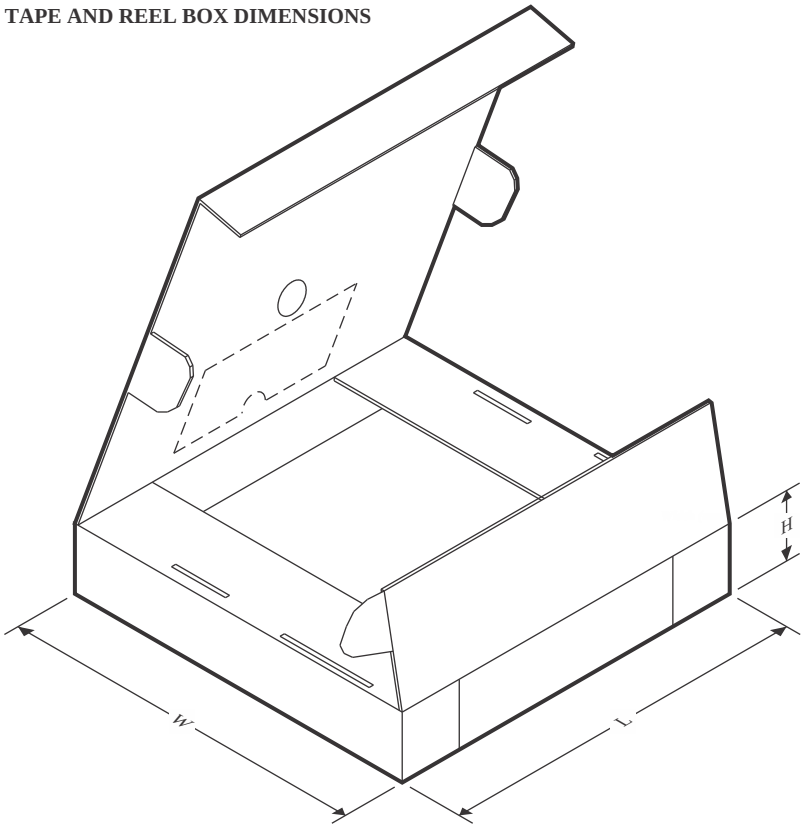
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC79L05ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC79L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

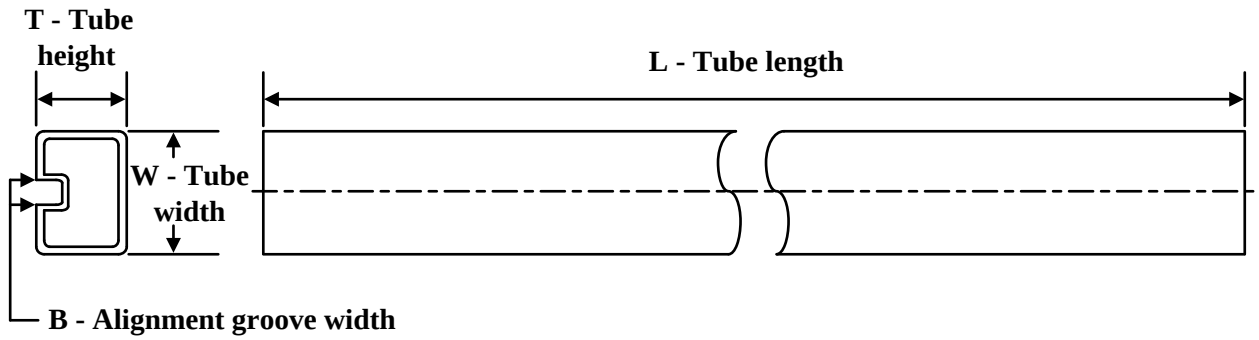
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

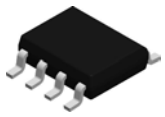
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC79L05ACDR	SOIC	D	8	2500	340.5	338.1	20.6
MC79L12ACDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MC79L05ACD	D	SOIC	8	75	507	8	3940	4.32
MC79L05ACDE4	D	SOIC	8	75	507	8	3940	4.32
MC79L05ACDG4	D	SOIC	8	75	507	8	3940	4.32
MC79L12ACD	D	SOIC	8	75	507	8	3940	4.32
MC79L12ACDE4	D	SOIC	8	75	507	8	3940	4.32

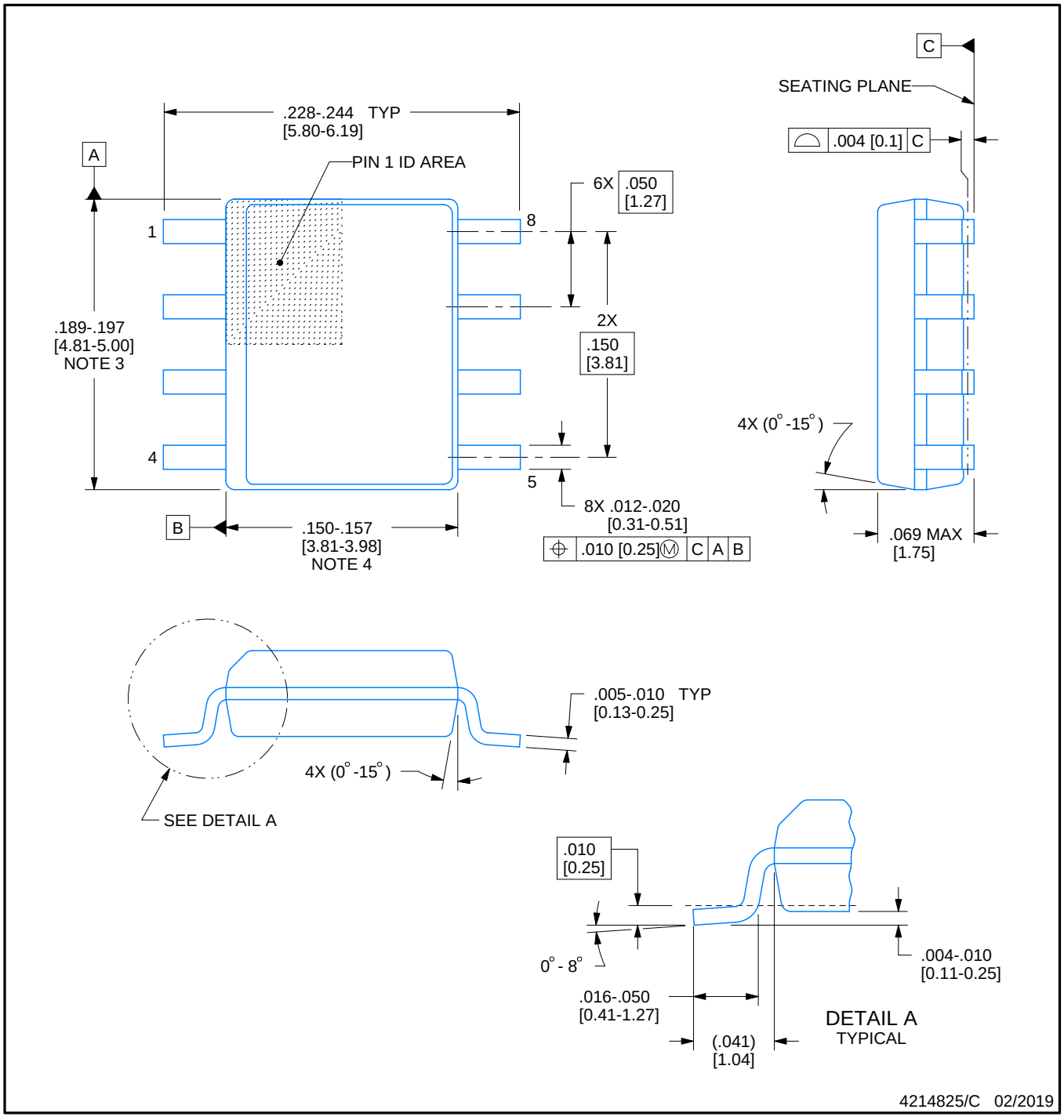


PACKAGE OUTLINE

D0008A

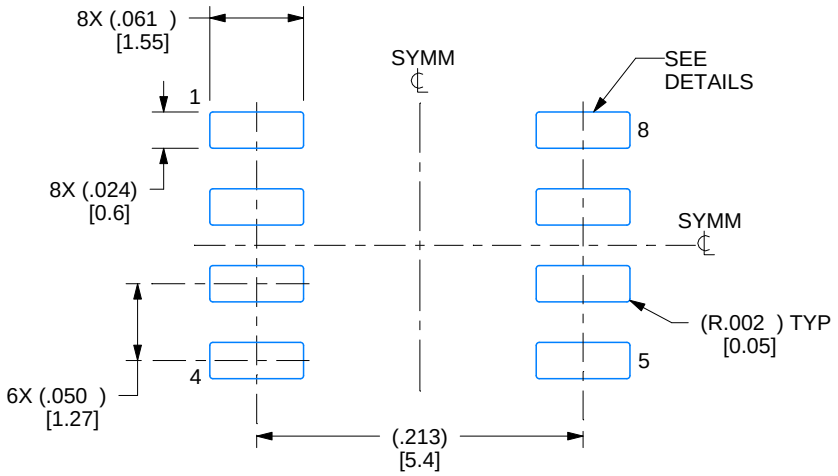
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

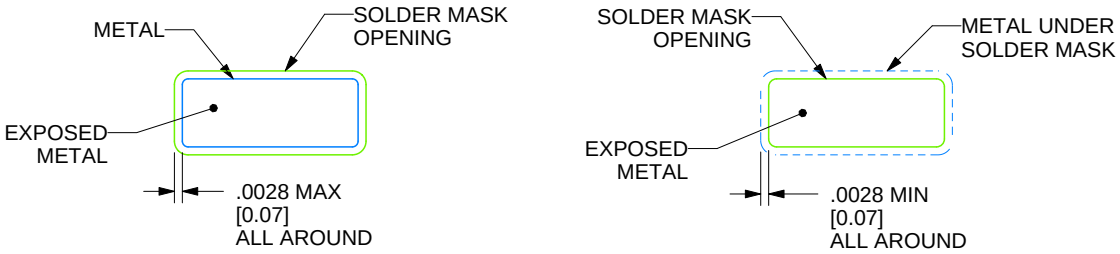


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

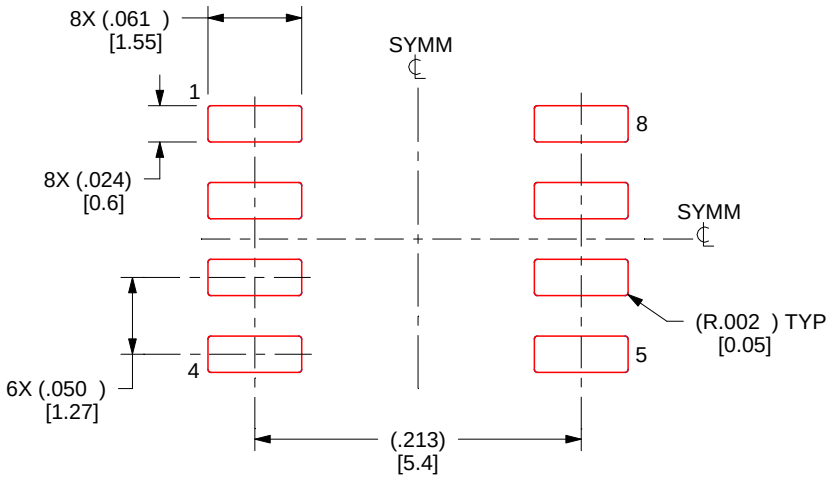
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

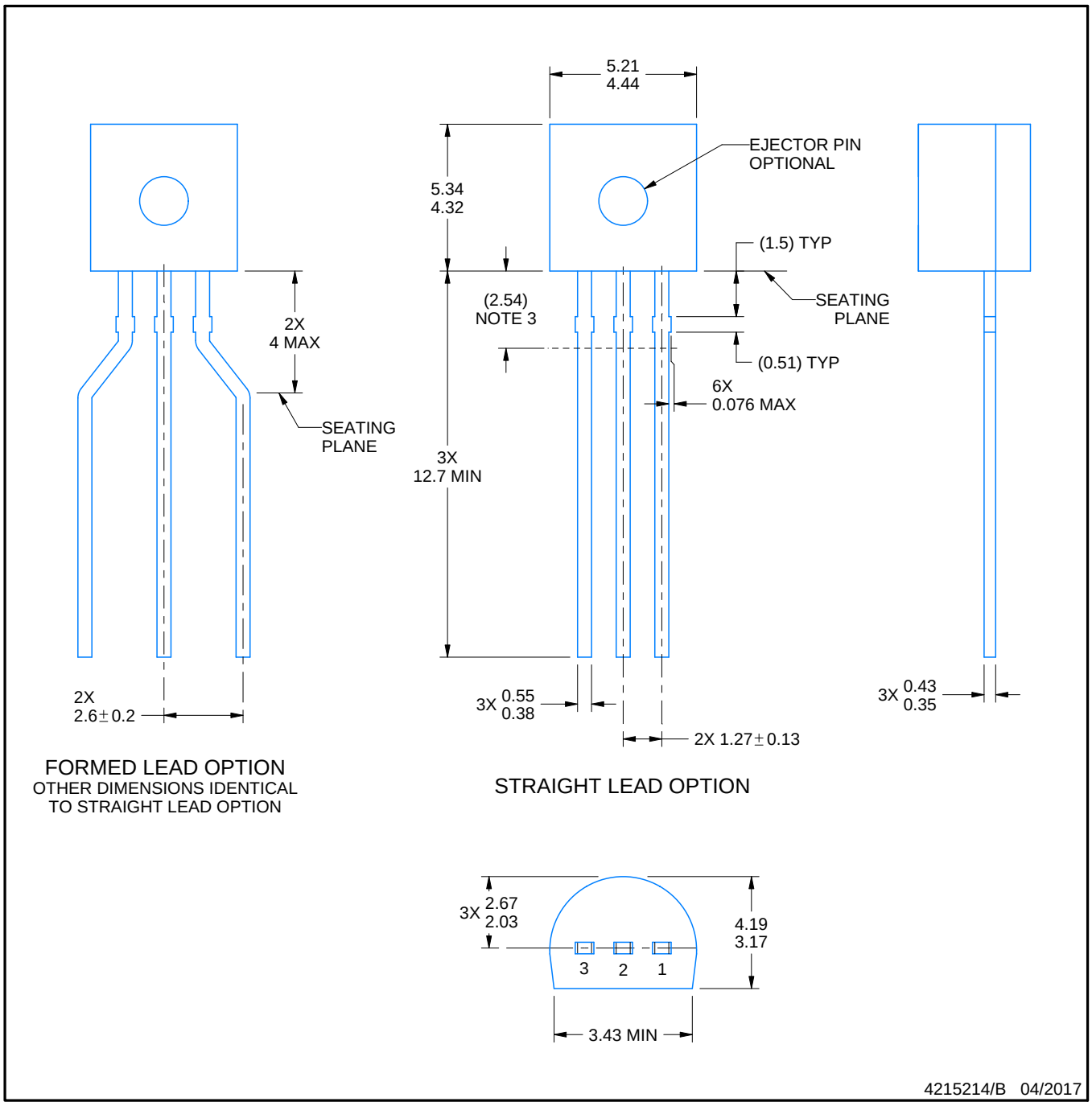




PACKAGE OUTLINE

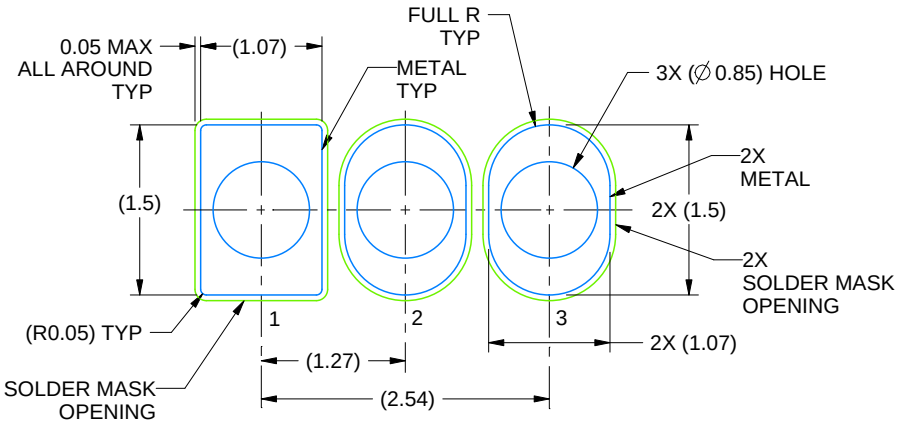
TO-92 - 5.34 mm max height

TO-92

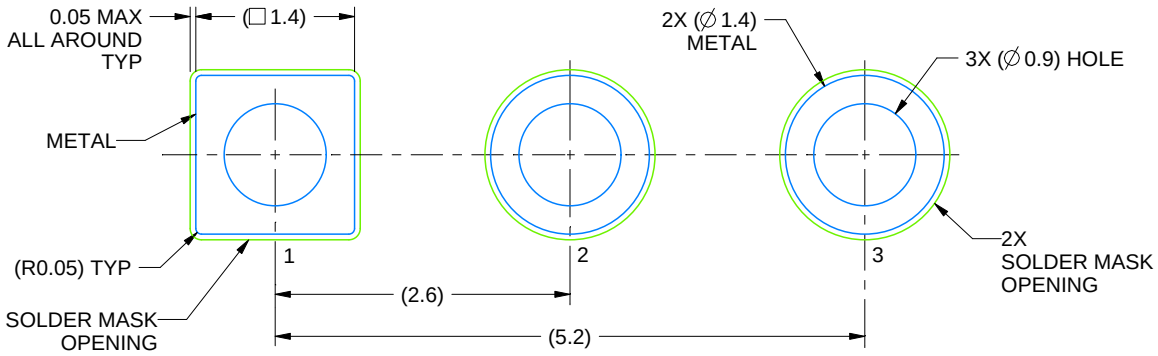


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



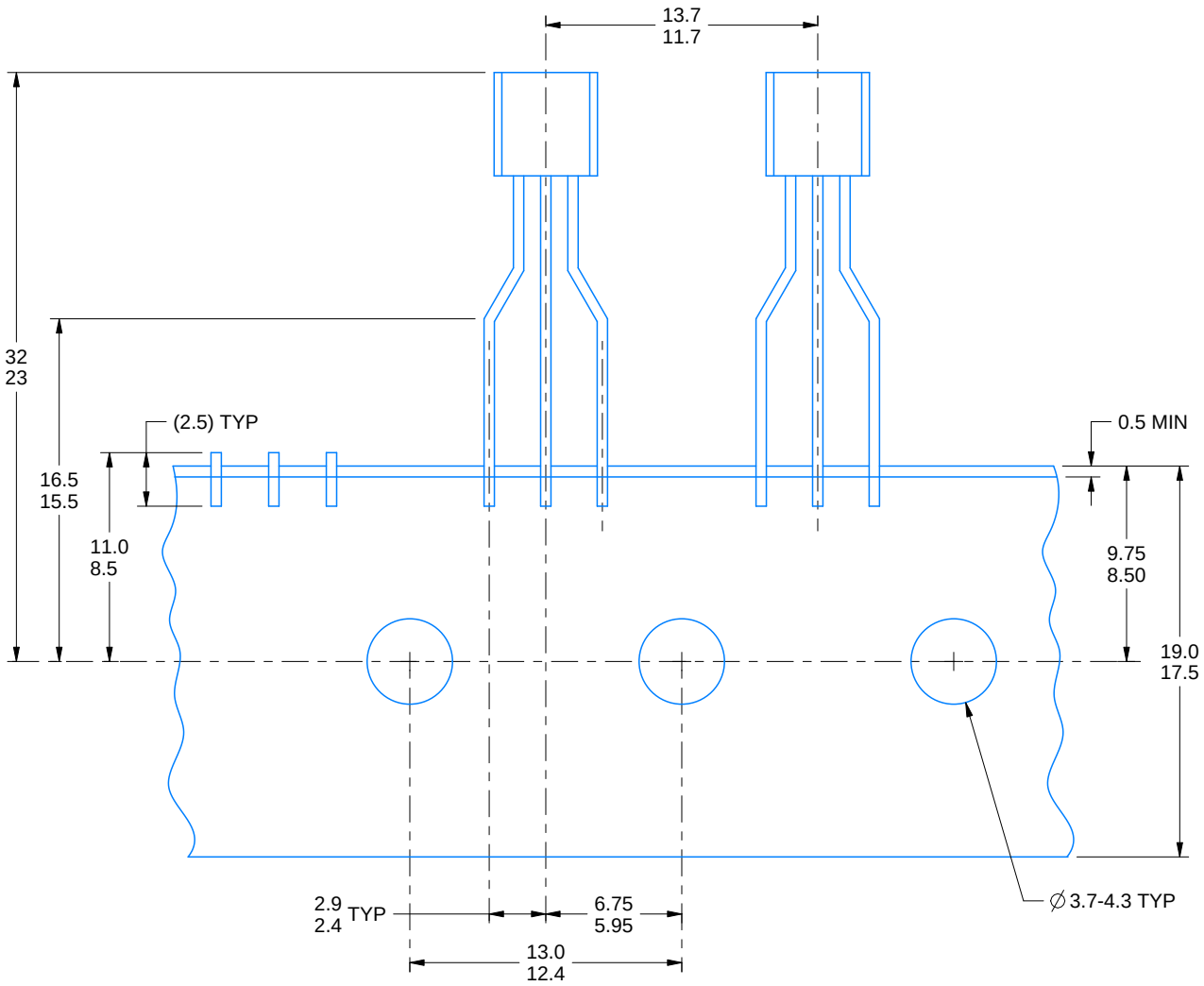
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

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