

MSP430F5310、MSP430F530x 混合信号微控制器

1 器件概述

1.1 特性

- 低电源电压范围：
3.6V 到低至 1.8V
- 超低功耗
 - 激活模式 (AM)
 - 所有系统时钟激活
 - 8MHz 时为 195μA/MHz (典型值)、3V、闪存程序执行
 - 8MHz 时为 115μA/MHz (典型值)、3V、RAM 程序执行
 - 待机模式 (LPM3)
 - 带有晶振的实时时钟，看门狗和电源监控器可用，完全 RAM 保持，快速唤醒：
2.2V 时为 1.9μA (典型值)，
3V 时为 2.1μA (典型值)
 - 低功耗振荡器 (VLO)，通用计数器，看门狗和电源监控器可用，完全 RAM 保持，快速唤醒：
3V 时为 1.4μA (典型值)
 - 关闭模式 (LPM4)
 - 完全 RAM 保持，电源监控器工作，快速唤醒：
3V 时为 1.1μA (典型值)
 - 关断模式 (LPM4.5)
 - 3V 时为 0.18μA (典型值)
- 在不到 5μs 的时间内从待机模式中唤醒
- 16 位精简指令集计算机 (RISC) 架构，扩展内存，高达 25MHz 的系统时钟
- 灵活的电源管理系统
 - 内置可编程的低压降稳压器 (LDO)
 - 电源电压监控、监视、和临时限电
- 统一时钟系统 (UCS)
 - 针对频率稳定的锁相环 (FLL) 控制环路
- 低功耗低频内部时钟源 (VLO)
- 低频修整内部基准源 (REFO)
- 32kHz 手表晶振 (XT1)
- 高达 32MHz 的高频晶振 (XT2)
- 具有 5 个捕捉/比较寄存器的 16 位定时器 TA0, Timer_A
- 具有 3 个捕捉/比较寄存器的 16 位定时器 TA1, Timer_A
- 具有 3 个捕捉/比较寄存器的 16 位定时器 TA2, Timer_A
- 具有 7 个捕捉/比较影子寄存器的 16 位定时器 TB0, Timer_B
- 两个通用串行通信接口 (USCI)
 - USCI_A0 和 USCI_A1
 - 增强型通用异步收发器 (UART) 支持自动波特率检测
 - IrDA 编码和解码
 - 同步串行外设接口 (SPI)
 - USCI_B0 和 USCI_B1
 - I²C
 - 同步 SPI
- 集成型 3.3V 电源系统
- 具有窗口比较器的 10 位模数转换器 (ADC)
- 比较器
- 硬件乘法器支持 32 位运算
- 串行板上编程，无需外部编程电压
- 3 通道内部 DMA
- 具有 RTC 特性的基本计时器
- [器件比较](#) 汇总了可用的产品系列成员

1.2 应用

- 模拟和数字传感器系统
- 数字电机控制
- 遥控
- 恒温器
- 数字定时器
- 手持仪表

1.3 说明

TI MSP 系列超低功耗微控制器种类繁多，各成员器件配备不同的外设集以满足各类应用的需求。该架构与五种低功耗模式配合使用，是延长便携式测量应用电池寿命的最优选择。该器件具有一个强大的 16 位精简指令集 (RISC) CPU，使用 16 位寄存器以及常数发生器，以便获得最高编码效率。此数控振荡器 (DCO) 可使器件在不到 5μs 的时间内从低功耗模式唤醒至激活模式。

MSP430F5310、MSP430F5309 和 MSP430F5308 器件为微控制器配置，具有 1 个 3.3V LDO、4 个 16 位计时器、1 个高性能 10 位 ADC、2 个 USCI ⁽¹⁾、1 个硬件乘法器、DMA、1 个具有警报功能的 RTC 模块以及 31 或 47 个 I/O 引脚。

(1) 在 48 引脚封装内，USCI 功能是否可用取决于用户使用端口映射控制器对端口 4 进行的配置。可能无法同时实现全部功能。



MSP430F5304 器件配置具有 1 个 3.3V LDO、4 个 16 位计时器、1 个高性能 10 位 ADC、1 个 USCI、1 个硬件乘法器、DMA、1 个具有警报功能的 RTC 模块和 31 个 I/O 引脚。

有关完整的模块说明，请参阅《MSP430F5xx 和 MSP430F6xx 系列用户指南》。

器件信息(1)

器件型号	封装	封装尺寸 ⁽²⁾
MSP430F5310RGC	VQFN (64)	9mm x 9mm
MSP430F5310ZQE	BGA (80)	5mm x 5mm
MSP430F5310PT	LQFP (48)	7mm x 7mm
MSP430F5310RGZ	VQFN (48)	7mm x 7mm

(1) 要获得最新的产品、封装和订购信息, 请参见封装选项附录 (节 8), 或者访问德州仪器 (TI) 网站 www.ti.com.cn。

(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸, 请参见机械数据(节8)。

1.4 功能方框图

图 1-1 至图 1-3 显示了功能方框图。

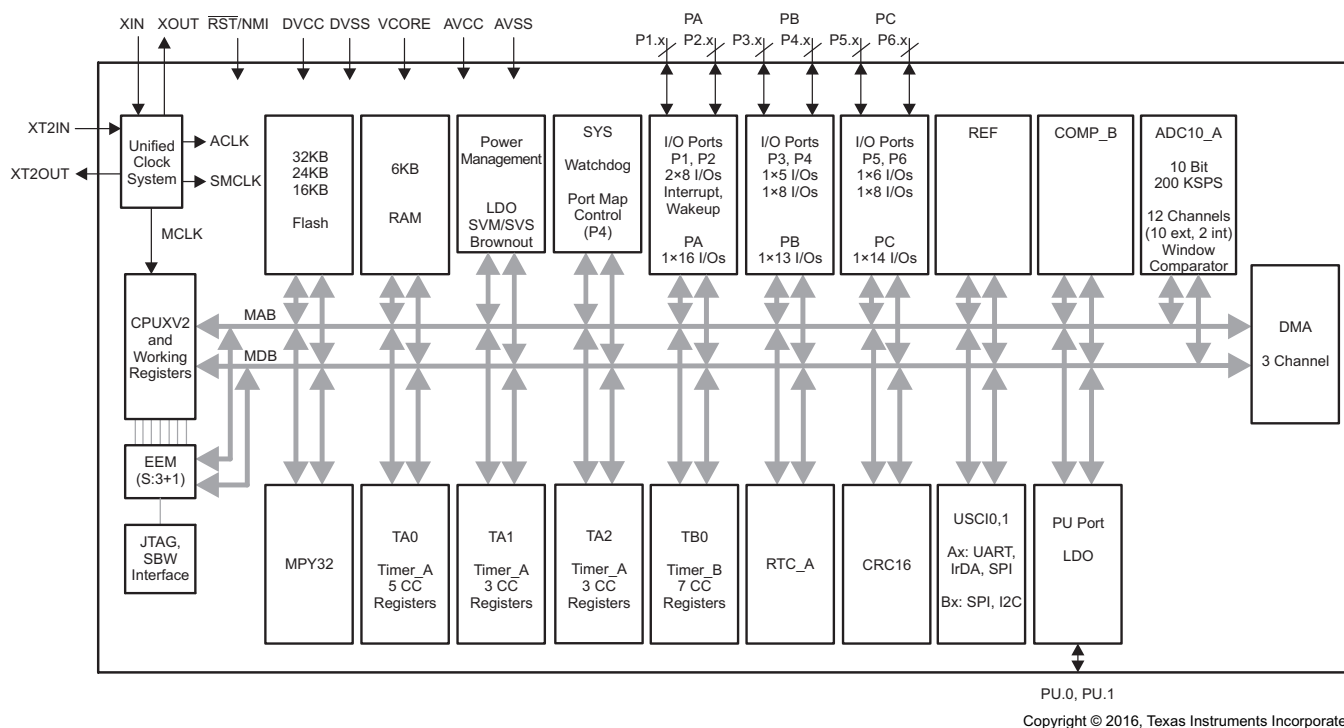
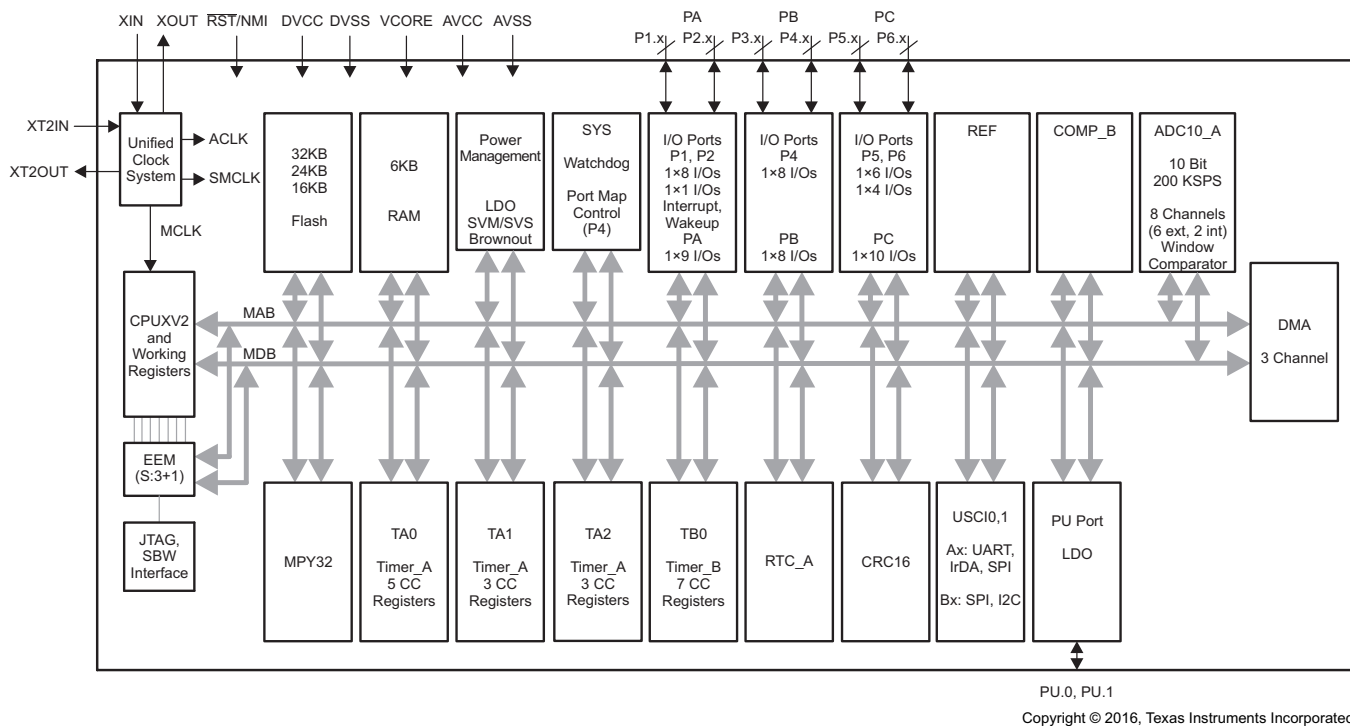


图 1-1. 功能方框图 – MSP430F5310IRGC、MSP430F5309IRGC、MSP430F5308IRG、MSP430F5310IZQE、MSP430F5309IZQE、MSP430F5308IZQE



NOTE: 有关 USCI 模块信号同时可用的限制条件, 请参阅Table 3-1。

图 1-2. 功能方框图 – MSP430F5310IRGZ、MSP430F5309IRGZ、MSP430F5308IRGZ、MSP430F5310IPT、MSP430F5309IPT、MSP430F5308IPT

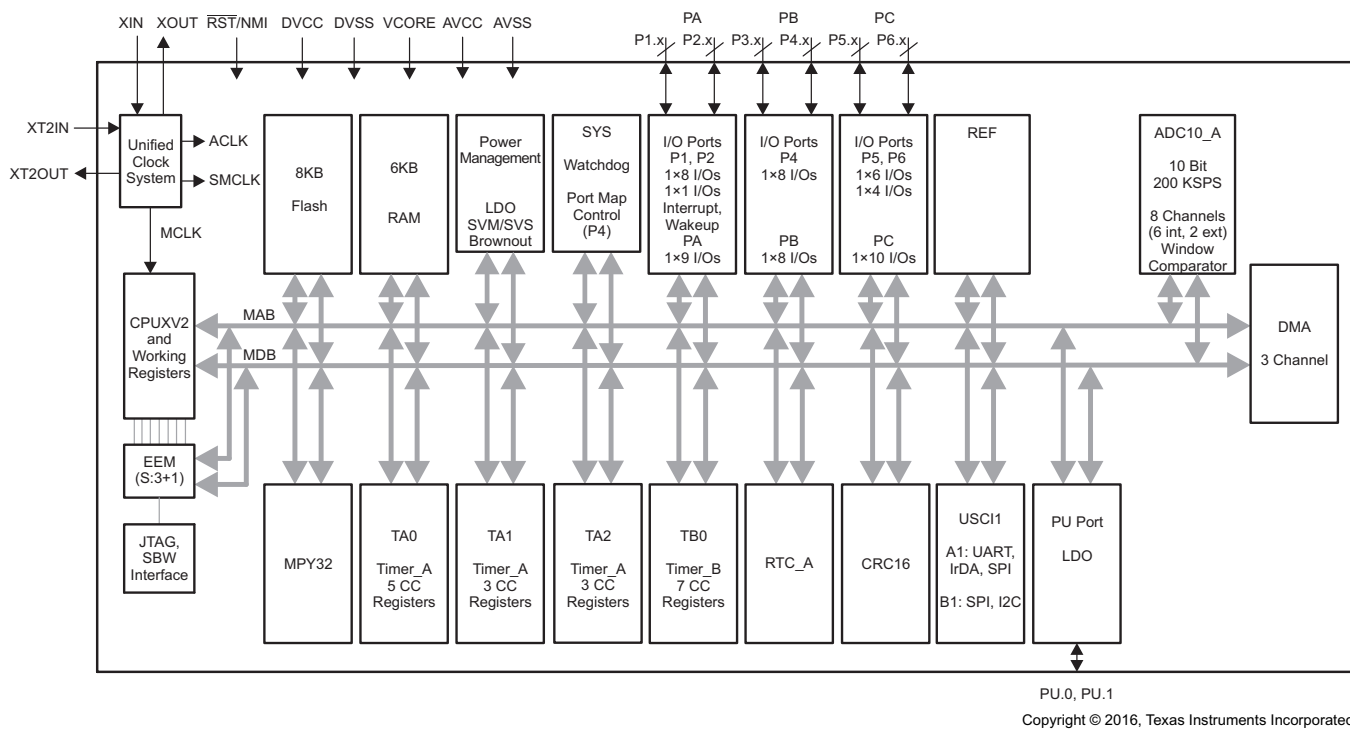


图 1-3. 功能方框图 – MSP430F5304IRGZ、MSP430F5304IPT

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2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from November 23, 2013 to September 25, 2018	Page
• 通篇更改了文档格式，其中包括更改结构并添加章节编号	1
• 添加了器件信息表	2
• 添加了节 1.4 并将所有功能方框图移到这里	2
• 更改了图 1-2 中 USCI 模块的数量并添加了注释	3
• 将图 1-3 中的 USCIO 更改成了 USC1	3
• Added Section 3, Device Comparison, and moved Table 3-1, Family Members, to it	6
• In Table 3-1, changed the number of USCI modules in the 48-pin packages from 1 to 2 and added note about limitations on simultaneous use	6
• Added Section 3.1, Related Products	6
• Changed the title of Table 4-1 from Terminal Functions to Signal Descriptions	11
• Added "with port interrupt" to P2.7 description in Table 4-1, Signal Descriptions	12
• Added "Port U is supplied by the LDOO rail" to the PU.0 and PU.1 descriptions in Table 4-1, Signal Descriptions ..	13
• Added typical conditions statements at the beginning of Section 5, Specifications	15
• Added Section 5 and moved all electrical specifications to it	15
• Added Section 5.2, ESD Ratings	15
• Moved Section 5.6, Thermal Resistance Characteristics	18
• Changed the TYP value of the $C_{L,eff}$ parameter with Test Conditions of "XTS = 0, XCAPx = 0" from 2 pF to 1 pF in Section 5.14, Crystal Oscillator, XT1, Low-Frequency Mode	22
• Changed the MIN value of the $V_{(DVCC_BOR_hys)}$ parameter from 60 mV to 50 mV in Section 5.19, PMM, Brownout Reset (BOR)	26
• Updated notes (1) and (2) and added note (3) in Section 5.25, Wake-up Times From Low-Power Modes and Reset	28
• Changed (corrected) the port pins muxed with ADC10 pins in $V_{(AX)}$ Test Conditions in Section 5.34, 10-Bit ADC, Power Supply and Input Range Conditions	34
• Removed ADC10DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Section 5.35, 10-Bit ADC, Timing Parameters, because ADC10CLK is after division	34
• Updated Test Conditions for all parameters in Section 5.36, 10-Bit ADC, Linearity Parameters: changed from " $C_{VREF+} = 20$ pF" to " $C_{VREF+} = 20$ pF"; changed from " $(V_{eREF+} - V_{eREF-})_{min} \leq (V_{eREF+} - V_{eREF-})$ " to " $1.4 V \leq (V_{eREF+} - V_{eREF-})$ "	35
• Added " $C_{VREF+} = 20$ pF" to E_I Test Conditions in Section 5.36, 10-Bit ADC, Linearity Parameters	35
• Added "ADC10SREFx = 11b" to Test Conditions for E_G and E_T in Section 5.36, 10-Bit ADC, Linearity Parameters ..	35
• Changed the MIN value of $AV_{CC(min)}$ with Test Conditions of "REFVSEL = {0}" for 1.5 V" from 2.2 V to 1.8 V in Section 5.38, REF, Built-In Reference	36
• Changed the value of CBREFACC in both Test Conditions for the I_{AVCC_REF} parameter (changed first row from 0 to 1; changed second row from 1 to 0) in Section 5.39, Comparator_B	37
• Changed the MAX value of the t_{EN_CMP} parameter with Test Conditions of "CBPWRMD = 10" from 1.5 μ s to 100 μ s in Section 5.39, Comparator_B	37
• Changed the note that starts "Tools that access the Spy-Bi-Wire and BSL interfaces..."	40
• Throughout document, changed all instances of "bootstrap loader" to "bootloader"	45
• Corrected spelling of NMIIFG in Table 6-8, System Module Interrupt Vector Registers	50
• Changed Figure 6-8, Port P5 (P5.3) Diagram, (added P5SEL.2 and XT2BYPASS inputs with AND and OR gates) ..	76
• Changed P5SEL.3 column from X to 0 for "P5.3 (I/O)" rows in Table 6-48, Port P5 (P5.2 and P5.3) Pin Functions ..	76
• Changed Figure 6-10, Port P5 (P5.5) Diagram, (added P5SEL.5 input and OR gate)	78
• Changed P5SEL.5 column from X to 0 for "P5.5 (I/O)" rows in Table 6-49, Port P5 (P5.4 and P5.5) Pin Functions ..	78
• Changed Table 6-51, Port PU.0, PU.1 Functions	81
• Added ZQE and PT packages in heading row of Table 6-53, Device Descriptors	84
• 添加了节 7, 器件和文档支持	87
• 添加了节 8 机械、封装和可订购信息	93

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Family Members⁽¹⁾⁽²⁾

DEVICE	PROGRAM MEMORY (KB)	SRAM (KB)	Timer_A ⁽³⁾	Timer_B ⁽⁴⁾	USCI		ADC10_A (CH)	Comp_B (CH)	I/Os	PACKAGE
					CHANNEL A: UART, LIN, IrDA, SPI	CHANNEL B: SPI, I ² C				
MSP430F5310	32	6	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					2 ⁽⁵⁾	2 ⁽⁵⁾	6 ext, 2 int	4	31	48 PT, 48 RGZ
MSP430F5309	24	6	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					2 ⁽⁵⁾	2 ⁽⁵⁾	6 ext, 2 int	4	31	48 PT, 48 RGZ
MSP430F5308	16	6	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					2 ⁽⁵⁾	2 ⁽⁵⁾	6 ext, 2 int	4	31	48 PT, 48 RGZ
MSP430F5304	8	6	5, 3, 3	7	1	1	6 ext, 2 int	-	31	48 PT, 48 RGZ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (5) Two USCIs are available; however, pinned out functions are limited to what the user configures on port 4 with the port mapping controller (see [Section 6.9.2](#)). It may not be possible to bring out all functions simultaneously.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Microcontrollers TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

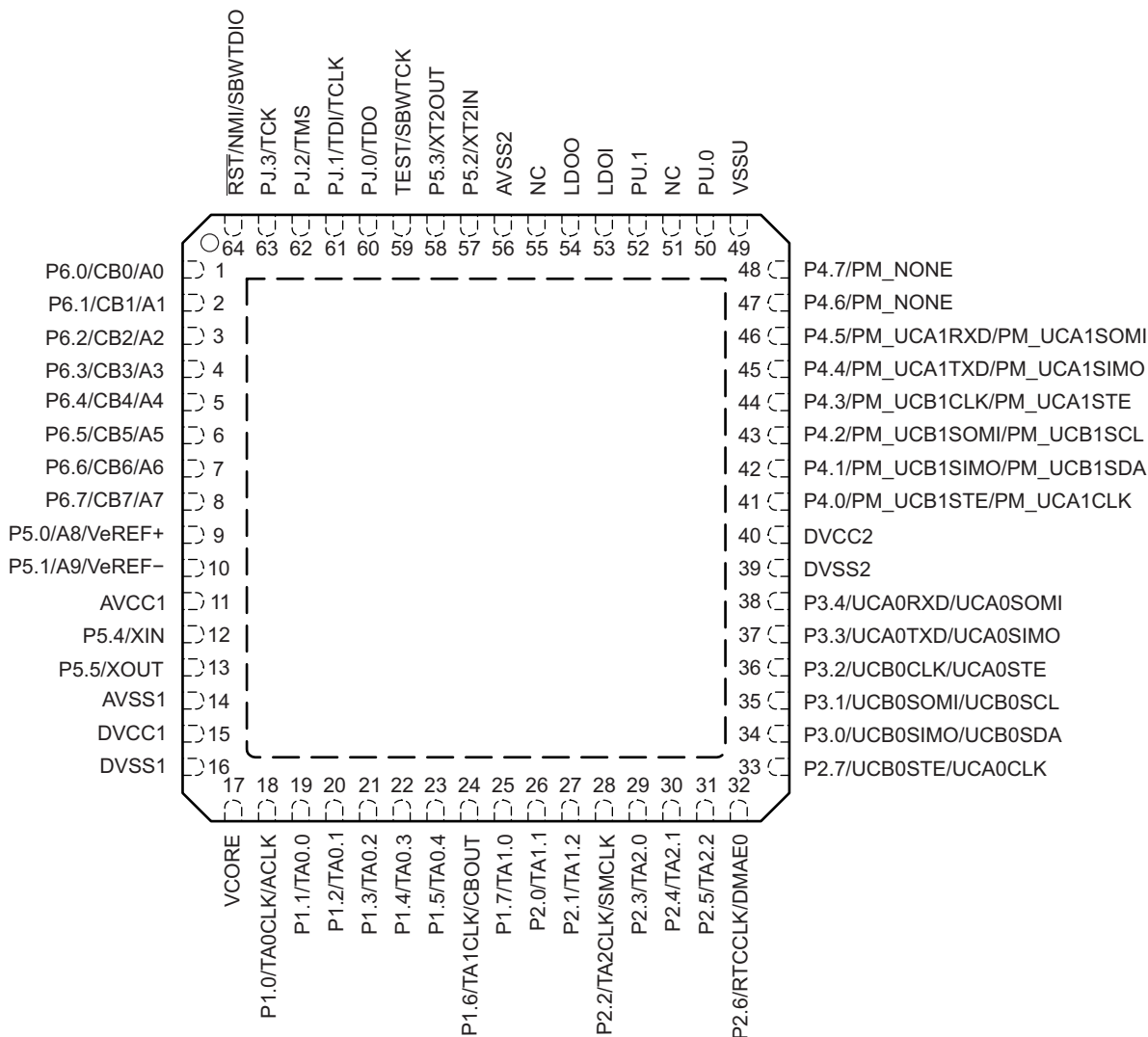
Companion Products for MSP430F5310 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for MSP430F5310 Find reference designs that leverage the best in TI technology to solve your system-level challenges.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the MSP430F5310, MSP430F5309, and MSP430F5308 devices in the 64-pin RGC package.



NOTE: TI recommends connection of exposed thermal pad to V_{SS}.

Figure 4-1. 64-Pin RGC Package (Top View)

Figure 4-2 shows the pinout for the MSP430F5310, MSP430F5309, and MSP430F5308 devices in the 80-pin ZQE package.

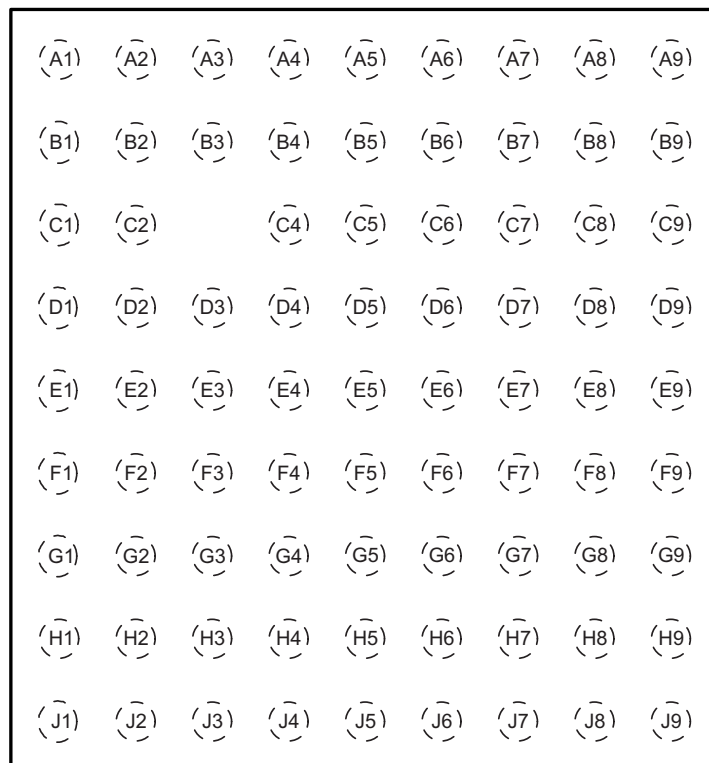
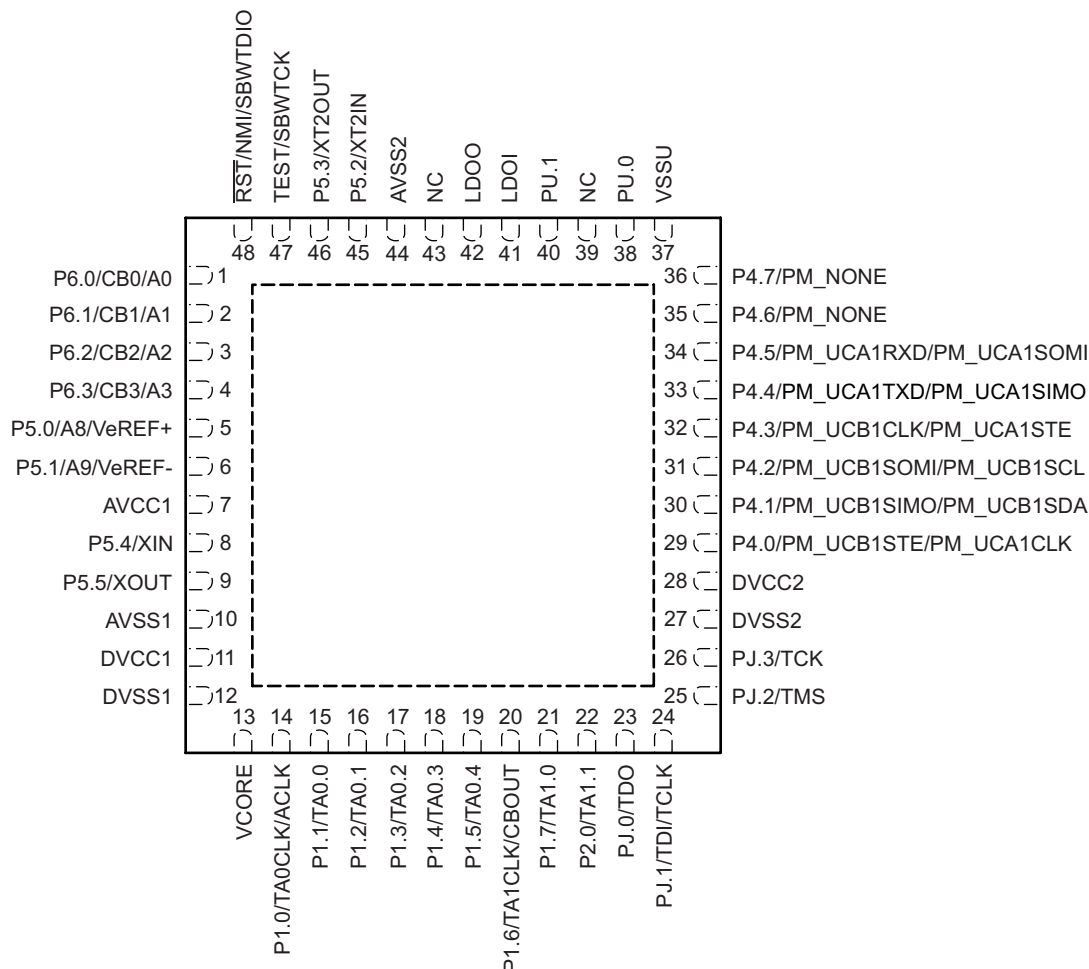


Figure 4-2. 80-Pin ZQE Package (Top View)

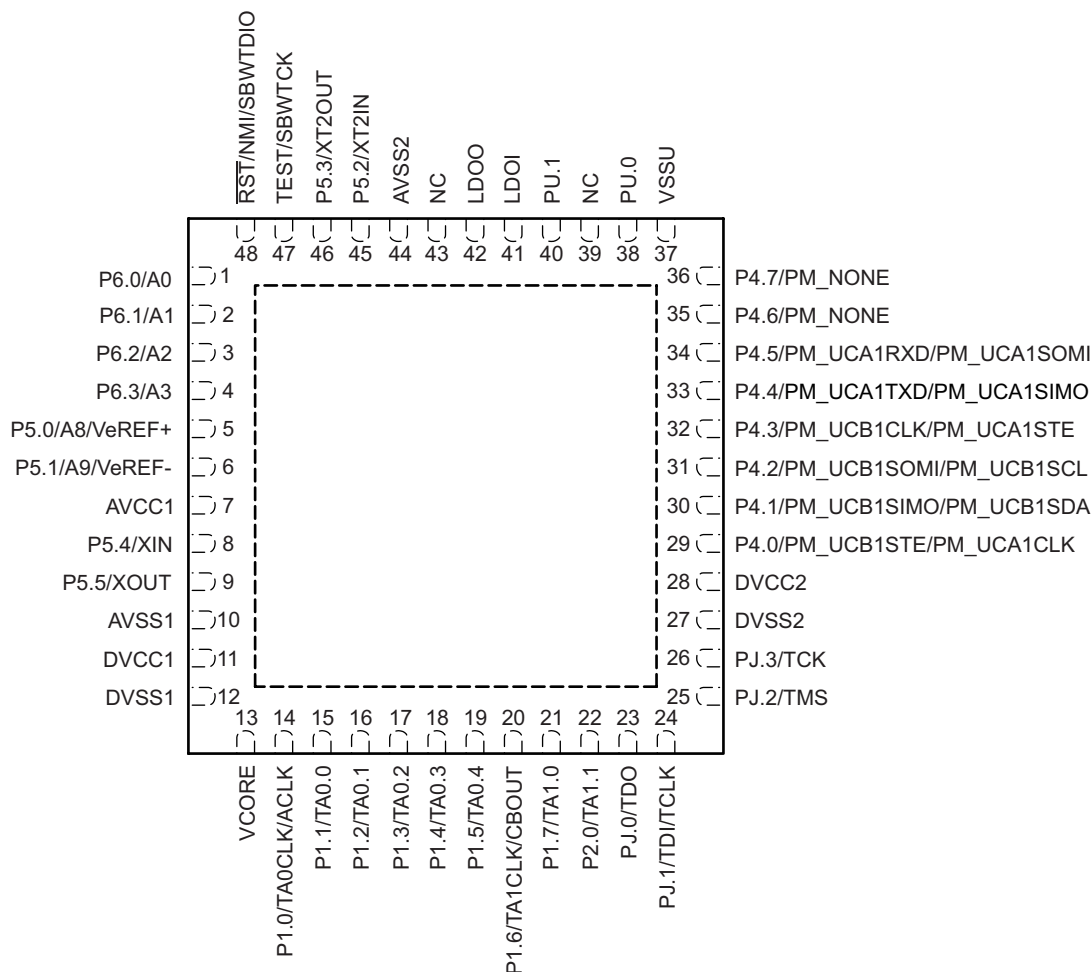
Figure 4-3 shows the pinout for the MSP430F5310, MSP430F5309, and MSP430F5308 devices in the 48-pin RGZ and PT packages.



NOTE: For the RGZ package, TI recommends connection of exposed thermal pad to V_{SS}.

Figure 4-3. 48-Pin RGZ or PT Package (Top View) – MSP430F5310, MSP430F5309, MSP430F5308

Figure 4-4 shows the pinout for the MSP430F5304 device in the 48-pin RGZ and PT packages.



NOTE: For the RGZ package, TI recommends connection of exposed thermal pad to V_{SS} .

Figure 4-4. 48-Pin RGZ or RT Package (Top View) – MSP430F5304

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

NAME	NO.			I/O ⁽¹⁾	DESCRIPTION
	RGZ	RGZ, PT	ZQE		
P6.4/CB4/A4	5	N/A	C1	I/O	General-purpose digital I/O Comparator_B input CB4 (not available on RGZ or PT package devices) Analog input A4 for ADC (not available on RGZ or PT package devices)
P6.5/CB5/A5	6	N/A	D2	I/O	General-purpose digital I/O Comparator_B input CB5 (not available on RGZ or PT package devices) Analog input A5 for ADC (not available on RGZ or PT package devices)
P6.6/CB6/A6	7	N/A	D1	I/O	General-purpose digital I/O Comparator_B input CB6 (not available on RGZ or PT package devices) Analog input A6 for ADC (not available on RGZ or PT package devices)
P6.7/CB7/A7	8	N/A	D3	I/O	General-purpose digital I/O Comparator_B input CB7 (not available on RGZ or PT package devices) Analog input A7 for ADC (not available on RGZ or PT package devices)
P5.0/A8/VeREF+	9	5	E1	I/O	General-purpose digital I/O Analog input A8 for ADC Input for an external reference voltage to the ADC
P5.1/A9/VeREF-	10	6	E2	I/O	General-purpose digital I/O Analog input A9 for ADC Negative terminal for an externally provided ADC reference
AVCC1	11	7	F2		Analog power supply
P5.4/XIN	12	8	F1	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P5.5/XOUT	13	9	G1	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS1	14	10	G2		Analog ground supply
DVCC1	15	11	H1		Digital power supply
DVSS1	16	12	J1		Digital ground supply
VCORE ⁽²⁾	17	13	J2		Regulated core power supply output (internal use only, no external current loading)
P1.0/TA0CLK/ACLK	18	14	H2	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	19	15	H3	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	20	16	J3	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	21	17	G4	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	22	18	H4	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	23	19	J4	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT	24	20	G5	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0	25	21	H5	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output

(1) I = input, O = output, N/A = not available

(2) VCore is for internal use only. No external current loading is possible. VCore should only be connected to the recommended capacitor value, C_{VCore}.

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O ⁽¹⁾	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P2.0/TA1.1	26	22	J5	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.1/TA1.2	27	N/A	G6	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.2/TA2CLK/SMCLK	28	N/A	J6	I/O	General-purpose digital I/O with port interrupt TA2 clock signal TA2CLK input ; SMCLK output
P2.3/TA2.0	29	N/A	H6	I/O	General-purpose digital I/O with port interrupt TA2 CCR0 capture: CCI0A input, compare: Out0 output
P2.4/TA2.1	30	N/A	J7	I/O	General-purpose digital I/O with port interrupt TA2 CCR1 capture: CCI1A input, compare: Out1 output
P2.5/TA2.2	31	N/A	J8	I/O	General-purpose digital I/O with port interrupt TA2 CCR2 capture: CCI2A input, compare: Out2 output
P2.6/RTCCLK/DMAE0	32	N/A	J9	I/O	General-purpose digital I/O with port interrupt RTC clock output for calibration DMA external trigger input
P2.7/UCB0STE/UCA0CLK	33	N/A	H7	I/O	General-purpose digital I/O with port interrupt Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.0/UCB0SIMO/UCB0SDA	34	N/A	H8	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I ² C data – USCI_B0 I ² C mode
P3.1/UCB0SOMI/UCB0SCL	35	N/A	H9	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I ² C clock – USCI_B0 I ² C mode
P3.2/UCB0CLK/UCA0STE	36	N/A	G8	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
P3.3/UCA0TXD/UCA0SIMO	37	N/A	G9	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.4/UCA0RXD/UCA0SOMI	38	N/A	G7	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P4.0/PM_UCB1STE/ PM_UCA1CLK	41	29	E8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	42	30	E7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I ² C data – USCI_B1 I ² C mode
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	43	31	D9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I ² C clock – USCI_B1 I ² C mode
P4.3/PM_UCB1CLK/ PM_UCA1STE	44	32	D8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode
DVSS2	39	27	F9		Digital ground supply
DVCC2	40	28	E9		Digital power supply

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O ⁽¹⁾	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	45	33	D7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	46	34	C9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode
P4.6/PM_NONE	47	35	C8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P4.7/PM_NONE	48	36	C7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
VSSU	49	37	B8, B9		PU ground supply
PU.0	50	38	A9	I/O	General-purpose digital I/O - controlled by PU control register. Port U is supplied by the LDOO rail.
NC	51	39	B7	I/O	No connect.
PU.1	52	40	A8	I/O	General-purpose digital I/O - controlled by PU control register Port U is supplied by the LDOO rail.
LDOI	53	41	A7		LDO input
LDOO	54	42	A6		LDO output
NC	55	43	B6		No connect.
AVSS2	56	44	A5		Analog ground supply
P5.2/XT2IN	57	45	B5	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	58	46	B4	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK	59	47	A4	I	Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock
PJ.0/TDO	60	23	C5	I/O	General-purpose digital I/O Test data output port
PJ.1/TDI/TCLK	61	24	C4	I/O	General-purpose digital I/O Test data input or test clock input
PJ.2/TMS	62	25	A3	I/O	General-purpose digital I/O Test mode select
PJ.3/TCK	63	26	B3	I/O	General-purpose digital I/O Test clock
$\overline{\text{RST}}$ /NMI/SBWTDIO	64	48	A2	I/O	Reset input active low ⁽³⁾ Nonmaskable interrupt input Spy-Bi-Wire data input/output
P6.0/CB0/A0	1	1	A1	I/O	General-purpose digital I/O Comparator_B input CB0 (not available on F5304 device) Analog input A0 for ADC
P6.1/CB1/A1	2	2	B2	I/O	General-purpose digital I/O Comparator_B input CB1 (not available on F5304 device) Analog input A1 for ADC
P6.2/CB2/A2	3	3	B1	I/O	General-purpose digital I/O Comparator_B input CB2 (not available on F5304 device) Analog input A2 for ADC

(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O ⁽¹⁾	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P6.3/CB3/A3	4	4	C2	I/O	General-purpose digital I/O Comparator_B input CB3 (not available on F5304 device) Analog input A3 for ADC
Reserved	N/A	N/A	(4)		
Thermal Pad	Pad	Pad	N/A		Exposed thermal pad on QFN packages. TI recommends connection to V _{SS} (not available on PT package devices).

(4) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	−0.3	4.1	V
Voltage applied to any pin (excluding V _{CORE} , LDO1) ⁽²⁾	−0.3	$V_{CC} + 0.3$	V
Diode current at any device pin		±2	mA
Maximum junction temperature, T_J		95	°C
Storage temperature, T_{stg} ⁽³⁾	−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

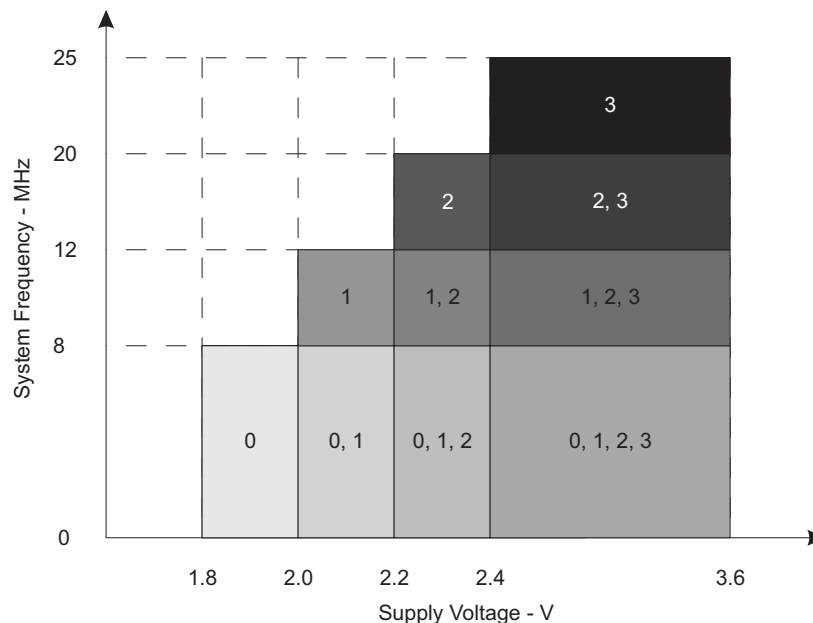
		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming ($AV_{CC} = DV_{CC1} = DV_{CC2} = V_{CC}$) ⁽¹⁾⁽²⁾	PMMCOREVx = 0	1.8	3.6	V
		PMMCOREVx = 0, 1	2.0	3.6	
		PMMCOREVx = 0, 1, 2	2.2	3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4	3.6	
V_{SS}	Supply voltage ($AV_{SS} = DV_{SS1/2} = DV_{SS}$)		0		V
T_A	Operating free-air temperature	−40		85	°C
T_J	Operating junction temperature	−40		85	°C
C_{VCORE}	Capacitor at V _{CORE} ⁽³⁾		470		nF
C_{DVCC}/C_{VCORE}	Capacitor ratio of DVCC to V _{CORE}	10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) ⁽⁴⁾ (see Figure 5-1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0	8.0	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0	12.0	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0	20.0	
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0	25.0	

- (1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the threshold parameters in [Section 5.21](#) for the exact values and further details.
- (3) A capacitor tolerance of ±20% or better is required.
- (4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Maximum System Frequency

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted) ⁽¹⁾ ⁽²⁾ ⁽³⁾

PARAMETER	EXECUTION MEMORY	V _{CC}	PMMCOREVx	FREQUENCY (f _{DCO} = f _{MCLK} = f _{SMCLK})										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{AM, Flash}	Flash	3 V	0	0.25	0.27	1.55	1.68							mA
			1	0.28		1.74		2.58	2.78					
			2	0.30		1.91		2.84		4.68	5.06			
			3	0.32		2.09		3.10		5.13		6.0	6.5	
I _{AM, RAM}	RAM	3 V	0	0.17	0.19	0.91	1.00							mA
			1	0.19		1.03		1.54	1.67					
			2	0.20		1.16		1.73		2.84	3.11			
			3	0.21		1.24		1.87		3.1		3.9	4.3	

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing. LDO disabled ($LDOEN = 0$).
 $f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
 $XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$.

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾ ⁽²⁾

PARAMETER		V _{CC}	PMMCOREVx	TEMPERATURE (T _A)								UNIT
				−40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
LPM0,1MHz	Low-power mode 0 ⁽³⁾ ⁽⁴⁾	2.2 V	0	73		77	85	80		80	97	μA
		3 V	3	79		83	92	88		95	105	
I _{LPM2}	Low-power mode 2 ⁽⁵⁾ ⁽⁴⁾	2.2 V	0	6.5		6.5	8	7.5		8	11	μA
		3 V	3	7.0		7.0	9	7.9		8.9	13	
I _{LPM3,XT1LF}	Low-power mode 3, crystal mode ⁽⁶⁾ ⁽⁴⁾	2.2 V	0	1.60		1.90		2.6		3.4		μA
			1	1.65		2.00		2.7		3.6		
			2	1.75		2.15		2.9		3.8		
		3 V	0	1.8		2.1	2.6	2.8		3.6	6.0	
			1	1.9		2.3		2.9		3.8		
			2	2.0		2.4		3.0		4.0		
			3	2.0		2.5	3.0	3.1		4.0	6.5	
I _{LPM3,VLO}	3 V	0	1.1		1.3	1.8	1.9		2.7	5.0	μA	
		1	1.1		1.4		2.0		2.8			
		2	1.2		1.5		2.1		2.9			
		3	1.3		1.5	2.0	2.2		3.0	5.5		
I _{LPM4}	Low-power mode 4 ⁽⁸⁾ ⁽⁴⁾	3 V	0	0.9		1.1	1.5	1.8		2.5	4.8	μA
			1	1.1		1.2		2.0		2.6		
			2	1.2		1.2		2.1		2.7		
			3	1.3		1.3	1.6	2.2		2.8	5.0	
I _{LPM4.5}	Low-power mode 4.5 ⁽⁹⁾	3 V		0.15		0.18	0.35	0.26		0.45	0.8	μA

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz LDO disabled (LDOEN = 0).

(4) Current for brownout, high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1-MHz operation, DCO bias generator enabled. LDO disabled (LDOEN = 0)

(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz LDO disabled (LDOEN = 0)

(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz LDO disabled (LDOEN = 0)

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz LDO disabled (LDOEN = 0)

(9) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

5.6 Thermal Resistance Characteristics⁽¹⁾

THERMAL METRIC		VALUE	UNIT	
RθJA	Junction-to-ambient thermal resistance, still air ⁽²⁾	VQFN (RGC)	30	°C/W
		VQFN (RGZ)	28.6	
		LQFP (PT)	62.8	
		BGA (ZQE)	55.5	
RθJC(TOP)	Junction-to-case (top) thermal resistance ⁽³⁾	VQFN (RGC)	15.6	°C/W
		VQFN (RGZ)	14.4	
		LQFP (PT)	18.2	
		BGA (ZQE)	21.2	
RθJC(BOTTOM)	Junction-to-case (bottom) thermal resistance ⁽⁴⁾	VQFN (RGC)	1.6	°C/W
		VQFN (RGZ)	1.6	
		LQFP (PT)	N/A	
		BGA (ZQE)	N/A	
RθJB	Junction-to-board thermal resistance ⁽⁵⁾	VQFN (RGC)	8.9	°C/W
		VQFN (RGZ)	5.5	
		LQFP (PT)	28.3	
		BGA (ZQE)	19.3	

(1) N/A = not applicable

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

5.7 Schmitt-Trigger Inputs – General-Purpose I/O⁽¹⁾

(P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7)
(P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+} Positive-going input threshold voltage		1.8 V	0.80		1.40	V
		3 V	1.50		2.10	
V _{IT-} Negative-going input threshold voltage		1.8 V	0.45		1.00	V
		3 V	0.75		1.65	
V _{hys} Input voltage hysteresis (V _{IT+} – V _{IT-})		1.8 V	0.3		0.85	V
		3 V	0.4		1.0	
R _{Pull} Pullup or pulldown resistor ⁽²⁾	For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC}		20	35	50	kΩ
C _I Input capacitance	V _{IN} = V _{SS} or V _{CC}			5		pF

(1) The same parametrics apply to the clock input pin when the crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

(2) Also applies to the RST pin when its pullup or pulldown resistor is enabled.

5.8 Inputs – Ports P1 and P2⁽¹⁾

(P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _(int) External interrupt timing ⁽²⁾	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag	2.2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

5.9 Leakage Current – General-Purpose I/O

(P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7)
(P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
I _{lkg} (P _{x.y}) High-impedance leakage current	⁽¹⁾ ⁽²⁾	1.8 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.10 Outputs – General-Purpose I/O (Full Drive Strength)

(P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH} High-level output voltage	I _(OHmax) = –3 mA ⁽¹⁾	1.8 V	V _{CC} – 0.25	V _{CC}	V
	I _(OHmax) = –10 mA ⁽²⁾		V _{CC} – 0.60	V _{CC}	
	I _(OHmax) = –5 mA ⁽¹⁾	3 V	V _{CC} – 0.25	V _{CC}	
	I _(OHmax) = –15 mA ⁽²⁾		V _{CC} – 0.60	V _{CC}	
OL Low-level output voltage	I _(OLmax) = 3 mA ⁽¹⁾	1.8 V	V _{SS}	V _{SS} + 0.25	V
	I _(OLmax) = 10 mA ⁽²⁾		V _{SS}	V _{SS} + 0.60	
	I _(OLmax) = 5 mA ⁽¹⁾	3 V	V _{SS}	V _{SS} + 0.25	
	I _(OLmax) = 15 mA ⁽²⁾		V _{SS}	V _{SS} + 0.60	

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

5.11 Outputs – General-Purpose I/O (Reduced Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH} High-level output voltage	I _(OHmax) = –1 mA ⁽²⁾	1.8 V	V _{CC} – 0.25	V _{CC}	V
	I _(OHmax) = –3 mA ⁽³⁾		V _{CC} – 0.60	V _{CC}	
	I _(OHmax) = –2 mA ⁽²⁾	3 V	V _{CC} – 0.25	V _{CC}	
	I _(OHmax) = –6 mA ⁽³⁾		V _{CC} – 0.60	V _{CC}	
V _{OL} Low-level output voltage	I _(OLmax) = 1 mA ⁽²⁾	1.8 V	V _{SS}	V _{SS} + 0.25	V
	I _(OLmax) = 3 mA ⁽³⁾		V _{SS}	V _{SS} + 0.60	
	I _(OLmax) = 2 mA ⁽²⁾	3 V	V _{SS}	V _{SS} + 0.25	
	I _(OLmax) = 6 mA ⁽³⁾		V _{SS}	V _{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.12 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f _{Px,y} Port output frequency (with load)	See ⁽¹⁾ ⁽²⁾	V _{CC} = 1.8 V PMMCOREVx = 0	16	MHz
		V _{CC} = 3 V PMMCOREVx = 3	25	
f _{Port_CLK} Clock output frequency	ACLK, SMCLK, MCLK, C _L = 20 pF ⁽²⁾	V _{CC} = 1.8 V PMMCOREVx = 0	16	MHz
		V _{CC} = 3 V PMMCOREVx = 3	25	

(1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.

(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

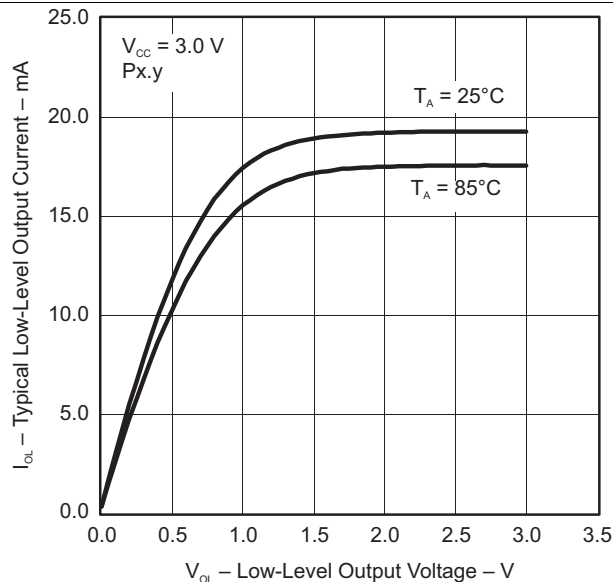


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

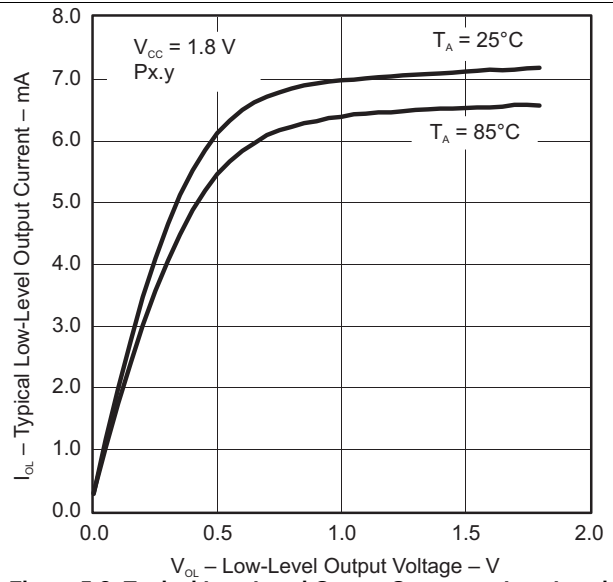


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

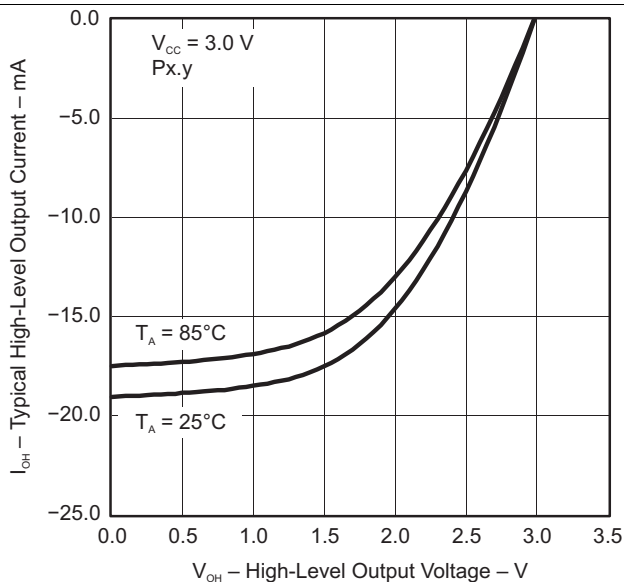


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

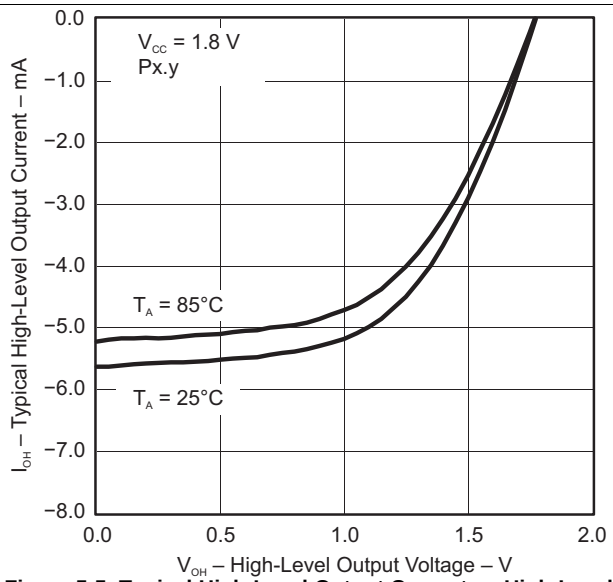


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.14 Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
ΔI _{DVCC,LF}	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C	3 V	0.075			μA
		f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C		0.170			
		f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C		0.290			
f _{XT1,LF0}	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0		32768			Hz
f _{XT1,LF,SW}	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1 ^{(2) (3)}		10	32.768	50	kHz
OA _{LF}	Oscillation allowance for LF crystals ⁽⁴⁾	XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, f _{XT1,LF} = 32768 Hz, C _{L,eff} = 6 pF		210			kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, f _{XT1,LF} = 32768 Hz, C _{L,eff} = 12 pF		300			
C _{L,eff}	Integrated effective load capacitance, LF mode ⁽⁵⁾	XTS = 0, XCAP _x = 0 ⁽⁶⁾		1			pF
		XTS = 0, XCAP _x = 1		5.5			
		XTS = 0, XCAP _x = 2		8.5			
		XTS = 0, XCAP _x = 3		12.0			
Duty cycle, LF mode		XTS = 0, Measured at ACLK, f _{XT1,LF} = 32768 Hz		30%	70%		
f _{Fault,LF}	Oscillator fault frequency, LF mode ⁽⁷⁾	XTS = 0 ⁽⁸⁾		10	10000		Hz
t _{START,LF}	Start-up time, LF mode	f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF	3 V	1000			ms
		f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF		500			

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF.
 - For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF.
 - For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF.
 - For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

5.15 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ^{(1) (2)}

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{DVCC.XT2}	XT2 oscillator crystal current consumption	f _{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C	3 V	200			μA
		f _{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 1, T _A = 25°C		260			
		f _{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C		325			
		f _{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 3, T _A = 25°C		450			
f _{XT2,HF0}	XT2 oscillator crystal frequency, mode 0	XT2DRIVE _x = 0, XT2BYPASS = 0 ⁽³⁾		4		8	MHz
f _{XT2,HF1}	XT2 oscillator crystal frequency, mode 1	XT2DRIVE _x = 1, XT2BYPASS = 0 ⁽³⁾		8		16	MHz
f _{XT2,HF2}	XT2 oscillator crystal frequency, mode 2	XT2DRIVE _x = 2, XT2BYPASS = 0 ⁽³⁾		16		24	MHz
f _{XT2,HF3}	XT2 oscillator crystal frequency, mode 3	XT2DRIVE _x = 3, XT2BYPASS = 0 ⁽³⁾		24		32	MHz
f _{XT2,HF,SW}	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1 ⁽⁴⁾ ⁽³⁾		0.7		32	MHz
O _{AHF}	Oscillation allowance for HF crystals ⁽⁵⁾	XT2DRIVE _x = 0, XT2BYPASS = 0, f _{XT2,HF0} = 6 MHz, C _{L,eff} = 15 pF		450			Ω
		XT2DRIVE _x = 1, XT2BYPASS = 0, f _{XT2,HF1} = 12 MHz, C _{L,eff} = 15 pF		320			
		XT2DRIVE _x = 2, XT2BYPASS = 0, f _{XT2,HF2} = 20 MHz, C _{L,eff} = 15 pF		200			
		XT2DRIVE _x = 3, XT2BYPASS = 0, f _{XT2,HF3} = 32 MHz, C _{L,eff} = 15 pF		200			
t _{START,HF}	Start-up time	f _{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF	3 V	0.5			ms
		f _{OSC} = 20 MHz XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C, C _{L,eff} = 15 pF		0.3			
C _{L,eff}	Integrated effective load capacitance, HF mode ⁽⁶⁾ ⁽¹⁾			1			pF
	Duty cycle	Measured at ACLK, f _{XT2,HF2} = 20 MHz		40%	50%	60%	
f _{FAULT,HF}	Oscillator fault frequency ⁽⁷⁾	XT2BYPASS = 1 ⁽⁸⁾		30		300	kHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the [Schmitt-Trigger Inputs](#) section of this data sheet.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

5.16 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df _{VLO} /dT	VLO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.5		%/°C
df _{VLO} /dV _{CC}	VLO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.17 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{REFO}	REFO oscillator current consumption	T _A = 25°C	1.8 V to 3.6 V		3		μA
f _{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5%	
		T _A = 25°C	3 V			±1.5%	
df _{REFO} /dT	REFO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.01		%/°C
df _{REFO} /dV _{CC}	REFO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t _{START}	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		μs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.18 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$ DCO frequency (0, 0) ⁽¹⁾	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$ DCO frequency (0, 31) ⁽¹⁾	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$ DCO frequency (1, 0) ⁽¹⁾	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$ DCO frequency (1, 31) ⁽¹⁾	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$ DCO frequency (2, 0) ⁽¹⁾	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$ DCO frequency (2, 31) ⁽¹⁾	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$ DCO frequency (3, 0) ⁽¹⁾	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$ DCO frequency (3, 31) ⁽¹⁾	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$ DCO frequency (4, 0) ⁽¹⁾	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$ DCO frequency (4, 31) ⁽¹⁾	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$ DCO frequency (5, 0) ⁽¹⁾	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$ DCO frequency (5, 31) ⁽¹⁾	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$ DCO frequency (6, 0) ⁽¹⁾	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$ DCO frequency (6, 31) ⁽¹⁾	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$ DCO frequency (7, 0) ⁽¹⁾	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$ DCO frequency (7, 31) ⁽¹⁾	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$ Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO} Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
Duty cycle	Measured at SMCLK	40%	50%	60%	
df_{DCO}/dT DCO frequency temperature drift ⁽²⁾	$f_{DCO} = 1$ MHz,		0.1		%/°C
df_{DCO}/dV_{CC} DCO frequency voltage drift ⁽³⁾	$f_{DCO} = 1$ MHz		1.9		%/V

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n,0),MAX} \leq f_{DCO} \leq f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.
- (2) Calculated using the box method: $(MAX(-40^{\circ}C \text{ to } 85^{\circ}C) - MIN(-40^{\circ}C \text{ to } 85^{\circ}C)) / MIN(-40^{\circ}C \text{ to } 85^{\circ}C) / (85^{\circ}C - (-40^{\circ}C))$
- (3) Calculated using the box method: $(MAX(1.8 \text{ V to } 3.6 \text{ V}) - MIN(1.8 \text{ V to } 3.6 \text{ V})) / MIN(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

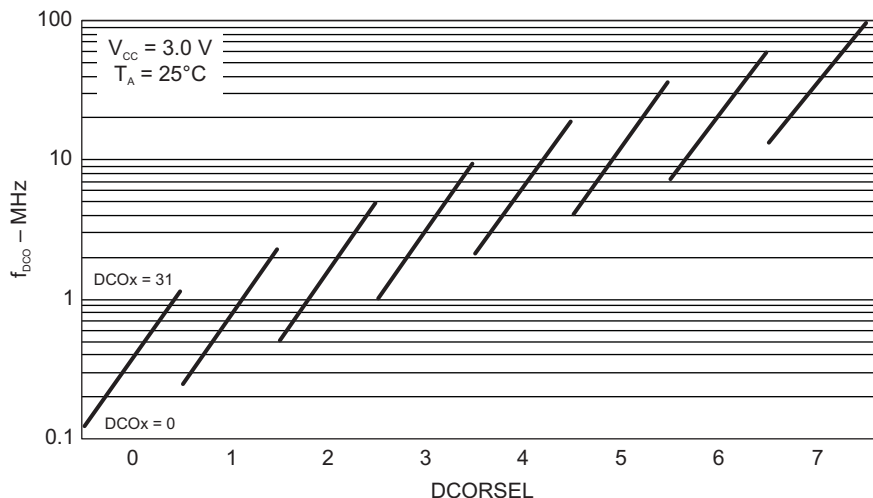


Figure 5-6. Typical DCO Frequency

5.19 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DVCC_BOR_IT-)}$ BOR _H on voltage, DV _{CC} falling level	$ dDV_{CC}/dt < 3 \text{ V/s}$			1.45	V
$V_{(DVCC_BOR_IT+)}$ BOR _H off voltage, DV _{CC} rising level	$ dDV_{CC}/dt < 3 \text{ V/s}$	0.80	1.30	1.50	V
$V_{(DVCC_BOR_hys)}$ BOR _H hysteresis		50		250	mV
t_{RESET} Pulse duration required at $\overline{RST}/NMI$ pin to accept a reset		2			μs

5.20 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CORE3(AM)}$ Core voltage, active mode, PMMCOREV = 3	$2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.90		V
$V_{CORE2(AM)}$ Core voltage, active mode, PMMCOREV = 2	$2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.80		V
$V_{CORE1(AM)}$ Core voltage, active mode, PMMCOREV = 1	$2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.60		V
$V_{CORE0(AM)}$ Core voltage, active mode, PMMCOREV = 0	$1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.40		V
$V_{CORE3(LPM)}$ Core voltage, low-current mode, PMMCOREV = 3	$2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.94		V
$V_{CORE2(LPM)}$ Core voltage, low-current mode, PMMCOREV = 2	$2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.84		V
$V_{CORE1(LPM)}$ Core voltage, low-current mode, PMMCOREV = 1	$2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.64		V
$V_{CORE0(LPM)}$ Core voltage, low-current mode, PMMCOREV = 0	$1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.44		V

5.21 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$ SVS current consumption	SVSHE = 0, DV _{CC} = 3.6 V		0		nA
	SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 0		200		
	SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 1		1.5		μA
$V_{(SVSH_IT-)}$ SVS _H on voltage level ⁽¹⁾	SVSHE = 1, SVSHRVL = 0	1.57	1.68	1.78	V
	SVSHE = 1, SVSHRVL = 1	1.79	1.88	1.98	
	SVSHE = 1, SVSHRVL = 2	1.98	2.08	2.21	
	SVSHE = 1, SVSHRVL = 3	2.10	2.18	2.31	
$V_{(SVSH_IT+)}$ SVS _H off voltage level ⁽¹⁾	SVSHE = 1, SVSMHRRRL = 0	1.62	1.74	1.85	V
	SVSHE = 1, SVSMHRRRL = 1	1.88	1.94	2.07	
	SVSHE = 1, SVSMHRRRL = 2	2.07	2.14	2.28	
	SVSHE = 1, SVSMHRRRL = 3	2.20	2.30	2.42	
	SVSHE = 1, SVSMHRRRL = 4	2.32	2.40	2.55	
	SVSHE = 1, SVSMHRRRL = 5	2.52	2.70	2.88	
	SVSHE = 1, SVSMHRRRL = 6	2.90	3.10	3.23	
	SVSHE = 1, SVSMHRRRL = 7	2.90	3.10	3.23	
$t_{pd(SVSH)}$ SVS _H propagation delay	SVSHE = 1, $dV_{DVCC}/dt = 10 \text{ mV}/\mu\text{s}$, SVSHFP = 1		2.5		μs
	SVSHE = 1, $dV_{DVCC}/dt = 1 \text{ mV}/\mu\text{s}$, SVSHFP = 0		20		
$t_{(SVSH)}$ SVS _H on or off delay time	SVSHE = 0 → 1, SVSHFP = 1		12.5		μs
	SVSHE = 0 → 1, SVSHFP = 0		100		
dV_{DVCC}/dt DV _{CC} rise time		0		1000	V/s

(1) The SVS_H settings that are available depend on the VCORE (PMMCOREVx) setting. See the *Power-Management Module and Supply Voltage Supervisor* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) for recommended settings and use.

5.22 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$ SVM _H current consumption	SVMHE = 0, DV _{CC} = 3.6 V		0		nA
	SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0		200		
	SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1		1.5		μA
$V_{(SVMH)}$ SVM _H on or off voltage level ⁽¹⁾	SVMHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
	SVMHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
	SVMHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
	SVMHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
	SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
	SVMHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
	SVMHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
	SVMHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
$t_{pd(SVMH)}$ SVM _H propagation delay	SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1		2.5		μs
	SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0		20		
$t_{(SVMH)}$ SVM _H on or off delay time	SVMHE = 0 → 1, SVMHFP = 1		12.5		μs
	SVMHE = 0 → 1, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the V_{CORE} (PMMCOREVx) setting. See the *Power-Management Module and Supply Voltage Supervisor* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) on recommended settings and use.

5.23 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$ SVS _L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
	SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		
	SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		2.0		μA
$t_{pd(SVSL)}$ SVS _L propagation delay	SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1		2.5		μs
	SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0		20		
$t_{(SVSL)}$ SVS _L on or off delay time	SVSLE = 0 → 1, SVSLFP = 1		12.5		μs
	SVSLE = 0 → 1, SVSLFP = 0		100		

5.24 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$ SVM _L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
	SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		
	SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		1.5		μA
$t_{pd(SVML)}$ SVM _L propagation delay	SVMLE = 1, dV _{CORE} /dt = 10 mV/μs, SVMLFP = 1		2.5		μs
	SVMLE = 1, dV _{CORE} /dt = 1 mV/μs, SVMLFP = 0		20		
$t_{(SVML)}$ SVM _L on or off delay time	SVMLE = 0 → 1, SVMLFP = 1		12.5		μs
	SVMLE = 0 → 1, SVMLFP = 0		100		

5.25 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{WAKE-UP-FAST}	Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	f _{MCLK} ≥ 4.0 MHz		5	μs
			f _{MCLK} < 4.0 MHz		6	
t _{WAKE-UP-SLOW}	Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽²⁾⁽³⁾	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0		150	165	μs
t _{WAKE-UP-LPM5}	Wake-up time from LPM4.5 to active mode ⁽⁴⁾			2	3	ms
t _{WAKE-UP-RESET}	Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽⁴⁾			2	3	ms

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVSL) and low-side monitor (SVM_L). t_{WAKE-UP-FAST} is possible with SVSL and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVSL) and low-side monitor (SVM_L). t_{WAKE-UP-SLOW} is set with SVSL and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
- (4) This value represents the time from the wake-up event to the reset vector execution.

5.26 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
t _{TA,cap}	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V, 3 V	20		ns

5.27 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
t _{TB,cap}	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20		ns

5.28 USCI (UART Mode) Clock Frequency

PARAMETER	CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{USCI} USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		f _{SYSTEM}		MHz
f _{BITCLK} BITCLK clock frequency (equals baud rate in MBaud)			1		MHz

5.29 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	V _{CC}	MIN	MAX	UNIT
t _r UART receive deglitch time ⁽¹⁾	2.2 V	50	600	ns
	3 V	50	600	

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.30 USCI (SPI Master Mode) Clock Frequency

PARAMETER	CONDITIONS	MIN	MAX	UNIT
f _{USCI} USCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%	f _{SYSTEM}		MHz

5.31 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

(see [Figure 5-7](#) and [Figure 5-8](#))

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{USCI} USCI input clock frequency	SMCLK or ACLK, Duty cycle = 50% ±10%		f _{SYSTEM}		MHz
t _{SU,MI} SOMI input data setup time	PMMCOREV = 0	1.8 V	55		ns
		3 V	38		
	PMMCOREV = 3	2.4 V	30		
		3 V	25		
t _{HD,MI} SOMI input data hold time	PMMCOREV = 0	1.8 V	0		ns
		3 V	0		
	PMMCOREV = 3	2.4 V	0		
		3 V	0		
t _{VALID,MO} SIMO output data valid time ⁽²⁾	UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 0	1.8 V		20	ns
		3 V		18	
	UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 3	2.4 V		16	
		3 V		15	
t _{HD,MO} SIMO output data hold time ⁽³⁾	C _L = 20 pF, PMMCOREV = 0	1.8 V	–10		ns
		3 V	–8		
	C _L = 20 pF, PMMCOREV = 3	2.4 V	–10		
		3 V	–8		

- (1) f_{UCXCLK} = 1/2t_{LO/HI} with t_{LO/HI} ≥ max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))
For the slave parameters t_{SU,SI}(Slave) and t_{VALID,SO}(Slave), see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-7](#) and [Figure 5-8](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 5-7](#) and [Figure 5-8](#).

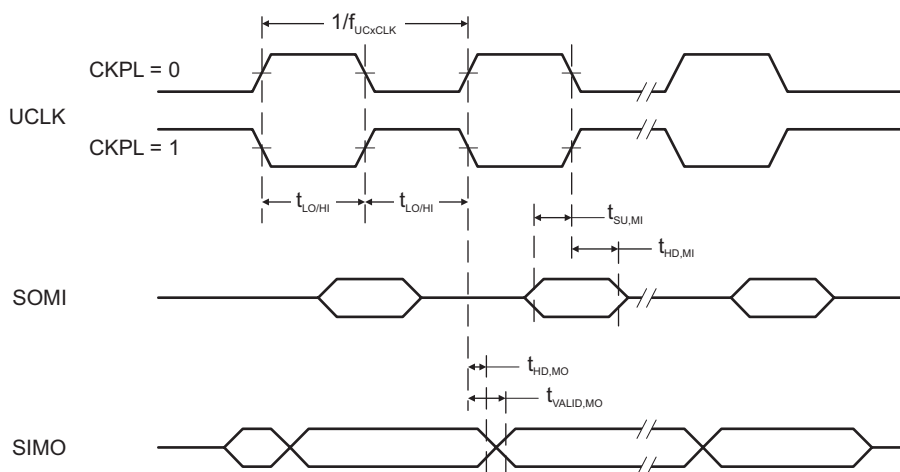


Figure 5-7. SPI Master Mode, CKPH = 0

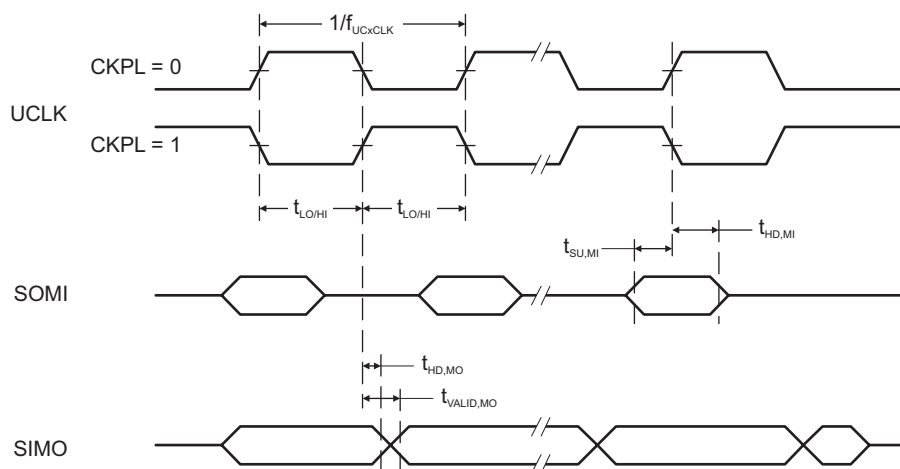


Figure 5-8. SPI Master Mode, CKPH = 1

5.32 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 5-9](#) and [Figure 5-10](#))

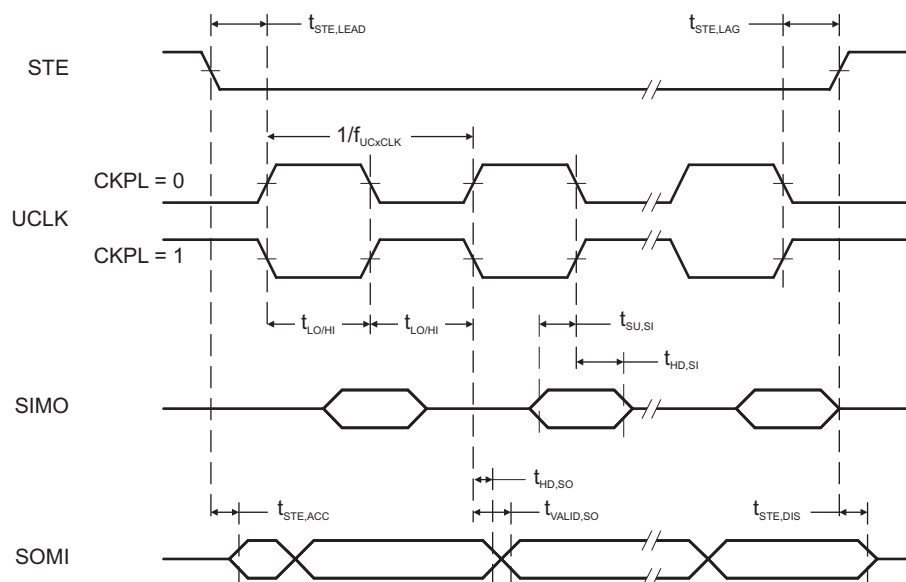
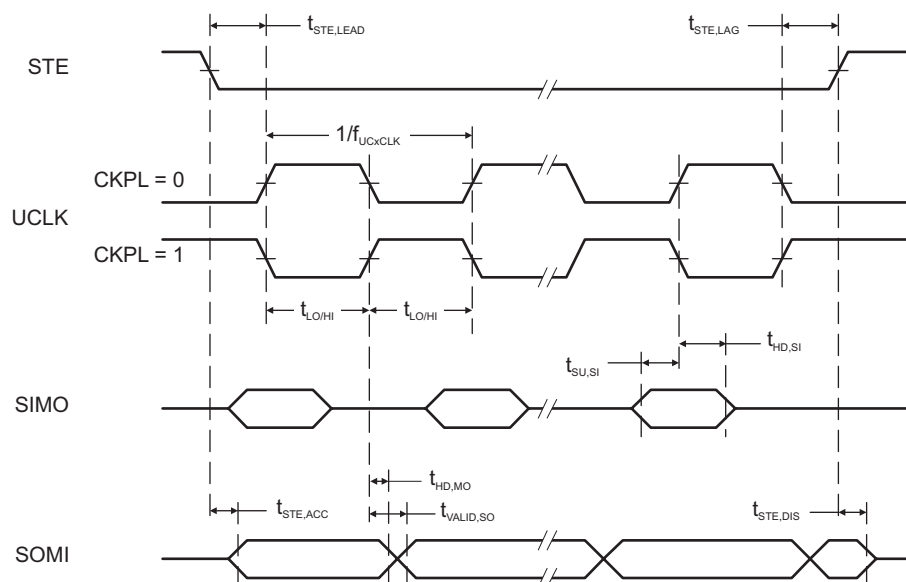
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$ STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11		ns
		3 V	8		
	PMMCOREV = 3	2.4 V	7		
		3 V	6		
$t_{STE,LAG}$ STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3		ns
		3 V	3		
	PMMCOREV = 3	2.4 V	3		
		3 V	3		
$t_{STE,ACC}$ STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V		66	ns
		3 V		50	
	PMMCOREV = 3	2.4 V		36	
		3 V		30	
$t_{STE,DIS}$ STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V		30	ns
		3 V		23	
	PMMCOREV = 3	2.4 V		16	
		3 V		13	
$t_{SU,SI}$ SIMO input data setup time	PMMCOREV = 0	1.8 V	5		ns
		3 V	5		
	PMMCOREV = 3	2.4 V	2		
		3 V	2		
$t_{HD,SI}$ SIMO input data hold time	PMMCOREV = 0	1.8 V	5		ns
		3 V	5		
	PMMCOREV = 3	2.4 V	5		
		3 V	5		
$t_{VALID,SO}$ SOMI output data valid time ⁽²⁾	UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 0	1.8 V		76	ns
		3 V		60	
	UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 3	2.4 V		44	
		3 V		40	
$t_{HD,SO}$ SOMI output data hold time ⁽³⁾	C _L = 20 pF, PMMCOREV = 0	1.8 V	18		ns
		3 V	12		
	C _L = 20 pF, PMMCOREV = 3	2.4 V	10		
		3 V	8		

(1) $f_{UCXCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$

For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-9](#) and [Figure 5-10](#).

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-9](#) and [Figure 5-10](#).

**Figure 5-9. SPI Slave Mode, CKPH = 0****Figure 5-10. SPI Slave Mode, CKPH = 1**

5.33 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-11](#))

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{USCI} USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		f _{SYSTEM}		MHz
f _{SCL} SCL clock frequency		2.2 V, 3 V	0	400	kHz
t _{HD,STA} Hold time (repeated) START	f _{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		μs
	f _{SCL} > 100 kHz		0.6		
t _{SU,STA} Setup time for a repeated START	f _{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7		μs
	f _{SCL} > 100 kHz		0.6		
t _{HD,DAT} Data hold time		2.2 V, 3 V	0		ns
t _{SU,DAT} Data setup time		2.2 V, 3 V	250		ns
t _{SU,STO} Setup time for STOP	f _{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		μs
	f _{SCL} > 100 kHz		0.6		
t _{SP} Pulse duration of spikes suppressed by input filter		2.2 V	50	600	ns
		3 V	50	600	

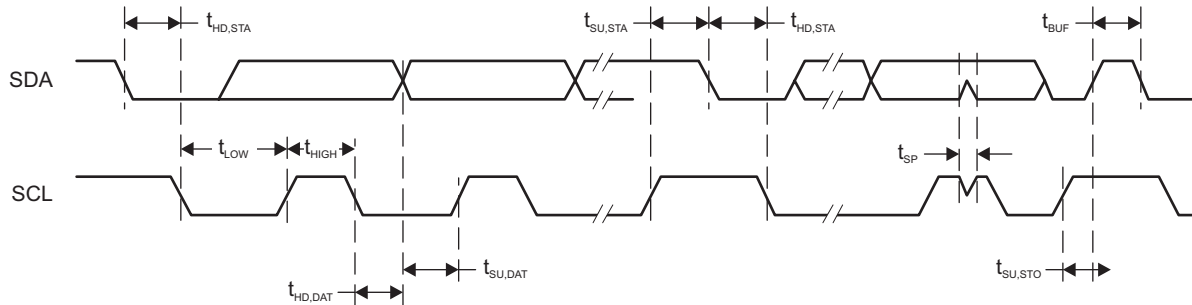


Figure 5-11. I²C Mode Timing

5.34 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
AV _{CC}	Analog supply voltage	AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V		1.8		3.6	V
V _(Ax)	Analog input voltage range ⁽²⁾	All ADC10_A pins: P6.0 to P6.7, P5.0, and P5.1 terminals		0		AV _{CC}	V
I _{ADC10_A}	Operating supply current into AVCC terminal. REF module and reference buffer off.	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00	2.2 V		60	100	μA
			3 V		75	110	
	Operating supply current into AVCC terminal. REF module on, reference buffer on.	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01	3 V		113	150	
	Operating supply current into AVCC terminal. REF module off, reference buffer on.	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V	3 V		105	140	
	Operating supply current into AVCC terminal. REF module off, reference buffer off.	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V	3 V		70	110	
C _I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad.	2.2 V		3.5		pF
R _I	Input MUX ON resistance	AV _{CC} > 2.0 V, 0 V ≤ V _{Ax} ≤ AV _{CC}				36	kΩ
		1.8 V < AV _{CC} < 2.0 V, 0 V ≤ V _{Ax} ≤ AV _{CC}				96	

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 μF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. See also the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

5.35 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{ADC10CLK}		For specified performance of ADC10_A linearity parameters	2.2 V, 3 V	0.45	5	5.5	MHz
f _{ADC10OSC}	Internal ADC10_A oscillator ⁽¹⁾	ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC}	2.2 V, 3 V	4.2	4.8	5.4	MHz
t _{CONVERT}	Conversion time	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, f _{ADC10OSC} = 4 MHz to 5 MHz	2.2 V, 3 V	2.4		3.0	μs
		External f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0			12 × 1 / f _{ADC10CLK}		
t _{ADC10ON}	Turnon settling time of the ADC	See ⁽²⁾				100	ns
t _{Sample}	Sampling time	R _S = 1000 Ω, R _I = 96 kΩ, C _I = 3.5 pF ⁽³⁾	1.8 V	3			μs
		R _S = 1000 Ω, R _I = 36 kΩ, C _I = 3.5 pF ⁽³⁾	3 V	1			μs

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.

(2) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

(3) Approximately 8 Tau (τ) are required for an error of less than ±0.5 LSB

5.36 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
E _I Integral linearity error	1.4 V ≤ (V _{eREF+} – V _{eREF–}) ≤ 1.6 V, C _{VeREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
	1.6 V < (V _{eREF+} – V _{eREF–}) ≤ V _{AVCC} , C _{VeREF+} = 20 pF				±1.0	
E _D Differential linearity error	1.4 V ≤ (V _{eREF+} – V _{eREF–}), C _{VeREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
E _O Offset error	1.4 V ≤ (V _{eREF+} – V _{eREF–}), C _{VeREF+} = 20 pF, Internal impedance of source R _S < 100 Ω	2.2 V, 3 V			±1.0	LSB
E _G Gain error	1.4 V ≤ (V _{eREF+} – V _{eREF–}), C _{VeREF+} = 20 pF, ADC10SREFX = 11b	2.2 V, 3 V			±1.0	LSB
E _T Total unadjusted error	1.4 V ≤ (V _{eREF+} – V _{eREF–}), C _{VeREF+} = 20 pF, ADC10SREFX = 11b	2.2 V, 3 V		±1.0	±2.0	LSB

5.37 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{eREF+} Positive external reference voltage input	V _{eREF+} > V _{eREF–} ⁽²⁾		1.4		V _{AVCC}	V
V _{eREF–} Negative external reference voltage input	V _{eREF+} > V _{eREF–} ⁽³⁾		0		1.2	V
(V _{eREF+} – V _{eREF–}) Differential external reference voltage input	V _{eREF+} > V _{eREF–} ⁽⁴⁾		1.4		V _{AVCC}	V
I _{VeREF+} I _{VeREF–} Static input current	1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF–} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x0001, Conversion rate 200 kpsps	2.2 V, 3 V		±8.5	±26	μA
	1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF–} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 kpsps				±1	
C _{VeREF+/-} Capacitance at VeREF+ or VeREF- terminal	(5)		10			μF

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. See also the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

5.38 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{REF+}	REFVSEL = {2} for 2.5 V, REFON = 1	3 V	2.51	±1.5%		V
	REFVSEL = {1} for 2.0 V, REFON = 1	3 V	1.99	±1.5%		
	REFVSEL = {0} for 1.5 V, REFON = 1	2.2 V, 3 V	1.5	±1.5%		
AV _{CC(min)}	REFVSEL = {0} for 1.5 V		1.8			V
	REFVSEL = {1} for 2.0 V		2.2			
	REFVSEL = {2} for 2.5 V		2.7			
I _{REF+}	f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V	3 V	18	24		μA
	f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V	3 V	15.5	21		
	f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V	3 V	13.5	21		
TC _{REF+}	I _{VREF+} = 0 A, REFVSEL = {0, 1, 2}, REFON = 1		30	50		ppm/°C
I _{SENSOR}	REFON = 0, INCH = 0Ah, ADC10ON = NA, T _A = 30°C	2.2 V	20	22		μA
		3 V	20	22		
V _{SENSOR}	ADC10ON = 1, INCH = 0Ah, T _A = 30°C	2.2 V	770			mV
		3 V	770			
V _{MID}	ADC10ON = 1, INCH = 0Bh, V _{MID} ≈ 0.5 × V _{AVCC}	2.2 V	1.06	1.1	1.14	V
		3 V	1.46	1.5	1.54	
t _{SENSOR(sample)}	ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB		30			μs
t _{VMID(sample)}	ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB		1			μs
PSRR _{DC}	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1		120			μV/V
PSRR _{AC}	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1		6.4			mV/V
t _{SETTLE}	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 0 → 1		75			μs

- (1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
- (2) The internal reference current is supplied through the AVCC terminal. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
- (3) Calculated using the box method: (MAX(−40°C to 85°C) − MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C − (−40°C)).
- (4) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
- (5) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
- (7) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.
- (8) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.39 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage			1.8		3.6	V
I _{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00, CBON = 1, CBRStx = 00	1.8 V			40	μA
			2.2 V		30	50	
			3 V		40	65	
		CBPWRMD = 01, CBON = 1, CBRStx = 00	2.2 V, 3 V		10	17	
		CBPWRMD = 10, CBON = 1, CBRStx = 00	2.2 V, 3 V		0.1	0.5	
I _{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Including REF module current	CBREFACC = 1, CBREFLx = 01, CBRStx = 10, REFON = 0, CBON = 0	2.2 V, 3 V		10	17	μA
		CBREFACC = 0, CBREFLx = 01, CBRStx = 10, REFON = 0, CBON = 0	2.2 V, 3 V			22	
V _{IC}	Common mode input range			0		V _{CC} – 1	V
V _{OFFSET}	Input offset voltage	CBPWRMD = 00				±20	mV
		CBPWRMD = 01, 10				±10	
C _{IN}	Input capacitance				5		pF
R _{SIN}	Series input resistance	On (switch closed)			3	4	kΩ
		Off (switch open)		50			MΩ
t _{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	
		CBPWRMD = 10, CBF = 0				50	μs
t _{PD,filter}	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.0	μs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	
t _{EN_CMP}	Comparator enable time	CBON = 0 to CBON = 1, CBPWRMD = 00, 01			1	2	μs
		CBON = 0 to CBON = 1, CBPWRMD = 10				100	
t _{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			1	1.5	μs
V _{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

5.40 Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH} High-level output voltage	$V_{LDOO} = 3.3 \text{ V} \pm 10\%$, $I_{OH} = -25 \text{ mA}$, See Figure 5-13 for typical characteristics	2.4		V
V_{OL} Low-level output voltage	$V_{LDOO} = 3.3 \text{ V} \pm 10\%$, $I_{OL} = 25 \text{ mA}$, See Figure 5-12 for typical characteristics		0.4	V
V_{IH} High-level input voltage	$V_{LDOO} = 3.3 \text{ V} \pm 10\%$, See Figure 5-14 for typical characteristics	2.0		V
V_{IL} Low-level input voltage	$V_{LDOO} = 3.3 \text{ V} \pm 10\%$, See Figure 5-14 for typical characteristics		0.8	V

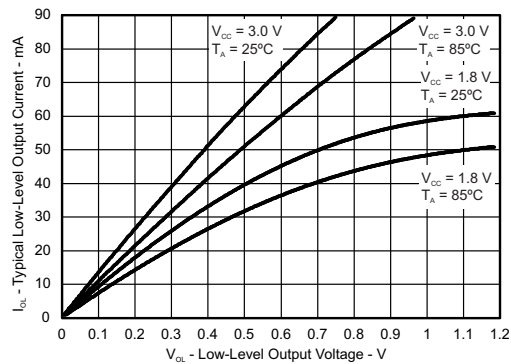


Figure 5-12. Ports PU.0, PU.1 Typical Low-Level Output Characteristics

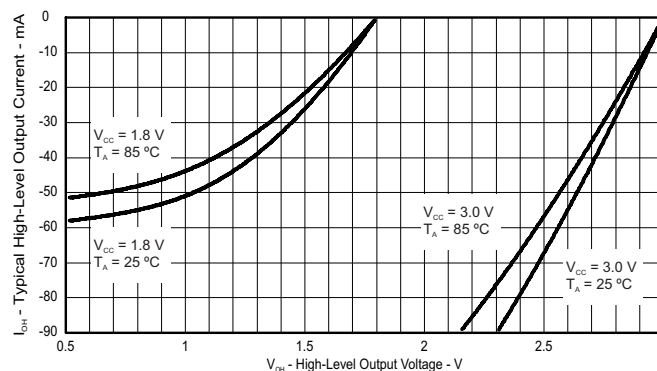


Figure 5-13. Ports PU.0, PU.1 Typical High-Level Output Characteristics

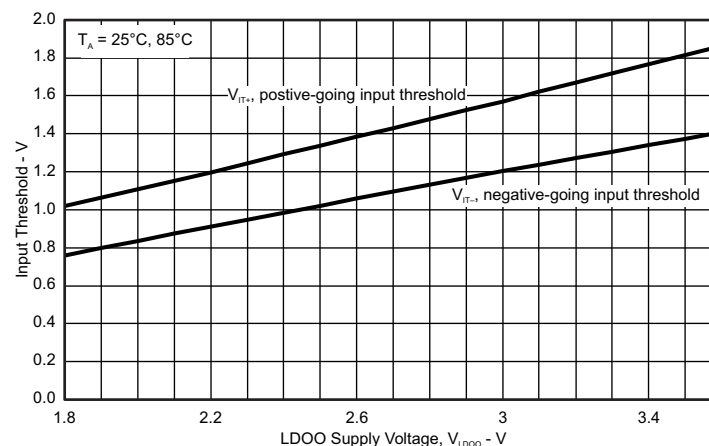


Figure 5-14. Ports PU.0, PU.1 Typical Input Threshold Characteristics

5.41 LDO-PWR (LDO Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{LAUNCH}	LDO input detection threshold				3.75	V
V _{LDOI}	LDO input voltage		3.76		5.5	V
V _{LDO}	LDO output voltage			3.3	±9%	V
V _{LDO_EXT}	LDOO terminal input voltage with LDO disabled	LDO disabled	1.8		3.6	V
I _{LDOO}	Maximum external current from LDOO terminal	LDO is on			20	mA
I _{DET}	LDO current overload detection ⁽¹⁾		60		100	mA
C _{LDOI}	LDOI terminal recommended capacitance			4.7		μF
C _{LDOO}	LDOO terminal recommended capacitance			220		nF
t _{ENABLE}	Settling time V _{LDO}	Within 2%, recommended capacitances			2	ms

(1) A current overload will be detected when the total current supplied from the LDO exceeds this value.

5.42 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T _J	MIN	TYP	MAX	UNIT
DV _{CC(PGM/ERASE)}	Program or erase supply voltage		1.8		3.6	V
t _{READMARGIN}	Read access time during margin mode				200	ns
I _{PGM}	Supply current from DV _{CC} during program			3	5	mA
I _{ERASE}	Supply current from DV _{CC} during erase			2	6.5	mA
I _{MERASE} , I _{BANK}	Supply current from DV _{CC} during mass erase or bank erase			2	6.5	mA
t _{CPT}	Cumulative program time ⁽¹⁾				16	ms
	Program and erase endurance		10 ⁴	10 ⁵		cycles
t _{Retention}	Data retention duration	25°C	100			years
t _{Word}	Word or byte program time ⁽²⁾		64		85	μs
t _{Block, 0}	Block program time for first byte or word ⁽²⁾		49		65	μs
t _{Block, 1–(N–1)}	Block program time for each additional byte or word, except for last byte or word ⁽²⁾		37		49	μs
t _{Block, N}	Block program time for last byte or word ⁽²⁾		55		73	μs
t _{Erase}	Erase time for segment, mass erase, and bank erase when available ⁽²⁾		23		32	ms

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) These values are hardwired into the state machine of the flash controller.

5.43 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	MIN	TYP	MAX	UNIT
f _{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
t _{SBW,Low}	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	μs
t _{SBW,En}	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾	2.2 V, 3 V			1	μs
t _{SBW,Rst}	Spy-Bi-Wire return to normal operation time		15		100	μs
f _{TCK}	TCK input frequency, 4-wire JTAG ⁽²⁾	2.2 V	0		5	MHz
		3 V	0		10	MHz
R _{internal}	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the t_{SBW,En} time after the first transition of the TEST/SBW_{TCK} pin (low to high), before the second transition of the pin (high to low) during the entry sequence.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 CPU ([Link to User's Guide](#))

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [Figure 6-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Figure 6-1. Integrated CPU Registers

6.2 Operating Modes

These microcontrollers have one active mode and six software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - Wake-up input from $\overline{\text{RST}}$ /NMI, P1, and P2

6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-1](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up External reset Watchdog time-out, password violation Flash memory password violation	WDTIFG, KEYV (SYSRSTIV) ^{(1) (2)}	Reset	0FFFEh	63, highest
System NMI PMM Vacant memory access JTAG mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾	(Non)maskable	0FFFCCh	62
User NMI NMI Oscillator fault Flash memory access violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) ^{(1) (2)}	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV) ^{(1) (3)}	Maskable	0FFF8h	60
TB0	TB0CCR0 CCIFG0 ⁽³⁾	Maskable	0FFF6h	59
TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV) ^{(1) (3)}	Maskable	0FFF4h	58
Watchdog Timer_A interval timer mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV) ^{(1) (3)}	Maskable	0FFF0h	56
USCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (UCAB0IV) ^{(1) (3)}	Maskable	0FFEEh	55
ADC10_A	ADC10IFG0 ^{(1) (3) (4)}	Maskable	0FFECCh	54
TA0	TA0CCR0 CCIFG0 ⁽³⁾	Maskable	0FFEAh	53
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) ^{(1) (3)}	Maskable	0FFE8h	52
LDO-PWR	LDOOFFIFG, LDOONIFG, LDOOVLIFG	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (3)}	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0 ⁽³⁾	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) ^{(1) (3)}	Maskable	0FFE0h	48
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (3)}	Maskable	0FFDEh	47
USCI_A1 receive or transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV) ^{(1) (3)}	Maskable	0FFDCh	46
USCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV) ^{(1) (3)}	Maskable	0FFDAh	45
TA2	TA2CCR0 CCIFG0 ⁽³⁾	Maskable	0FFD8h	44
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) ^{(1) (3)}	Maskable	0FFD6h	43
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (3)}	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) ^{(1) (3)}	Maskable	0FFD2h	41

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.

(3) Interrupt flags are in the module.

(4) Only on devices with ADC, otherwise reserved.

Table 6-1. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Reserved	Reserved ⁽⁵⁾		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

6.4 Memory Organization

Table 6-2 summarizes the memory map for all device variants.

Table 6-2. Memory Organization⁽¹⁾

		MSP430F5304	MSP430F5308	MSP430F5309	MSP430F5310
Memory (flash) Main: interrupt vector Main: code memory	Total Size	8KB 00FFFFh to 00FF80h 00FFFFh to 00E000h	16KB 00FFFFh to 00FF80h 00FFFFh to 00C000h	24KB 00FFFFh to 00FF80h 00FFFFh to 00A000h	32KB 00FFFFh to 00FF80h 00FFFFh to 008000h
RAM	Sector 1	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h
	Sector 0	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h
	Sector 7	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h
Information memory (flash)	Info A	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h
	Info B	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h
	Info C	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h
Bootloader (BSL) memory (flash)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 0h	4KB 000FFFh to 0h	4KB 000FFFh to 0h	4KB 000FFFh to 0h

(1) N/A = Not available

6.5 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory through the BSL is protected by user-defined password. Use of the UART BSL requires external access to six pins (see [Table 6-3](#)). For complete description of the features of the BSL and its implementation, see [MSP430 Flash Device Bootloader \(BSL\) User's Guide](#). [Table 6-3](#) lists the BSL pin requirements.

Table 6-3. BSL Pin Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

6.6 JTAG Operation

6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. [Table 6-4](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

Table 6-4. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. [Table 6-5](#) lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

Table 6-5. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWDIO	IN, OUT	Spy-Bi-Wire data input and output
VCC		Power supply
VSS		Ground supply

6.7 Flash Memory ([Link to User's Guide](#))

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

6.8 RAM ([Link to User's Guide](#))

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors. See [Section 6.4](#) for the size of a sector.
- Each sector 0 to n can be completely disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

6.9.1 Digital I/O ([Link to User's Guide](#))

Up to six 8-bit I/O ports are implemented: For 64-pin options, P1, P2, P4, and P6 are complete, P5 is reduced to 6-bit I/O, and P3 is reduced to 5-bit I/O. For 48-pin options, P6 is reduced to 4-bit I/O, P2 is reduced to 1-bit I/O, and P3 is completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wakeup input capability is available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P6) or word-wise in pairs (PA through PC).

6.9.2 Port Mapping Controller ([Link to User's Guide](#))

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4 (see [Table 6-6](#)). [Table 6-7](#) lists the default settings for all pins that support port mapping.

Table 6-6. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_CBOUT0	–	Comparator_B output
	PM_TB0CLK	TB0 clock input	–
2	PM_ADC10CLK	–	ADC10CLK
	PM_DMAE0	DMAE0 input	–
3	PM_SVMOUT	–	SVM output
	PM_TB0OUTH	TB0 high impedance input TB0OUTH	–
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI – input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA1TXD	USCI_A1 UART TXD (Direction controlled by USCI – output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	
14	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
	PM_UCB1SCL	USCI_B1 I ² C clock (open drain and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
	PM_UCB1SDA	USCI_B1 I ² C data (open drain and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
17	PM_CBOUT1	None	Comparator_B output
18	PM_MCLK	None	MCLK
19	PM_RTCCLK	None	RTCCLK output
20	PM_UCA0RXD	USCI_A0 UART RXD (Direction controlled by USCI – input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
21	PM_UCA0TXD	USCI_A0 UART TXD (Direction controlled by USCI – output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
22	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI)	
23	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I ² C clock (open drain and direction controlled by USCI)	
24	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I ² C data (open drain and direction controlled by USCI)	
25	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI)	
26-30	Reserved	None	DVSS

Table 6-6. Port Mapping Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
31 (0FFh) ⁽¹⁾	PM_ANALOG	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

Table 6-7. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI)	
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I ² C data (open drain and direction controlled by USCI)	
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I ² C clock (open drain and direction controlled by USCI)	
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI)	
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction controlled by USCI – output) USCI_A1 SPI slave in master out (direction controlled by USCI)	
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Direction controlled by USCI – input) USCI_A1 SPI slave out master in (direction controlled by USCI)	
P4.6/P4MAP6	PM_NONE	None	DVSS
P4.7/P4MAP7	PM_NONE	None	DVSS

6.9.3 Oscillator and System Clock ([Link to User's Guide](#))

The clock system is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode not supported), an internal very low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 5 μ s. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32 kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.9.4 Power-Management Module (PMM) ([Link to User's Guide](#))

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, and brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

6.9.5 Hardware Multiplier ([Link to User's Guide](#))

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.9.6 Real-Time Clock (RTC_A) ([Link to User's Guide](#))

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

6.9.7 Watchdog Timer (WDT_A) ([Link to User's Guide](#))

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.8 System Module (SYS) ([Link to User's Guide](#))

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators (see [Table 6-8](#)), bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application.

Table 6-8. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$ /NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wake up from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT time-out (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

6.9.9 DMA Controller ([Link to User's Guide](#))

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion register to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. [Table 6-9](#) lists the triggers for DMA transfers.

Table 6-9. DMA Trigger Assignments ⁽¹⁾

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC10IFG0 ⁽²⁾	ADC10IFG0 ⁽²⁾	ADC10IFG0 ⁽²⁾
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	reserved	reserved	reserved
28	reserved	reserved	reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) If a reserved trigger source is selected, no trigger is generated.

(2) Only on devices with ADC. Reserved on devices without ADC.

6.9.10 Universal Serial Communication Interface (USCI) (Links to User's Guide: [UART Mode](#), [SPI Mode](#), [I²C Mode](#))

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) or I²C.

The MSP430F53xx series includes one or two complete USCI modules.

6.9.11 TA0 (Link to User's Guide)

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see [Table 6-10](#)). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
18, H2-P1.0	14-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
18, H2-P1.0	14-P1.0	TA0CLK	TACLK	CCR0	TA0	TA0.0		
19, H3-P1.1	15-P1.1	TA0.0	CCI0A				19, H3-P1.1	15-P1.1
		DV _{SS}	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}	CCR1	TA1	TA0.1		
20, J3-P1.2	16-P1.2	TA0.1	CCI1A				20, J3-P1.2	16-P1.2
		CBOUT (internal)	CCI1B				ADC10 (internal) ⁽¹⁾	ADC10 (internal) ⁽¹⁾
							ADC10SHSx = {1}	ADC10SHSx = {1}
		DV _{SS}	GND	CCR2	TA2	TA0.2		
		DV _{CC}	V _{CC}					
21, G4-P1.3	17-P1.3	TA0.2	CCI2A				21, G4-P1.3	17-P1.3
		ACLK (internal)	CCI2B					
		DV _{SS}	GND	CCR3	TA3	TA0.3		
		DV _{CC}	V _{CC}					
22, H4-P1.4	18-P1.4	TA0.3	CCI3A				22, H4-P1.4	18-P1.4
		DV _{SS}	CCI3B					
		DV _{SS}	GND	CCR4	TA4	TA0.4		
		DV _{CC}	V _{CC}					
23, J4-P1.5	19-P1.5	TA0.4	CCI4A				23, J4-P1.5	19-P1.5
		DV _{SS}	CCI4B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

(1) Only on devices with ADC.

6.9.12 TA1 [\(Link to User's Guide\)](#)

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing (see [Table 6-11](#)). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-11. TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
24, G5-P1.6	20-P1.6	TA1CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
24, G5-P1.6	20-P1.6	TA1CLK	$\overline{\text{TACLK}}$	CCR0	TA0	TA1.0	25, H5-P1.7	21-P1.7
25, H5-P1.7	21-P1.7	TA1.0	CCI0A					
		DV _{SS}	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}	CCR1	TA1	TA1.1	26, J5-P2.0	22-P2.0
26, J5-P2.0	22-P2.0	TA1.1	CCI1A					
		CBOUT (internal)	CCI1B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}	CCR2	TA2	TA1.2	27, G6-P2.1	
27, G6-P2.1		TA1.2	CCI2A					
		ACLK (internal)	CCI2B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

6.9.13 TA2 [\(Link to User's Guide\)](#)

TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see [Table 6-12](#)). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. TA2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
28, J6-P2.2		TA2CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
28, J6-P2.2		TA2CLK	$\overline{\text{TACLK}}$	CCR0	TA0	TA2.0	29, H6-P2.3	
29, H6-P2.3		TA2.0	CCI0A					
		DV _{SS}	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}	CCR1	TA1	TA2.1		
30, J7-P2.4		TA2.1	CCI1A				30, J7-P2.4	
		CBOUT (internal)	CCI1B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}	CCR2	TA2	TA2.2		
31, J8-P2.5		TA2.2	CCI2A				31, J8-P2.5	
		ACLK (internal)	CCI2B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

6.9.14 TB0 [\(Link to User's Guide\)](#)

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple capture/compares, PWM outputs, and interval timing (see [Table 6-13](#)). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE ⁽¹⁾	RGZ, PT ⁽¹⁾						RGC, ZQE ⁽¹⁾	RGZ, PT ⁽¹⁾
		TB0CLK	TBCLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
		TB0CLK	$\overline{\text{TBCLK}}$					
		TB0.0	CCI0A	CCR0	TB0	TB0.0	ADC10 (internal) ⁽²⁾ ADC10SHSx = {2}	ADC10 (internal) ⁽²⁾ ADC10SHSx = {2}
		TB0.0	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.1	CCI1A	CCR1	TB1	TB0.1	ADC10 (internal) ADC10SHSx = {3}	ADC10 (internal) ADC10SHSx = {3}
		CBOUT (internal)	CCI1B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.2	CCI2A	CCR2	TB2	TB0.2		
		TB0.2	CCI2B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.3	CCI3A	CCR3	TB3	TB0.3		
		TB0.3	CCI3B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.4	CCI4A	CCR4	TB4	TB0.4		
		TB0.4	CCI4B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.5	CCI5A	CCR5	TB5	TB0.5		
		TB0.5	CCI5B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.6	CCI6A	CCR6	TB6	TB0.6		
		ACLK (internal)	CCI6B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

(1) Timer functions selectable by the port mapping controller.

(2) Only on devices with ADC.

6.9.15 Comparator_B ([Link to User's Guide](#))

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.9.16 ADC10_A ([Link to User's Guide](#))

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

6.9.17 CRC16 ([Link to User's Guide](#))

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.9.18 Reference (REF) Module Voltage Reference ([Link to User's Guide](#))

The REF generates all critical reference voltages that can be used by the various analog peripherals in the device.

6.9.19 LDO and Port U

The integrated 3.3-V power system incorporates an integrated 3.3-V LDO regulator that allows the entire microcontroller to be powered from nominal 5-V LDO1 when it is made available for the system. Alternatively, the power system can supply power only to other components within the system, or it can be unused altogether. The Port U Pins (PU.0 and PU.1) function as general-purpose high-current I/O pins. These pins must be configured together as either both inputs or both outputs. Port U is supplied by the LDO0 rail. If the 3.3-V LDO is not being used in the system (disabled), the LDO0 pin can be supplied externally.

6.9.20 Embedded Emulation Module (EEM) (S Version) ([Link to User's Guide](#))

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.10 Peripheral File Map

Table 6-14 lists the register base address for all supported peripherals.

Table 6-14. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 6-15)	0100h	000h to 01Fh
PMM (see Table 6-16)	0120h	000h to 01Fh
Flash Control (see Table 6-17)	0140h	000h to 00Fh
CRC16 (see Table 6-18)	0150h	000h to 007h
RAM Control (see Table 6-19)	0158h	000h to 001h
Watchdog (see Table 6-20)	015Ch	000h to 001h
UCS (see Table 6-21)	0160h	000h to 01Fh
SYS (see Table 6-22)	0180h	000h to 01Fh
Shared Reference (see Table 6-23)	01B0h	000h to 001h
Port Mapping Control (see Table 6-24)	01C0h	000h to 002h
Port Mapping Port P4 (see Table 6-24)	01E0h	000h to 007h
Port P1, P2 (see Table 6-25)	0200h	000h to 01Fh
Port P3, P4 (see Table 6-26)	0220h	000h to 00Bh
Port P5, P6 (see Table 6-27)	0240h	000h to 00Bh
Port PJ (see Table 6-28)	0320h	000h to 01Fh
TA0 (see Table 6-29)	0340h	000h to 02Eh
TA1 (see Table 6-30)	0380h	000h to 02Eh
TB0 (see Table 6-31)	03C0h	000h to 02Eh
TA2 (see Table 6-32)	0400h	000h to 02Eh
Real-Time Clock (RTC_A) (see Table 6-33)	04A0h	000h to 01Bh
32-Bit Hardware Multiplier (see Table 6-34)	04C0h	000h to 02Fh
DMA General Control (see Table 6-35)	0500h	000h to 00Fh
DMA Channel 0 (see Table 6-35)	0510h	000h to 00Ah
DMA Channel 1 (see Table 6-35)	0520h	000h to 00Ah
DMA Channel 2 (see Table 6-35)	0530h	000h to 00Ah
USCI_A0 (see Table 6-36)	05C0h	000h to 01Fh
USCI_B0 (see Table 6-37)	05E0h	000h to 01Fh
USCI_A1 (see Table 6-38)	0600h	000h to 01Fh
USCI_B1 (see Table 6-39)	0620h	000h to 01Fh
ADC10_A (see Table 6-40)	0740h	000h to 01Fh
Comparator_B (see Table 6-41)	08C0h	000h to 00Fh
LDO-PWR and Port U Configuration (see Table 6-42)	0900h	000h to 014h

Table 6-15. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-16. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 6-17. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 6-18. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-19. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 6-20. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-21. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh

Table 6-21. UCS Registers (Base Address: 0160h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 8	UCSCTL8	10h

Table 6-22. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 6-23. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

**Table 6-24. Port Mapping Registers
(Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)**

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping password	PMAPPWD	00h
Port mapping control	PMAPCTL	02h
Port P4.0 mapping	P4MAP0	00h
Port P4.1 mapping	P4MAP1	01h
Port P4.2 mapping	P4MAP2	02h
Port P4.3 mapping	P4MAP3	03h
Port P4.4 mapping	P4MAP4	04h
Port P4.5 mapping	P4MAP5	05h
Port P4.6 mapping	P4MAP6	06h
Port P4.7 mapping	P4MAP7	07h

Table 6-25. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-26. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

Table 6-27. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 resistor enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 resistor enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 6-28. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 6-29. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
Capture/compare 3	TA0CCR3	18h
Capture/compare 4	TA0CCR4	1Ah
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-30. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-31. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 6-32. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 6-33. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPSEL0CTL	08h
RTC prescaler 1 control	RTCPSEL1CTL	0Ah
RTC prescaler 0	RTCPSEL0	0Ch
RTC prescaler 1	RTCPSEL1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter 1	RTCSEC/RTCNT1	10h
RTC minutes/counter 2	RTCMIN/RTCNT2	11h
RTC hours/counter 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

Table 6-34. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

Table 6-35. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Ah

Table 6-36. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 6-37. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 6-38. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 6-39. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 6-40. ADC10_A Registers (Base Address: 0740h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC10_A control 0	ADC10CTL0	00h
ADC10_A control 1	ADC10CTL1	02h
ADC10_A control 2	ADC10CTL2	04h
ADC10_A window comparator low threshold	ADC10LO	06h
ADC10_A window comparator high threshold	ADC10HI	08h
ADC10_A memory control 0	ADC10MCTL0	0Ah
ADC10_A conversion memory	ADC10MEM0	12h
ADC10_A interrupt enable	ADC10IE	1Ah
ADC10_A interrupt flags	ADC10IGH	1Ch
ADC10_A interrupt vector word	ADC10IV	1Eh

Table 6-41. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control 0	CBCTL0	00h
Comp_B control 1	CBCTL1	02h
Comp_B control 2	CBCTL2	04h
Comp_B control 3	CBCTL3	06h
Comp_B interrupt	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 6-42. LDO and Port U Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
LDO key/ID	LDOKEYPID	00h
PU port control	PUCTL	04h
LDO power control	LDOPWRCTL	08h

6.11 Input/Output Diagrams

6.11.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-43 summarizes the selection of the pin functions.

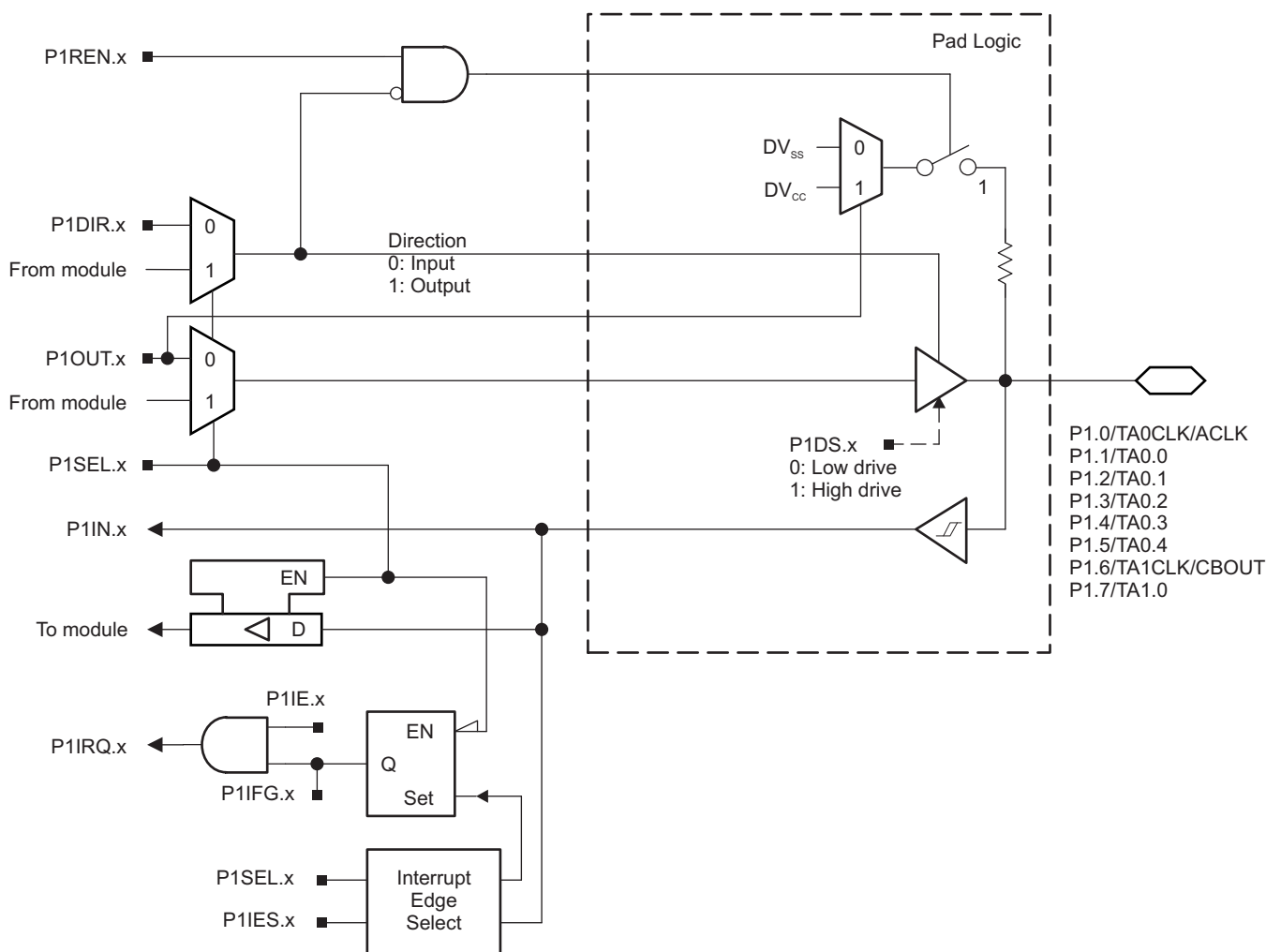


Figure 6-2. Port P1 (P1.0 to P1.7) Diagram

Table 6-43. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

6.11.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-44 summarizes the selection of the pin functions.

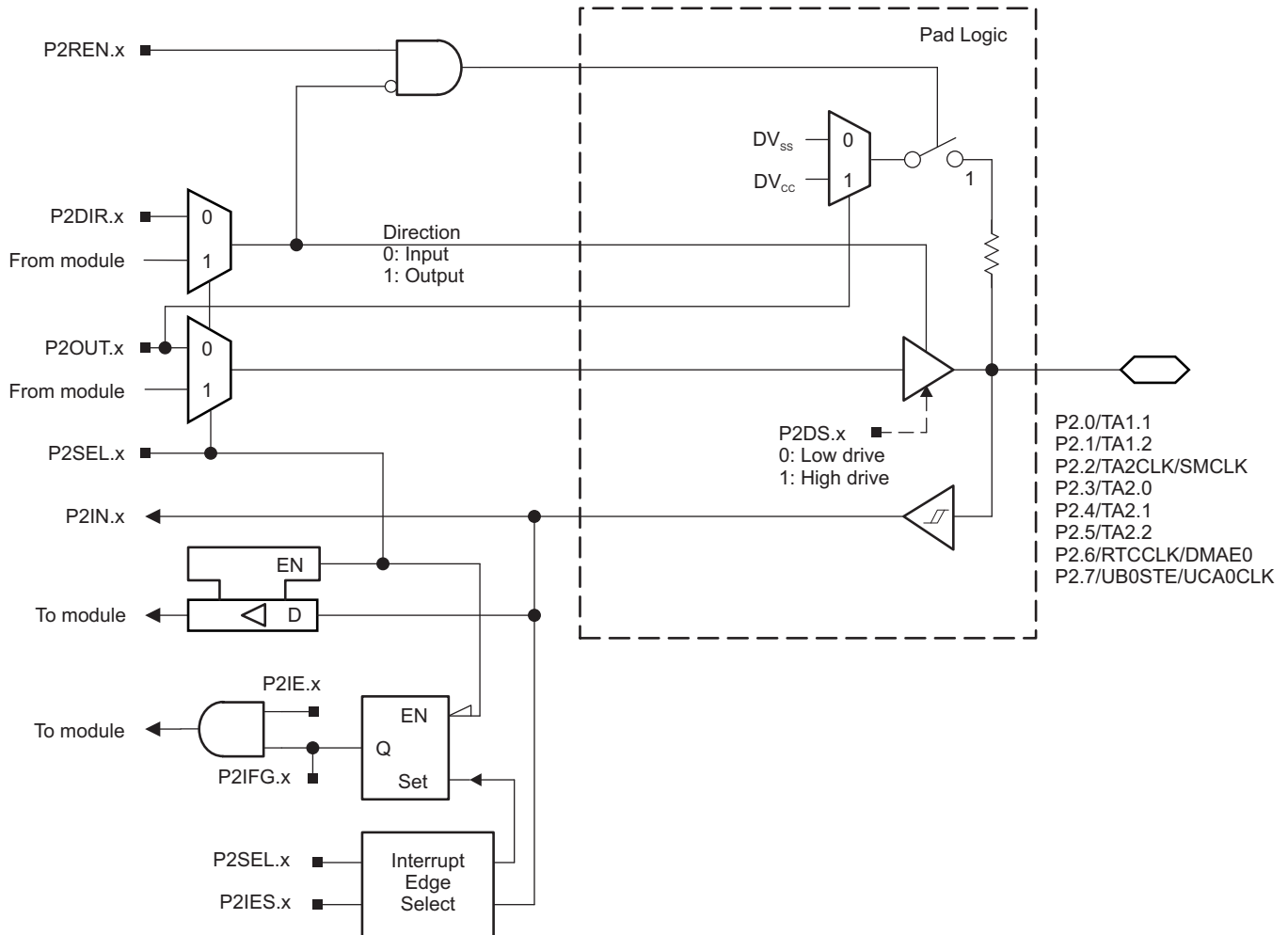


Figure 6-3. Port P2 (P2.0 to P2.7) Diagram

Table 6-44. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾	
			P2DIR.x	P2SEL.x
P2.0/TA1.1	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.1/TA1.2	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.2/TA2CLK/SMCLK	2	P2.2 (I/O)	I: 0; O: 1	0
		TA2CLK	0	1
		SMCLK	1	1
P2.3/TA2.0	3	P2.3 (I/O)	I: 0; O: 1	0
		TA2.CCI0A	0	1
		TA2.0	1	1
P2.4/TA2.1	4	P2.4 (I/O)	I: 0; O: 1	0
		TA2.CCI1A	0	1
		TA2.1	1	1
P2.5/TA2.2	5	P2.5 (I/O)	I: 0; O: 1	0
		TA2.CCI2A	0	1
		TA2.2	1	1
P2.6/RTCCLK/DMAE0	6	P2.6 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		RTCCLK	1	1
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK ^{(2) (3)}	X	1

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.11.3 Port P3 (P3.0 to P3.4) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-45 summarizes the selection of the pin functions.

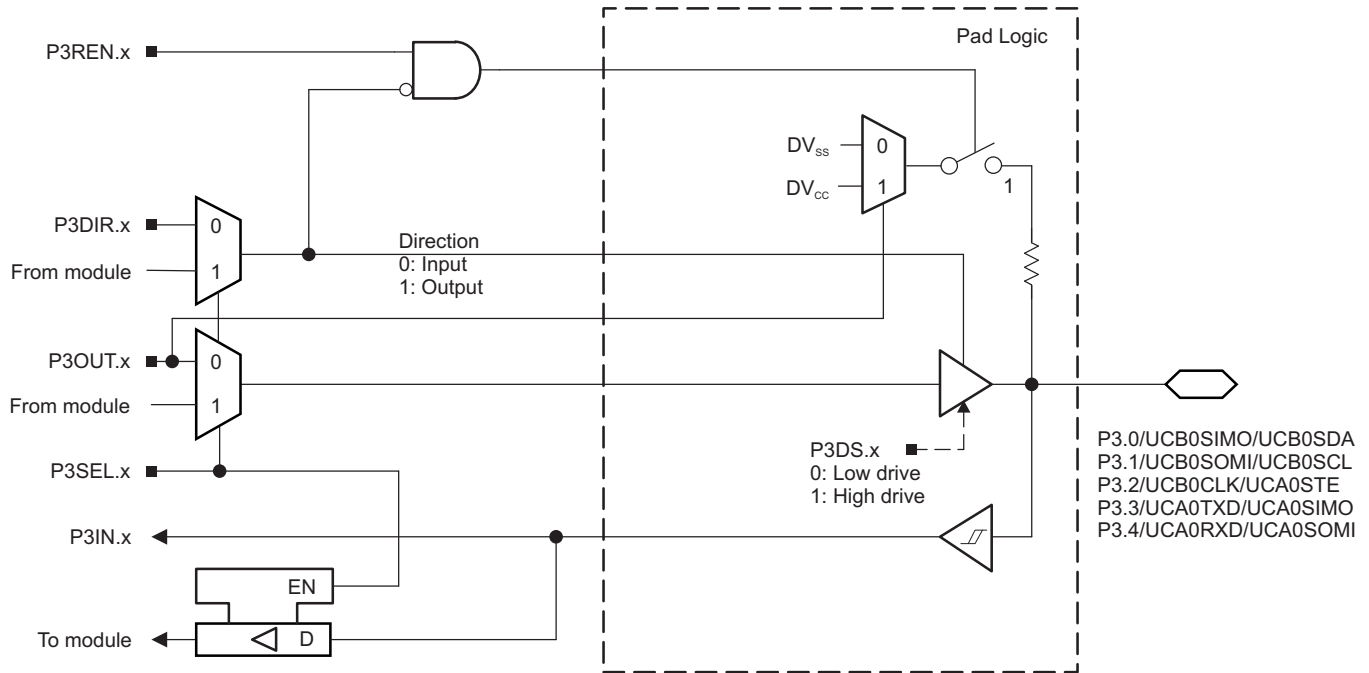


Figure 6-4. Port P3 (P3.0 to P3.7) Diagram

Table 6-45. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾	
			P3DIR.x	P3SEL.x
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA ^{(2) (3)}	X	1
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL ^{(2) (3)}	X	1
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE ^{(2) (4)}	X	1
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO ⁽²⁾	X	1
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI ⁽²⁾	X	1

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) If the I²C functionality is selected, the output drives only the logical 0 to V_{SS} level.

(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USC1_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.11.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-46 summarizes the selection of the pin functions.

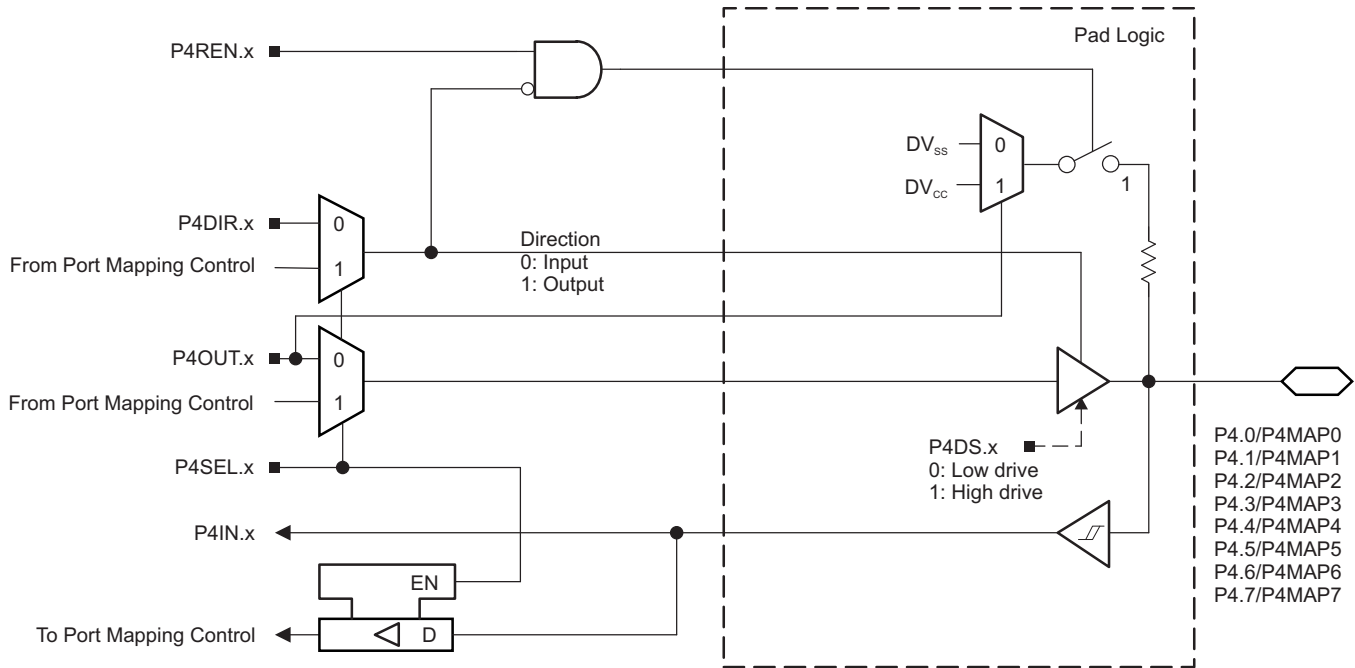


Figure 6-5. Port P4 (P4.0 to P4.7) Diagram

Table 6-46. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P4DIR.x ⁽¹⁾	P4SEL.x	P4MAPx
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30

(1) The direction of some mapped secondary functions are controlled directly by the module. See Table 6-6 for specific direction control information of mapped secondary functions.

6.11.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.

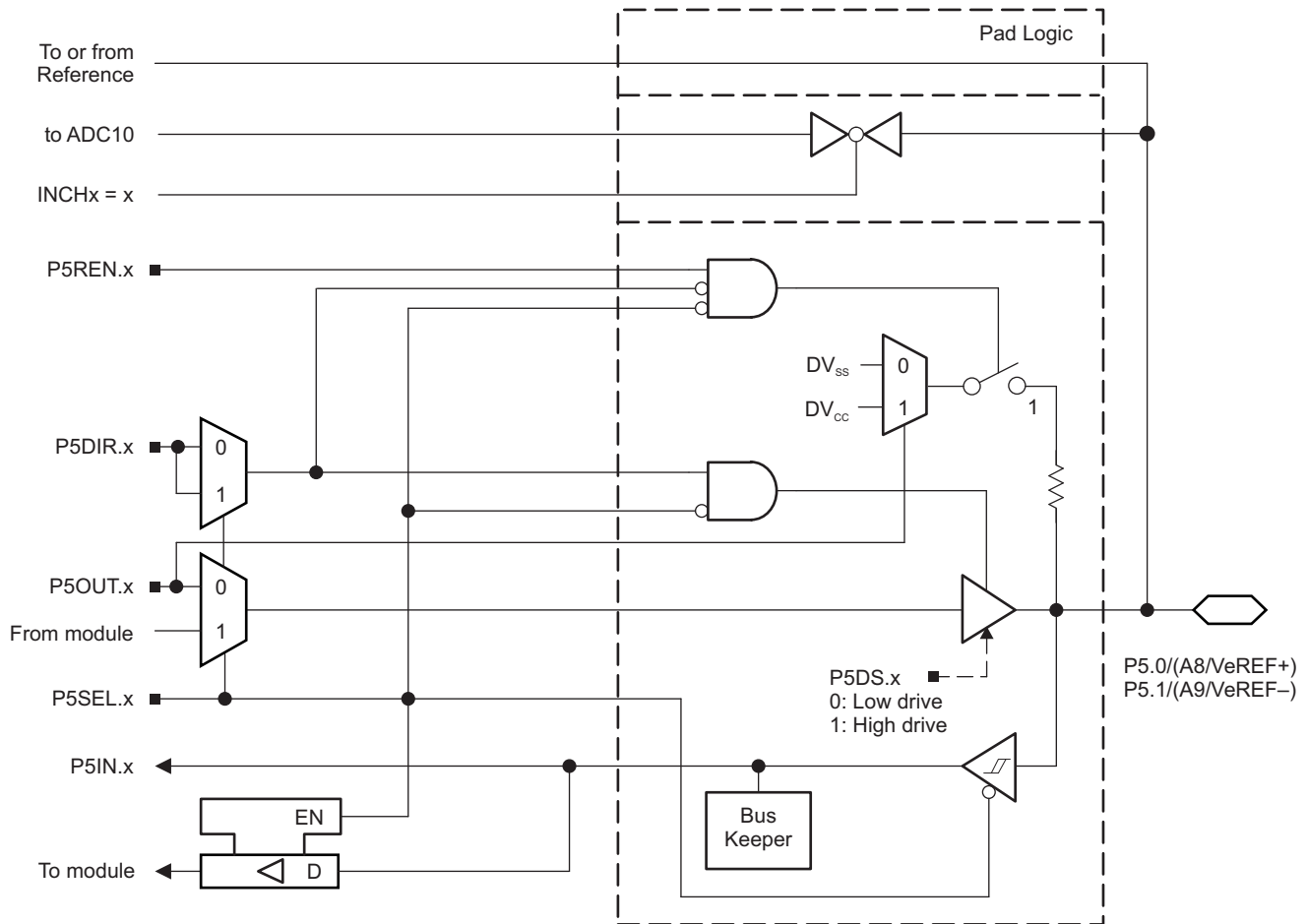


Figure 6-6. Port P5 (P5.0 and P5.1) Diagram

Table 6-47. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾	
			P5DIR.x	P5SEL.x
P5.0/A8/VeREF+ ⁽²⁾	0	P5.0 (I/O) ⁽³⁾	I: 0; O: 1	0
		A8/VeREF+ ⁽⁴⁾	X	1
P5.1/A9/VeREF- ⁽⁵⁾	1	P5.1 (I/O) ⁽³⁾	I: 0; O: 1	0
		A9/VeREF- ⁽⁶⁾	X	1

(1) X = Don't care

(2) VeREF+ available on devices with ADC10_A.

(3) Default condition

(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC10_A when available.

(5) VeREF- available on devices with ADC10_A.

(6) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC10_A when available.

6.11.6 Port P5 (P5.2) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-48 summarizes the selection of the pin functions.

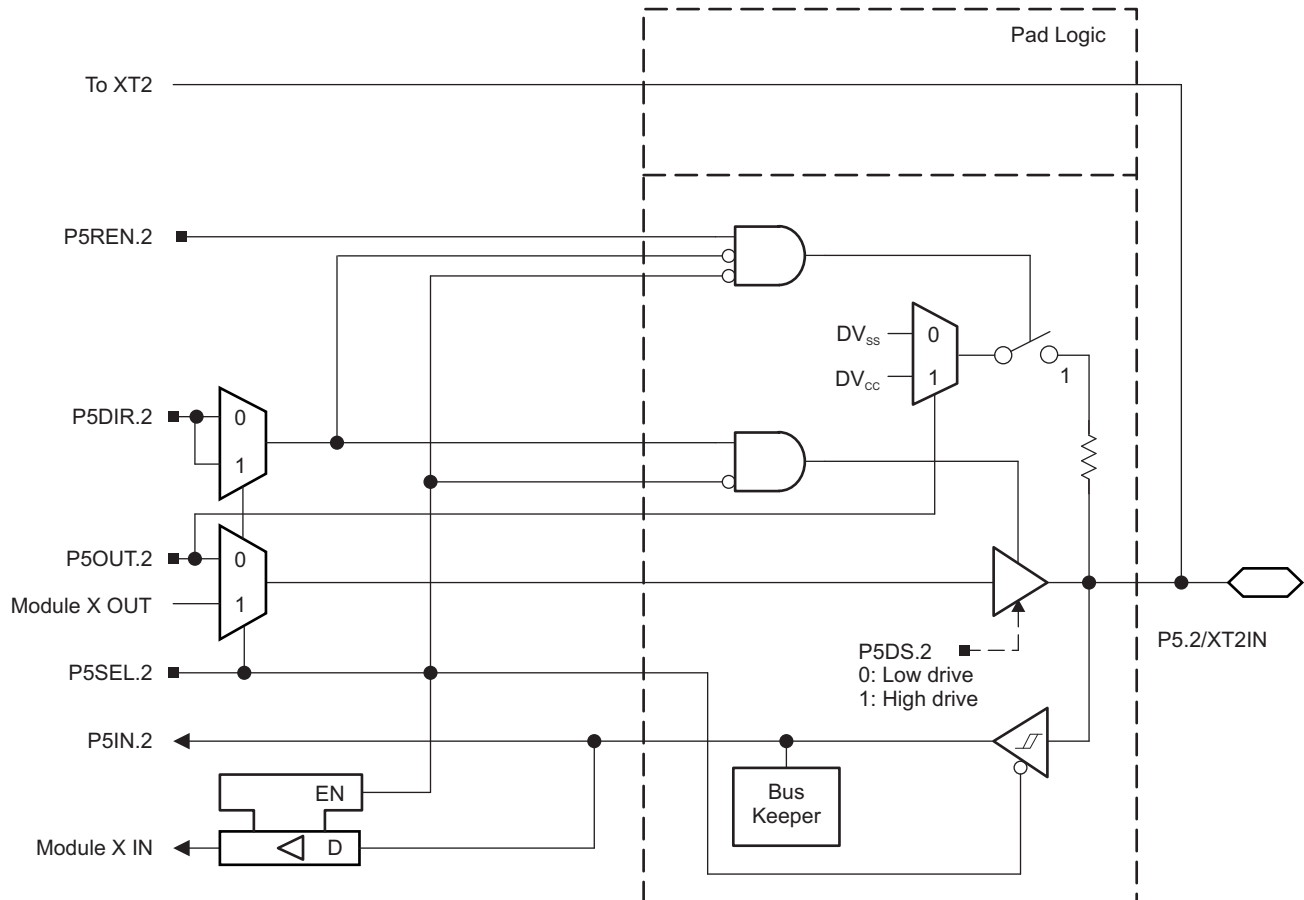


Figure 6-7. Port P5 (P5.2) Diagram

6.11.7 Port P5 (P5.3) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-48 summarizes the selection of the pin functions.

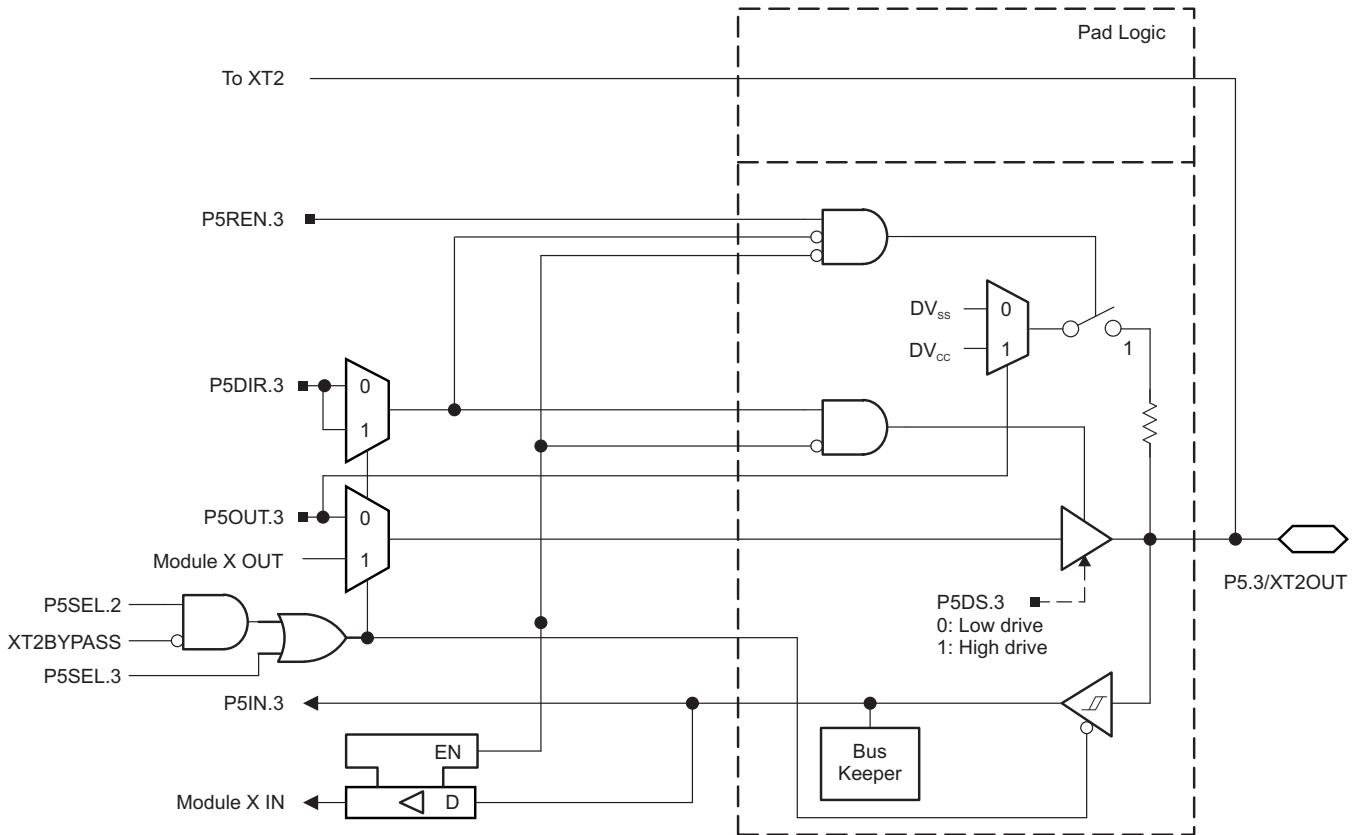


Figure 6-8. Port P5 (P5.3) Diagram

Table 6-48. Port P5 (P5.2 and P5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode ⁽²⁾	X	1	X	0
		XT2IN bypass mode ⁽²⁾	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	0	X
		XT2OUT crystal mode ⁽³⁾	X	1	X	0
		P5.3 (I/O) ⁽³⁾	X	1	0	1

(1) X = Don't care

(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

6.11.8 Port P5 (P5.4 and P5.5) Input/Output With Schmitt Trigger

Figure 6-9 and Figure 6-10 show the port diagrams. Table 6-49 summarizes the selection of the pin functions.

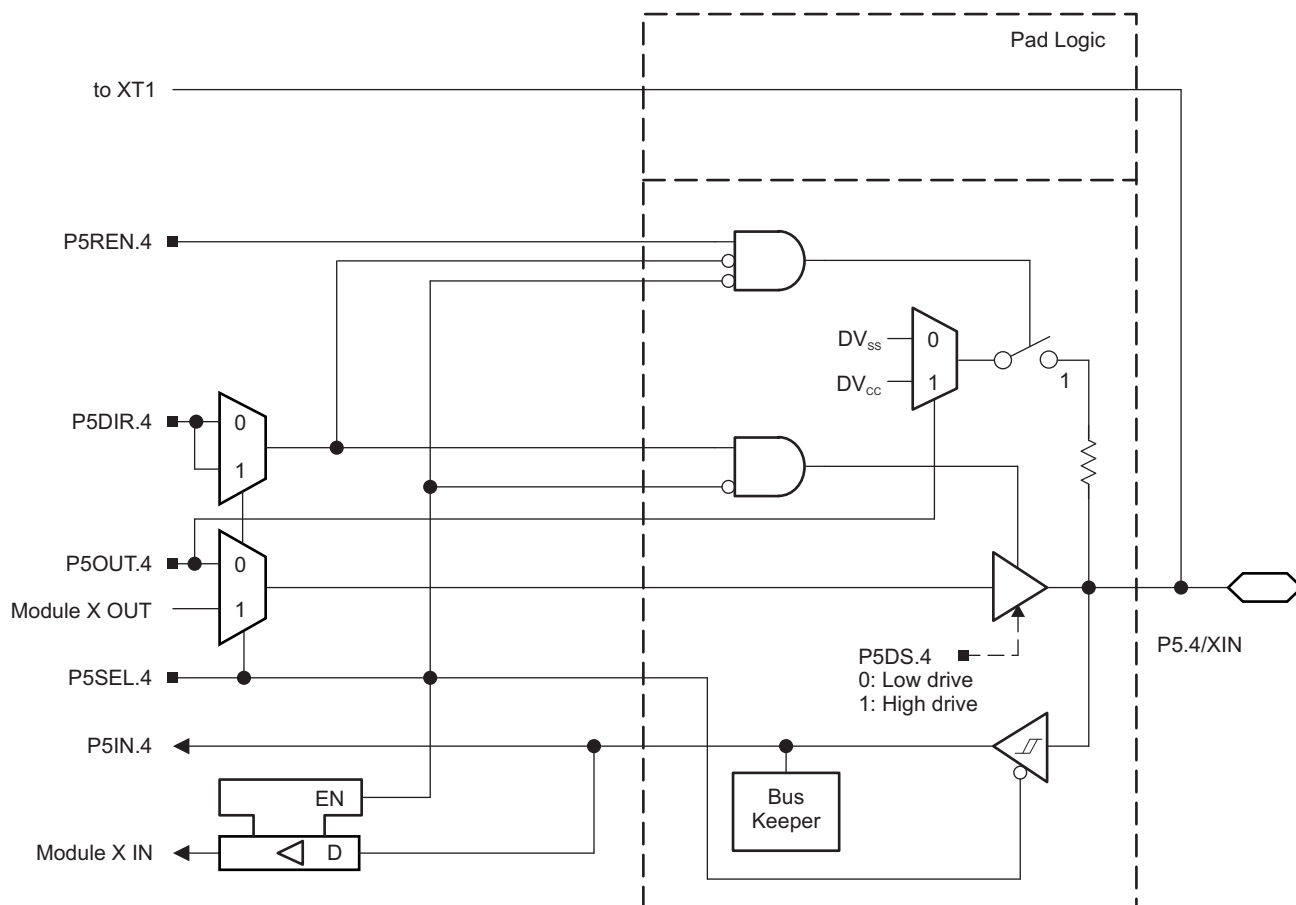


Figure 6-9. Port P5 (P5.4) Diagram

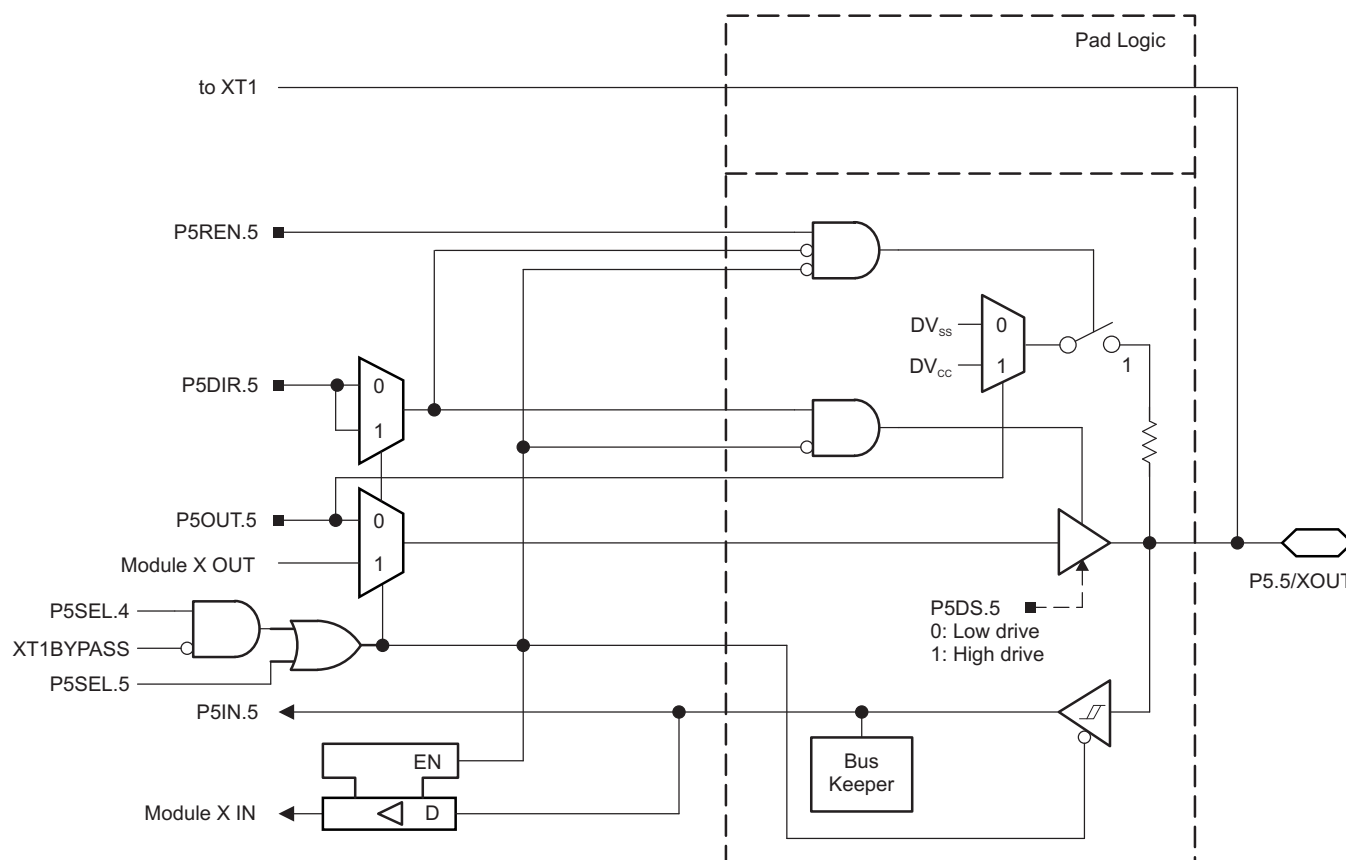


Figure 6-10. Port P5 (P5.5) Diagram

Table 6-49. Port P5 (P5.4 and P5.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P5DIR.x	P5SEL.4	P5SEL.5	XT1BYPASS
P5.4/XIN	4	P5.4 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode ⁽²⁾	X	1	X	0
		XIN bypass mode ⁽²⁾	X	1	X	1
P5.5/XOUT	5	P5.5 (I/O)	I: 0; O: 1	0	0	X
		XOUT crystal mode ⁽³⁾	X	1	X	0
		P5.5 (I/O) ⁽³⁾	X	1	0	1

(1) X = Don't care

(2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

6.11.9 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-50 summarizes the selection of the pin functions.

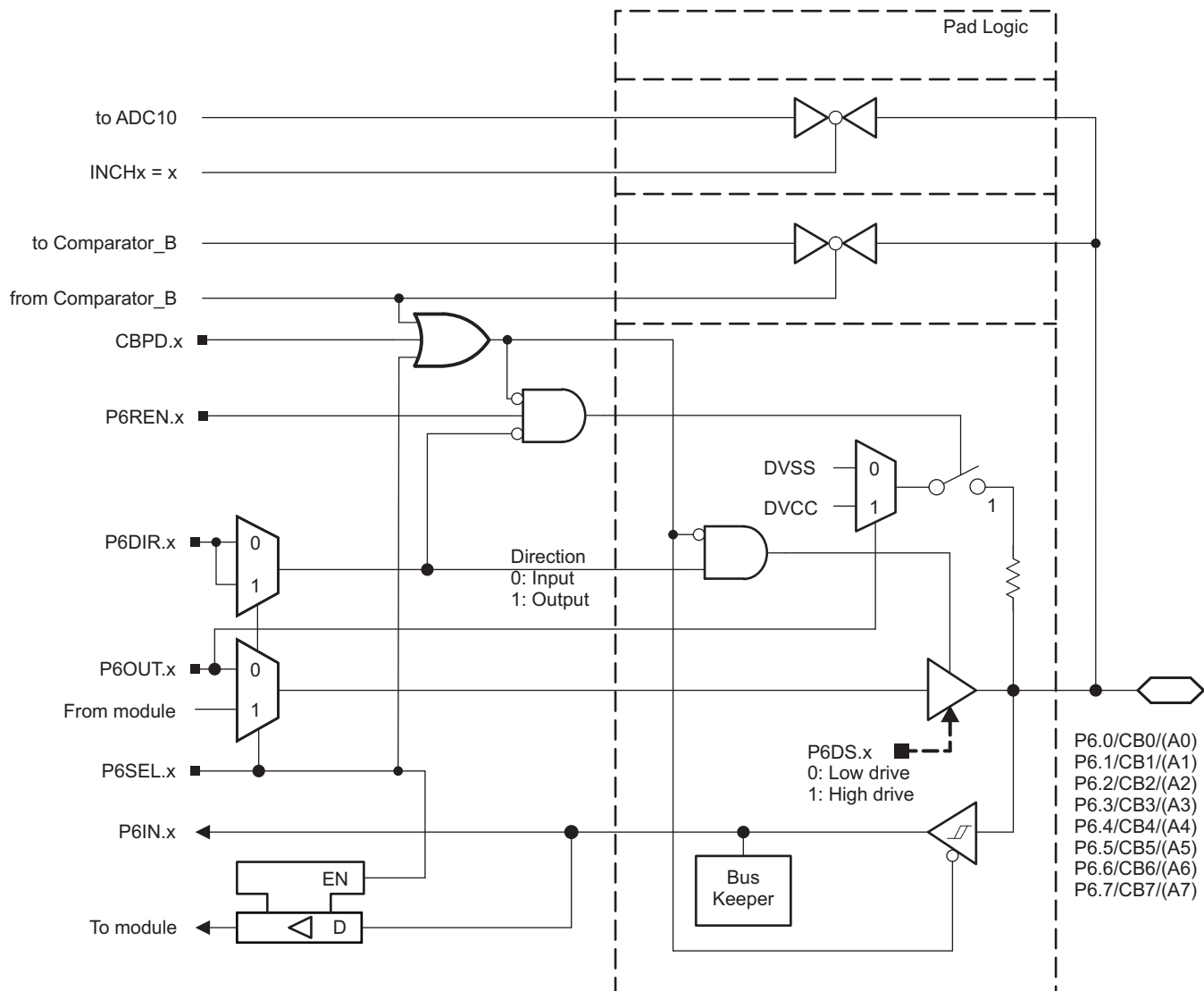


Figure 6-11. Port P6 (P6.0 to P6.7) Diagram

Table 6-50. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P6DIR.x	P6SEL.x	CBPD
P6.0/CB0/(A0)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		A0 (only on devices with ADC)	X	1	X
		CB0 ⁽¹⁾	X	X	1
P6.1/CB1/(A1)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		A1 (only on devices with ADC)	X	1	X
		CB1 ⁽¹⁾	X	X	1
P6.2/CB2/(A2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		A2 (only on devices with ADC)	X	1	X
		CB2 ⁽¹⁾	X	X	1
P6.3/CB3/(A3)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		A3 (only on devices with ADC)	X	1	X
		CB3 ⁽¹⁾	X	X	1
P6.4/CB4/(A4)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4 (only on devices with ADC)	X	1	X
		CB4 ⁽¹⁾	X	X	1
P6.5/CB5/(A5)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		A5 (only on devices with ADC)	X	1	X
		CB5 ⁽¹⁾	X	X	1
P6.6/CB6/(A6)	6	P6.6 (I/O)	I: 0; O: 1	0	0
		A6 (only on devices with ADC)	X	1	X
		CB6 ⁽¹⁾	X	X	1
P6.7/CB7/(A7)	7	P6.7 (I/O)	I: 0; O: 1	0	0
		A7 (only on devices with ADC)	X	1	X
		CB7 ⁽¹⁾	X	X	1

- (1) Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

6.11.10 Port U (PU.0 and PU.1) Input/Output

Figure 6-12 shows the port diagram. Table 6-51 summarizes the selection of the pin functions.

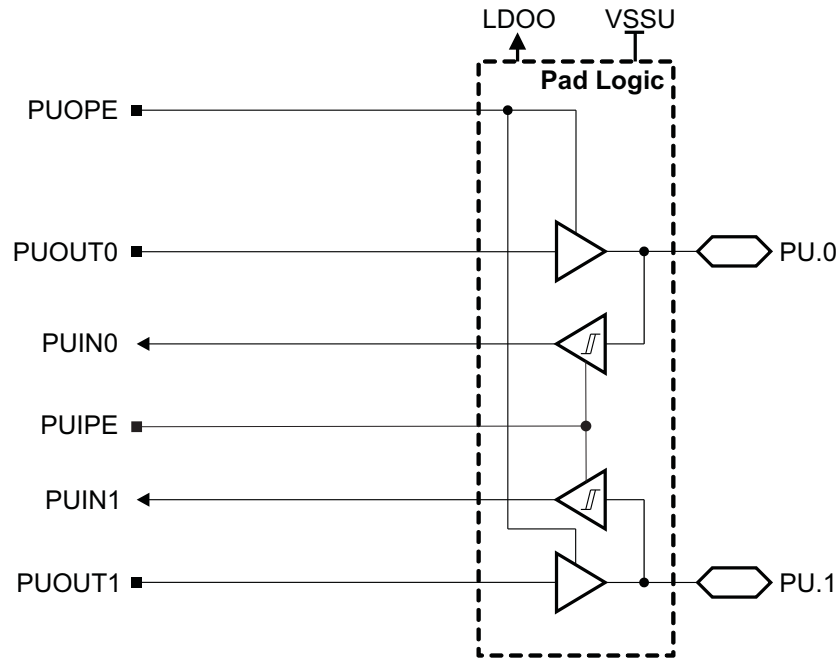


Figure 6-12. Port U (PU.0 and PU.1) Diagram

Table 6-51. Port U (PU.0 and PU.1) Pin Functions⁽¹⁾

PUIPE	PUOPE	PUOUT1	PUOUT0	PU.1	PU.0	PORT U FUNCTION
0	1	0	0	Output low	Output low	Outputs enabled
0	1	0	1	Output low	Output high	Outputs enabled
0	1	1	0	Output high	Output low	Outputs enabled
0	1	1	1	Output high	Output high	Outputs enabled
1	0	X	X	Input enabled	Input enabled	Inputs enabled
0	0	X	X	Hi-Z	Hi-Z	Outputs and inputs disabled

(1) PU.1 and PU.0 inputs and outputs are supplied from LDOO. LDOO can be generated by the device using the integrated 3.3-V LDO when enabled. LDOO can also be supplied externally when the 3.3-V LDO is not being used and is disabled.

6.11.11 Port J (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-13 shows the port diagram. Table 6-52 summarizes the selection of the pin functions.

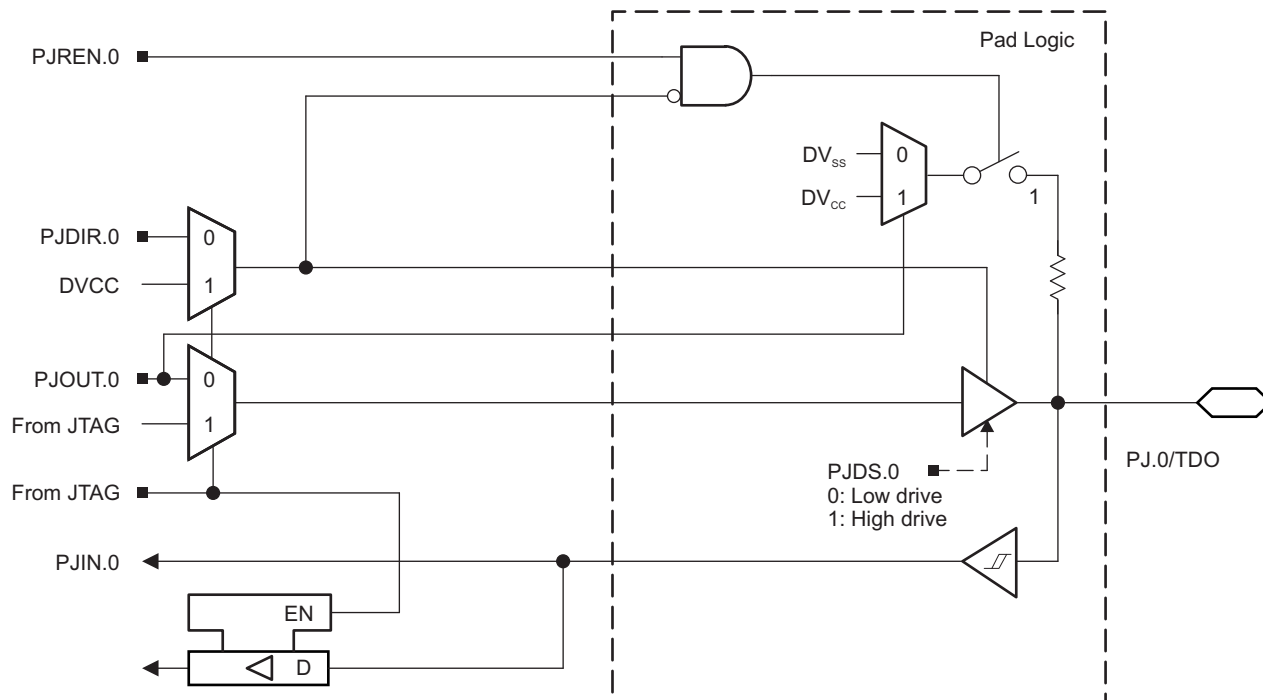


Figure 6-13. Port PJ (PJ.0) Diagram

6.11.12 Port J (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-14 shows the port diagram. Table 6-52 summarizes the selection of the pin functions.

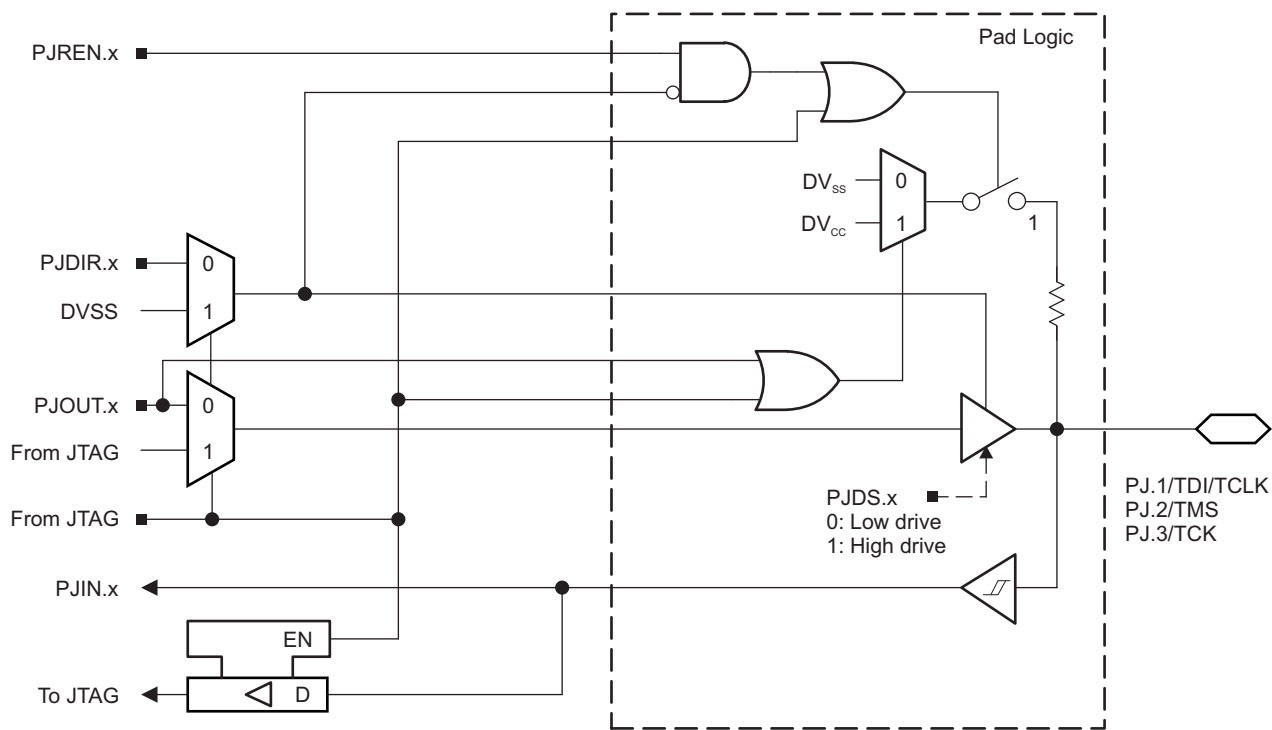


Figure 6-14. Port PJ (PJ.1 to PJ.3) Diagram

Table 6-52. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O) ⁽²⁾	I: 0; O: 1
		TDO ⁽³⁾	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O) ⁽²⁾	I: 0; O: 1
		TDI/TCLK ^{(3) (4)}	X
PJ.2/TMS	2	PJ.2 (I/O) ⁽²⁾	I: 0; O: 1
		TMS ^{(3) (4)}	X
PJ.3/TCK	3	PJ.3 (I/O) ⁽²⁾	I: 0; O: 1
		TCK ^{(3) (4)}	X

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.12 Device Descriptors

Table 6-53 lists the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 6-53. Device Descriptors⁽¹⁾

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE						
				F5304	F5308 RGC, ZQE	F5308 RGZ, PT	F5309 RGC, ZQE	F5309 RGZ, PT	F5310 RGC, ZQE	F5310 RGZ, PT
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	1	12h	13h	13h	14h	14h	15h	15h
	Device ID	01A05h	1	81h	81h	81h	81h	81h	81h	81h
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
ADC10 Calibration	ADC10 Calibration Tag	01A14h	1	13h	13h	13h	13h	13h	13h	13h
	ADC10 Calibration Length	01A15h	1	10h	10h	10h	10h	10h	10h	10h
	ADC Gain Factor	01A16h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC Offset	01A18h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V Reference Temperature sensor 30°C	01A1Ah	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V Reference Temperature sensor 85°C	01A1Ch	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V Reference Temperature sensor 30°C	01A1Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V Reference Temperature sensor 85°C	01A20h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V Reference Temperature sensor 30°C	01A22h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V Reference Temperature sensor 85°C	01A24h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h	12h	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h	06h	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit

(1) N/A = Not applicable

Table 6-53. Device Descriptors⁽¹⁾ (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE						
				F5304	F5308 RGC, ZQE	F5308 RGZ, PT	F5309 RGC, ZQE	F5309 RGZ, PT	F5310 RGC, ZQE	F5310 RGZ, PT
Peripheral Descriptor	Peripheral descriptor tag	01A2Eh	1	02h	02h	02h	02h	02h	02h	02h
	Peripheral descriptor length	01A2Fh	1	5Ch	60h	60h	61h	61h	60h	60h
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Dh	0Eh 2Dh	0Eh 2Dh	0Eh 2Dh	0Eh 2Dh	0Eh 2Dh	0Eh 2Dh
	Memory 4		2	2Ah 70h	2Ah 60h	2Ah 60h	2Ah 50h	2Ah 50h	2Ah 40h	2Ah 40h
	Memory 5		2/1	8Eh	90h	90h	91h 8Eh	91h 8Eh	92h	92h
	Delimiter		1	00h	00h	00h	00h	00h	00h	00h
	Peripheral count		1	1Eh	20h	20h	20h	20h	20h	20h
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-S		2	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h
	Port Mapping		2	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1 and 2		2	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3 and 4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5 and 6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h

Table 6-53. Device Descriptors⁽¹⁾ (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE						
				F5304	F5308 RGC, ZQE	F5308 RGZ, PT	F5309 RGC, ZQE	F5309 RGZ, PT	F5310 RGC, ZQE	F5310 RGZ, PT
Peripheral Descriptor (continued)	JTAG		2	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A, USCI_B		2	10h 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A, USCI_B		2	N/A	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h
	ADC10_A		2	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h
	COMP_B		2	N/A	18h A8h	18h A8h	18h A8h	18h A8h	18h A8h	18h A8h
	LDO		2	1Ch 5Ch	04h 5Ch	04h 5Ch	04h 5Ch	04h 5Ch	04h 5Ch	04h 5Ch
Interrupts	COMP_B		1	01h	A8h	A8h	A8h	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h	40h	40h
	USCI_A0		1	01h	90h	90h	90h	90h	90h	90h
	USCI_B0		1	01h	91h	91h	91h	91h	91h	91h
	ADC10_A		1	D0h	D0h	D0h	D0h	D0h	D0h	D0h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h	61h	61h
	LDO-PWR		1	5Ch	5Ch	5Ch	5Ch	5Ch	5Ch	5Ch
	DMA		1	46h	46h	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h	68h	68h
	Delimiter		1	00h	00h	00h	00h	00h	00h	00h

7 器件和文档支持

7.1 入门和后续步骤

有关 MSP430 系列器件以开发协助工具和库的更多信息, 请访问 [MSP430 超低功耗传感和测量 MCU 概述](#)。

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [图 7-1](#) provides a legend for reading the complete device name.

MSP 430 F 5 438 A I ZQW T -EP		
Processor Family	MCU Platform	Optional: Additional Features
	Device Type	Optional: Tape and Reel
	Series	Packaging
	Feature Set	Optional: Temperature Range
		Optional: A = Revision
Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	Memory Type C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	Specialized Application AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C) -Q1 = Automotive Q100 Qualified	

图 7-1. Device Nomenclature

7.3 工具与软件

所有 MSP 微控制器均受多种软件和硬件开发工具的支持。相关工具由 TI 以及多家第三方供应商提供。请参阅 [MSP430 超低功耗 MCU – 工具与软件](#)，了解所有工具。

表 7-1 列出了 MSP430F530x 和 MSP430F5310 MCU 的调试功能。请参阅《[适用于 MSP430 的 Code Composer Studio 用户指南](#)》，以了解可用功能的详细信息。

表 7-1. 硬件调试 特性

MSP430 架构	四线制 JTAG	两线制 JTAG	断点 (N)	范围断点	时钟控制	状态序列发生器	跟踪缓冲器	LPMx.5 调试支持
MSP430Xv2	有	有	3	有	是	否	否	否

设计套件与评估模块

适用于 MSP430F5x MCU 的 64 引脚目标开发板 MSP-TS430PN64B 是一款独立的 64 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy-Bi-Wire（两线制 JTAG）协议在系统内对 MSP430 MCU 进行编程和调试。

适用于 MSP430F5x MCU 的 64 引脚目标开发板和 MSP-FET 编程器捆绑包 MSP-FET 是一款强大的闪存仿真工具，可在 MSP430 MCU 上快速开始应用开发。它包含 USB 调试接口，用于通过 JTAG 接口或节省引脚的 Spy-Bi-Wire（两线制 JTAG）协议在系统内对 MSP430 进行编程和调试。只需按几下键即可在数秒钟内擦除闪存并对其进行编程，此外，由于 MSP430 闪存具有超低功耗，因此无需外部电源。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 MCU 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430F530x、MSP430F5310 代码示例 根据不同应用需求配置各集成外设的 C 代码示例。

MSP 驱动程序库 驱动程序库的抽象化 API 通过提供易于使用的函数调用使您不再拘泥于 MSP430 硬件的细节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可以使用驱动程序库功能，以最低开销编写完整项目。

MSP EnergyTrace™ 技术 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

ULP（超低功耗）Advisor ULP Advisor™ 软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP 和 MSP432 微控制器独特的超低功耗功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地利用应用程序。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

IEC60730 软件包 IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 中运行的客户应用，从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

适用于 MSP 的定点数学运算库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时应用，而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP430 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。这是标量函数的浮点数学运算库，能够充分利用器件的智能外设，使性能提升高达 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio 和 IAR IDE 中。如需深入了解该数学运算库及相关基准，请阅读用户指南。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio 是一种集成开发环境 (IDE)，支持所有 MSP 微控制器。Code Composer Studio 包含一整套开发和调试嵌入式应用的嵌入式软件实用程序的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种功能。直观的 IDE 提供了单个用户界面，有助于完成应用程序开发流程的每个步骤。熟悉的实用程序和界面可提升用户的入门速度。Code Composer Studio 将 Eclipse 软件框架的优点和 TI 先进的嵌入式调试功能相结合，为嵌入式开发人员提供了一种功能丰富的优异开发环境。当 CCS 与 MSP MCU 搭配使用时，可以使用独特而强大的插件和嵌入式软件实用程序，从而充分利用 MSP 微控制器的功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件 (.txt 或 .hex 文件) 直接下载到 MSP 微控制器，而无需使用 IDE。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件，以进行验证和调试。MSP-FET 在主机和目标 MSP 间提供调试通信通道。此外，MSP-FET 还可在计算机的 USB 接口和 MSP UART 间提供反向通道 UART 连接。这为 MSP 编程器提供了一种在 MSP 和计算机上运行的终端之间进行串行通信的便捷方法。它还支持使用 BSL（引导加载程序）通过 UART 和 I²C 通信协议将程序（通常称为固件）加载到 MSP 目标中。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。MSP Gang 编程器配有扩展板，即“Gang 分离器”，可在 MSP Gang 编程器和多个目标器件间实施互连。提供了八条电缆，用于将扩展板与八个目标器件相连（通过 JTAG 或 SPY-Bi-Wire 连接器）。编程工作可在 PC 或独立设备上完成。PC 端具备基于 DLL 的图形化用户界面。

7.4 文档支持

以下文档介绍 MSP430F5310 和 MSP430F530x 器件。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见表 7-2）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

- 《[MSP430F5310 器件勘误表](#)》 说明了针对 MSP430F5310 器件功能技术规格的已知例外情况。
- 《[MSP430F5309 器件勘误表](#)》 说明了针对 MSP430F5309 器件功能技术规格的已知例外情况。
- 《[MSP430F5308 器件勘误表](#)》 说明了针对 MSP430F5308 器件功能技术规格的已知例外情况。
- 《[MSP430F5304 器件勘误表](#)》 说明了针对 MSP430F5304 器件功能技术规格的已知例外情况。

用户指南

- 《[MSP430F5xx 和 MSP430F6xx 系列用户指南](#)》 详细介绍了该器件系列提供的模块和外设。
- 《[MSP430 闪存器件引导加载程序 \(BSL\) 用户指南](#)》 MSP430 引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 可根据相关要求进行变更。不要将此处的引导加载程序与某些数字信号处理器 (DSP) 中将外部存储器中的程序代码（和数据）自动加载到 DSP 内部存储器的引导加载程序混为一谈。
- 《[通过 JTAG 接口对 MSP430 进行编程](#)》 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。
- 《[MSP430 硬件工具用户指南](#)》 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

- 《[MSP430 32kHz 晶体振荡器](#)》 选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。
- 《[MSP430 系统级 ESD 注意事项](#)》 随着芯片技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告阐述了三个不同的 ESD 主题，以帮助电路板设计人员和 OEM 了解并实现强大的系统级设计：(1) 组件级 ESD 测试和系统级 ESD 测试；(2) 实现系统级 ESD 保护的通用设计指南；(3) 系统高效 ESD 设计 (SEED) 简介，这是一种板载和片上 ESD 保护协同设计方法。该应用报告介绍了一些真实的系统级 ESD 保护设计示例及其结果。

7.5 相关链接

表 7-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 7-2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
MSP430F5310	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5309	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5308	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5304	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

7.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的《使用条款》。

TI E2E™ 社区

TI 的工程师交流 (E2E) 社区。此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页

德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.7 商标

MSP430Ware, EnergyTrace, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

7.8 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.9 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5304IPT	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5304
MSP430F5304IPT.B	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5304
MSP430F5304IPTR	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5304
MSP430F5304IPTR.B	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5304
MSP430F5304IRGZR	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5304
MSP430F5304IRGZR.B	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5304
MSP430F5304IRGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5304
MSP430F5304IRGZT.B	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5304
MSP430F5308IPT	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IPT.B	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IPTR	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IPTR.B	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IRGCR	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IRGCR.B	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IRGCT	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IRGCT.B	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5308
MSP430F5308IRGZR	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5308
MSP430F5308IRGZR.B	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5308
MSP430F5308IRGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5308
MSP430F5308IRGZT.B	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5308

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5308IZXH	Active	Production	NFBGA (ZXH) 80	576 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5308
MSP430F5308IZXH.B	Active	Production	NFBGA (ZXH) 80	576 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5308
MSP430F5308IZXHR	Active	Production	NFBGA (ZXH) 80	2500 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5308
MSP430F5308IZXHR.B	Active	Production	NFBGA (ZXH) 80	2500 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5308
MSP430F5309IPT	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5309
MSP430F5309IPT.B	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5309
MSP430F5309IRGCR	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5309
MSP430F5309IRGCR.B	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5309
MSP430F5309IRGCT	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5309
MSP430F5309IRGCT.B	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5309
MSP430F5309IRGZR	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5309
MSP430F5309IRGZR.B	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5309
MSP430F5309IRGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5309
MSP430F5309IRGZT.B	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5309
MSP430F5309IZXH	Active	Production	NFBGA (ZXH) 80	576 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5309
MSP430F5309IZXH.B	Active	Production	NFBGA (ZXH) 80	576 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5309
MSP430F5309IZXHR	Active	Production	NFBGA (ZXH) 80	2500 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5309
MSP430F5309IZXHR.B	Active	Production	NFBGA (ZXH) 80	2500 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5309
MSP430F5310IPT	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IPT.B	Active	Production	LQFP (PT) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IPTR	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IPTR.B	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5310IRGCR	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IRGCR.B	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IRGCRG4	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IRGCRG4.B	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IRGCT	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IRGCT.B	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5310
MSP430F5310IRGZR	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5310
MSP430F5310IRGZR.B	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5310
MSP430F5310IRGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5310
MSP430F5310IRGZT.B	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5310
MSP430F5310IZQE	Obsolete	Production	BGA MICROSTAR JUNIOR (ZQE) 80	-	-	Call TI	Call TI	-40 to 85	M430F5310
MSP430F5310IZQER	Obsolete	Production	BGA MICROSTAR JUNIOR (ZQE) 80	-	-	Call TI	Call TI	-40 to 85	M430F5310
MSP430F5310IZXH	Active	Production	NFBGA (ZXH) 80	576 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5310
MSP430F5310IZXH.B	Active	Production	NFBGA (ZXH) 80	576 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5310
MSP430F5310IZXHR.B	Active	Production	NFBGA (ZXH) 80	2500 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5310

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

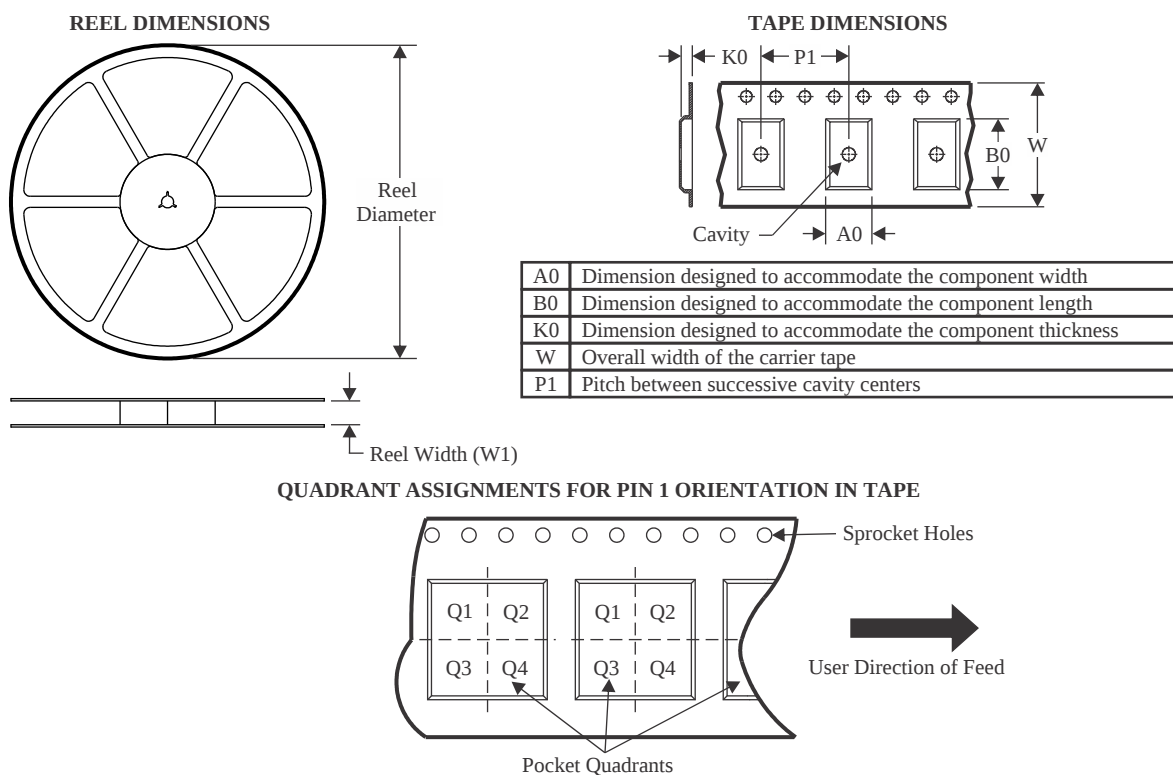
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

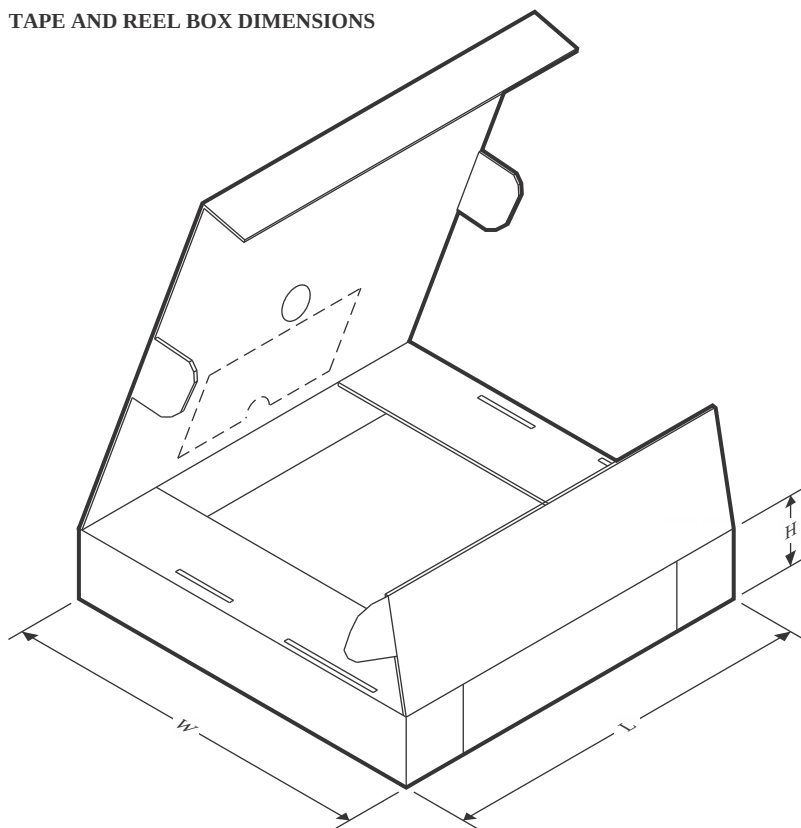


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5304IPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430F5304IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5304IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5308IPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430F5308IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5308IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5308IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5308IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5308IZXHR	NFBGA	ZXH	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5309IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5309IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5309IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5309IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5309IZXHR	NFBGA	ZXH	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5310IPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430F5310IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5310IRGCRG4	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5310IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5310IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5310IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

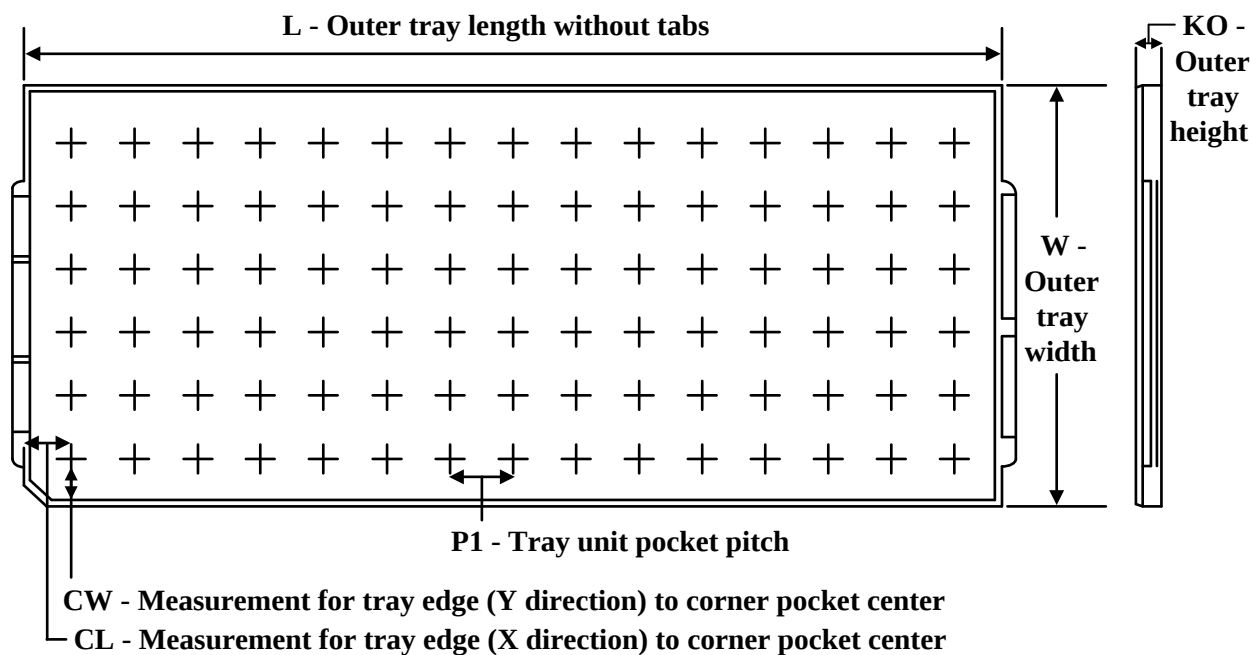


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5304IPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430F5304IRGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
MSP430F5304IRGZT	VQFN	RGZ	48	250	213.0	191.0	35.0
MSP430F5308IPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430F5308IRGCR	VQFN	RGC	64	2000	353.0	353.0	32.0
MSP430F5308IRGCT	VQFN	RGC	64	250	213.0	191.0	35.0
MSP430F5308IRGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
MSP430F5308IRGZT	VQFN	RGZ	48	250	213.0	191.0	35.0
MSP430F5308IZXHR	NFBGA	ZXH	80	2500	350.0	350.0	43.0
MSP430F5309IRGCR	VQFN	RGC	64	2000	353.0	353.0	32.0
MSP430F5309IRGCT	VQFN	RGC	64	250	213.0	191.0	35.0
MSP430F5309IRGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
MSP430F5309IRGZT	VQFN	RGZ	48	250	213.0	191.0	35.0
MSP430F5309IZXHR	NFBGA	ZXH	80	2500	350.0	350.0	43.0
MSP430F5310IPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430F5310IRGCR	VQFN	RGC	64	2000	353.0	353.0	32.0
MSP430F5310IRGCRG4	VQFN	RGC	64	2000	353.0	353.0	32.0
MSP430F5310IRGCT	VQFN	RGC	64	250	213.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5310IRGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
MSP430F5310IRGZT	VQFN	RGZ	48	250	213.0	191.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F5304IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5304IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5308IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5308IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5308IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5308IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5308IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5308IZXHR	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5308IZXHR.B	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5309IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5309IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5309IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5309IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5309IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5309IZXHR	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F5309IZXHR.B	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5310IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5310IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5310IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5310IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5310IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5310IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5310IZXHR.B	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7

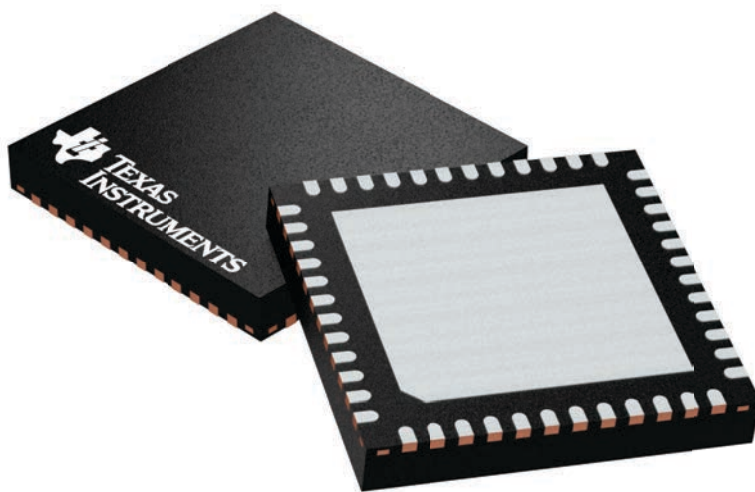
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

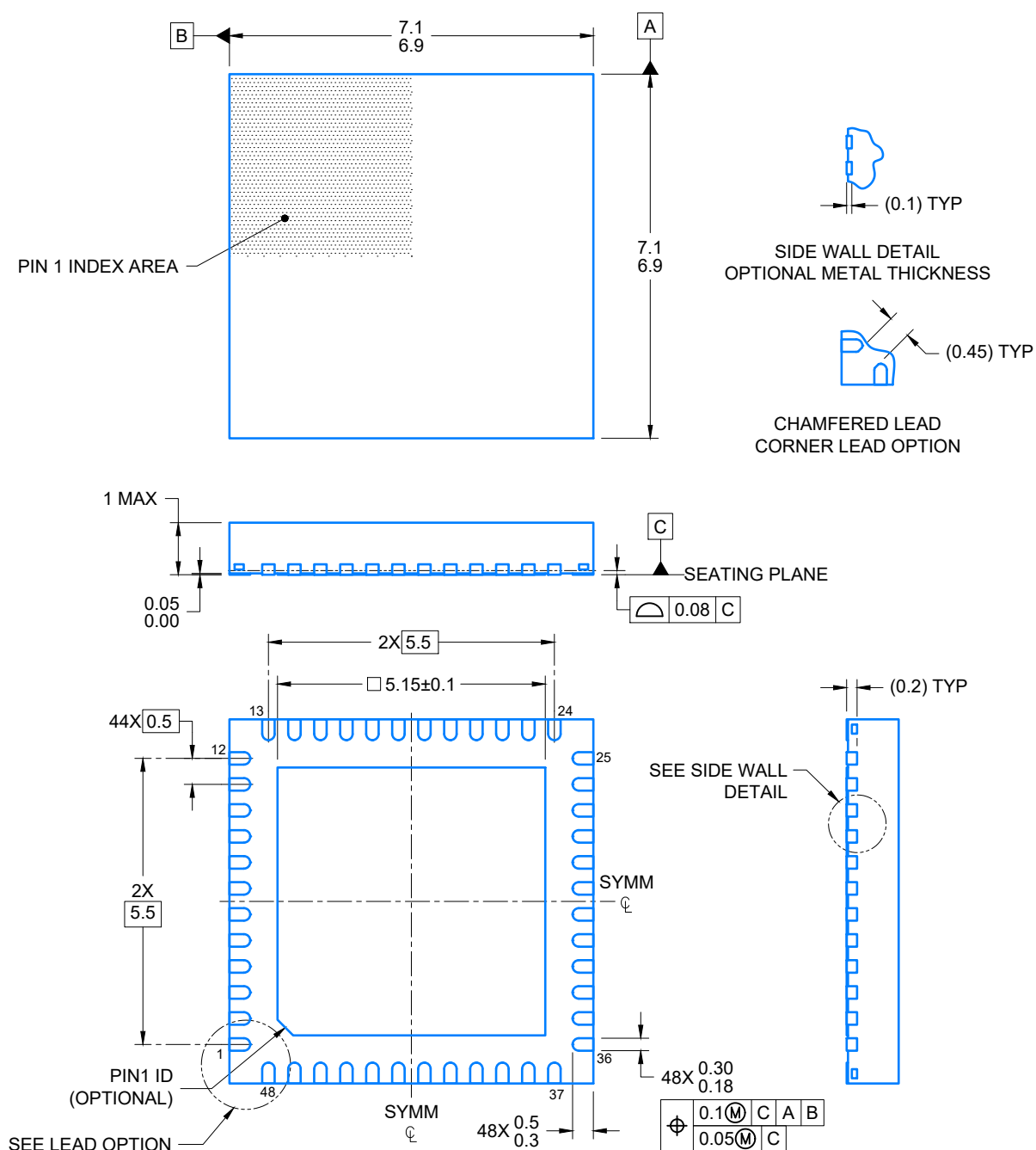
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

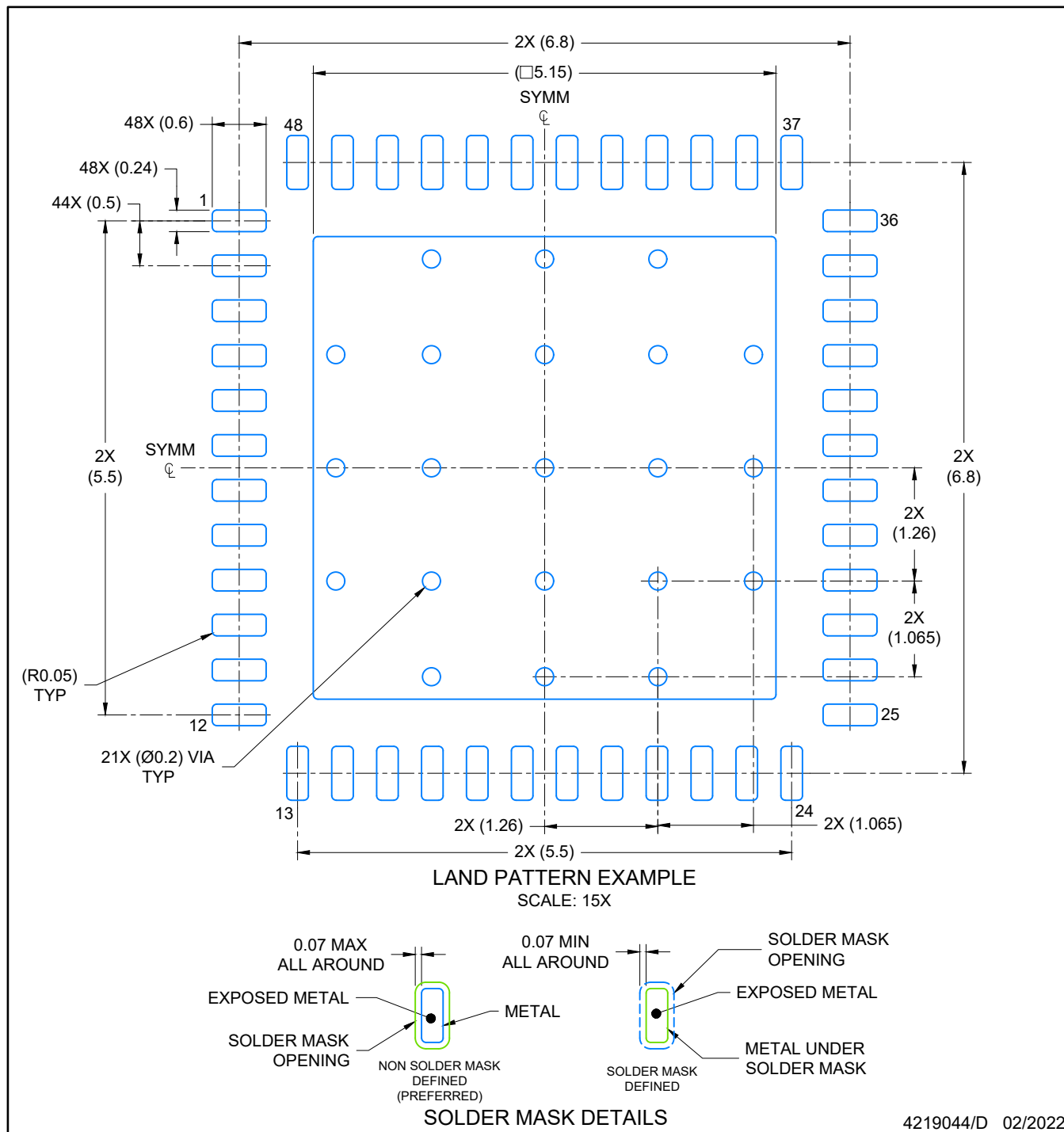
4224671/A



4219044/D 02/2022

NOTES:

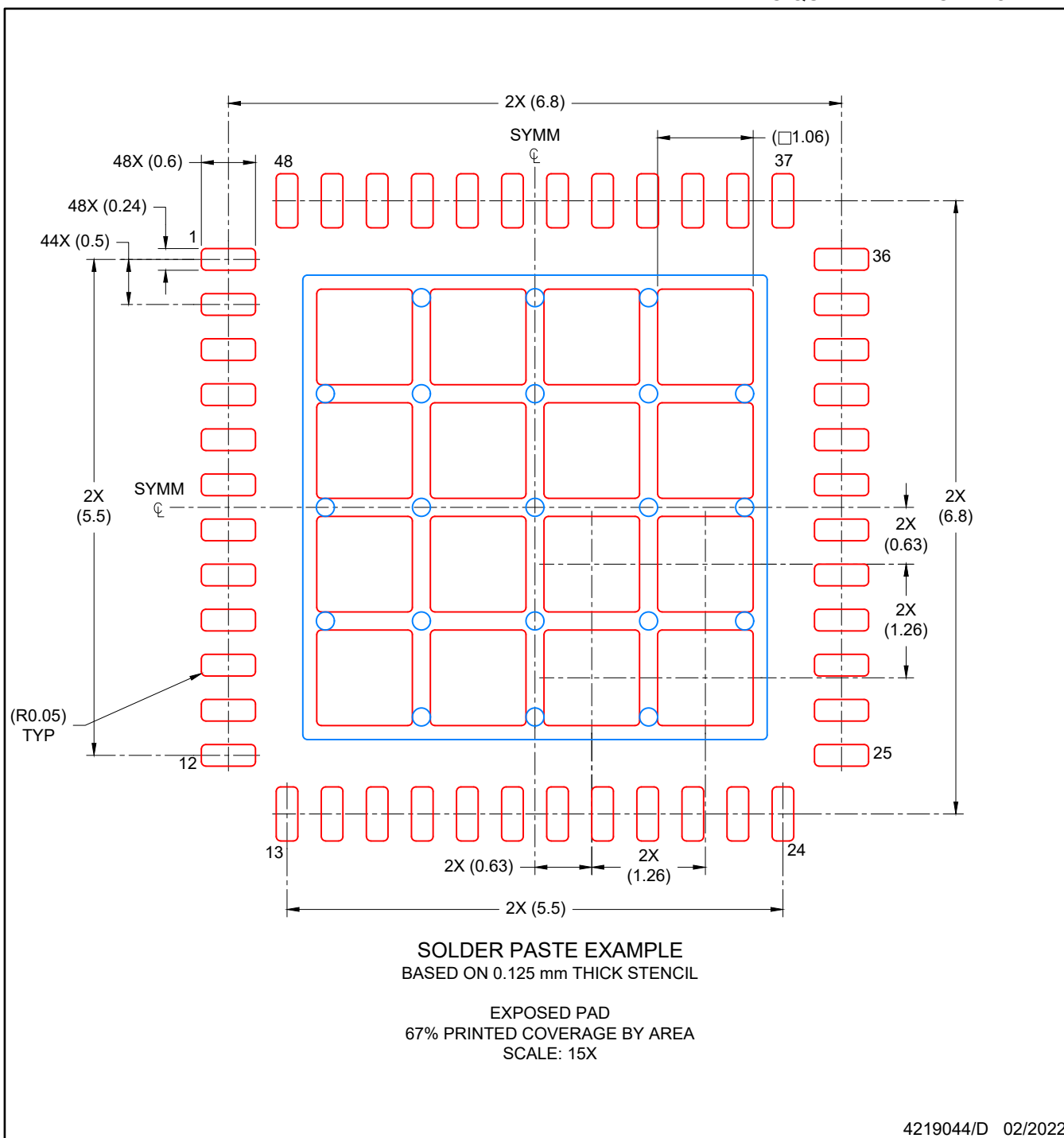
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



4219044/D 02/2022

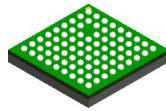
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

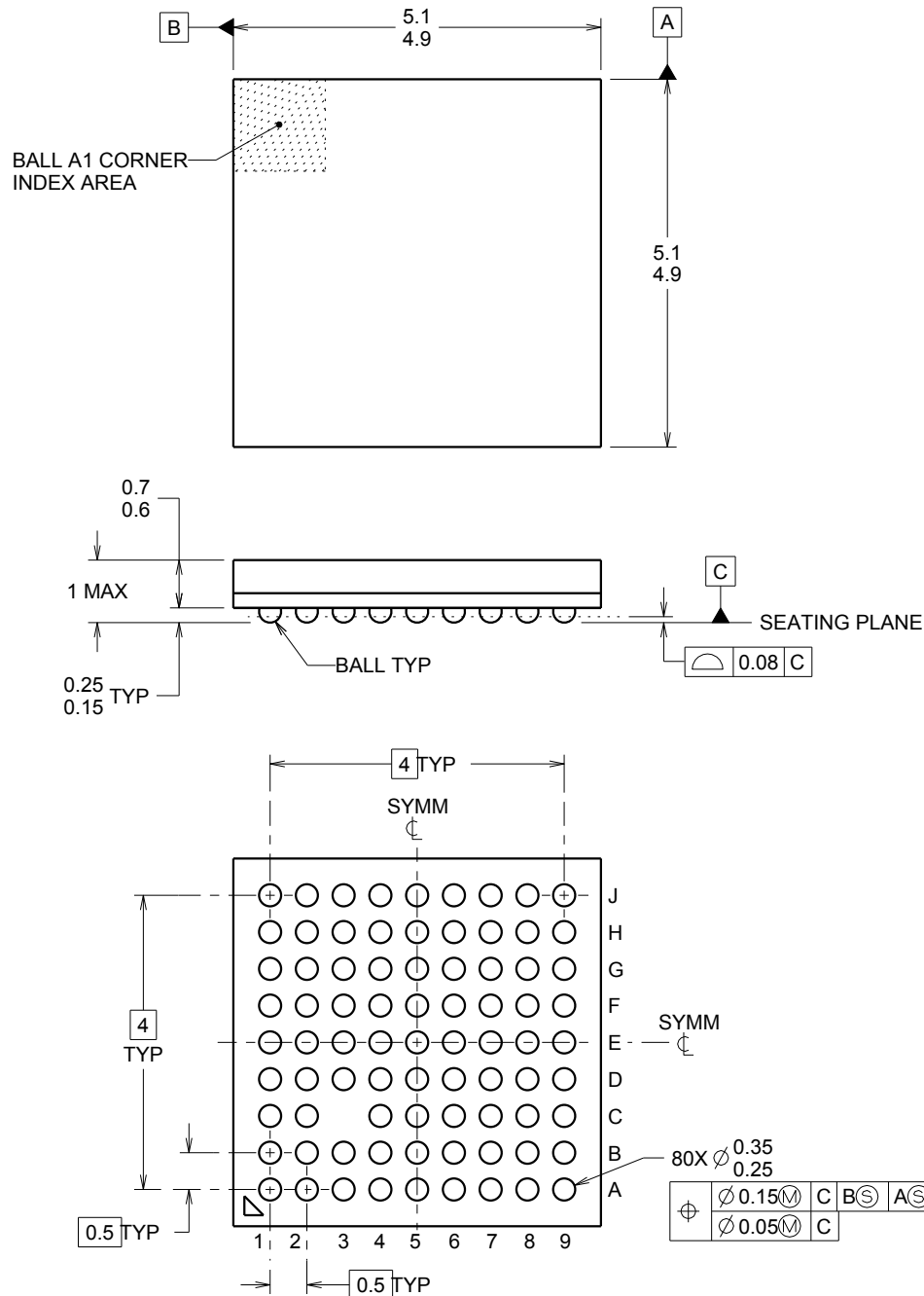


ZXH0080A

PACKAGE OUTLINE

NFBGA - 1 mm max height

BALL GRID ARRAY



4221325/A 01/2014

NOTES:

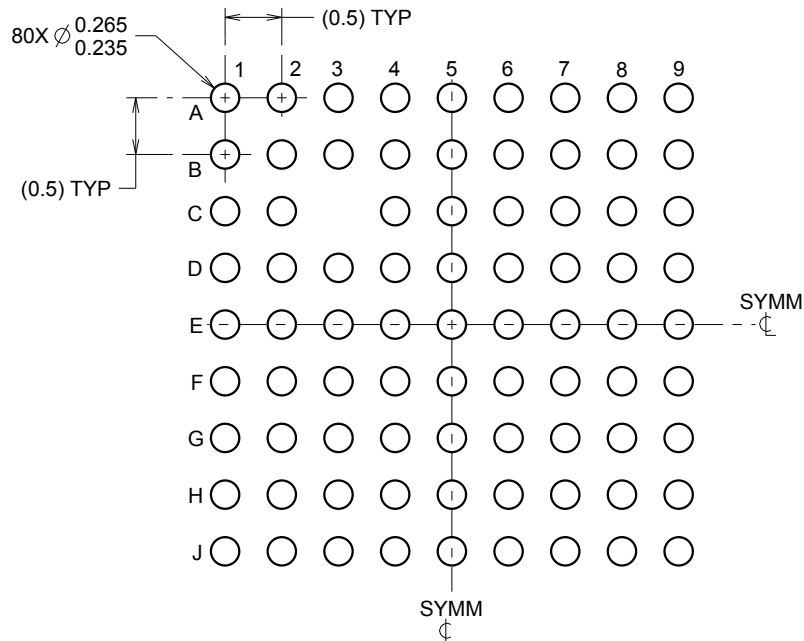
1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.

EXAMPLE BOARD LAYOUT

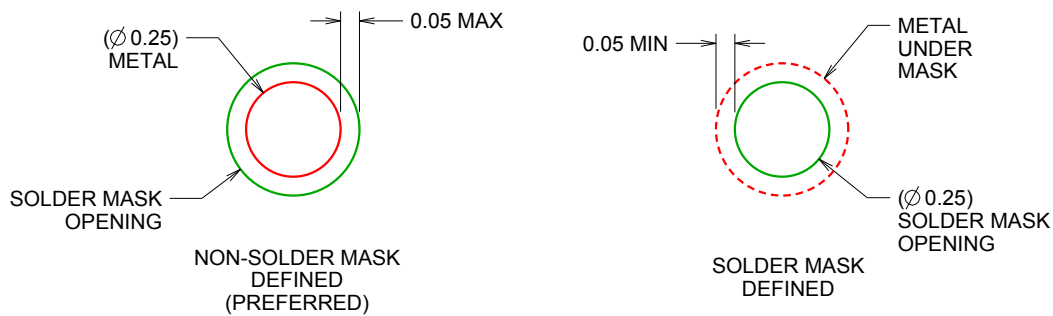
ZXH0080A

NFBGA - 1 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

4221325/A 01/2014

NOTES: (continued)

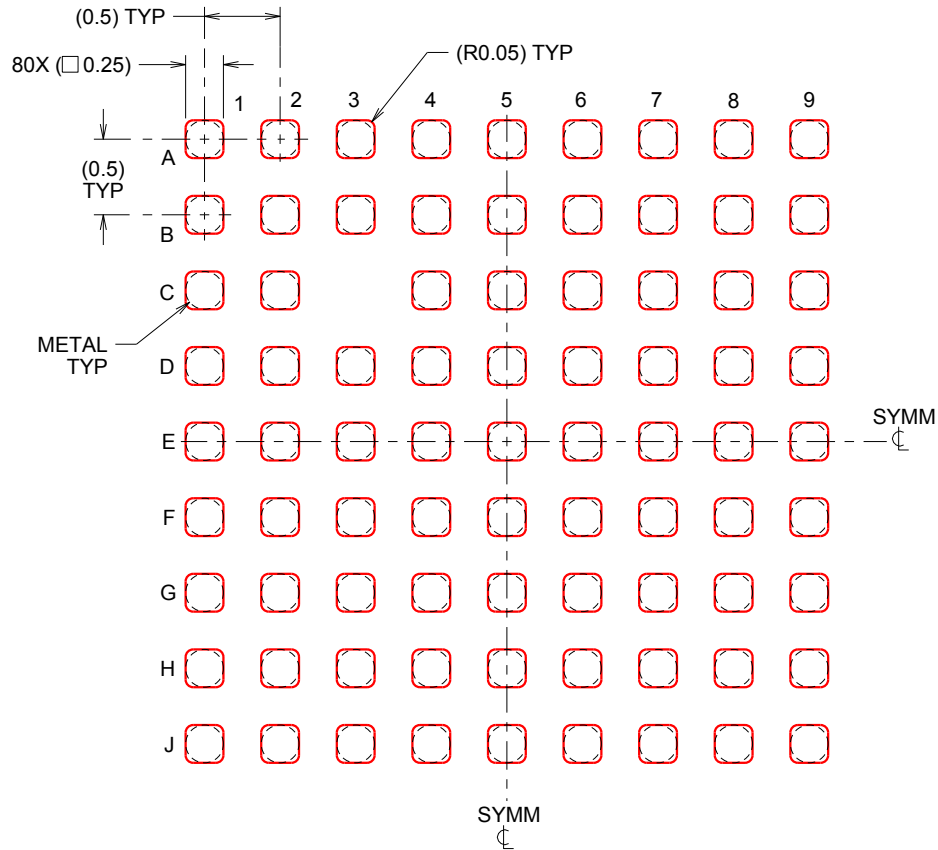
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

ZXH0080A

NFBGA - 1 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 SCALE:20X

4221325/A 01/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



LQFP - 1.6 mm max height

Technical drawing of a square electronic component, likely a microchip, showing dimensions and feature callouts.

Top View Dimensions:

- Overall width: 9.2
- Overall height: 9.2
- Distance from top edge to center of top pins: 8.8
- Distance from left edge to center of left pins: 7.2
- Distance from right edge to center of right pins: 6.8
- Distance from bottom edge to center of bottom pins: 7.2
- Distance from left edge to center of left pins: 6.8

Pin Dimensions:

- Pin pitch (distance between adjacent pins): 0.5
- Pin width: 0.27
- Pin thickness: 0.17
- Pin length: 48X
- Pin spacing (distance between pin groups): 44X
- Pin group width: 5.5

Feature Callouts:

- SEE DETAIL A:** Points to a circular detail view of the pin profile.
- 1.6 MAX:** Dimension for the height of the pin profile.
- 0.08 M C A B:** Feature control frame for the pin profile, indicating a maximum material condition (M) and a tolerance of 0.08.
- 0.1 C:** Feature control frame for the seating plane, indicating a tolerance of 0.1.
- SEATING PLANE:** The surface of the component that mates with the carrier.
- 0.25 GAGE PLANE:** The surface used for gaging the component.
- 0.75 0.45:** Dimensions for the gage plane.
- 0.05 MIN:** Dimension for the minimum thickness of the component.
- 0° - 7°:** Angle specification for the gage plane.

DETAIL A: A circular detail view showing the profile of the pins, with dimensions 0.25, 0.75, 0.45, 0.05 MIN, and 0° - 7°.

NOTES:

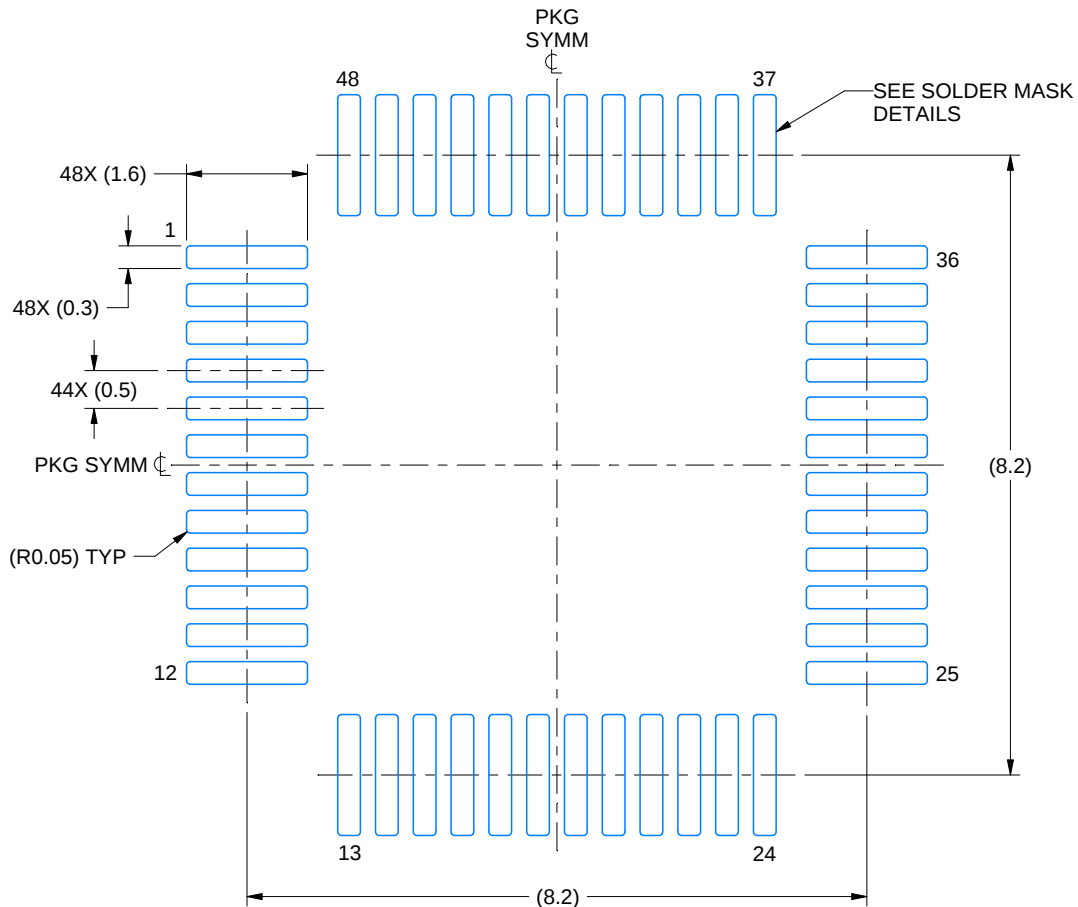
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

EXAMPLE BOARD LAYOUT

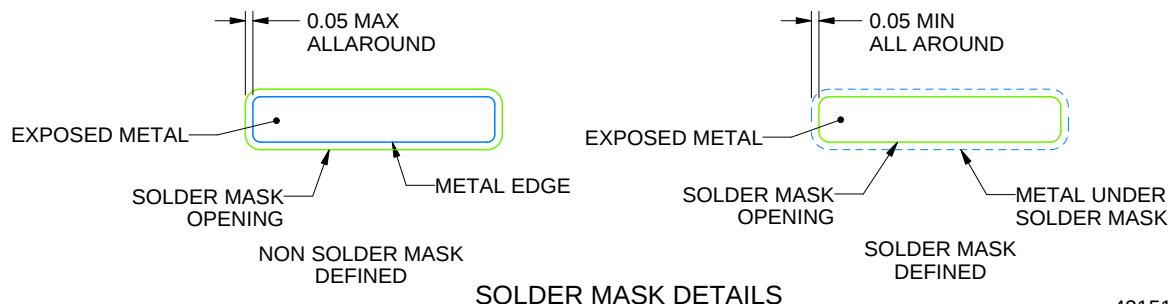
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



4215159/B 11/2023

NOTES: (continued)

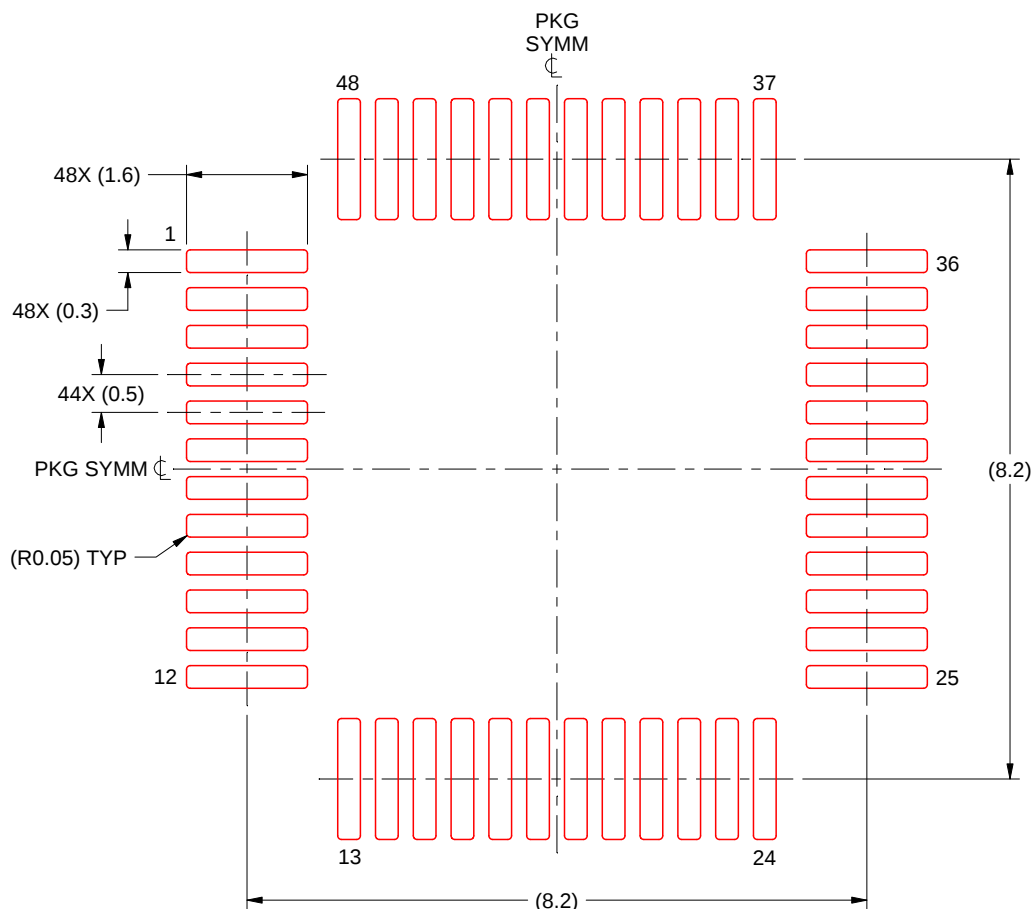
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

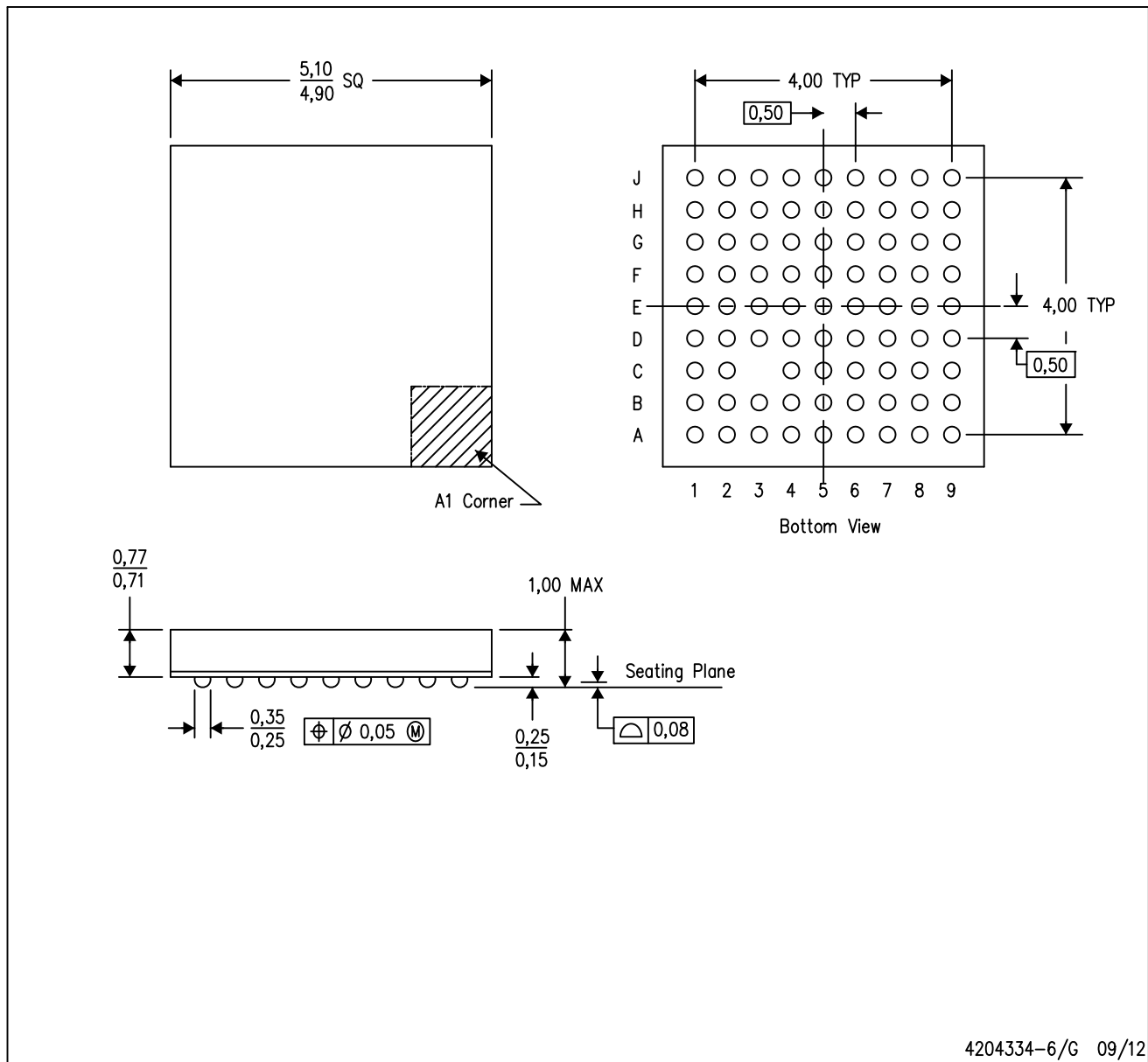
4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

ZQE (S-PBGA-N80)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225
 - D. This is a Pb-free solder ball design.

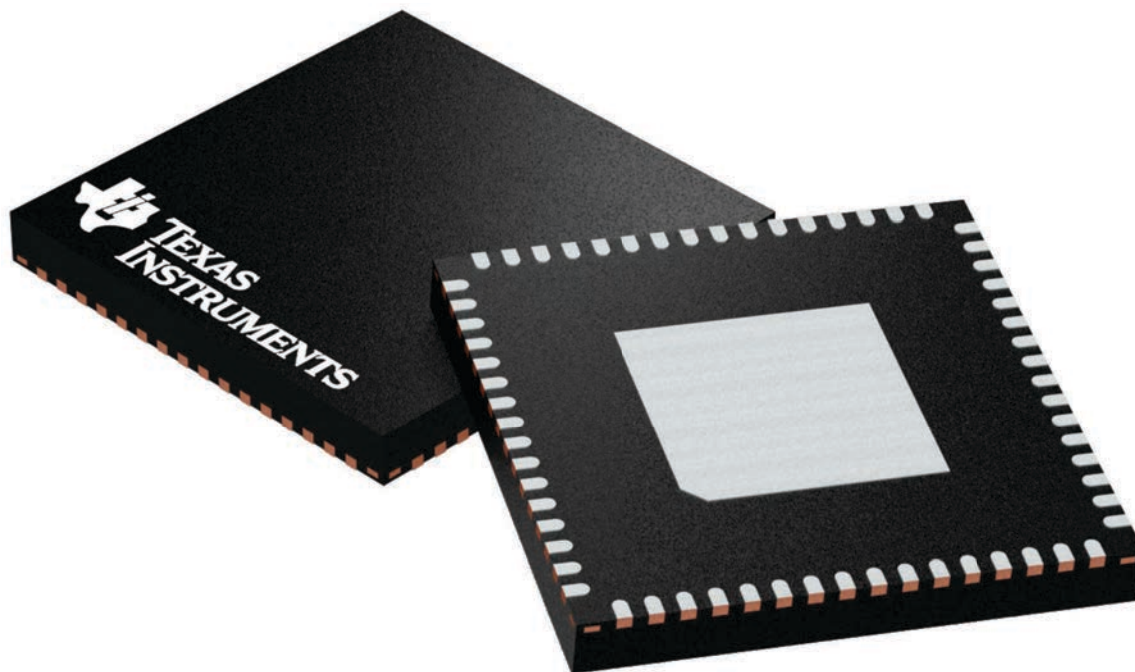
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

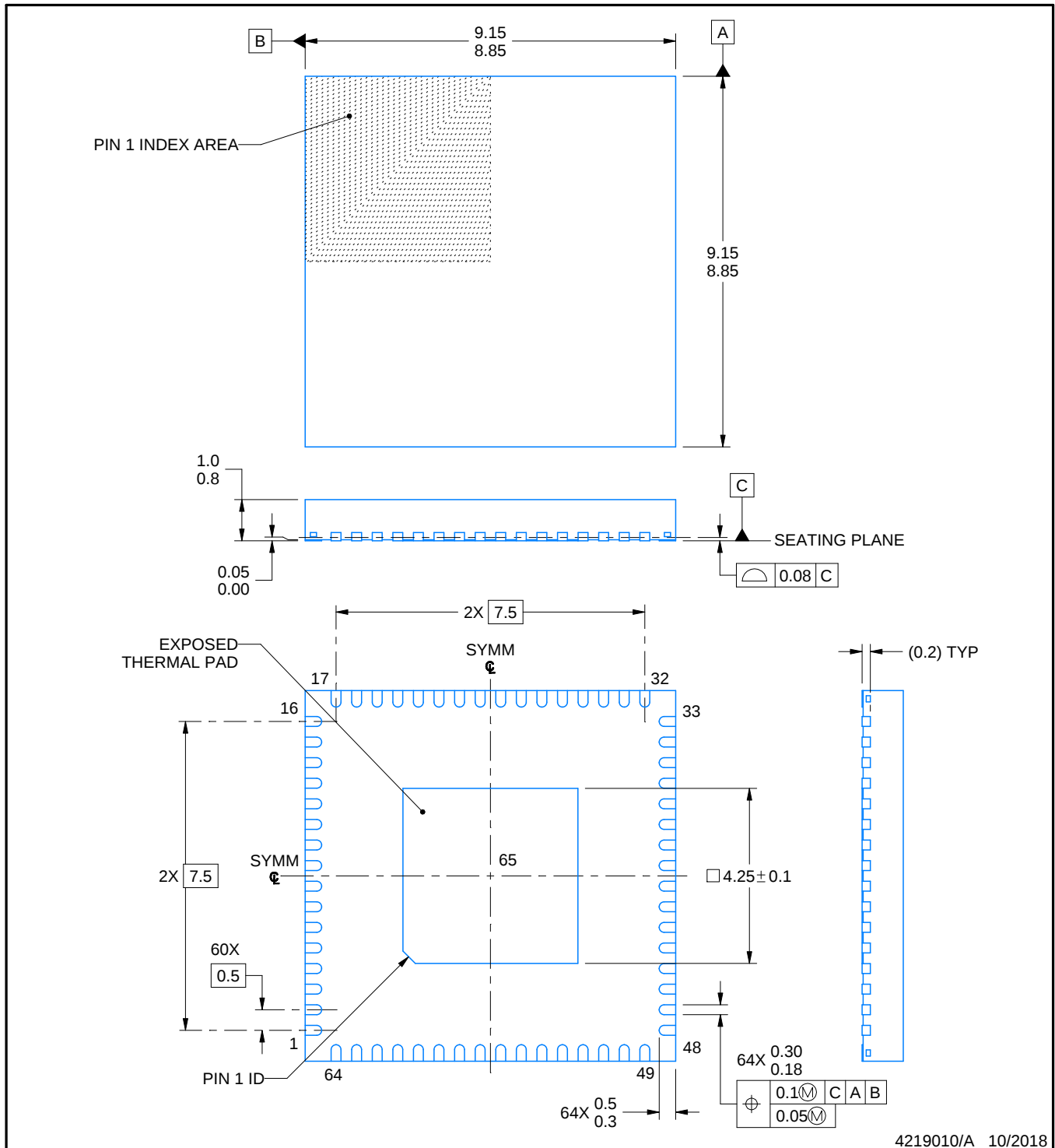
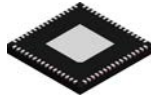
9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A



NOTES:

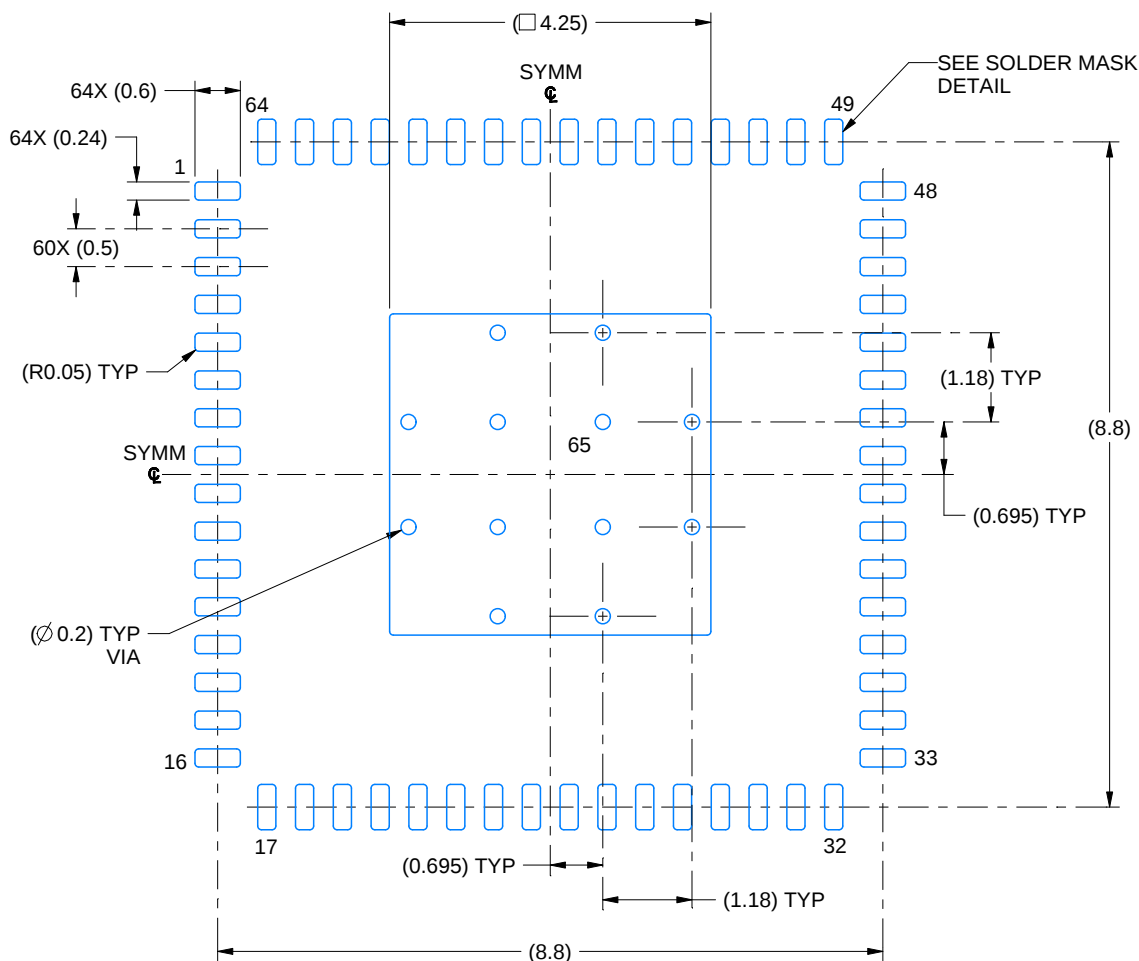
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

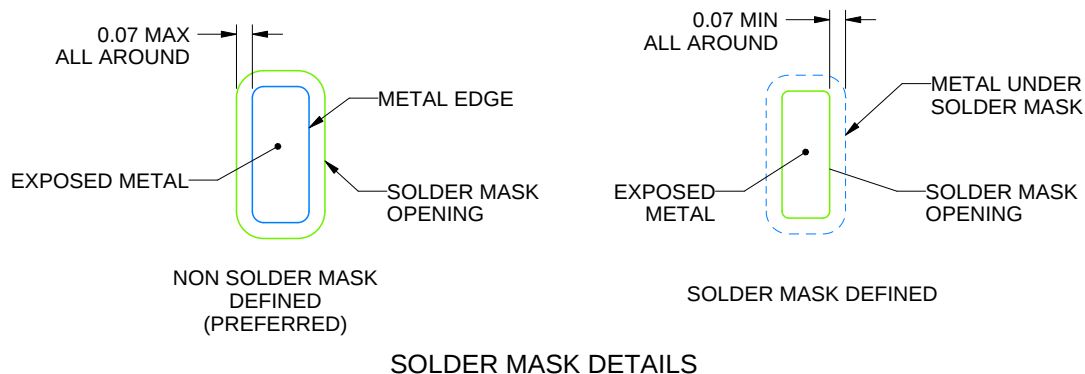
RGC0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

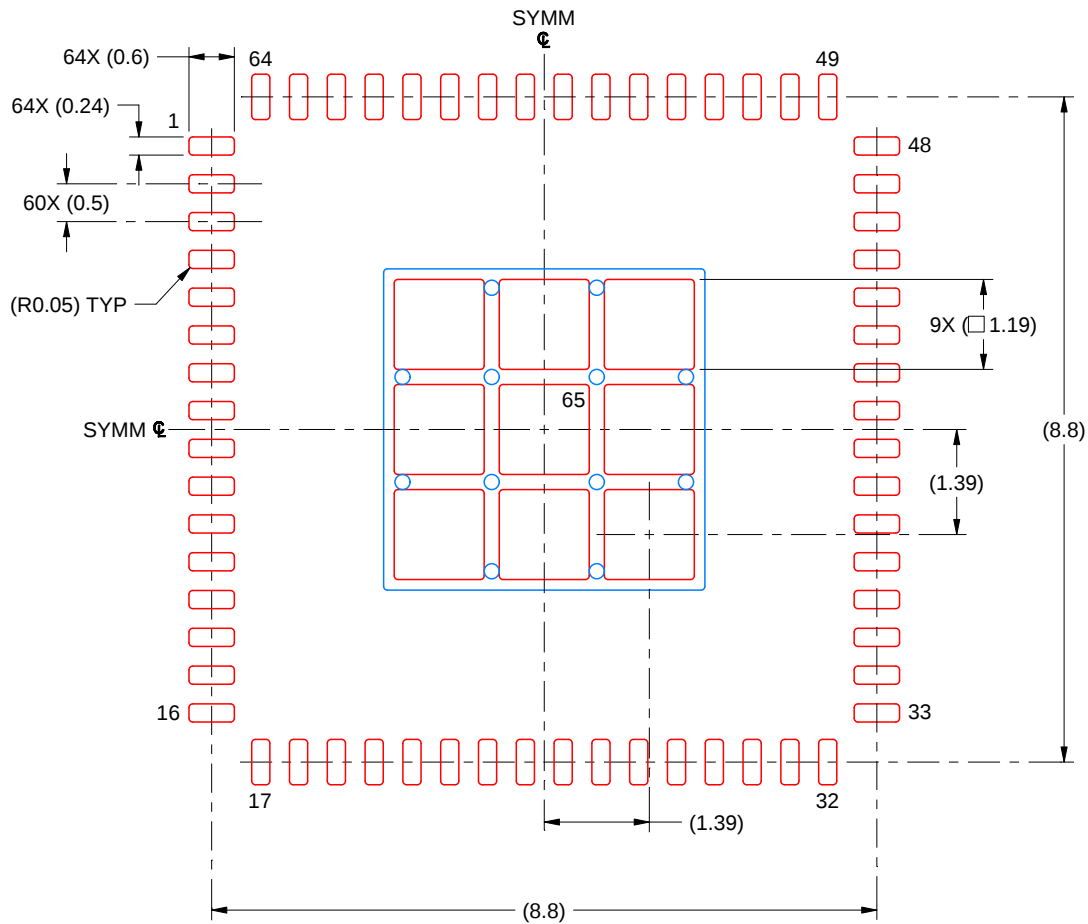
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGC0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 10X

EXPOSED PAD 65
 71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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