ONET1131EC 集成时钟和数据恢复 (CDR) 功能的外部调制激光器驱动器

1 特性

- 集成调制器驱动器，其最小输出幅值最高可达 2 Vpp（单端），偏置电流最高可达 150mA（拉电流）。
- 支持外部调制激光器，包括电吸收调制器激光器 (EML) 和基于 Mach-Zahnder 调制器 (MZM) 的激光器。
- 集成 CDR 功能，支持 9.80Gbps 至 11.7Gbps 无参考运行
- 集成数模转换器 (DAC) 和模数转换器 (ADC) 的双线制数字接口，可实现控制和诊断管理
- 输出极性选择
- 用于调节 CDR 带宽的可编程抖动传输带宽
- CDR 旁路模式，支持以低数据速率运行
- 具有可选监视器光电二极管 (PD) 范围的自动功率控制 (APC) 回路
- 可编程发送输入均衡器
- 发送器交叉点调节和去加重功能
- 包括激光安全 特性
- 电源监视器和温度传感器
- 2.5V 单电源
- 工作温度范围：-40°C 至 100°C
- 表面贴装 4mm x 4mm 32 引脚四方扁平无引线 (QFN) 封装（间距为 0.4mm）

2 应用

- 10Gbps 无源光纤网络 (PON)、针对 FTTx 部署的光线路终端 (OLT) 收发器
- XFP 和 SFP+ 10Gbps 同步光纤网络 (SONET) OC-192 光学收发器
- XFP 和 SFP+ 10GBASE-ER/ZR 光学收发器
- 8x 和 10x 光纤通道光学收发器

3 说明

ONET1131EC 是一款 2.5V EML 调制器驱动器，支持发送时钟和数据恢复 (CDR) 功能，无需基准时钟即可在 9.8Gbps 至 11.7Gbps 范围内运行。该器件在 CDR 旁路模式下能够以较低数据速率运行，其双线制串行接口支持针对 多项功能 （如输出极性选择和输入均衡）进行数字控制。

发送路径由 1 个可调节输入均衡器（可均衡长达 300mm
（12 英寸）FR4 印刷电路板微带或带状传输线）、1 个多速率 CDR 及 1 个输出调制器驱动器组成。该器件以交叉点调节和去加重的形式提供输出波形控制，从而增加光学眼图波罩裕度。该器件提供激光器偏置电流并集成自动功率控制 (APC) 回路，以补偿平均光学功率随电压、温度和时间的变化。

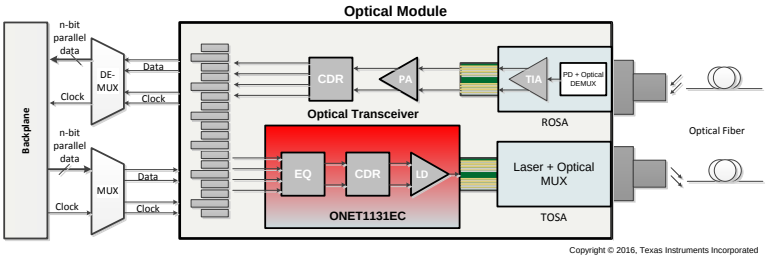
ONET1131EC 内置模数转换器和数模转换器，支持管理收发器，无需使用专用微控制器。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ONET1131EC	VQFN (32)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化框图



目录

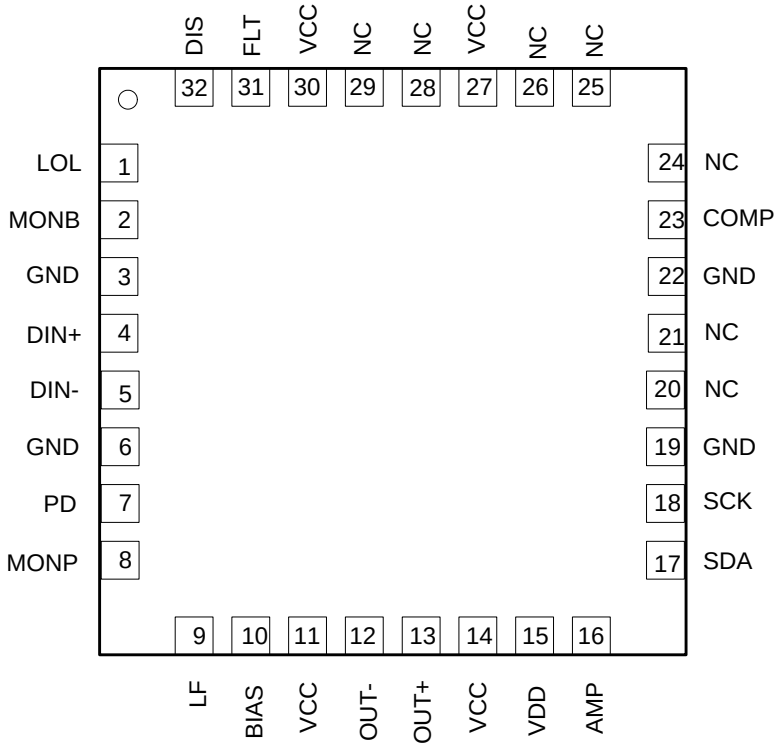
4 修订历史记录

日期	修订版本	注释
2016 年 9 月	*	首次发布。

5 Pin Configuration and Function

The ONET1131EC is packaged in a small footprint 4 mm x 4 mm 32 pin RoHS compliant QFN package with a lead pitch of 0.4 mm.

RSM Package
32 PIN VQFN
(Top View)



Pin Functions

NUMBER	NAME	Type	DESCRIPTION
LOL	1	Digital-out	Loss of lock indicator. High level indicates the transmitter CDR is out of lock. Open drain output. Requires an external 4.7 kΩ to 10 kΩ pull-up resistor to VCC for proper operation. This pin is 3.3 V tolerant.
MONB	2	Analog-out	Bias current monitor.
GND	3, 6, 19, 22	Supply	Circuit ground.
DIN+	4	Analog-in	Non-inverted transmitter data input. On-chip differentially 100 Ω terminated to TXIN–. Must be AC coupled.
DIN–	5	Analog-in	Inverted transmitter data input. On-chip differentially 100 Ω terminated to TXIN+. Must be AC coupled.
PD	7	Analog	Photodiode input. Pin can source or sink current dependent on register setting.
MONP	8	Analog-out	Photodiode current monitor.
LF	9	Analog-in	Transmitter loop filter capacitor.
BIAS	10	Analog	Sinks or sources the bias current for the laser in both APC and open loop modes.
VCC	11, 14, 27, 30	Supply	2.5 V ± 5% supply.
OUT–	12	CML-out	Inverted transmitter data output. Internally terminated in single-ended operation mode.
OUT+	13	CML-out	Non-Inverted transmitter data output.
VDD	15	Supply	2.5 V ± 5% supply for the digital circuitry.
AMP	16	Analog-in	Output amplitude control. Output amplitude can be adjusted by applying a voltage of 0 to 2 V to this pin. Leave open when not used.

Pin Functions (continued)

NUMBER	NAME	Type	DESCRIPTION
SDA	17	Digital-in/out	2-wire interface serial data input. Requires an external 4.7-kΩ to10-kΩ pull-up resistor to VCC. This pin is 3.3-V tolerant.
SCK	18	Digital-in	2-wire interface serial clock input. Requires an external 4.7-kΩ to10-kΩ pull-up resistor to VCC. This pin is 3.3-V tolerant.
NC	20, 21, 24, 25, 26, 28, 29		Do not connect
COMP	23	Analog	Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01-µF capacitor to ground.
FLT	31	Digital-out	Transmitter fault detection flag. High level indicates that a fault has occurred. Open drain output. Requires an external 4.7 kΩ to 10 kΩ pull-up resistor to VCC for proper operation. This pin is 3.3-V tolerant.
DIS	32	Digital-in	Disables the bias current when set to high state. Includes a 250-kΩ pull-up resistor to VCC. Requires an external 4.7 kΩ to 10 kΩ pull-up resistor to VCC for proper operation Toggle to reset a fault condition. This is an ORed function with the TXBIASEN bit (bit 2 in *register 1*). This pin is 3.3-V tolerant.

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	at VCC, VDD	–0.5	3	V
Voltage	at 3.3-V tolerant pins LOL, SDA, SCK, FLT, DIS	–0.5	3.6	V
	at all other pins MONB, DIN+, DIN–, PD, MONP, LF, BIAS, OUT–, OUT+, AMP, COMP	–0.5	3	V
Maximum current at transmitter input pins	DIN+, DIN–		10	mA
Maximum current at transmitter output pins	OUT+, OUT–		125	mA
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		2.37	2.5	2.63	V
V_{IH}	Digital input high voltage	DIS, SCK, SDA, 3.3-V tolerant IOs	2			V
V_{IL}	Digital input low voltage				0.8	V
	Photodiode current range	Control bit TXPDRNG = 1x, step size = 3 µA		3080		µA
		Control bit TXPDRNG = 01, step size = 1.5 µA		1540		
		Control bit TXPDRNG = 00, step size = 0.75 µA		770		
	Serial Data rate	TXCDR_DIS = 0	9.8		11.7	Gbps
		TXCDR_DIS = 1	1		11.7	
V_{AMP}	Amplitude control input voltage range		0		2	V
$t_{R(IN)}$	Input rise time	20%–80%		30	45	ps
$t_{F(IN)}$	Input fall time	20%–80%		30	45	ps
T_C	Temperature at thermal pad		–40		100	°C

6.4 Thermal Information

THERMAL METRIC(1)		RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	30.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

Over recommended operating conditions, open loop operation, V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 80 mA, unless otherwise noted. Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.37	2.5	2.63	V
I_{VCC}	Supply current in single-ended TX mode with CDRs enabled	TXMODE = 1, TXCDR_DIS = 0, TX V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA		158	193	mA
	Power dissipation in single-ended TX mode with CDRs enabled			380	508	mW
	Supply current in differential TX mode with CDRs enabled	TXMODE = 0, TXCDR_DIS = 0, TX V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA		197	237	mA
	Power dissipation in differential TX mode with CDRs enabled			493	623	mW
	Supply current in single-ended TX mode with CDRs disabled	TXMODE = 1, TXCDR_DIS = 1, TX V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA		119	193	mA
	Power dissipation in single-ended TX mode with CDRs disabled			298	376	mW
	Supply current in differential TX mode with CDRs disabled	TXMODE = 0, TXCDR_DIS = 1, TX V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA;		164	200	mA
	Power dissipation in differential TX mode with CDRs disabled			410	526	mW
$R_{(IN)}$	Data input resistance	Differential between DIN+ / DIN–		100		Ω
	Data input termination mismatch				5%	
$R_{(OUT)}$	Ooutput resistance	Single-ended at OUT+ or OUT–		60		Ω
	Digital input current	DIS pull up to VCC	–20		20	µA
V_{OH}	Digital output high voltage	LOL, FLT pull-up to V_{CC}, I_{SOURCE} = 37.5 µA	2.1			V
V_{OL}	Digital output low voltage	LOL, FLT pull-up to V_{CC}, I_{SINK} = 350 µA			0.4	V
$I_{(BIAS-MIN)}$	Minimum bias current	See (1)			5	mA
$I_{(BIAS-MAX)}$	Maximum bias current	Source. BIASPOL = 0, DAC set to maximum, open and closed loop	145	150		mA
		Sink. BIASPOL = 1, DAC set to maximum, open and closed loop	95	100		mA
$I_{(BIAS-DIS)}$	Bias current during disable				100	µA
	Average power stability	APC loop enabled		±0.5		dB
	Bias pin compliance voltage	Source. TXBIASPOL = 0			V_{CC} - 0.45	V
		Sink. TXBIASPOL = 1	0.45			V
	Temperature sensor accuracy	With 1-point external mid-scale calibration		±3		°C

(1) The bias current can be set below the specified minimum according to the corresponding register setting; however, in closed loop operation settings below the specified value may trigger a fault.

DC Electrical Characteristics (continued)

Over recommended operating conditions, open loop operation, V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 80 mA, unless otherwise noted. Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PD)}$	Photodiode reverse bias voltage	APC active, $I_{(PD)}$ = 1500 µA	1.3	2.3		V
	Photodiode fault current level	Percent of target $I_{(PD)}$ (2)		150%		
	Photodiode current monitor ratio	$I_{(MONP)}$ / $I_{(PD)}$ with control bit PDRNG = 1X	10%	12.5%	15%	
		$I_{(MONP)}$ / $I_{(PD)}$ with control bit PDRNG = 01	20%	25%	30%	
		$I_{(MONP)}$ / $I_{(PD)}$ with control bit TXPDRNG = 00	40%	50%	60%	
Monitor diode DMI accuracy		With external mid-scale calibration	–15%		15%	
Bias current monitor ratio		$I_{(MONB)}$ / $I_{(BIAS)}$ (nominal 1/100 = 1%), $V_{(MONB)}$ < 1.5V	0.9%	1%	1..1%	
Bias current DMI accuracy		$I_{(BIAS)}$ ≥ 20 mA	–15%		15%	
Power supply monitor accuracy		With external mid-scale calibration	–2%		2%	
$V_{CC(RST)}$	V_{CC} reset threshold voltage	V_{CC} voltage level which triggers power-on reset		1.8	2.1	V
$V_{CC(RSTHYS)}$	V_{CC} reset threshold voltage hysteresis			100		mV
$V_{(MONB-FLT)}$	Fault voltage at MONB	TXFLTEN = 1, TXDMONB = 0, Fault occurs if voltage at MONB exceeds this value	1.15	1.2	1.25	V
$V_{(MONP-FLT)}$	Fault voltage at MONP	TXFLTEN = 1, TXMONPFLT = 1, TXDMONP = 0, Fault occurs if voltage at MONP exceeds this value	1.15	1.2	1.25	V

(2) Specified by design over process, supply and temperature variation

6.6 AC Electrical Characteristics

Over recommended operating conditions, open loop operation, V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 80 mA unless otherwise noted. Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX INPUT SPECIFICATIONS						
	CDR lock range	CPRI, Ethernet, SONET, Fibre Channel	9.80		11.7	Gbps
SDD11	Differential input return loss	0.05 GHz < f ≤ 0.1 GHz	20			dB
		0.1 GHz < f ≤ 5.5 GHz	12	15		
		5.5 GHz < f < 12 GHz	8			
SDD11	Differential to common mode conversion	0.1 GHz < f < 12 GHz	10	15		dB
SDD11	Common mode input return loss	0.1 GHz < f < 12 GHz	3			dB
	Input AC common mode voltage tolerance		15			mV
	Total Non-DDJ	Total jitter less ISI			0.45	UI_{PP}
$T_{(JTX)}$	Total Jitter				0.65	UI_{PP}
$S_{(JTX)}$	Sinusoidal Jitter Tolerance	With addition of input jitter, See Figure 1				UI_{PP}
V_{IN}	Differential input voltage swing		100		1000	mV_{PP}
$EQ_{(boost)}$	EQ high freq boost	Maximum setting; 7 GHz	6	9		dB
TX OUTPUT SPECIFICATIONS						
	Differential output return loss	0.01 GHz < f < 12 GHz		12		dB
$V_{O(MIN)}$	Minimum output amplitude	AC Coupled Outputs, 50-Ω single-ended load			0.5	V_{PP}
TX OUTPUT SPECIFICATIONS in SINGLE-ENDED MODE of OPERATION (TXMODE = 1)						
$V_{O(MAX)}$	Maximum output amplitude	AC Coupled Outputs, 50-Ω load, single-ended	2			V_{PP}
	Output amplitude stability	AC Coupled Outputs, 50-Ω load, single-ended		230		mV_{PP}
	High Cross Point Control Range	50-Ω load, single-ended	70%	75%		
	Low Cross Point Control Range	50-Ω load, single-ended		35%	40%	
	Cross Point Stability	50-Ω load, single-ended	-5		5	pp
	Output de-emphasis	TXDEADJ[0..3] = 1111, TXPKSEL = 0		5		dB
		TXDEADJ[0..3] = 1111, TXPKSEL = 1		6		
TX OUTPUT SPECIFICATIONS in DIFFERENTIAL MODE of OPERATION (TXMODE = 0)						
$V_{O(MAX)}$	Maximum output amplitude	AC Coupled Outputs, 100-Ω differential load	3.6			V_{PP}
	Output amplitude stability	AC Coupled Outputs, 100-Ω differential load		230		mV_{PP}
	High Cross Point Control Range	100-Ω differential load	65%	75%		
	Low Cross Point Control Range	100-Ω differential load		35%	40%	
	Cross Point Stability	100-Ω differential load	–5		5	pp
	Output de-emphasis	TXDEADJ[0..3] = 1111, TXPKSEL = 0		5		dB
		TXDEADJ[0..3] = 1111, TXPKSEL = 1		6		
CDR SPECIFICATIONS						
$BW_{(TX)}$	Jitter Transfer Bandwidth	9.95 Gbps, PRBS31			8	MHz
$J_{(PTX)}$	Jitter Peaking	> 120 kHz			1	dB
$J_{GEN(rms)}$	Random RMS jitter generation	Clock pattern, 50 kHz to 80 MHz			6	mUI_{rms}
$J_{GEN(PP)}$	Total jitter generation	Clock pattern, 50 kHz to 80 MHz, BER = 10^{-12}			60	mUI_{PP}

6.7 Timing Requirements

Over recommended operating conditions, typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

			MIN	TYP	MAX	UNIT
$t_{(APC)}$	APC time constant	C_{APC} 0.01 µF, I_{PD} = 500 µA, PD coupling ratio CR = 150, PDRNG = 01		50		µs
$t_{(INIT1)}$	Power-on to initialize	Power-on to registers ready to be loaded		0.2	1	ms
$t_{(INIT2)}$	Initialize to transmit	Register load STOP command to part ready to transmit valid data			2	ms
$t_{(OFF)}$	Transmitter disable time	Rising edge of DIS to $I_{(BIAS)} \le 0.1 \times I_{(BIAS\text{-}NOMINAL)}$		1	5	µs
$t_{(ON)}$	Disable negate time	Falling edge of DIS to $I_{(BIAS)} \ge 0.9 \times I_{(BIAS\text{-}NOMINAL)}$			1	ms
$t_{(RESET)}$	DIS pulse width	Time DIS must held high to reset part	100			ns
$t_{(FAULT)}$	Fault assert time	Time from fault condition to FLT high			50	µs
OUTPUT SPECIFICATIONS in SINGLE-ENDED MODE of OPERATION (TXMODE = 1)						
$t_{R(OUTTX)}$	Output rise time	20% - 80%, AC Coupled Outputs, 50-Ω load, single-ended		30	42	ps
$t_{F(OUTTX)}$	Output fall time	20% - 80%, AC Coupled Outputs, 50-Ω load, single-ended		30	42	ps
$ISI_{(TX)}$	Intersymbol interference	TXEQ_DIS = 1, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage		4	12	ps
		TXEQ_DIS = 0, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage, maximum equalization with 18-inch transmission line at the input.		7		
$R_{(JTX)}$	Serial data output random jitter			0.4	0.75	ps_{RMS}
	Output de-emphasis width	TXPKSEL = 0		28		ps
		TXPKSEL = 1		35		
OUTPUT SPECIFICATIONS in DIFFERENTIAL MODE of OPERATION (TXMODE = 0)						
$t_{R(OUTTX)}$	Output rise time	20%–80%, AC Coupled Outputs, 100-Ω differential load		30	42	ps
$t_{F(OUTTX)}$	Output fall time	20%–80%, AC Coupled Outputs, 100-Ω differential load		30	42	ps
$ISI_{(TX)}$	Intersymbol interference	TXEQ_DIS = 1, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage		4	10	ps
		TXEQ_DIS = 0, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage, maximum equalization with 18-inch transmission line at the input.		7		
$R_{(JTX)}$	Serial data output random jitter			0.4	0.75	ps_{RMS}
	Output Peaking Width	TXPKSEL = 0		28		ps
		TXPKSEL = 1		35		
CDR SPECIFICATIONS						
$t_{(Lock,TX)}$	CDR Acquisition time				2	ms
	LOL assert time				500	µs

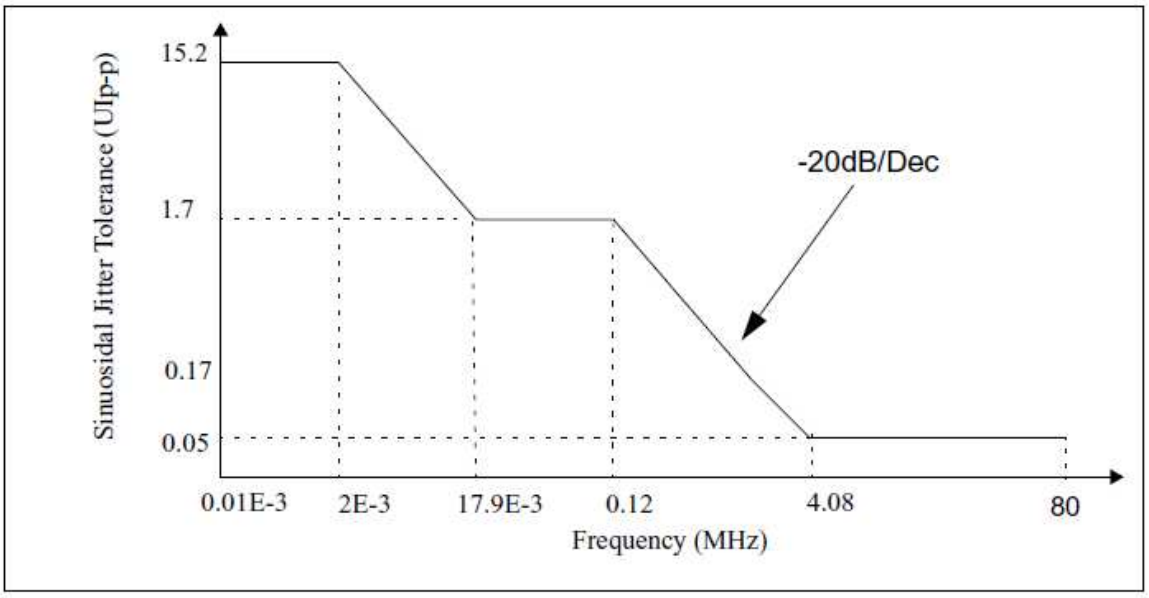


Figure 1. Input Sinusoidal Jitter Tolerance (INF-8077i Rev. 4.5 XFP MSA)

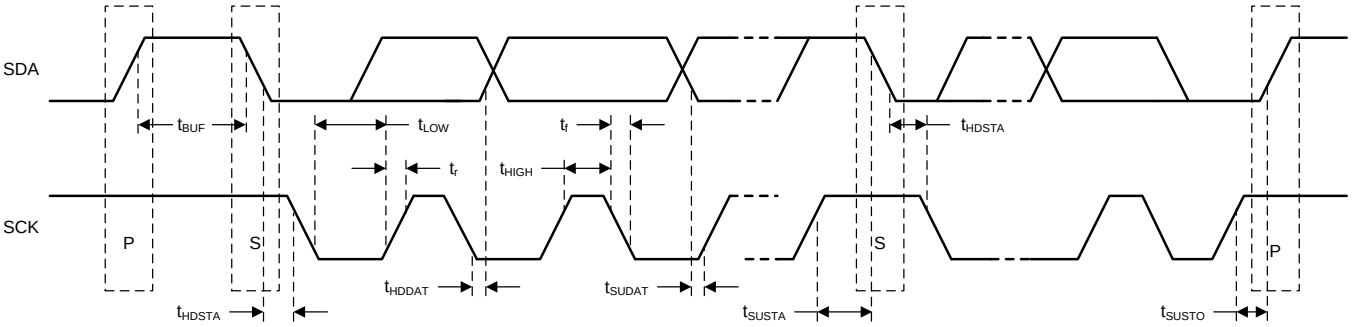


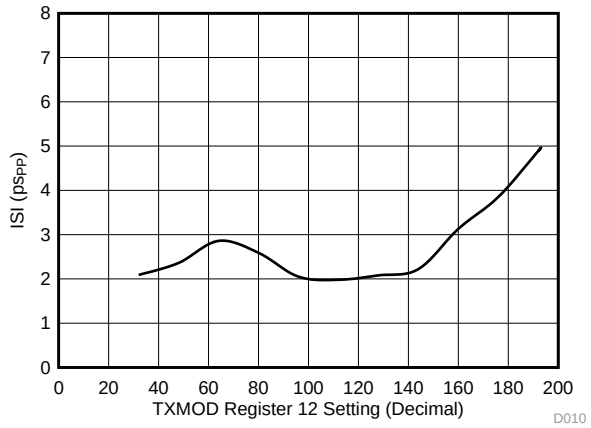
Figure 2. 2-Wire Interface Diagram

6.8 Timing Diagram Definitions

		MIN	TYP	MAX	UNIT
f_{SCK}	SCK clock frequency			400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	Low period of the SCK clock	1.3			µs
t_{HIGH}	High period of the SCK clock	0.6			µs
t_{SUSTA}	Setup time for a repeated START condition	0.6			µs
t_{HDDAT}	Data HOLD time	0			µs
t_{SUDAT}	Data setup time	100			ns
t_R	Rise time of both SDA and SCK signals			300	ns
t_F	Fall time of both SDA and SCK signals			300	ns
t_{SUSTO}	Setup time for STOP condition	0.6			µs

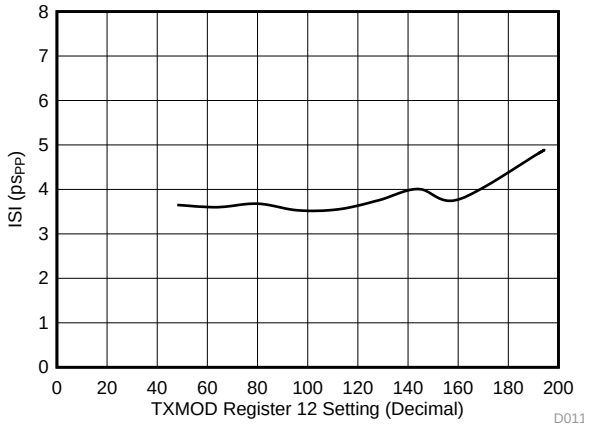
6.9 Typical Characteristics

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, V_{OUT} = 2 V_{PP} Single-ended, DIN = 600 mV_{PP} differential, CDR enabled (unless otherwise noted).



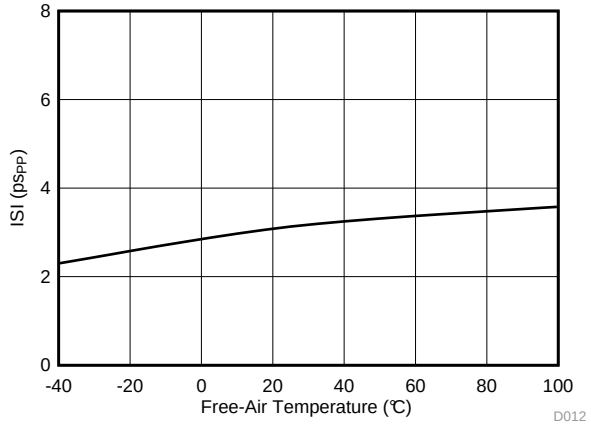
TXMODE = 0

Figure 3. Deterministic Jitter vs Modulation Current



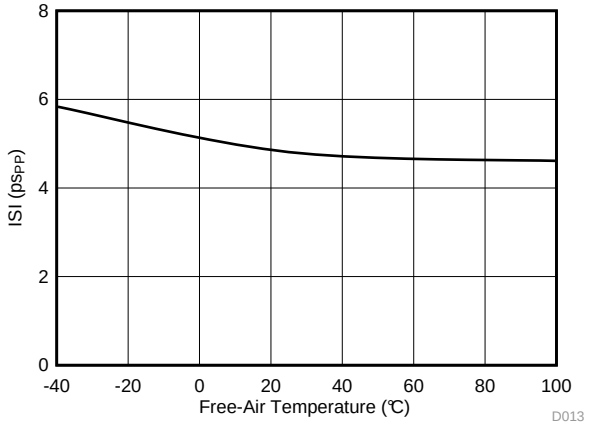
TXMODE = 1

Figure 4. Deterministic Jitter vs Modulation Current



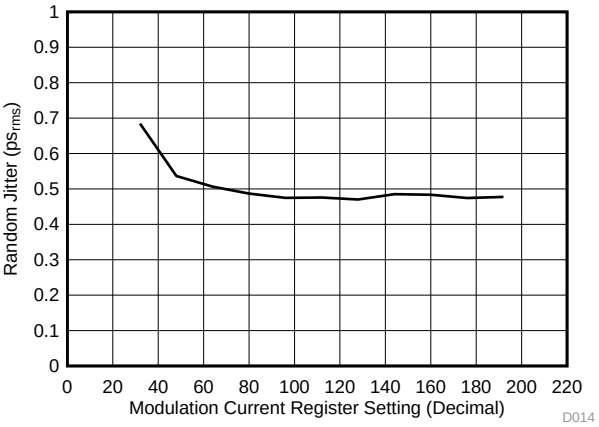
TXMODE = 0

Figure 5. Deterministic Jitter vs Temperature



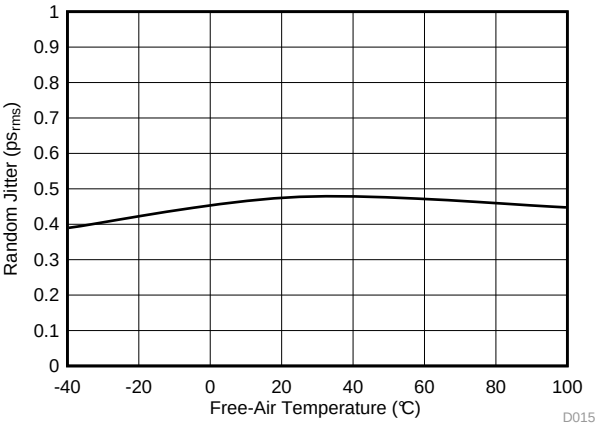
TXMODE = 1

Figure 6. Deterministic Jitter vs Temperature



TXMODE = 1

Figure 7. Random Jitter vs Modulation Current

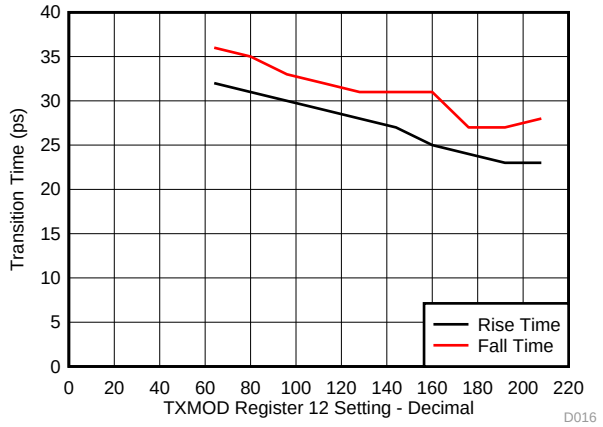


TXMODE = 1

Figure 8. Random Jitter vs Temperature

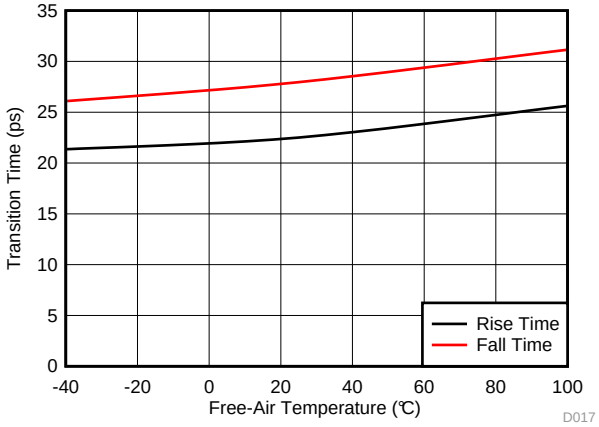
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, V_{OUT} = 2 V_{PP} Single-ended, DIN = 600 mV_{PP} differential, CDR enabled (unless otherwise noted).



TXMODE = 1

Figure 9. Rise-Time and Fall-Time vs Modulation Current



TXMODE = 1

Figure 10. Rise-Time and Fall-Time vs Temperature

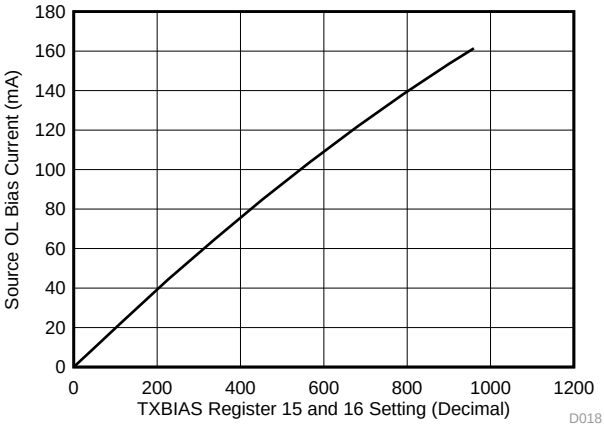


Figure 11. Source Bias Current in Open Loop Mode vs Bias Register Setting

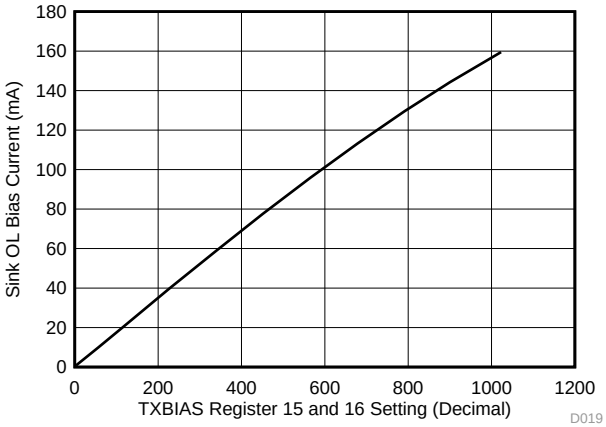


Figure 12. Sink Bias Current in Open Loop Mode vs Bias Register Setting

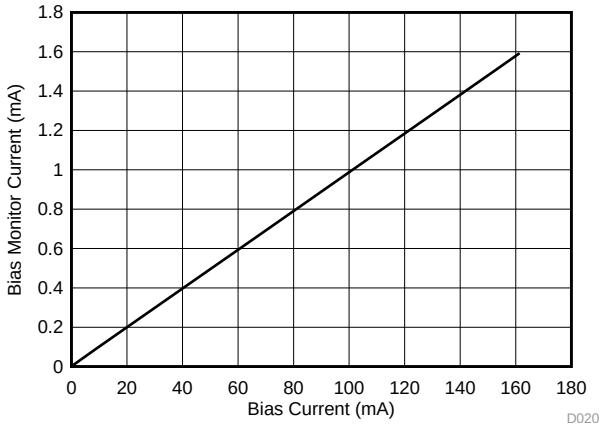
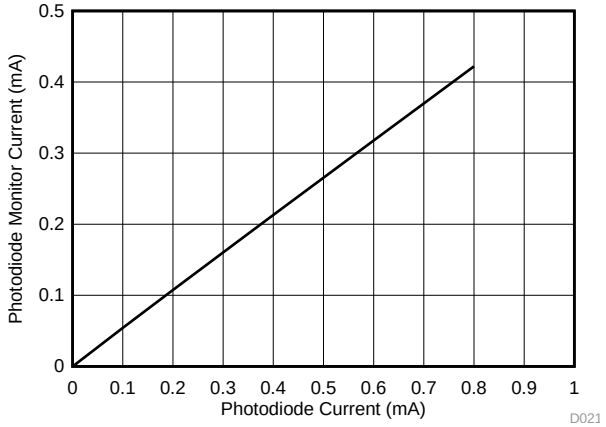


Figure 13. Bias-Monitor Current $I_{(MONB)}$ vs Bias Current

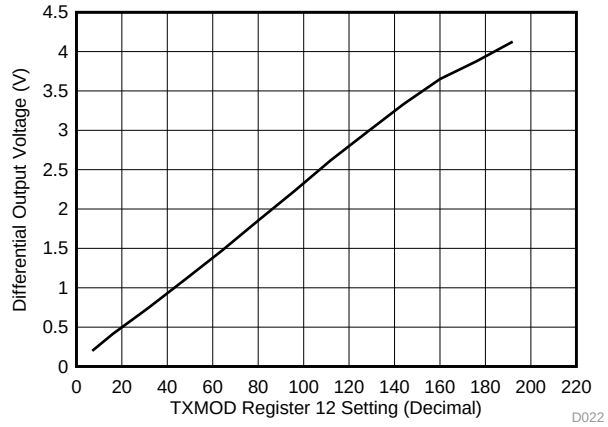


TXPDRNG[0..1] = 00

Figure 14. Photodiode-Monitor Current $I_{(MONP)}$ vs PD Current

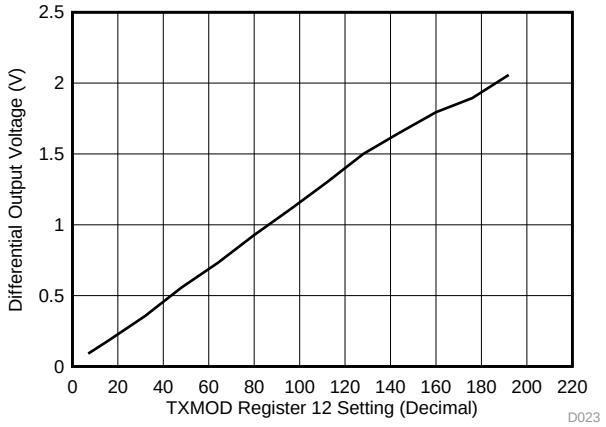
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, V_{OUT} = 2 V_{PP} Single-ended, DIN = 600 mV_{PP} differential, CDR enabled (unless otherwise noted).



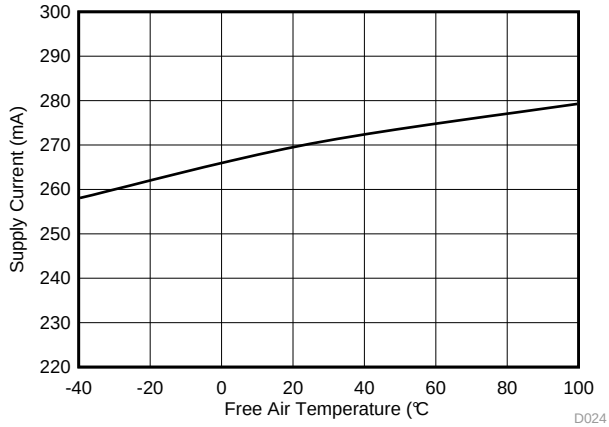
TXMODE = 0

Figure 15. Output Voltage vs Modulation Current



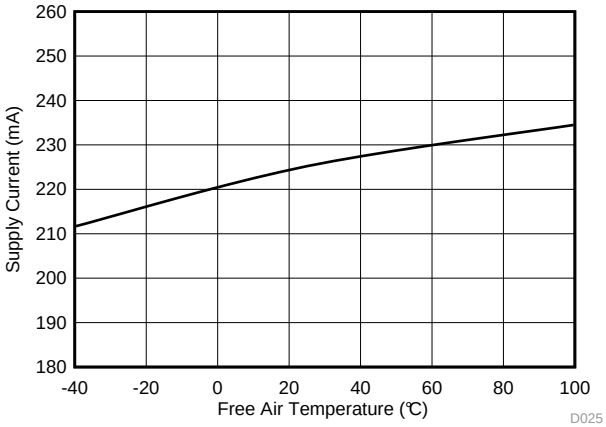
TXMODE = 1

Figure 16. Output Voltage vs Modulation Current



TXMODE = 0 Bias Current = 0

Figure 17. Supply Current vs Temperature



TXMODE = 1 Bias Current = 0

Figure 18. Supply Current vs Temperature

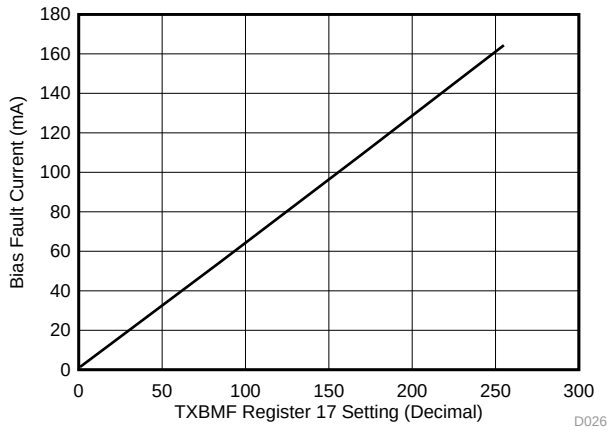


Figure 19. Bias Current Monitor Fault vs TXBMF Register Setting

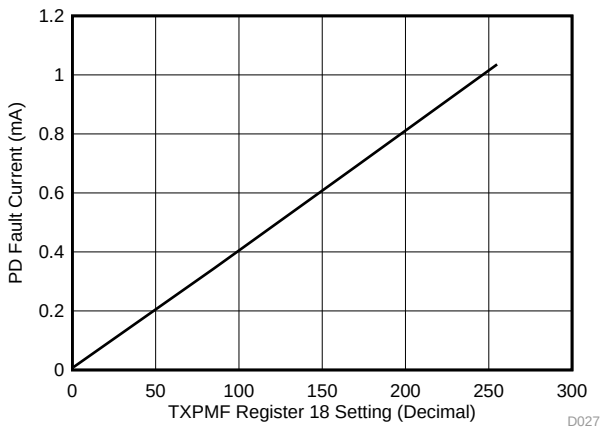
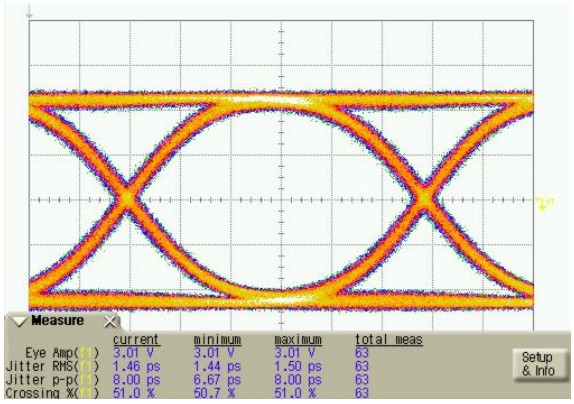


Figure 20. Photodiode Current Monitor Fault vs TXPMF Register Setting

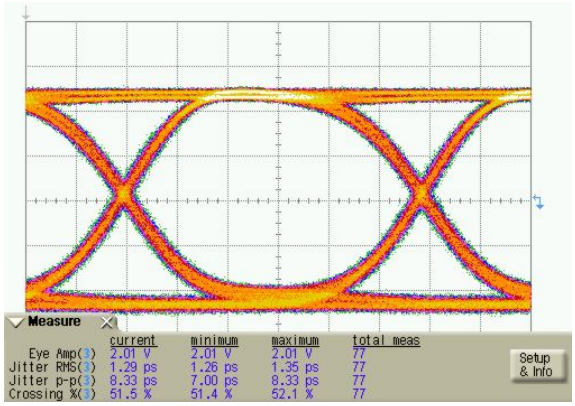
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, V_{OUT} = 2 V_{PP} Single-ended, DIN = 600 mV_{PP} differential, CDR enabled (unless otherwise noted).



TXMODE = 0 15 ps/Div

Figure 21. Eye-Diagram at 11.3 Gbps



TXMODE = 1 15 ps/Div

Figure 22. Eye-Diagram at 11.3 Gbps

7 Detailed Description

7.1 Overview

A simplified block diagram of the ONET1131EC is shown in *Functional Block Diagram*.

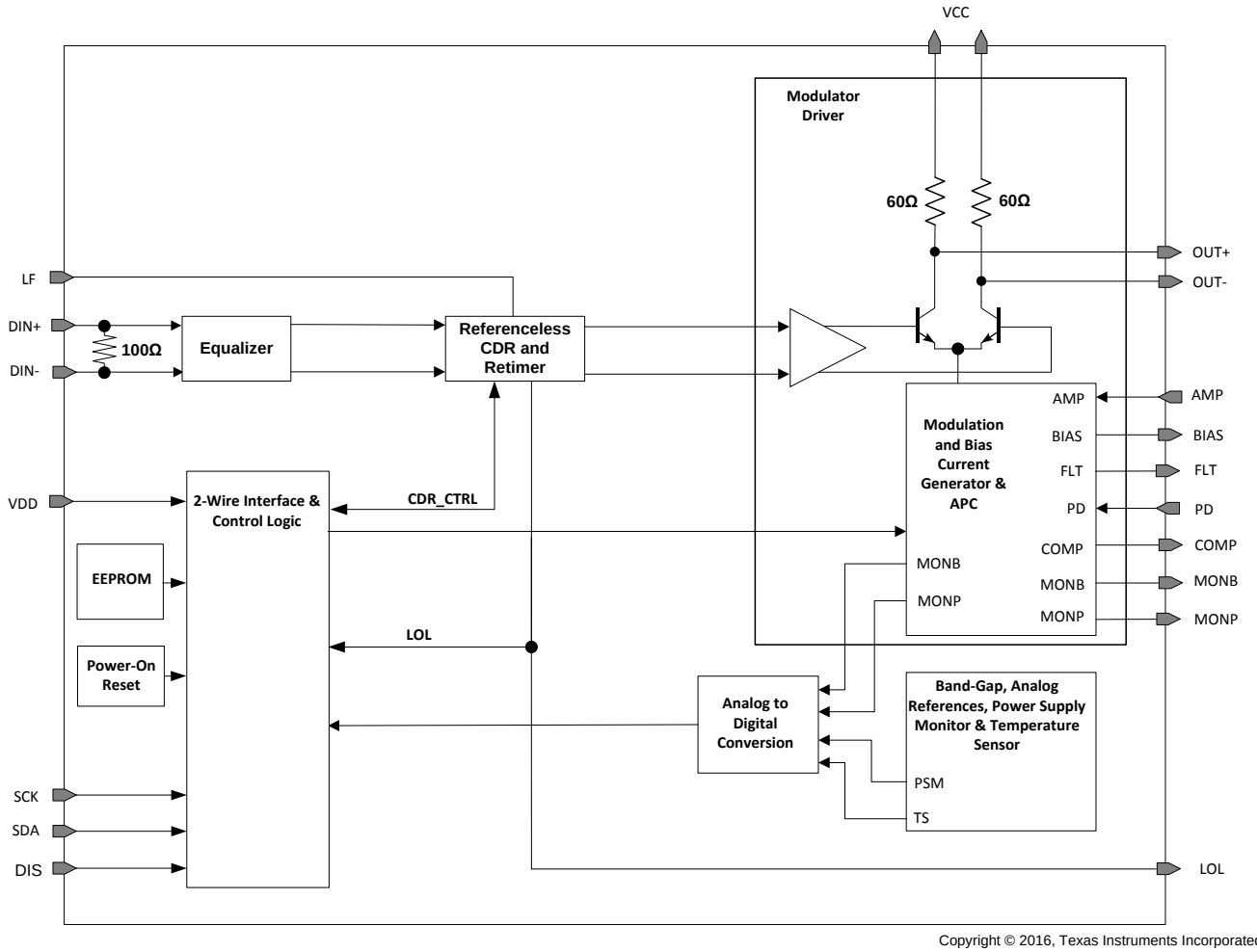
The ONET1131EC consists of a transmitter path, an analog reference block, an analog to digital converter, and a 2-wire serial interface and control logic block with power-on reset.

The transmit path consists of an adjustable input equalizer, a multi-rate CDR and an output modulator driver. The output driver provides a differential output voltage but can be operated in a single-ended mode to reduce the power consumption. Output waveform control, in the form of cross-point adjustment and de-emphasis are available to improve the optical eye mask margin. Bias current for the laser is provided and an integrated automatic power control (APC) loop to compensate for variations in average optical power over voltage, temperature and time is included.

The ONET1131EC contains an analog to digital converter to support transceiver digital diagnostics and can report the supply voltage, laser bias current, laser photodiode current and internal temperature.

The 2-wire serial interface is used to control the operation of the device and read the status of the control registers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Equalizer

The data signal is applied to an input equalizer by means of the input signal pins DIN+ / DIN–, which provide on-chip differential 100-Ω line termination. The equalizer is enabled by default and can be disabled by setting the transmitter equalizer disable bit TXEQ_DIS = 1 (bit 1 of *register 10*). Equalization of up to 300 mm (12 inches) of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is set through register settings TXCTLE [0..3] (*register 11*). The device can accept input amplitude levels from 100 mVpp up to 1000 mVpp.

7.3.2 CDR

The clock and data recovery function consists of a Phase-Locked Loop (PLL) and retimer. The CDR can be operated without a reference clock and the Voltage Controlled Oscillator (VCO) can cover 9.8 Gbps to 11.7 Gbps data rates. The PLL is phase locked to the incoming data stream and attenuates the high frequency jitter on the data, producing a recovered clean clock with substantially reduced jitter. An external capacitor for the PLL loop filter is connected to the LF pin. A value of 2.2 nF is recommended. The clean clock is used to retime the incoming data, producing an output signal with reduced jitter, and in effect, resetting the jitter budget for the transmitter.

The CDR is enabled by default. The CDR can be disabled and bypassed by setting the transmitter CDR disable bit TXCDR_DIS = 1 (bit 4 of *register 10*). Alternatively, the CDR can be left powered on but bypassed by setting the transmitter CDR bypass bit TX_CDRBP = 1 (bit 3 of *register 10*); however, this function only works if the receiver CDR bypass bit RX_CDRBP (bit 3 of *register 4*) is also set to 1.

The CDR is designed to meet the XFP Datacom requirements and Telecom requirements for a maximum of 1-dB jitter peaking at a frequency greater than 120 kHz. The CDR is not designed to meet the Telecom regenerator requirements of jitter peaking less than 0.03 dB at a frequency less than 120 kHz. The default CDR bandwidth is typically 4.5 MHz and can be adjusted using the SEL_RES[0..2] bits (bits 5 to 7 of *register 51*). Adjusting these bits changes the bandwidth of both the transmitter and receiver CDRs.

For the majority of applications, the default settings in *register 19* for the transmitter CDR can be used. However, for some applications or for test purposes, some modes of operation may be useful. The frequency detector for the PLL is set to an automatic mode of operation by default. When a signal is applied to the transmitter input the frequency detector search algorithm will be initiated to determine the frequency of the data. The default algorithm ensures a fast CDR lock time of less than 2 ms. The fast lock can be disabled by setting the transmitter CDR fast lock disable bit TXFL_DIS = 1 (bit 3 of *register 19*). Once the frequency has been detected then the frequency detector will be disabled and the supply current will decrease by approximately 10mA. In some applications, such as when there are long periods of idle data, it may be advantageous to keep the frequency detector permanently enabled by setting the transmitter frequency detector enable bit TXFD_EN = 1 (bit 5 of *register 19*). For test purposes, the frequency detector can be permanently disabled by setting the transmitter frequency detector disable bit TXFD_DIS = 1 (bit 4 of *register 19*). For fast lock times the frequency detector can be set to one of two preselected data rates using the transmitter frequency detection mode selection bits TXFD_MOD[0..1] (bits 6 and 7 of *register 19*). If it is desired to use the retimer at lower data rates than the standard 9.8 to 11.7Gbps then the transmitter divider ratio should be adjusted accordingly through TXDIV[0..2] (bits 0 to 2 of *register 19*). For example, for re-timed operation at 2.5 Gbps the divider should be set to divide by 4.

7.3.3 Modulator Driver

The modulation current is sunk from the common emitter node of the limiting output driver differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire serial interface.

The collector nodes of the output stages are connected to the transmitter output pins TXOUT+ and TXOUT–. The collectors have internal 50Ω back termination resistors to VCC_TX. The outputs are optimized to drive a 50 Ω single-ended load and to obtain the maximum single-ended output voltage of 2.0Vpp, AC coupling and inductive pull-ups to VCC are required. For reduced power consumption the DC resistance of the inductive pull-ups should be minimized to provide sufficient headroom on the TXOUT+ and TXOUT– pins.

The polarity of the output pins can be inverted by setting the transmitter output polarity switch bit, TXOUTPOL (bit 5 of *register 10*) to 1. In addition, the output driver can be disabled by setting the transmitter output driver disable bit TXOUT_DIS = 1 (bit 6 of *register 10*).

Feature Description (continued)

The output driver is set to differential output by default. In order to reduce the power consumption for single-ended applications driving an electroabsorptive modulated laser (EML) the output drive *register 13* should be set to single-ended mode. The single-ended output signal is enabled by setting the transmitter mode select bit TXMODE = 1 (bit 6 of *register 13*). The positive output is active by default. To enable the negative output and disable the positive output set TXOUTSEL = 1 (bit 7 of *register 13*).

Output de-emphasis can be applied to the signal by adjusting the transmitter de-emphasis bits TXDEADJ[0..3] (bits 0 to 3 of *register 13*). In addition, the width of the applied de-emphasis can be increased by setting the transmitter output peaking width TXPKSEL = 1 (bit 6 of *register 11*). The wide peaking width would typically be useful for a more capacitive transmitter load. How de-emphasis is applied is controlled through the TXSTEP bit (bit 5 of *register 13*). Setting TXSTEP = 1 delays the time of the applied de-emphasis and has more of an impact on the falling edge. A graphical representation of the two de-emphasis modes is shown in Figure 23. Using de-emphasis can help to optimize the transmitted output signal; however, it will add to the power consumption.

The output edge speed can be set to slow mode of operation through the TXSLOW bit (bit 4 of *register 13*). For transmitter modulation output settings (TXMOD - *register 12*) below 0xC0 it is recommended to set TXSLOW = 1 to reduce the output jitter.

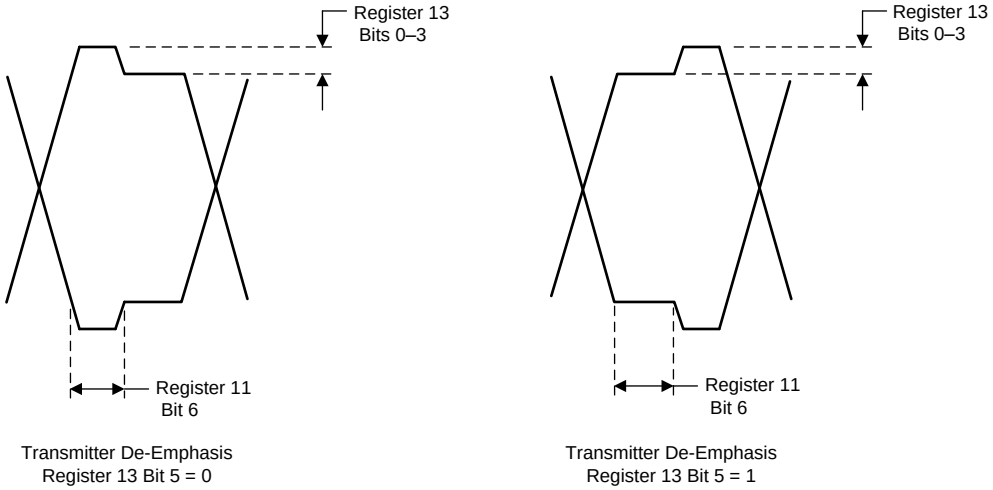


Figure 23. Transmitter De-Emphasis Modes

7.3.4 Modulation Current Generator

The modulation current generator provides the current for the high speed output driver described above. The circuit can be digitally controlled through the 2-wire interface block or controlled by applying an analog voltage in the range of 0 to 2 V to the AMP pin. The default method of control is through the 2-wire interface. To use the AMP pin set the transmitter amplitude control bit TXAMPCTRL = 1 (bit 0 of *register 10*).

An 8-bit wide control bus, TXMOD[0..7] (*register 12*), is used to set the desired modulation current and the output voltage.

The entire transmitter signal path, including CDR, can be disabled and powered down by setting TX_DIS = 1 (bit 7 of *register 10*).

Feature Description (continued)

7.3.5 DC Offset Cancellation and Cross Point Control

The ONET1131EC transmitter has DC offset cancellation to compensate for internal offset voltages. The offset cancellation can be disabled by setting TXOC_DIS = 1 (bit 2 of *register 10*).

The crossing point can be moved toward the one level by setting TXCPSGN = 1 (bit 7 of *register 14*) and it can be moved toward the zero level by setting TXCPSGN = 0. The percentage of shift depends upon the register settings of the transmitter cross-point adjustment bits TXCPADJ[0..6] (*register 14*).

7.3.6 Bias Current Generation and APC Loop

The bias current for the laser is turned off by default and has to be enabled by setting the laser bias current enable bit TXBIASEN = 1 (bit 2 of *register 1*). In open loop operation, selected by setting TXOLENA = 1 (bit 4 of *register 1*), the bias current is set directly by the 10-bit wide control word TXBIAS[0..9] (*register 15* and *register 16*). In Automatic Power Control (APC) mode, selected by setting TXOLENA = 0, the bias current depends on the register settings TXBIAS[0..9] and the coupling ratio (CR) between the laser bias current and the photodiode current. CR = I_{BIAS}/I_{PD}. If the photodiode cathode is connected to VCC and the anode is connected to the PD pin (PD pin is sinking current) set TXPDPOL = 1 (bit 0 of *register 1*). If the photodiode anode is connected to ground and the cathode is connected to the PD pin (PD pin is sourcing current), set TXPDPOL = 0.

Three photodiode current ranges can be selected by means of the photodiode current range bits TXPDRNG[0..1] (bits 5 and 6 of *register 1*). The photodiode range should be chosen to keep the laser bias control DAC, TXBIAS[0..9], close to the center of its range. This keeps the laser bias current set point resolution high. For details regarding the bias current setting in open-loop mode as well as in closed-loop mode, see the *Register Mapping* table.

The ONET1131EC has the ability to source or sink the bias current. The default condition is for the BIAS pin to source the current (TXBIASPOL = 0). To act as a sink, set TXBIASPOL = 1 (bit 1 of *register 1*).

The bias current is monitored using a current mirror with a gain equal to 1/100. By connecting a resistor between MONB and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used. The bias current can also be monitored as a 10 bit unsigned digital word by setting the transmitter bias current digital monitor selection bit TXDMONB = 1 (bit 5 of *register 16*) and removing the resistor from MONB to ground.

The photodiode current is monitored using a current mirror with various gains that are dependent upon the photodiode current range being used. By connecting a resistor between MONP and GND, the photodiode current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used. The photodiode current can also be monitored as a 10 bit unsigned digital word by setting the transmitter photodiode current digital monitor selection bit TXDMONP = 1 (bit 6 of *register 16*) and removing the resistor from MONP to ground.

7.3.7 Laser Safety Features and Fault Recovery Procedure

The ONET1131EC provides built in laser safety features. The following fault conditions are detected if the transmitter fault detection enable bit TXFLTEN = 1 (bit 3 of *register 1*):

1. Voltage at MONB exceeds the bandgap voltage (1.2 V) or, alternately, if TXDMONB = 1 and the bias current exceeds the bias current monitor fault threshold set by TXBMF[0..7] (*register 17*). When using the digital monitor, the resistor from the MONB pin to ground must be removed.
2. Voltage at MONP exceeds the bandgap voltage (1.2 V) and the analog photodiode current monitor fault trigger bit, TXMONPFLT (bit 7 of *register 1*), is set to 1. Alternately, a fault can be triggered if TXDMONP = 1 and the photodiode current exceeds the photodiode current monitor fault threshold set by TXPMF[0..7] (*register 18*). When using the digital monitor, the resistor from the MONP pin to ground must be removed.
3. Photodiode current exceeds 150% of its set value,
4. Bias control DAC drops in value by more than 50% in one step.

If the fault detection is being used then to avoid a fault from occurring at start-up it is recommended to set up the required bias current and APC loop conditions first and enable the laser bias current (TXBIASEN = 1) as the last step in the sequence of commands.

Feature Description (continued)

If one or more fault conditions occur and the transmitter fault enable bit TXFLTEN is set to 1, the ONET1131EC responds by:

1. Setting the bias current to zero.
2. Asserting and latching the TX_FLT pin.
3. Setting the TX_FLT bit (bit 5 of *register 43*) to 1.

Fault recovery is performed by the following procedure:

1. The transmitter disable pin TX_DIS and/or the transmitter bias current enable bit TXBIASEN are toggled for at least the fault latch reset time.
2. The TX_FLT pin de-asserts while the transmitter disable pin TX_DIS is asserted or the transmitter bias current enable bit TXBIASEN is de-asserted.
3. If the fault condition is no longer present, the part returns to normal operation with its prior output settings after the disable negate time.
4. If the fault condition is still present, TX_FLT re-asserts once TX_DIS is set to a low level and/or TXBIASEN is set to 0 and the part will not return to normal operation.

7.3.8 Analog Block

7.3.8.1 Analog Reference and Temperature Sensor

The ONET1131EC is supplied by a single 2.5 V ±5% supply voltage connected to the VCC and VDD pins. This voltage is referred to ground (GND) and can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

In order to minimize the module component count, the ONET1131ECprovides an on-chip temperature sensor. The temperature can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

7.3.8.2 Power-On Reset

The ONET1131EC has power on reset circuitry which ensures that all registers are reset to default values during startup. After the power-on to initialize time (t_{INIT1}), the internal registers are ready to be loaded. The part is ready to transmit data after the initialize to transmit time (t_{INIT2}), assuming that the enable chip bit EN_CHIP = 1 (bit 0 of *register 0*). In addition, the disable pin DIS must be set to zero.

The ONET1131EC bias current can be disabled by setting the DIS pin high. The internal registers are not reset. After the transmitter disable pin DIS is set low the part returns to its prior output settings.

7.3.8.3 Analog to Digital Converter

The ONET1131EC has an internal 10 bit analog to digital converter (ADC) that converts the analog monitors for temperature, power supply voltage, bias current and photodiode current into a 10 bit unsigned digital word. The first 8 most significant bits (MSBs) are available in *register 40* and the 2 least significant bits (LSBs) are available in *register 41*. Depending on the accuracy required, 8 bits or 10 bits can be read. However, due to the architecture of the 2-wire interface, in order to read the 2 registers, 2 separate read commands have to be sent.

The ADC is enabled by default so to monitor a particular parameter, select the parameter with ADCSEL[0..2] (bits 0 to 2 of *register 3*). Table 1 shows the ADCSEL bits and the parameter that is monitored.

Table 1. ADC Selection Bits and the Monitored Parameter

ADCSEL2	ADCSEL1	ADCSEL0	MONITORED PARAMETER
0	0	0	Temperature
0	0	1	Supply voltage
0	1	0	Bias current
0	1	1	Photodiode current

To digitally monitor the photodiode current, ensure that TXDMONP = 1 (bit 6 of *register 16*) and that a resistor is not connected to the MONP pin. To digitally monitor the bias current, ensure that TXDMONB = 1 (bit 5 of *register 16*) and that a resistor is not connected to the MONB pin. The ADC is disabled by default. To enable the ADC, set the ADC oscillator enable bit OSCEN = 1 (bit 6 of *register 3*) and set the ADC enable bit ADCEN = 1 (bit 7 of *register 3*).

The digital word read from the ADC can be converted to its analog equivalent through the following formulas.

7.3.8.3.1 Temperature

$$\text{Temperature (°C)} = (0.5475 \times \text{ADCx}) - 273 \quad (1)$$

7.3.8.3.2 Power Supply Voltage

$$\text{Power supply voltage (V)} = (1.36\text{m} \times \text{ADCx}) + 1.76 \quad (2)$$

7.3.8.3.3 Photodiode Current Monitor

$$\text{IPD}(\mu\text{A}) = 2 \times [(0.62 \times \text{ADCx}) - 16] \text{ for TXPDRNG00} \quad (3)$$

$$\text{IPD}(\mu\text{A}) = 4 \times [(0.62 \times \text{ADCx}) - 16] \text{ for TXPDRNG01} \quad (4)$$

$$\text{IPD}(\mu\text{A}) = 8 \times [(0.62 \times \text{ADCx}) - 16] \text{ for TXPDRNG1x} \quad (5)$$

7.3.8.3.4 Bias Current Monitor

$$\text{IBIAS (mA)} = (0.2 \times \text{ADCx}) - 4.5 \quad (6)$$

Where: ADCx = the decimal value read from the ADC

7.3.8.4 2-Wire Interface and Control Logic

The ONET1131EC uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. The SDA and SCK pins require external 4.7-kΩ to 10-kΩ pull-up resistor to VCC for proper operation.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The ONET1131EC is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. Seven (7) bit slave address (0001000) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the ONET1131EC is I^2C compatible. The typical timing is shown in Figure 2 and a complete data transfer is shown in Figure 24. Parameters for Figure 2 are defined in the *Timing Diagram Definitions*.

7.3.8.5 Bus Idle

Both SDA and SCK lines remain HIGH

7.3.8.6 Start Data Transfer

A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

7.3.8.7 Stop Data Transfer

A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

7.3.8.8 Data Transfer

Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

7.3.9 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition, see Figure 2.

7.4 Device Functional Modes

The ONET1131EC has two main functional modes of operation: differential transmitter output and single-ended transmitter output.

7.4.1 Differential Transmitter Output

Operation with differential output is the default mode of operation. This mode is intended for externally modulated lasers requiring differential drive such as Mach Zehnder modulators.

7.4.2 Single-Ended Transmitter Output

In order to reduce the power consumption for single-ended EML applications the output driver should be set to single-ended mode. The single-ended output signal can be enabled by setting the transmitter mode select bit TXMODE = 1 (bit 6 of *register 13*). The positive output is active by default. To enable the negative output and disable the positive output set TXOUTSEL = 1 (bit 7 of *register 13*).

7.5 Programming

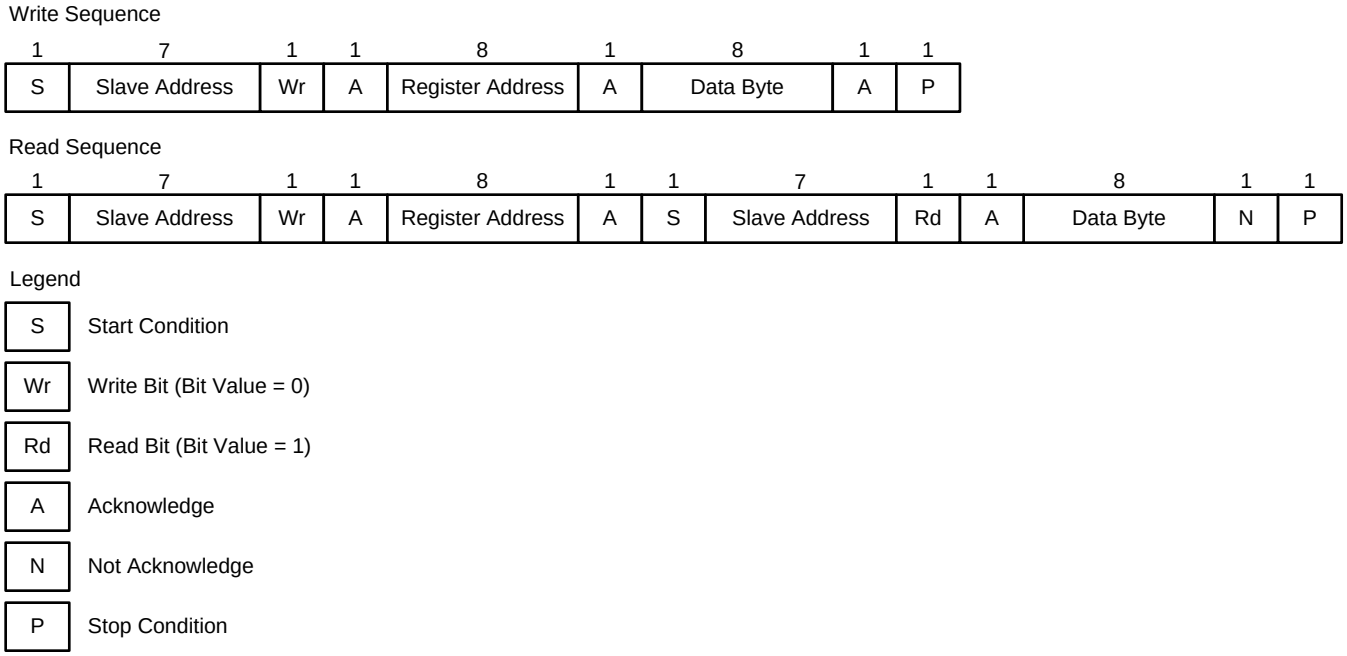


Figure 24. Programming Sequence

7.6 Register Mapping

7.6.1 R/W Control Registers

7.6.1.1 Core Level Register 0 (offset = 0100 0001 [reset = 41h]

Figure 25. Core Level Register 0

7	6	5	4	3	2	1	0
GLOBAL SW_PIN RESET	Reserved					I2C RESET	EN_CHIP
RWSC	RW				RWSC	RWSC	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset. RWSC = Read/Write self clearing (always reads back to zero)

Table 2. Core Level Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL SW_PIN RESET	RWSC	0	**Global Reset SW** 1 = reset, resets all I2C and EEPROM modules to default 0 = normal operation (self-clearing, always reads back ‘0’)
6:3	Reserved	R/W	1	Reserved
2		RWSC	0	Reserved
1	I2C RESET	RWSC	0	**Chip reset bit** 1 = resets all I2C registers to default 0 = normal operation (self-clearing, always reads back ‘0’)
0	EN_CHIP	R/W	1	**Enable chip bit** 1 = Chip enabled 0 = Chip disabled

7.6.1.2 Core Level Register 1 (offset = 0000 0000) [reset = 0h]

Figure 26. Core Level Register 1

7	6	5	4	3	2	1	0
TXMONPFLT	TXPDRNG1	TXPDRNG0	TXOLENA	TXFLTEN	TXBIASEN	TTXBIASPOL	TXPDPOL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. Core Level Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXMONPFLT	R/W	0	Analog photodiode current monitor fault trigger bit 1 = Fault trigger on MONP pin is enabled 0 = Fault trigger on MONP pin is disabled
6 5	TXPDRNG1 TXPDRNG0	R/W	0	**Photodiode current range bits** 1X: up to 3080 μA / 3 μA resolution 01: up to 1540 μA / 1.5 μA resolution 00: up to 770 μA / 0.75 μA resolution
4	TXOLENA	R/W	0	**Open loop enable bit** 1 = Open loop bias current control 0 = Closed loop bias current control
3	TXFLTEN	R/W	0	**Fault detection enable bit** 1 = Fault detection on 0 = Fault detection off
2	TXBIASEN	R/W	0	**Laser Bias current enable bit** 1 = Bias current enabled. Toggle to 0 to reset a fault condition. 0 = Bias current disabled
1	TXBIASPOL	R/W	0	**Laser Bias current polarity bit** 1 = Bias pin sinks current 0 = Bias pin sources current
0	TXPDPOL	R/W	0	**Photodiode polarity bit** 1 = Photodiode cathode connected to V_{CC} 0 = Photodiode anode connected to GND

7.6.1.3 Core Level Register 2 (offset = 0000 0000) [reset = 0h]

Figure 27. Core Level Register 2

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Core Level Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R/W	0	Reserved

7.6.1.4 Core Level Register 3 (offset = 0000 0000) [reset = 0h]

Figure 28. Core Level Register 3

7	6	5	4	3	2	1	0
ADCEN	OSCEN	Reserved	ADCRST	Reserved	ADCSEL2	ADCSEL1	ADCSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Core Level Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	ADCEN	R/W	0h	**ADC enabled bit** 1 = ADC enabled 0 = ADC disabled
6	OSCEN	R/W	0h	**ADC oscillator bit** 1 = Oscillator enabled 0 = Oscillator disabled
5	Reserved	R/W	0h	Reserved
4	ADCRST	R/W	0h	**ADC reset** 1 = ADC reset 0 = ADC no reset
3	Reserved	R/W	0h	Reserved
2	ADCSEL2	R/W	0h	**ADC input selection bits <2:0>** 000 selects the temperature sensor 001 selects the power supply monitor 010 selects IMONB 011 selects IMONP 1XX are reserved
1	ADCSEL1	R/W	0h	
0	ADCSEL0	R/W	0h	

7.6.2 RX Registers

7.6.2.1 RX Register 4 (offset = 0000 0000) [reset = 0h]

Figure 29. RX Register 4

7	6	5	4	3	2	1	0
DIS	Reserved						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. RX Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS	R/W	0	Set bit to 1
6:0	Reserved	R/W	0	Reserved

7.6.2.2 RX Register 5 (offset = 0000 0000) [reset = 0h]

Figure 30. Reserved Register 5 - 9

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Reserved Register 5 - 9 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R/W	0	Reserved

7.6.3 TX Registers

7.6.3.1 TX Register 10 (offset = 0000 0000) [reset = 0h]

Figure 31. TX Register 10

7	6	5	4	3	2	1	0
TX_DIS	TXOUT_DIS	TXOUTPOL	TXCDR_DIS	TX_CDRBP	TXOC_DIS	TXEQ_DIS	TXAMPCTRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. TX Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_DIS	R/W	0	**TX disable bit** 1 = TX disabled (power-down) 0 = TX enabled
6	TXOUT_DIS	R/W	0	**TX Output Driver disable bit** 1 = output disabled 0 = output enabled
5	TXOUTPOL	R/W	0	**TX Output polarity switch bit** 1 = inverted polarity 0 = normal polarity
4	TXCDR_DIS	R/W	0	**TX CDR disable bit** 1 = TX CDR is disabled and bypassed 0 = TX CDR is enabled
3	TX_CDRBP	R/W	0	**TX CDR bypass bit** 1 = TX-CDR bypassed. RX_CDRBP must be set to 1 for this function to operate. 0 = TX-CDR not bypassed
2	TXOC_DIS	R/W	0	**TX OC disable bit** 1 = TX Offset Cancellation disabled 0 = TX Offset Cancellation enabled
1	TXEQ_DIS	R/W	0	**TX Equalizer disable bit** 1 = TX Equalizer is disabled and bypassed 0 = TX Equalizer is enabled
0	TXAMPCTRL	R/W	0	**TX AMP Ctrl** 1 = TX AMP Control is enabled (analog amplitude control) 0 = TX AMP Control is disabled (digital amplitude control)

7.6.3.2 TX Register 11 (offset = 0000 0000) [reset = 0h]

Figure 32. TX Register 11

7	6	5	4	3	2	1	0
TXAMPRNG	TXPKSEL	TXTCSEL1	TXTCSEL0	TXCTLE3	TXCTLE2	TXCTLE1	TXCTLE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. TX Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXAMPRNG	R/W	0	**TX output AMP range** 1 = Half TX output amplitude range 0 = Full TX output amplitude range
6	TXPKSEL	R/W	0	**TX output peaking width** 1 = wide peaking width 0 = narrow peaking width
5	TXTCSEL1	R/W	0	TXOUT temperature compensation select bit 1
4	TXTCSEL0	R/W	0	TXOUT temperature compensation select bit 0
3	TXCTLE3	R/W	0	**TX input CTLE setting** 0000 = minimum 1111 = maximum
2	TXCTLE2	R/W	0	
1	TXCTLE1	R/W	0	
0	TXCTLE0	R/W	0	

7.6.3.3 TX Register 12 (offset = 0000 0000) [reset = 0h]

Figure 33. TX Register 12

7	6	5	4	3	2	1	0
TXMOD7	TXMOD76	TXMOD5	TXMOD4	TXMOD3	TXMOD2	TXMOD1	TXMOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. TX Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXMOD7	R/W	0	**TX Modulation current setting: sets the output voltage** Output Voltage: 2.4 Vpp / 9.5 mVpp steps
6	TXMOD6	R/W	0	
5	TXMOD5	R/W	0	
4	TXMOD4	R/W	0	
3	TXMOD3	R/W	0	
2	TXMOD2	R/W	0	
1	TXMOD1	R/W	0	
0	TXMOD0	R/W	0	

7.6.3.4 TX Register 13 (offset = 0h) [reset = 0]

Figure 34. TX Register 13

7	6	5	4	3	2	1	0
TXOUTSEL	TXMODE	TXSTEP	TXSLOW	TXDEADJ3	TXDEADJ2	TXDEADJ1	TXDEADJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. TX Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXOUTSEL	R/W	0	**TX output selection bit** 1 = The negative output TXOUT– is active 0 = The positive output TXOUT+ is active
6	TXMODE	R/W	0	**TX output mode selection bit** 1 = Single-ended mode 0 = Differential mode
5	TXSTEP	R/W	0	**TX output de-emphasis mode selection bit** 1 = Delayed de-emphasis 0 = Normal de-emphasis
4	TXSLOW	R/W	0	**TX edge speed selection bit** 1 = Slow edge speed 0 = Normal operation
3	TXDEADJ3	R/W	0	**TX de-emphasis setting** 0000 = minimum 1111 = maximum
2	TXDEADJ2	R/W	0	
1	TXDEADJ1	R/W	0	
0	TXDEADJ0	R/W	0	

7.6.3.5 TX Register 14 (offset = 0000 0000) [reset = 0h]

Figure 35. TX Register 14

7	6	5	4	3	2	1	0
TXCPSGN	TXCPADJ6	TXCPADJ5	TXCPADJ4	TXCPADJ3	TXCPADJ2	TXCPADJ61	TXCPADJ60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. TX Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXCPSGN	R/W	0	**TX Eye cross-point adjustment setting** TXCPSGN = 1 (positive shift) Maximum shift for 1111111 Minimum shift for 0000000 TXCPSGN = 0 (negative shift) Maximum shift for 1111111 Minimum shift for 0000000
6	TXCPADJ6	R/W	0	
5	TXCPADJ5	R/W	0	
4	TXCPADJ4	R/W	0	
3	TXCPADJ3	R/W	0	
2	TXCPADJ2	R/W	0	
1	TXCPADJ1	R/W	0	
0	TXCPADJ0	R/W	0	

7.6.3.6 TX Register 15 (offset = 0000 0000) [reset = 0h]

Figure 36. TX Register 15

7	6	5	4	3	2	1	0
TXBIAS9	TXBIAS8	TXBIAS7	TXBIAS6	TXBIAS5	TXBIAS4	TXBIAS3	TXBIAS2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. TX Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXBIAS9	R/W	0	**Bias current settings (8MSB; 2LSBs are in register 16)** **Closed loop (APC):** Coupling ratio CR = I_{BIAS} / I_{PD}, TXBIAS = 0..1023, I_{BIAS} ≤ 150 mA: TXPDRNG = 00; I_{BIAS} = 0.75 µA x CR x TXBIAS TXPDRNG = 01; I_{BIAS} = 1.5 µA x CR x TXBIAS TXPDRNG = 1X; I_{BIAS} = 3 µA x CR x TXBIAS **Open Loop:** I_{BIAS} ~ 147 µA x TXBIAS in source mode I_{BIAS} ~ 147 µA x TXBIAS in sink mode
6	TXBIAS8	R/W	0	
5	TXBIAS7	R/W	0	
4	TXBIAS6	R/W	0	
3	TXBIAS5	R/W	0	
2	TXBIAS4	R/W	0	
1	TXBIAS3	R/W	0	
0	TXBIAS2	R/W	0	

7.6.3.7 TX Register 16 (offset = 0000 0000) [reset = 0h]

Figure 37. TX Register 16

7	6	5	4	3	2	1	0
Reserved	TXDMONP	TXDMONB	Reserved			TXBIAS1	TXBIAS1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. TX Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6	TXDMONP	R/W	0	**Digital photodiode current monitor selection bit (MONP)** 1 = Digital photodiode monitor is active (no external resistor is needed) 0 = Analog photodiode monitor is active (external resistor is required)
5	TXDMONB	R/W	0	**Digital bias current monitor selection bit (MONB)** 1 = Digital bias current monitor is active (no external resistor is needed) 0 = Analog bias current monitor is active (external resistor is required)
4:2	Reserved	R/W	0	Reserved
1	TXBIAS1	R/W	0	Laser Bias current setting (2 LSBs)
0	TXBIAS0	R/W	0	

7.6.3.8 TX Register 17 (offset = 0000 0000) [reset = 0h]

Figure 38. TX Register 17

7	6	5	4	3	2	1	0
TXBMF7	TXBMF6	TXBMF5	TXBMF4	TXBMF3	TXBMF2	TXBMF1	TXBMF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. TX Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXBMF7	R/W	0	**Bias current monitor fault threshold** With TXDMONB = 1 Register sets the value of the bias current that will trigger a fault. The external resistor on the MONB pin must be removed to use this feature.
6	TXBMF6	R/W	0	
5	TXBMF5	R/W	0	
4	TXBMF4	R/W	0	
3	TXBMF3	R/W	0	
2	TXBMF2	R/W	0	
1	TXBMF1	R/W	0	
0	TXBMF0	R/W	0	

7.6.3.9 TX Register 18 (offset = 0000 0000) [reset = 0h]

Figure 39. TX Register 18

7	6	5	4	3	2	1	0
TXPMF7	TXPMF6	TXPMF5	TXPMF4	TXPMF3	TXPMF2	TXPMF1	TXPMF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. TX Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXPMF7	R/W	0	**Power monitor fault threshold** With TXDMONP = 1 Register sets the value of the photodiode current that will trigger a fault. The external resistor on the MONP pin must be removed to use this feature.
6	TXPMF6	R/W	0	
5	TXPMF5	R/W	0	
4	TXPMF4	R/W	0	
3	TXPMF3	R/W	0	
2	TXPMF2	R/W	0	
1	TXPMF1	R/W	0	
0	TXPMF0	R/W	0	

7.6.3.10 TX Register 19 (offset = 0000 0000) [reset = 0h]

Figure 40. TX Register 19

7	6	5	4	3	2	1	0
TXFD_MOD1	TXFD_MOD0	TXFD_EN	TXFD_DIS	0TXFL_DIS	TXDIV2	TXDIV1	TXDIV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. TX Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXFD_MOD1	R/W	0	**TX frequency detection mode selection** 00 = auto selection enabled 01 = Pre-selected to 10.3 Gbps 10 = Pre-select to 11.1 Gbps 11 = test mode (do not use)
6	TXFD_MOD0	R/W	0	
5	TXFD_EN	R/W	0	**TX frequency detector enable bit** 1 =TX frequency detector is always enabled 0 = TX frequency detector in automatic mode
4	TXFD_DIS	R/W	0	**TX frequency detector disable bit** 1 = TX frequency detector is always disabled 0 = TX frequency detector is in automatic mode
3	TXFL_DIS	R/W	0	**TX CDR fast lock disable bit** 1 = TX CDR fast lock disabled 0 = TX CDR in fast lock mode
2	TXDIV2	R/W	0	**TX Divider Ratio** 000: Full-Rate, 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 101: Divide by 32
1	TXDIV1	R/W	0	
0	TXDIV0	R/W	0	

7.6.4 Reserved Registers

7.6.4.1 Reserved Registers 20-39

Figure 41. Reserved Registers 20-39

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Reserved Registers 20-39 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	0	Reserved

7.6.5 Read Only Registers

7.6.5.1 Core Level Register 40 (offset = 0000 0000) [reset = 0h]

Figure 42. Core Level Register 40

7	6	5	4	3	2	1	0
ADC9	ADC8	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Core Level Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC9 (MSB)	R	0	Digital representation of the ADC input source (read only)
6	ADC8	R	0	
5	ADC7	R	0	
4	ADC6	R	0	
3	ADC5	R	0	
2	ADC4	R	0	
1	ADC3	R	0	
0	ADC2	R	0	

7.6.5.2 Core Level Register 41 (offset = 0000 0000) [reset = 0h]

Figure 43. Core Level Register 41

7	6	5	4	3	2	1	0
Reserved						ADC1	ADC0
R						R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Core Level Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	Resereved	R	0h	Reserved
1	ADC1	R	0h	Digital representation of the ADC input source (read only)
0	ADC0 (LSB)	R	0h	

7.6.5.3 RX Registers 42 (offset = 0000 0000) [reset = 0h]

Figure 44. RX Registers 42

7	6	5	4	3	2	1	0
Reserved							
R	RCLR	R	RCLR			R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; RCLR = Read clear

Table 21. RX Registers 42 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6	Reserved	RCLR	0	Reserved
5	Reserved	R	0	Reserved
4	Reserved	RCLR	0	Reserved
3:0	Reserved	R	0	Reserved

7.6.5.4 TX Register 43 (offset = 0000 0000) [reset = 0h]

Figure 45. Core Level Register 43

7	6	5	4	3	2	1	0
TXCDRLock	TXCDRLock	TX_FLT	TX_DRVDIS	Reserved			
R	R	R	R	R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; RCLR = Read clear

Table 22. TX Registers 43 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXCDRLock	R	0	**TX CDR lock status bit** 1 = TX CDR is not locked 0 = TX CDR is locked
6	TXCDRLock (latched Low)	RCLR	0	Latched low status of bit 7. Cleared when read. Latched low bit set to 0 when raw status goes low and keep it low even if raw status goes high.
5	TX_FLT	R	0	**TX fault status bit** 1 = TX fault detected 0 = TX fault not detected
4	TX_DRVDIS	R	0	**TX driver disable status bit** 1 = TX fault logic disables the driver 0 = TX fault logic does not disable the driver
3:0	Reserved	R	0	Reserved

7.6.6 Adjustment Registers

7.6.6.1 Adjustment Registers 44-50

Figure 46. Adjustment Registers 44-50

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Adjustment Registers 44-50 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	0	Reserved

7.6.6.2 Adjustment Register 51 (offset = 0100 0000) [reset = 40h]

Figure 47. Adjustment Register 51

7	6	5	4	3	2	1	0
SEL_RES_2	SEL_RES_1	SEL_RES_0	Reserved				
R	R	R	R				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Adjustment Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
7	SEL_RES_2	R/W	0	**CDR Loop Filter Resistor** 000: 75, 001: 150 010: 225 011: 300 100: 375 101: 450 110: 525 111: 600 Default = 225
6	SEL_RES_1	R/W	1	
5	SEL_RES_0	R/W	0	
4:0	Reserved	R/W	0	Reserved

7.6.6.3 Adjustment Registers 52-55

Figure 48. Adjustment Registers 52-55

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Adjustment Registers 52-55 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	0	Reserved

8 Application Information and Implementations

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ONET1131EC is designed to be used in conjunction with a Transmitter Optical Sub-Assembly (TOSA). The ONET1131EC, TOSA, microcontroller and power management circuitry will typically be used in an XFP or SFP+ 10 Gbps optical transceiver. Figure 49 shows the ONET1131EC in differential mode of operation modulating a differentially driven Mach Zehnder (MZ) modulator TOSA and Figure 51 and Figure 52 show the device in single-ended output mode with an Electroabsorptive Modulated Laser (EML) TOSA. Figure 51 has the photodiode cathode available and Figure 52 has the photodiode anode available.

8.2 Typical Application, Transmitter Differential Mode

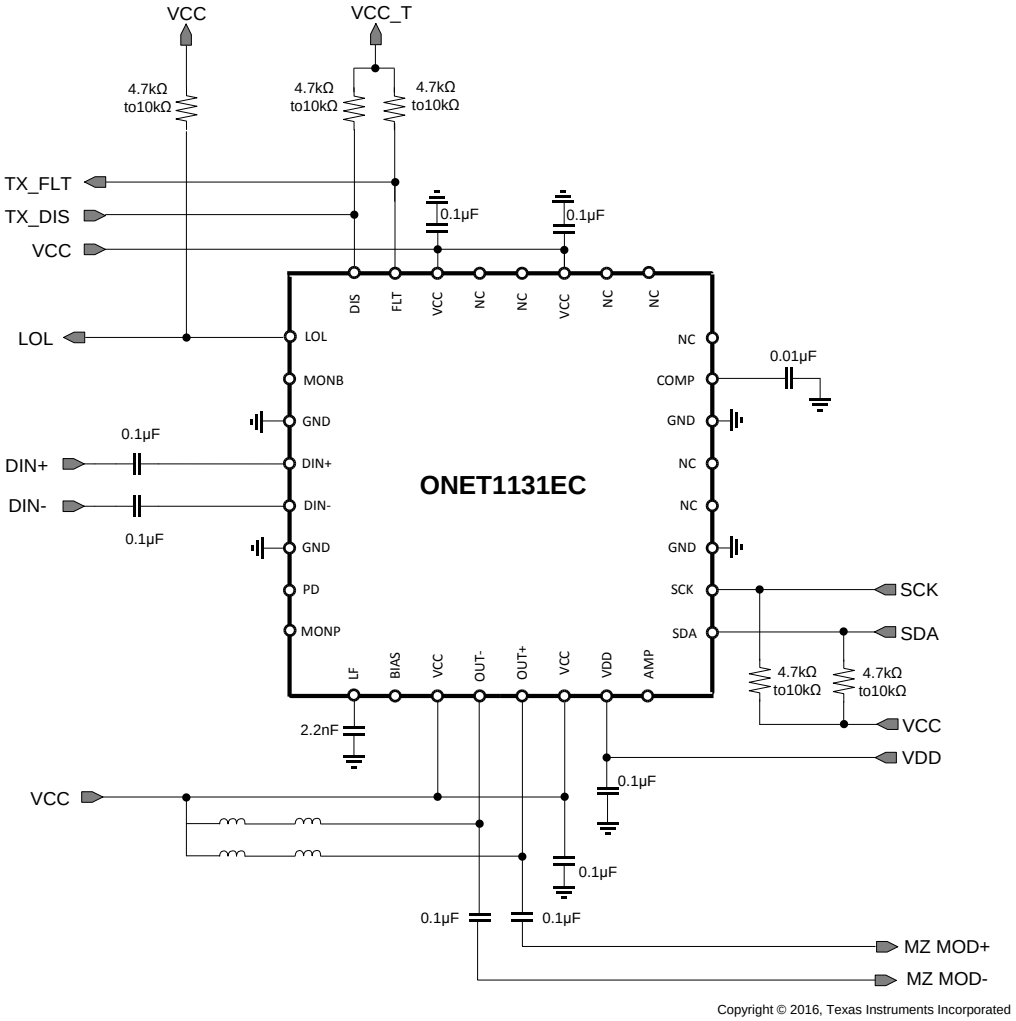


Figure 49. Typical Application Circuit in Differential Mode

Typical Application, Transmitter Differential Mode (continued)

8.2.1 Design Requirements

Table 26. Design Parameters

PARAMETER	VALUE
Supply voltage	2.5 V
Transmitter input voltage	100 mVpp to 1000 mVpp differential
Transmitter output voltage	1 Vpp to 3.6 Vpp differential

8.2.2 Detailed Design Procedure

In the transmitter differential mode of operation, the output driver is intended to be used with a differentially driven Mach Zehnder (MZ) modulator TOSA. On the input side, the DIN+ and DIN- pins are required to be AC coupled to the signal from the host system and the input voltage should be between 100 mVpp and 1000 mVpp differential. On the output side, the OUT+ pin is AC coupled to the modulator positive input and the OUT– pin is AC coupled to the modulator negative input. A bias-T from VCC to both the OUT+ and OUT– pins is required to supply sufficient headroom voltage for the output driver transistors. It is recommended that the inductance in the bias-T have low DC resistance to limit the DC voltage drop and maximize the voltage supplied to the OUT+ and OUT– pins. If the voltage on these pins drops below approximately 2.1 V then the output rise and fall times can be adversely affected.

8.2.3 Application Curve

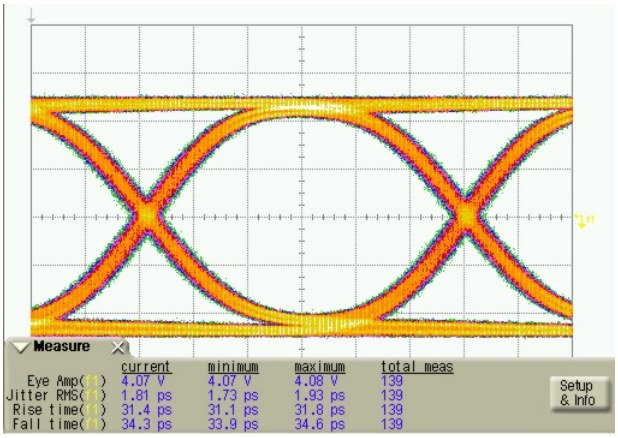


Figure 50. Differential Mode Transmitter Output Eye Diagram

8.2.4 Typical Application, Transmitter Single-Ended Mode

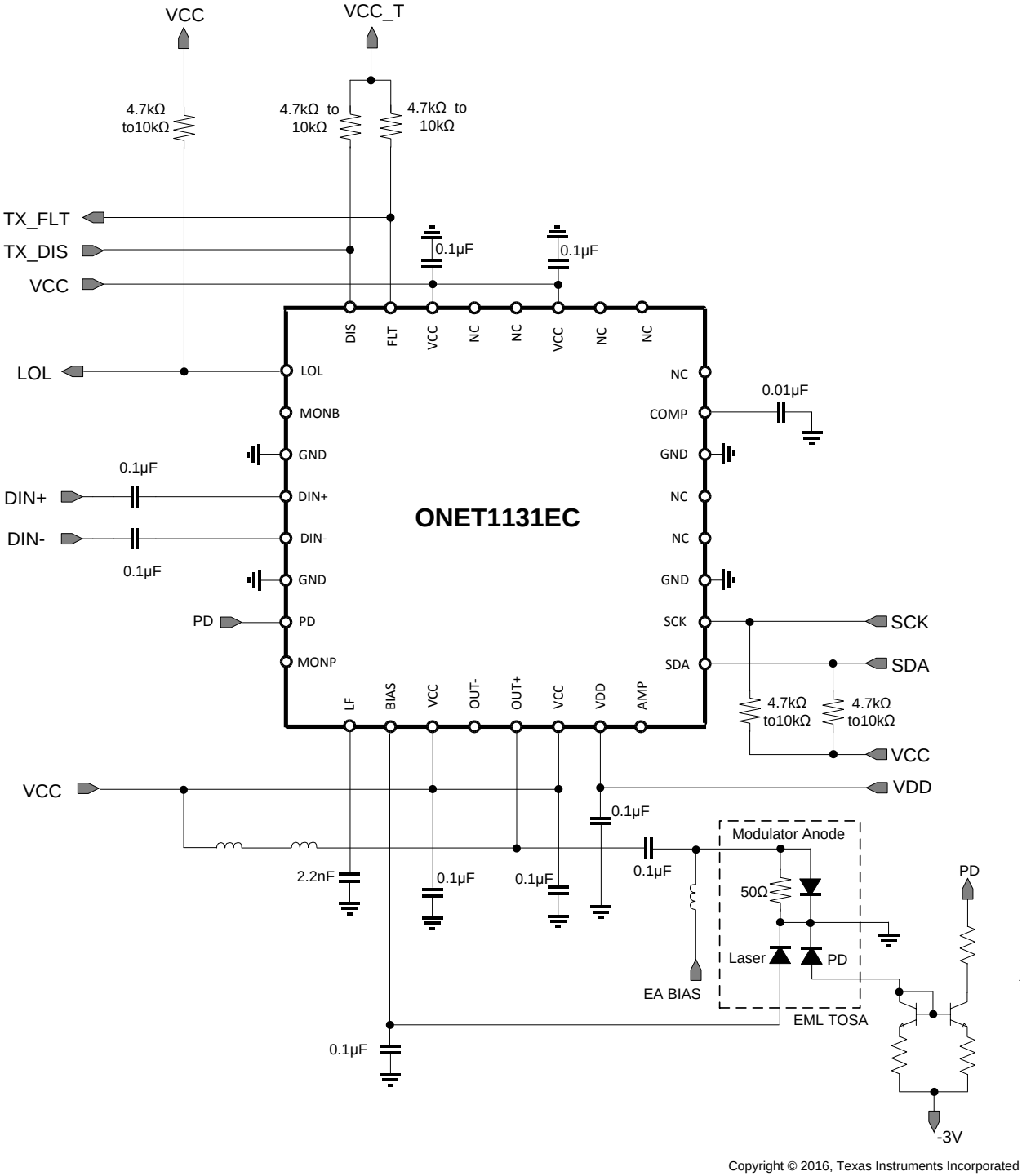


Figure 51. Typical Application Circuit in Single-Ended Mode with an EML and the PD Monitor Cathode Available

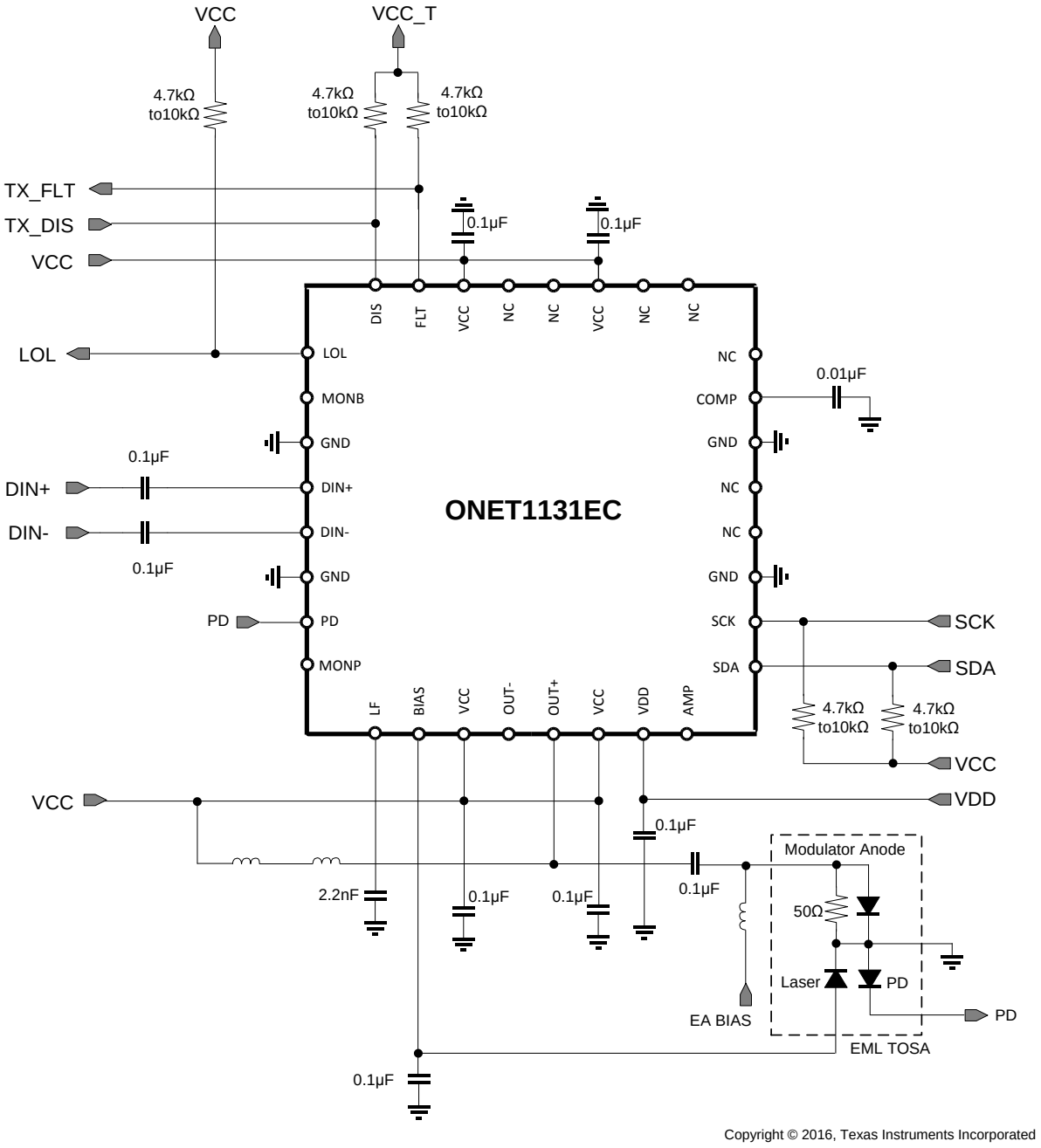


Figure 52. Typical Application Circuit in Single-Ended Mode with an EML and the PD Monitor Anode Available

8.2.4.1 Design Requirements

Table 27. Design Parameters

PARAMETER	VALUE
Supply voltage	2.5 V
Transmitter input voltage	100 mVpp to 1000 mVpp differential
Transmitter output voltage	0.5 Vpp to 2 Vpp single-ended

8.2.4.2 Detailed Design Procedure

In the transmitter single-ended mode of operation, the output driver is intended to be used with a single-ended driven Electroabsorptive Modulated Laser (EML) TOSA. On the input side, the DIN+ and DIN– pins are required to be AC coupled to the signal from the host system and the input voltage should be between 100 mVpp and 1000 mVpp differential. On the output side, it is recommended that the OUT+ pin is AC coupled to the modulator input and the OUT– pin can be left unterminated or terminated to VCC through a 50-Ω resistor. A bias-T from VCC to the OUT+ pin is required to supply sufficient headroom voltage for the output driver transistors. It is recommended that the inductance in the bias-T have low DC resistance to limit the DC voltage drop and maximize the voltage supplied to the TXOUT+ pin. If the voltage on this pins drops below approximately 2.1V then the output rise and fall times can be adversely affected.

8.2.4.3 Application Curves

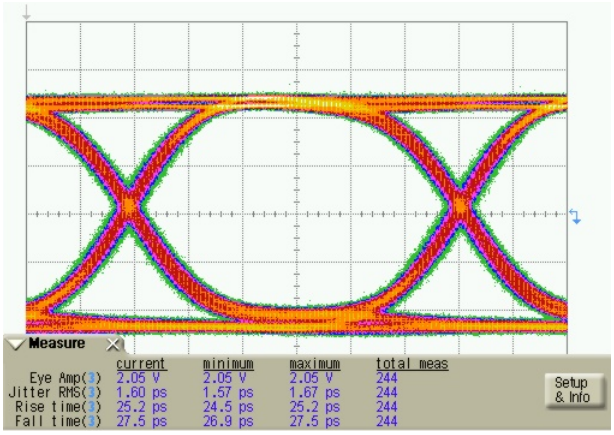


Figure 53. Single-Ended Mode Transmitter Output Eye Diagram

9 Power Supply Recommendations

The ONET1131EC is designed to operate from an input supply voltage range between 2.37 V and 2.63 V. To reduce digital coupling into the analog circuitry, there are separate supplies for the transmitter, and digital circuitry. VCC is used to supply power to the transmitter, and VDD is used to supply power to the digital block. Power supply decoupling capacitors should be placed as close as possible to the respective power supply pins.

10 Layout

10.1 Layout Guidelines

For optimum performance, use 50-Ω transmission lines (100-Ω differential) for connecting the high speed inputs and outputs. The length of transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter.

If the single-ended mode of operation is being used (TXMODE = 1) then it is recommended to terminate the unused output with a 50-Ω resistor to VCC. Figure 54 shows a typical layout for the high speed inputs and outputs.

10.2 Layout Example

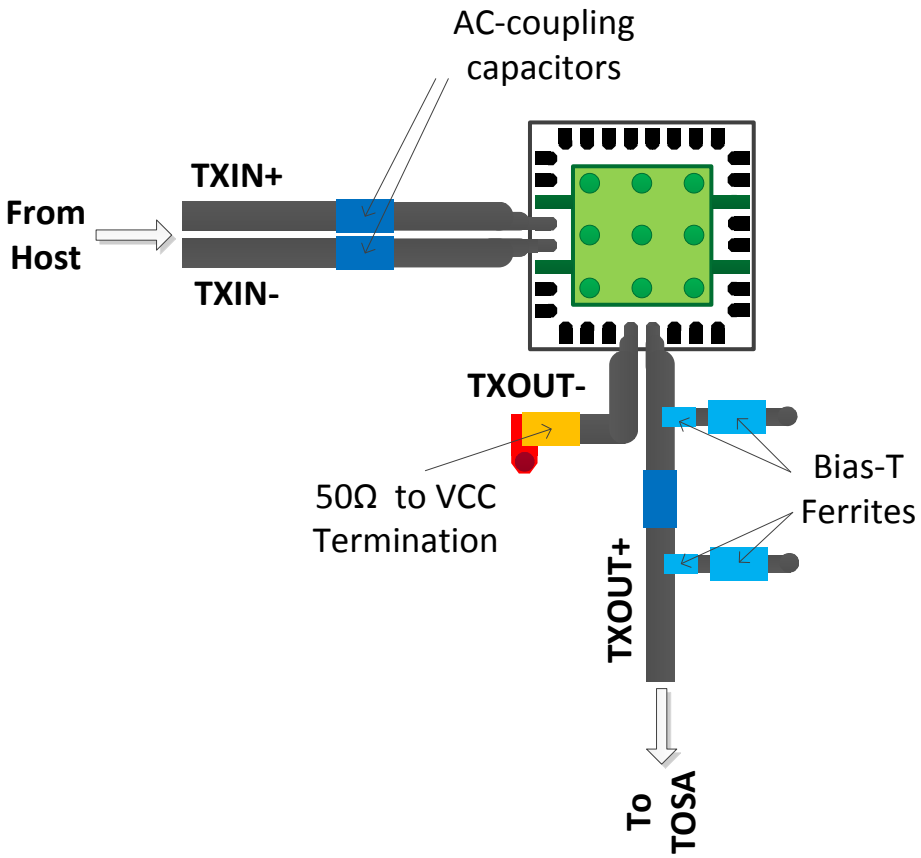


Figure 54. Board Layout

11 器件和文档支持

11.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.2 社区资源

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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11.3 商标

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ONET1131ECRSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1131EC
ONET1131ECRSMR.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1131EC
ONET1131ECRSMT	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1131EC
ONET1131ECRSMT.A	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1131EC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

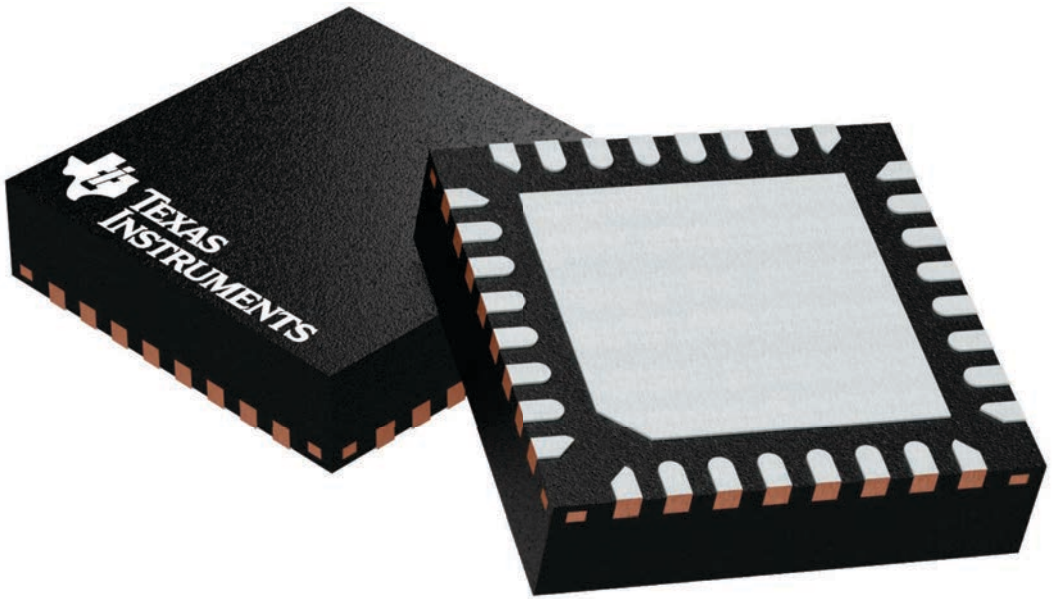
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



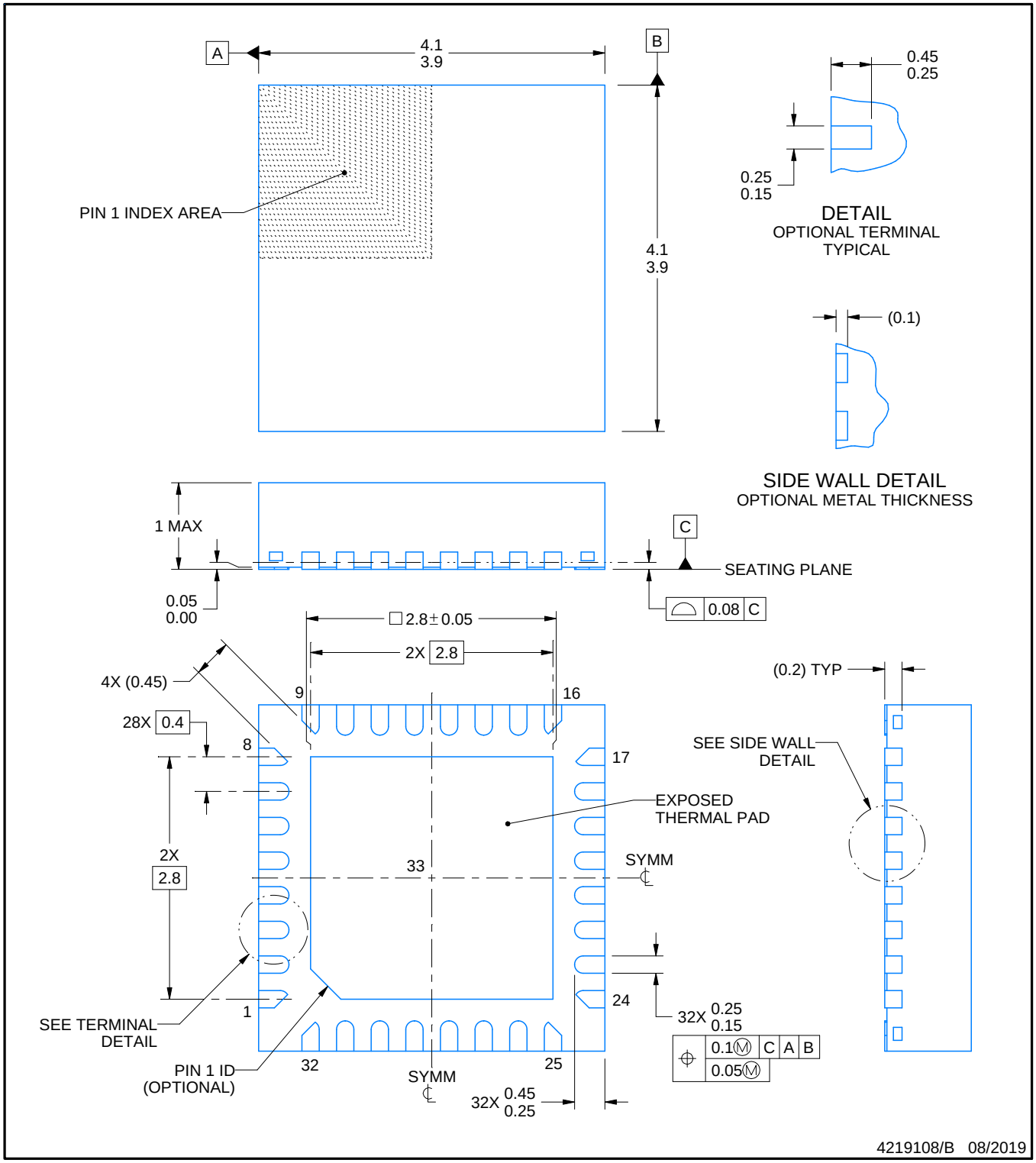
4224982/A

PACKAGE OUTLINE

RSM0032B

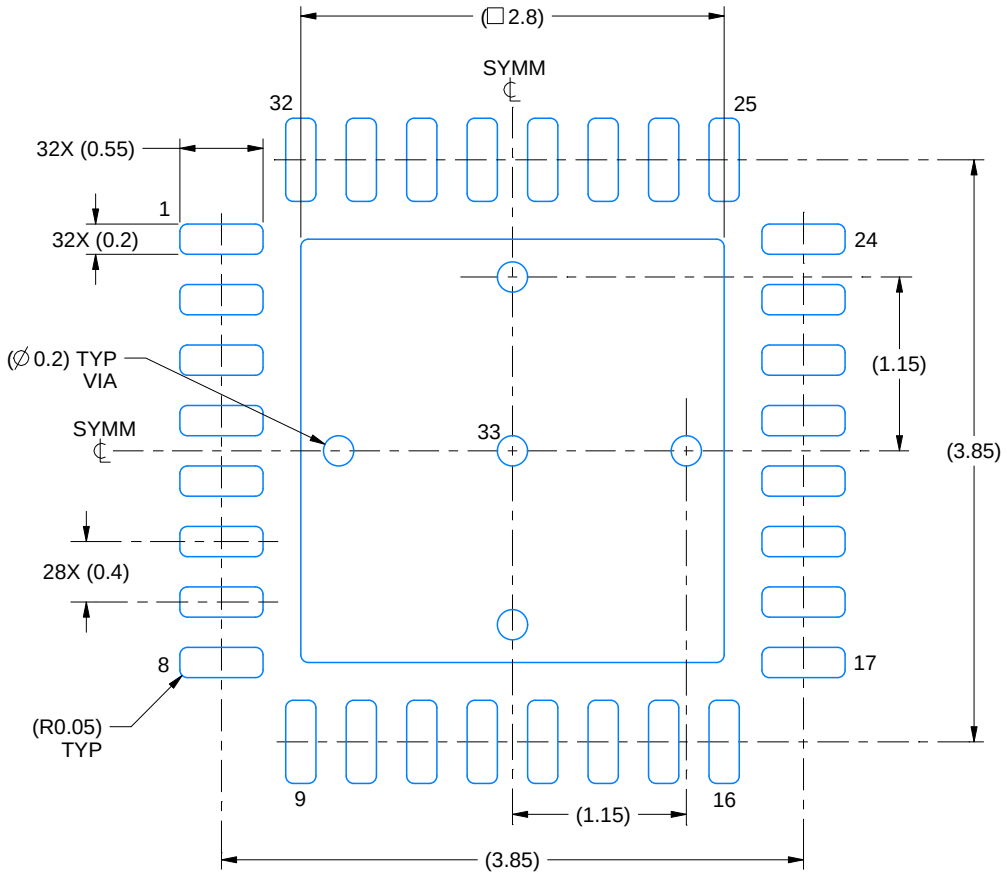
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

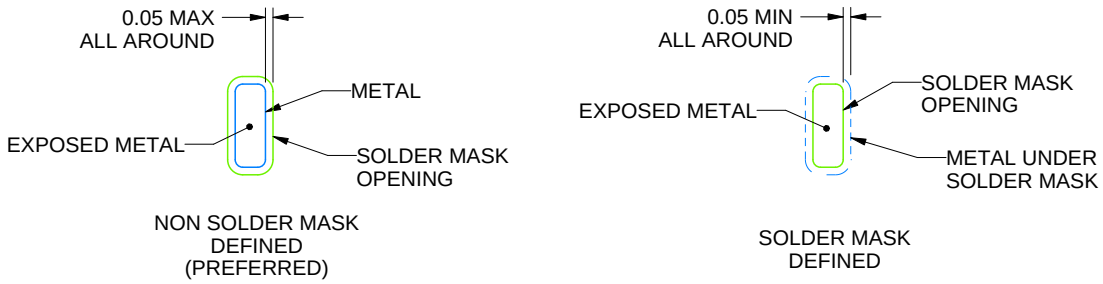


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

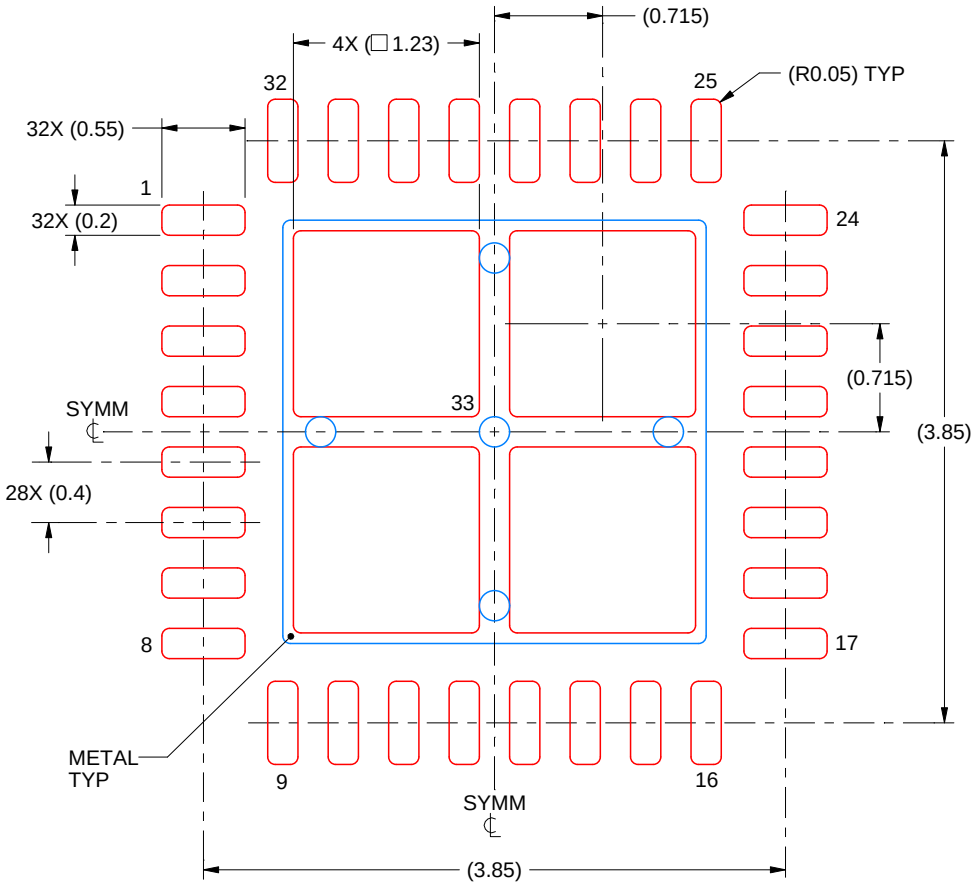


SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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