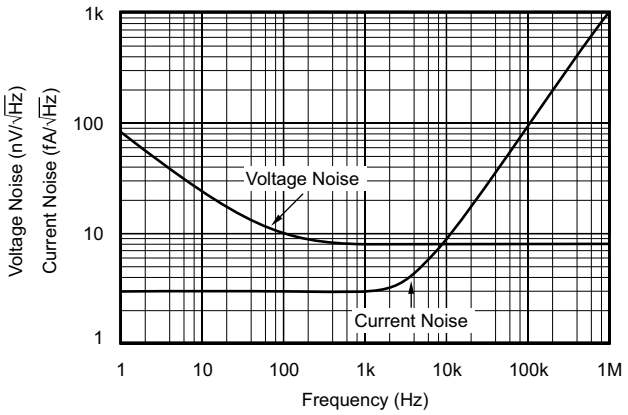
OPAx132 高速 FET 输入运算放大器

1 特性

- 此器件的新版本现已上市：OPA2156
- FET 输入：I_B = 50pA（最大值）
- 高带宽：8MHz
- 高压摆率：20V/μs
- 低噪声： 8nV/√Hz (1kHz)
- 低失真：0.00008%
- 高开环增益：126dB（2kΩ 负载）
- 宽电源电压范围：±2.5V 至 ±18V
- 低失调电压：500μV（最大值）
- 单通道、双通道和四通道版本

2 应用

- SAR ADC 驱动器
- 电压基准缓冲器
- 跨阻放大器
- 光电二极管放大器
- 有源滤波器
- 积分器



低噪声 JFET 输入

3 说明

OPA132、OPA2132 和 OPA4132 (OPAx132) 系列 FET 输入运算放大器提供高速特性和出色的直流性能。高压摆率和宽带宽的组合可提供快速稳定时间。单通道、双通道和四通道版本均具有相同的规格，可更大程度地提高设计灵活性。单通道和双通道版本均具有高性能级别。它们都是通用、音频、数据采集和通信应用的理想选择，尤其是会遇到高源阻抗的应用。

OPAx132 运算放大器易于使用，而且不存在常见 FET 输入运算放大器中经常会出现的相位反转和过载问题。输入共源共栅电路提供出色的共模抑制，并在宽输入电压范围内保持低输入偏置电流。OPAx132 系列运算放大器是单位增益稳定型放大器，可在宽负载条件范围（包括高负载电容）内提供出色的动态行为。双通道和四通道版本有完全独立的电路，即使在过驱或过载时，也可尽可能减少串扰并消除相互干扰。

单通道版本采用 8 引脚 SOIC 表面贴装封装，双通道版本采用 8 引脚 DIP 和 SOIC 表面贴装封装。四通道版本采用 SOIC 表面贴装封装。所有器件的额定工作温度范围为 –40°C 至 +85°C。

OPA2156 是下一代版本，可提供更低的宽带噪声 (3nV/√Hz)、更宽的带宽 (25MHz) 以及轨到轨输入。

器件信息

器件型号	通道数	封装(1)
OPA132	单通道	D（SOIC，8）
OPA2132	双通道	D（SOIC，8）
		P（PDIP，8）
OPA4132	四通道	D（SOIC，14）

(1) 有关更多信息，请参阅节 10。

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

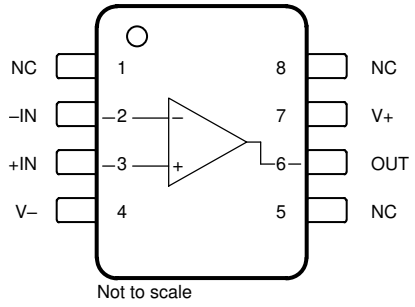

图 4-1. OPA132: D Package, 8-Pin SOIC (Top View)

Pin Functions: OPA132

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
– IN	2	Input	Inverting input
NC	1, 5	—	Do not connect these pins(1)
NC	8	—	No internal connection. Float this pin.
Output	6	Output	Output
V+	7	Power	Positive power supply
V –	4	Power	Negative power supply

(1) Existing layouts for the OPA132 before revision C of this data sheet do not need to be redesigned.

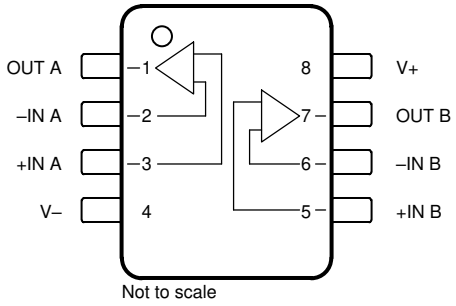

图 4-2. OPA2132: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

表 4-1. Pin Functions: OPA2132

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
– IN A	2	Input	Inverting input, channel A
– IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V –	4	Power	Negative (lowest) power supply

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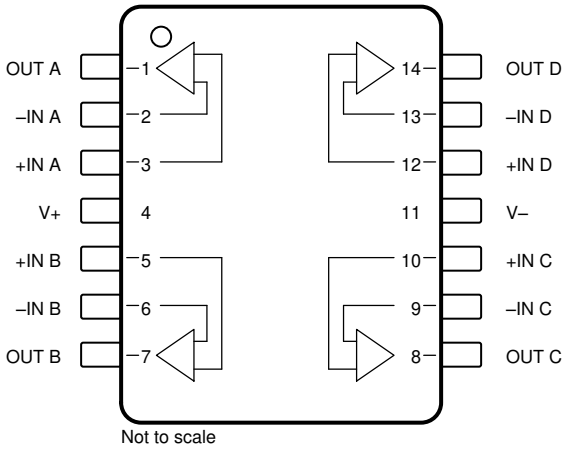

图 4-3. OPA4132- D Package, 14-Pin SOIC (Top View)

表 4-2. Pin Functions: OPA4132

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
– IN A	2	Input	Inverting input, channel A
– IN B	6	Input	Inverting input, channel B
– IN C	9	Input	Inverting input, channel C
– IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V –	11	Power	Negative (lowest) power supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)		36	V
	Input voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Input current(2)		±10	mA
I_{SC}	Output short-circuit(3)	Continuous		
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
OPA132 in SOIC Package, OPA2132 in PDIP Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
OPA2132 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
OPA4132				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±2.5	±15	±18	V
		Single supply	9	30	36	
T_A	Ambient temperature		–40		85	°C

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5.4 Thermal Information - OPA132

THERMAL METRIC(1)		OPA132 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information - OPA2132

THERMAL METRIC(1)		OPA2132 D (SOIC) 8 PINS	OPA2132 P (PDIP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	71	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	36	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9	16	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50	35	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information - OPA4132

THERMAL METRIC(1)		OPA4132 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.7 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPAx132U			±0.2	±0.5	mV
		OPAx132UA			±0.5	±2	
dV_{OS}/dT	Input offset voltage drift	T_A = – 40°C to +85°C			±2	±10	µV/°C
PSRR	Power-supply rejection ratio	±2.5V ≤ V_S ≤ ±18V	OPAx132U		±5	±15	µV/V
			OPAx132UA		±5	±30	
	Channel separation (dual and quad)	R_L = 2kΩ			0.2		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±5	±50	pA
		T_A = – 40°C to +85°C			See *Typical Characteristics*		
I_{OS}	Input offset current(1)				±2	±50	pA
NOISE							
e_n	Input voltage noise density	f = 10Hz			23		nV/√Hz
		f = 100Hz			10		
		f = 1kHz			8		
		f = 10kHz			8		
I_n	Input current noise density	f = 1kHz			3		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V –) + 2.5	±13	(V+) – 3.5	V
CMRR	Common-mode rejection ratio	– 12.5V ≤ V_{CM} ≤ 11.5V	OPAx132U	96	100		dB
			OPAx132UA	86	94		
INPUT IMPEDANCE							
	Differential				10^{13} || 10		Ω || pF
	Common-mode	– 12.5V ≤ V_{CM} ≤ 11.5V			10^{13} || 7		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 10kΩ, – 14.5V ≤ V_O ≤ 13.8V	OPAx132U	110	120		dB
			OPAx132UA	104	120		
		R_L = 2kΩ, – 13.8V ≤ V_O ≤ 13.5V	OPAx132U	110	126		
			OPAx132UA	104	120		
		R_L = 600Ω, – 12.8V ≤ V_O ≤ 12.5V	OPAx132U	110	130		
			OPAx132UA	104	120		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				8		MHz
SR	Slew rate				±20		V/µs
	Settling time	10V step, G = 1, C_L = 100pF	0.1%		0.7		µs
			0.01%		1		
THD+N	Total harmonic distortion plus noise	f = 1kHz, G = 1, V_O = 3.5V_{rms}	R_L = 2kΩ		0.0008%		
			R_L = 600Ω		0.0009%		
	Overload recovery time	G = ±1			600		ns
OUTPUT							
V_O	Voltage output	R_L = 10kΩ	Positive	(V+) – 1.2	(V+) – 0.9		V
			Negative		(V –) + 0.3	(V –) + 0.5	
		R_L = 2kΩ	Positive	(V+) – 1.5	(V+) – 1.1		
			Negative		(V –) + 1.2	(V –) + 0.9	
		R_L = 600Ω	Positive	(V+) – 2.5	(V+) – 2.0		
			Negative		(V –) + 2.2	(V –) + 1.5	
I_{SC}	Short-circuit current	Sourcing			36		mA
		Sinking			– 30		mA
	Capacitive load drive (stable operation)				See *Typical Characteristics*		
POWER SUPPLY							

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at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current (per amplifier)	I_O = 0mA		±4	±4.8	mA

(1) High-speed test at T_J = 25°C.

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5.8 Typical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

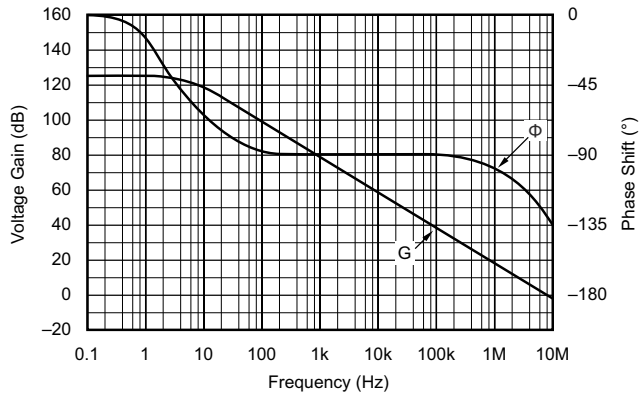

图 5-1. Open-Loop Gain and Phase vs Frequency

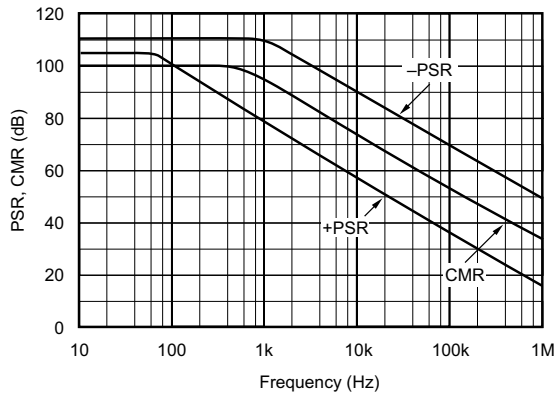

图 5-2. Power Supply and Common-Mode Rejection vs Frequency

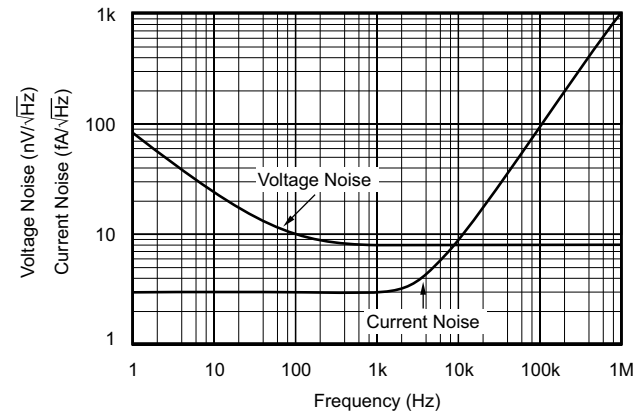

图 5-3. Input Voltage vs Frequency

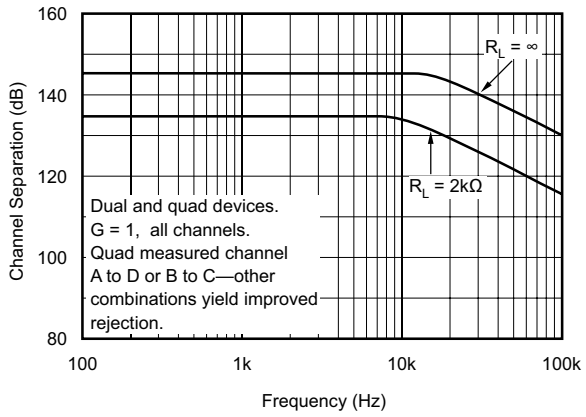

图 5-4. Channel Separation vs Frequency

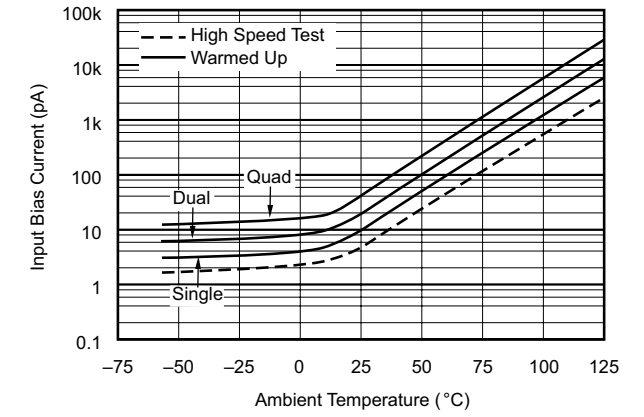

图 5-5. Input Bias Current vs Temperature

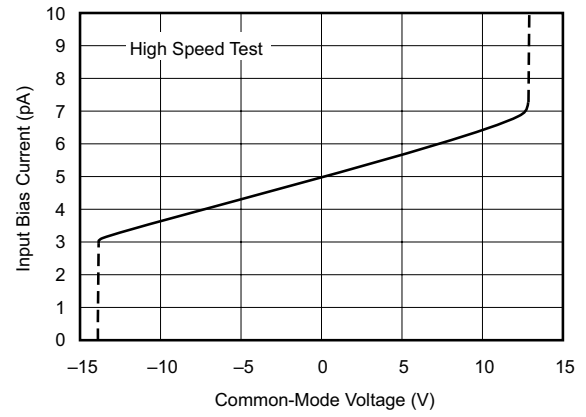

图 5-6. Input Bias Current vs Input Common-Mode Voltage

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

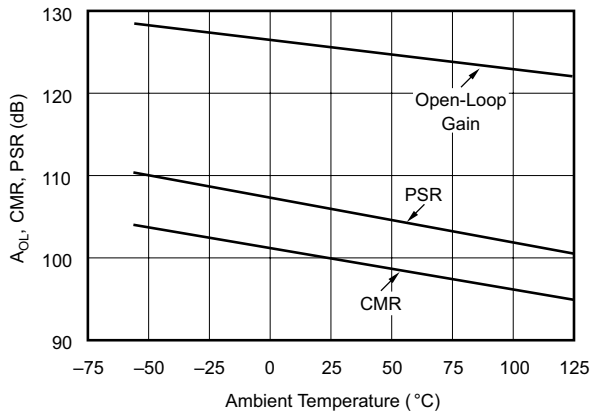

图 5-7. A_{OL}, CMR, PSR vs Temperature

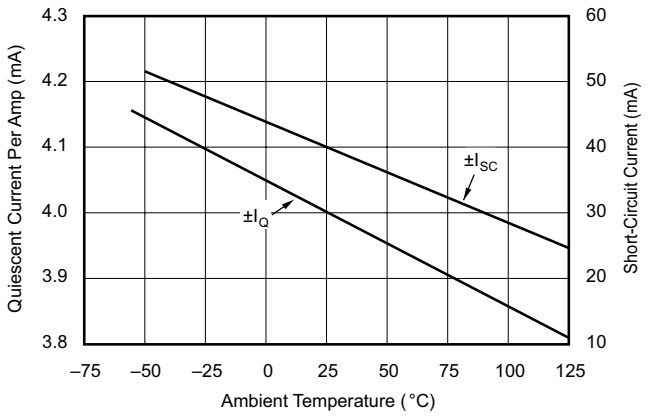

图 5-8. Quiescent Current and Short-Circuit Current vs Temperature

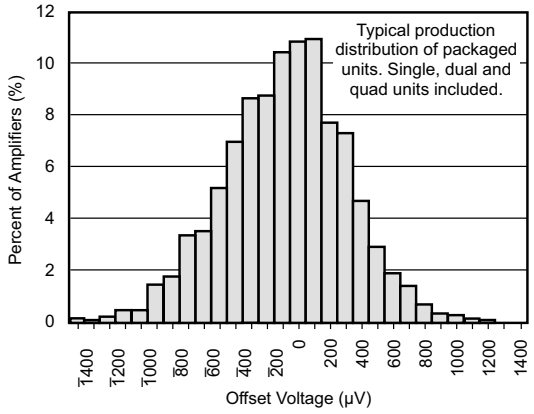

图 5-9. Offset Voltage Production Distribution

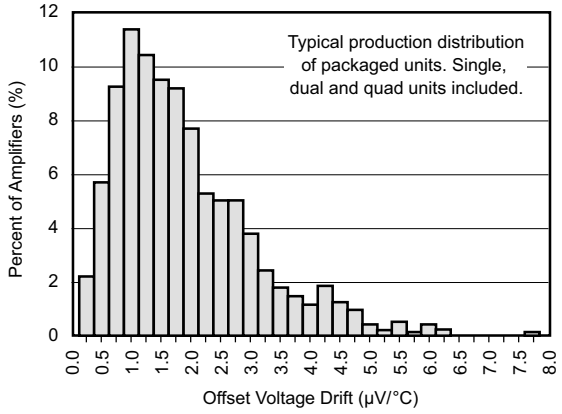

图 5-10. Offset Voltage Drift Production Distribution

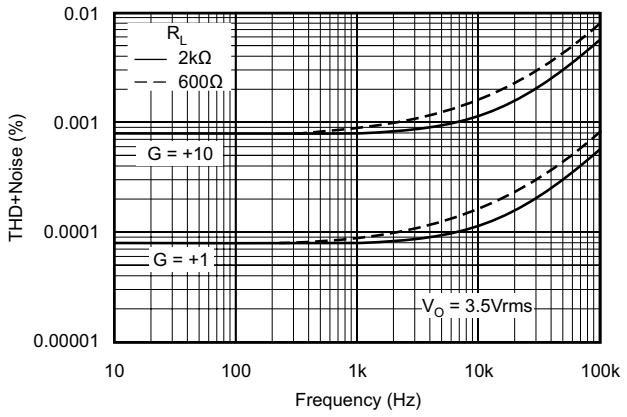

图 5-11. Total Harmonic Distortion + Noise vs Frequency

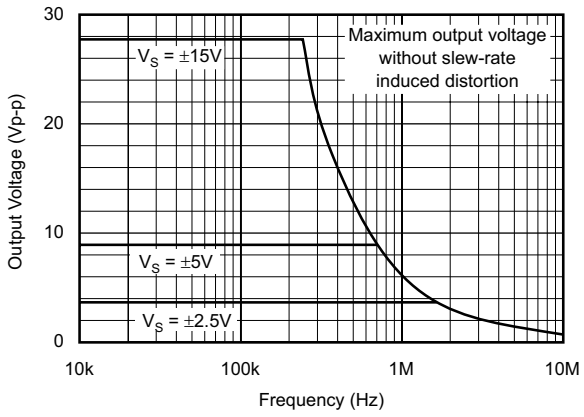

图 5-12. Maximum Output Voltage vs Frequency

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

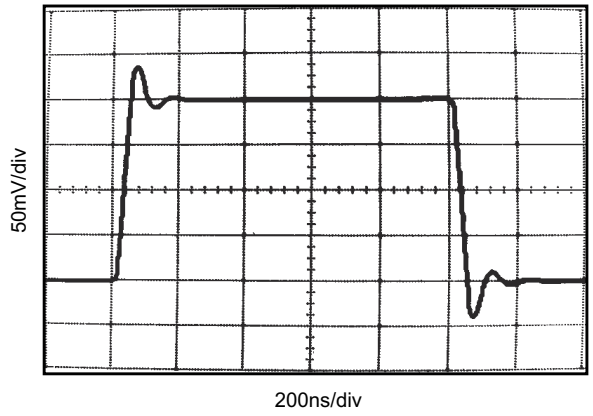


图 5-13. Small-Signal Step Response

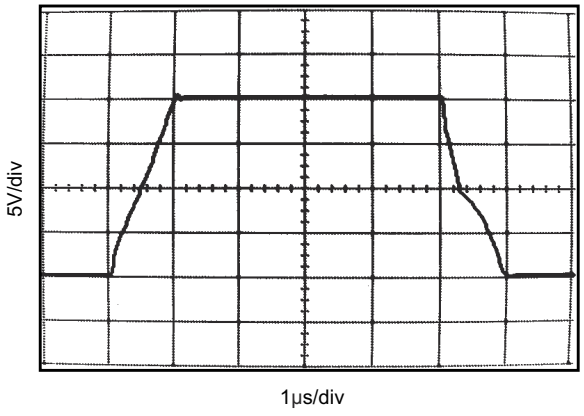


图 5-14. Large-Signal Step Response

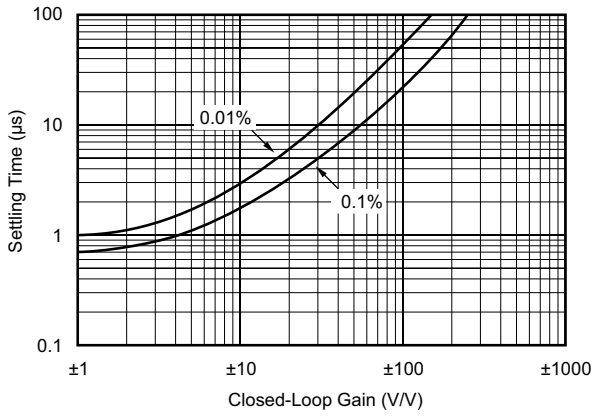


图 5-15. Settling Time vs Closed-Loop Gain

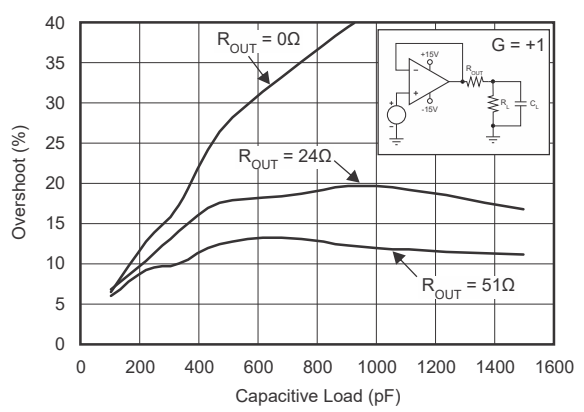
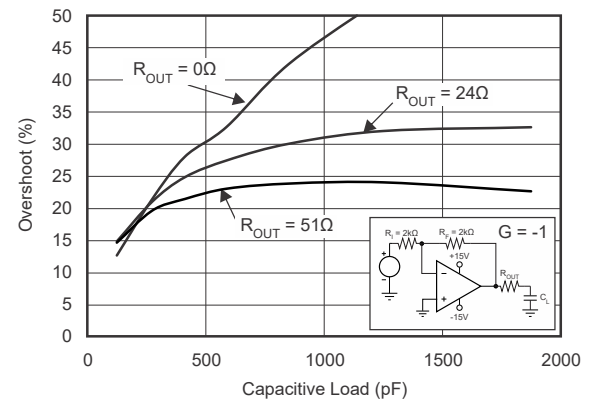
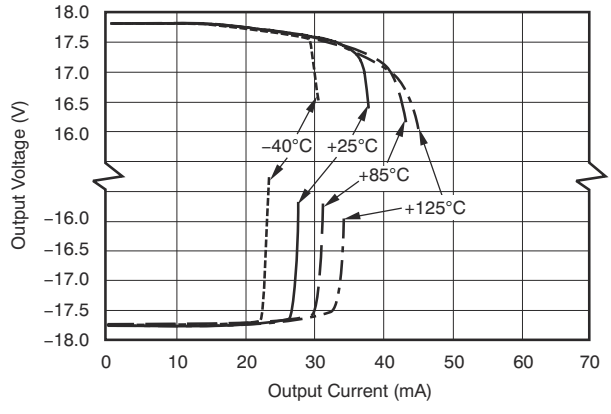


图 5-16. Small-Signal Overshoot vs Load Capacitance



G = +1

图 5-17. Small-Signal Overshoot vs Load Capacitance



G = –1

图 5-18. Output Voltage Swing vs Output Current

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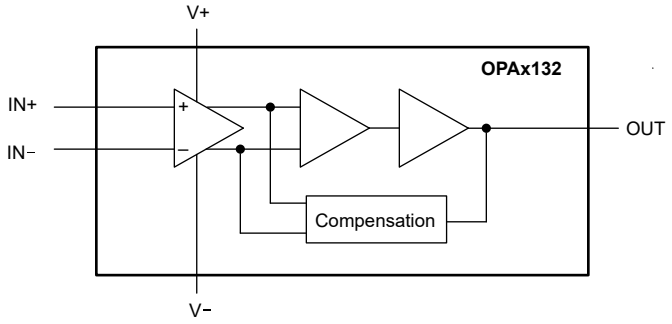
6 Detailed Description

6.1 Overview

The OPAx132 series of FET-input operational amplifiers provides high speed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All devices are an excellent choice for general-purpose, audio, data acquisition and communications applications; especially, where high source impedance is encountered.

6.2 Functional Block Diagram



6.3 Feature Description

The OPAx132 series of JFET operational amplifiers combine low noise and wide bandwidth with precision and low input bias current to make the these devices an excellent choice for applications with a high source impedance. The OPAx132 is unity-gain stable and features high slew rate (±20V/μs) and wide bandwidth (8MHz).

6.4 Device Functional Modes

The OPAx132 has a single functional mode and is operational when the power-supply voltage is greater than 5V (±2.5V). The maximum power supply voltage for the OPAx132 is 36V (±18V).

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The OPAx132 series operational amplifiers are unity-gain stable and an excellent choice for a wide range of general-purpose applications. Bypass power-supply pins with 10nF ceramic capacitors or larger.

The OPAx132 series operational amplifiers are free from unexpected output phase reversal common with FET operational amplifiers. Many FET-input operational amplifiers exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This phase reversal can occur in voltage-follower circuits, causing serious problems in control-loop applications. The OPAx132 series of operational amplifiers are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, maintaining normal behavior when one amplifier in a package is overdriven or short-circuited.

7.1.1 Operating Voltage

The OPAx132 series of operation amplifiers operate with power supplies from ±2.5V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in *节 5.8* .

7.1.2 Offset Voltage Trim

The offset voltage of the OPAx132 amplifiers is laser trimmed and usually requires no user adjustment. The OPAx132 provide less than ±500μV of input offset voltage and less than 10μV/°C of input offset voltage drift over the operating temperature range

7.1.3 Input Bias Current

The FET-inputs of the OPAx132 series provide very low input bias current and cause negligible errors in most applications. For applications where low input bias current is crucial, minimize junction temperature rise. The input bias current of FET-input operational amplifiers increases with temperature; see also 图 5-5.

The OPAx132 series can be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±3V supplies reduces power dissipation to one-fifth used at ±15V.

The dual and quad versions have higher total power dissipation than the single version, leading to higher junction temperature. Thus, a warmed-up quad has higher input bias current than a warmed-up single. Furthermore, an SOIC generally has higher junction temperature than a DIP at the same ambient temperature because of a larger θ_{JA}.

Printed-circuit-board (PCB) layout also helps minimize junction temperature rise. Minimize temperature rise by soldering the devices to the PCB rather than using a socket. Wide copper traces also help dissipate the heat by acting as an additional heat sink.

Input stage cascode circuitry keeps the input bias current virtually unchanged throughout the full input common-mode range of the OPAx132 series. See also 图 5-6.

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7.2 Typical Application

The OPAx132 family offers outstanding dc precision and ac performance. These devices operate up to 36V supply rails and offer ultra-low input bias current and input bias current noise, as well as 8MHz bandwidth and high capacitive load drive. These features make the OPAx132 a robust, high-performance operational amplifier for high-voltage industrial applications with high source impedance.

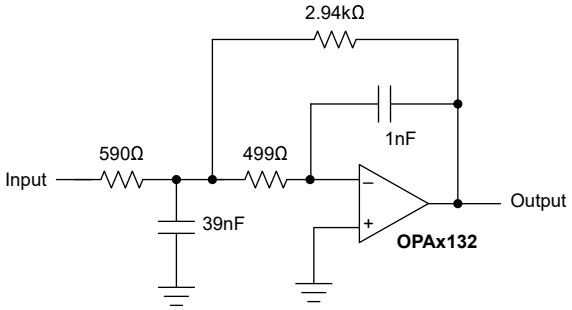

图 7-1. OPA132 2nd Order 30kHz, Low Pass Filter Schematic

7.2.1 Design Requirements

Use the following parameters for this application:

- Gain = 5V/V
- Low-pass cutoff frequency = 30kHz
- –40db/dec filter response
- Maintain less than 3dB gain peaking in the gain versus frequency response

7.2.2 Detailed Design Procedure

WEBENCH® Circuit Designer creates customized power supply and active filter circuits based on your system requirements. The environment gives you end-to-end selection, design, and simulation capabilities that save you time during all phases of the analog design process.

Use our tools to help with your designs:

- Filter design tool
- Powerstage designer
- WEBENCH® Power designer
- PCB thermal calculator

7.2.3 Application Curve

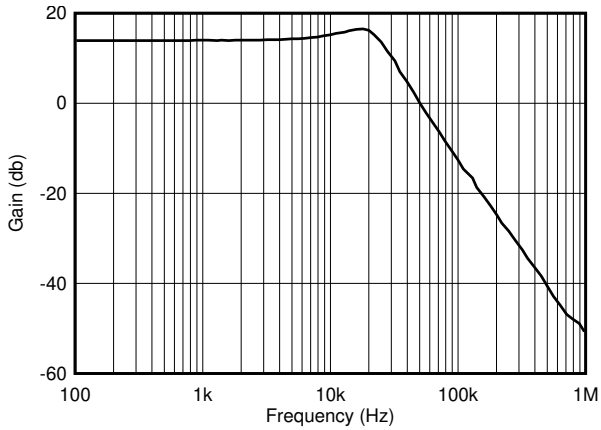

图 7-2. OPA132 2nd-Order 30kHz, Low-Pass Filter Response

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7.3 Power Supply Recommendations

The OPAx132 is specified for operation from 5V to 36V (±2.5V to ±18V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in 节 5.8.

> 小心
>
> Supply voltages larger than 36V can permanently damage the device; see 节 5.1 .

Place 10nF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see 节 7.4.1 .

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier individually. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 10nF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see also *Circuit Board Layout Techniques* .
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep RF and RG close to the inverting input minimizes parasitic capacitance; see also 节 7.4.2 .
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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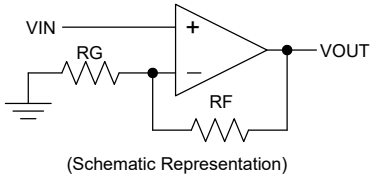
7.4.2 Layout Example



(Schematic Representation)

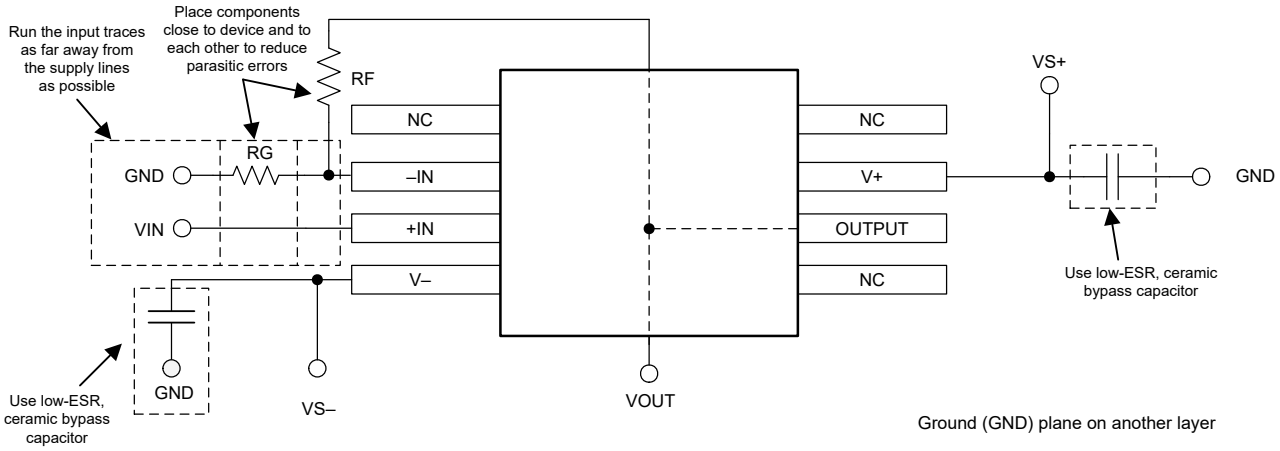


图 7-3. OPA132 Layout Example for the Noninverting Configuration

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.1.1.2 TINA-TI™ 仿真软件（免费下载）

TINA-TI™ 仿真软件是一款简单易用、功能强大且基于 SPICE 引擎的电路仿真程序。TINA-TI 仿真软件是 TINA™ 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 仿真软件提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 仿真软件提供全面的后处理能力，便于用户以多种方式获得结果，用户可从设计工具和仿真网页免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的能力，从而构建一个动态的快速启动工具。

备注

必须安装 TINA 软件或者 TINA-TI 软件后才能使用这些文件。请从 TINA-TI™ 软件文件夹中下载免费的 TINA-TI 仿真软件。

8.1.1.3 TI 参考设计

TI 参考设计是由 TI 的精密模拟应用专家创建的模拟解决方案。TI 参考设计提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。TI 参考设计可在线获取，网址为 https://www.ti.com/reference-designs。

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*
- Texas Instruments, *Circuit Board Layout Techniques*

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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8.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (September 2015) to Revision C (August 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了有关新的下一代 OPA2156 的信息	1
• 将高开环增益从 130dB（600Ω 负载）更改为 126dB（2kΩ 负载）	1
• 删除了数据表中所有单通道和四通道 PDIP 封装参考	1
• 更新了 *器件信息* 表	1
• Updated *Pin Configuration and Functions* format	3
• Changed OPA132 pin 1 and pin 8 from "Offset Trim" to "NC"	3
• Changed input voltage from (V–) – 0.7 and (V+) + 0.7 to (V–) – 0.5 and (V+) + 0.5 in *Absolute Maximum Ratings*	5
• Added input current and related footnote to *Absolute Maximum Ratings*	5
• Added *Thermal Information*	6
• Changed format of *Electrical Characteristics* to latest standard	7
• Updated nominal conditions in the header of *Electrical Characteristics*	7
• Added ± to power supply rejection ratio (offset vs temperature) and input bias current values	7
• Changed common-mode voltage MAX value from (V+) – 2.5V to (V+) – 3.5V	7
• Changed common-mode rejection ratio and common-mode input impedance test conditions from –12.5V ≤ V_{CM} ≤ 12.5V to –12.5V ≤ V_{CM} ≤ 11.5V	7
• Changed differential input impedance from $10^{10}\Omega$ || 2pF to $10^{10}\Omega$ || 10pF	7
• Changed common-mode input impedance from $10^{10}\Omega$ || 6pF to $10^{10}\Omega$ || 7pF	7
• Changed overload recovery time from 0.5µs to 600ns	7
• Changed overload recovery time test condition from G = ± to G = ±1 to fix typo	7
• Moved voltage output negative MIN values to MAX values	7
• Deleted redundant power supply and temperature range sections already covered in *Recommended Operating Conditions*	7
• Deleted note 1 from Electrical Characteristics	7
• Changed *Typical Characteristics* header test conditions to match *Electrical Characteristics*	9
• Changed Figure 16, *Small-Signal Overshoot vs Load Capacitance* into two plots, Figure 5-16 for G = +1 and Figure 5-17 for G = –1	9
• Updated Figure 5-18, *Output Voltage Swing vs Output Current*	9
• Updated *Functional Block Diagram*	12
• Updated *Offset Voltage Trim*	13
• Updated Figure 7-3, *OPA132 Layout Example for the Noninverting Configuration*	16

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Changes from Revision A (June 2004) to Revision B (September 2015) **Page**

- 添加了 *ESD 等级*、*特性说明*、*器件功能模式*、*应用和实施*、*电源相关建议*、*布局*、*器件和文档支持* 以及 *机械、封装和可订购信息* 部分 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA132U	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U
OPA132U.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U
OPA132U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U
OPA132U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U
OPA132UA	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U A
OPA132UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U A
OPA132UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U A
OPA132UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 132U A
OPA2132P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 125	OPA2132P
OPA2132P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 125	OPA2132P
OPA2132PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 125	OPA2132P A
OPA2132PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 125	OPA2132P A
OPA2132PAG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 125	OPA2132P A
OPA2132U	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	(O2132U, OPA) 2132U
OPA2132U.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	(O2132U, OPA) 2132U
OPA2132U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	(O2132U, OPA) 2132U

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2132U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	(O2132U, OPA) 2132U
OPA2132UA	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	(O2132UA, OPA) 2132U A
OPA2132UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Level-3-260C-168 HR	-40 to 125	(O2132UA, OPA) 2132U A
OPA2132UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O2132UA, OPA) 2132U A
OPA2132UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O2132UA, OPA) 2132U A
OPA4132UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA
OPA4132UA.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA
OPA4132UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA
OPA4132UA/2K5.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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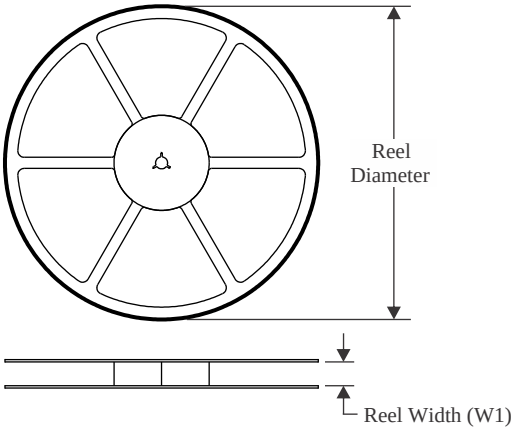
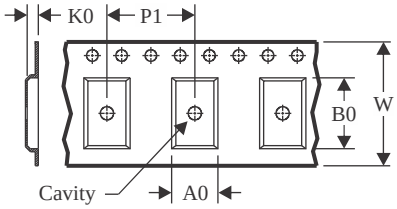
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

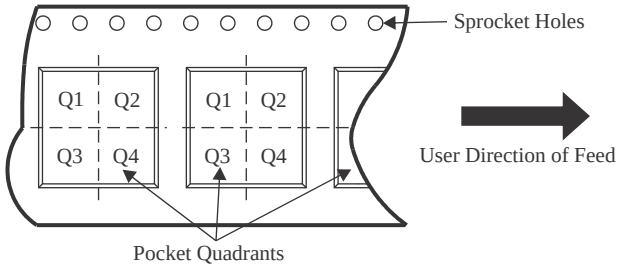


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

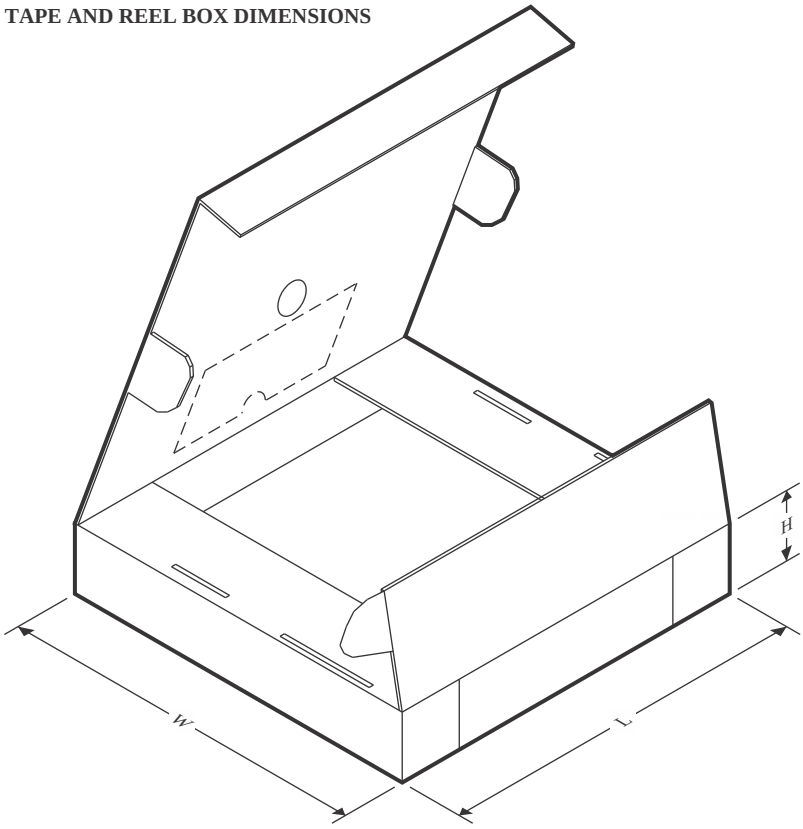
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4132UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

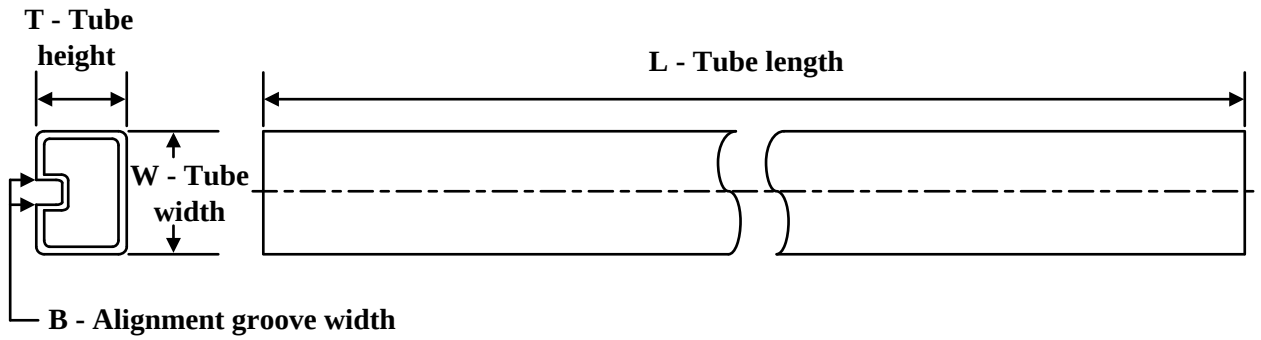
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA132U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA132UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2132U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2132UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4132UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

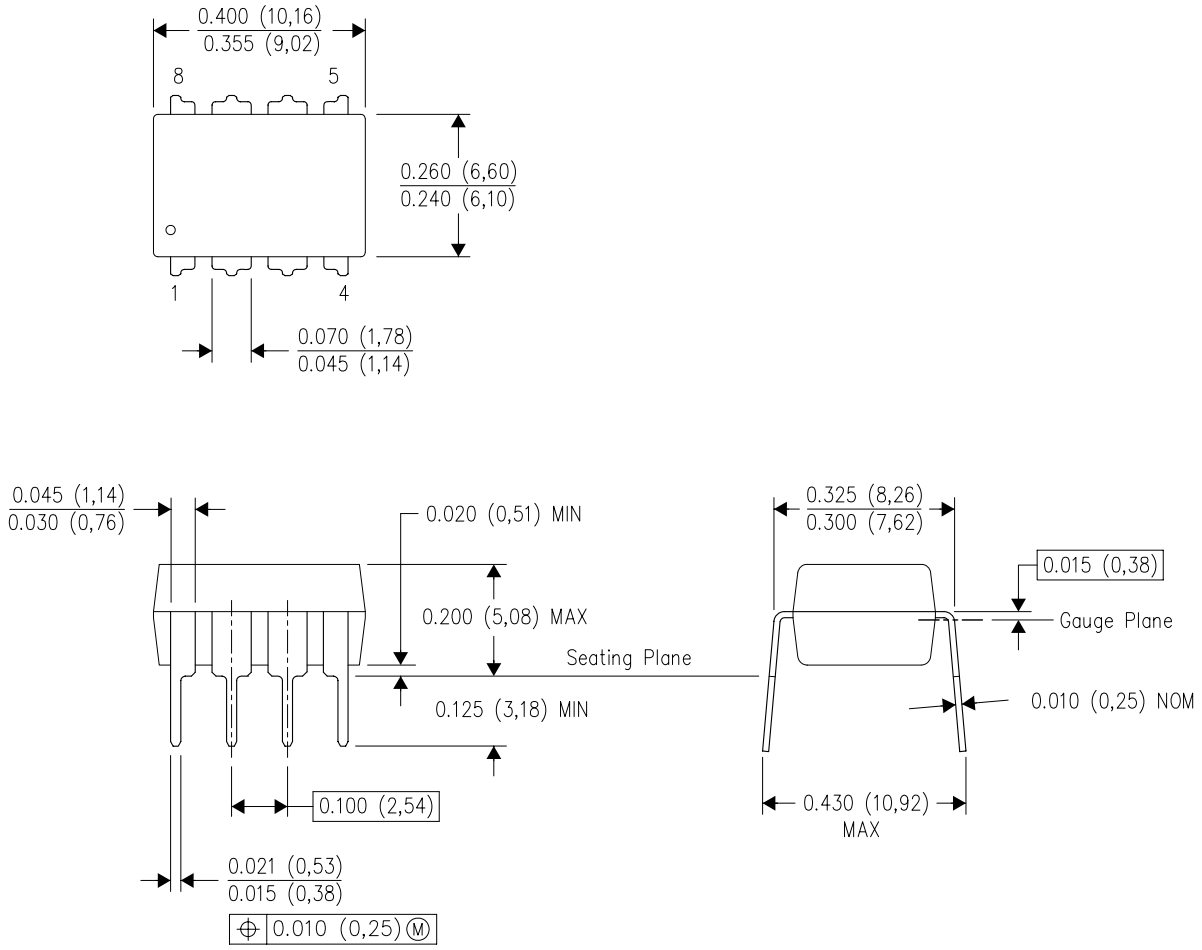
TUBE



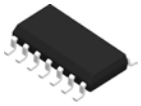
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA132U	D	SOIC	8	75	506.6	8	3940	4.32
OPA132U.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA132UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA132UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2132P	P	PDIP	8	50	506	13.97	11230	4.32
OPA2132P.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA2132PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2132PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA2132PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2132U	D	SOIC	8	75	506.6	8	3940	4.32
OPA2132U.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2132UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2132UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4132UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4132UA.B	D	SOIC	14	50	506.6	8	3940	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

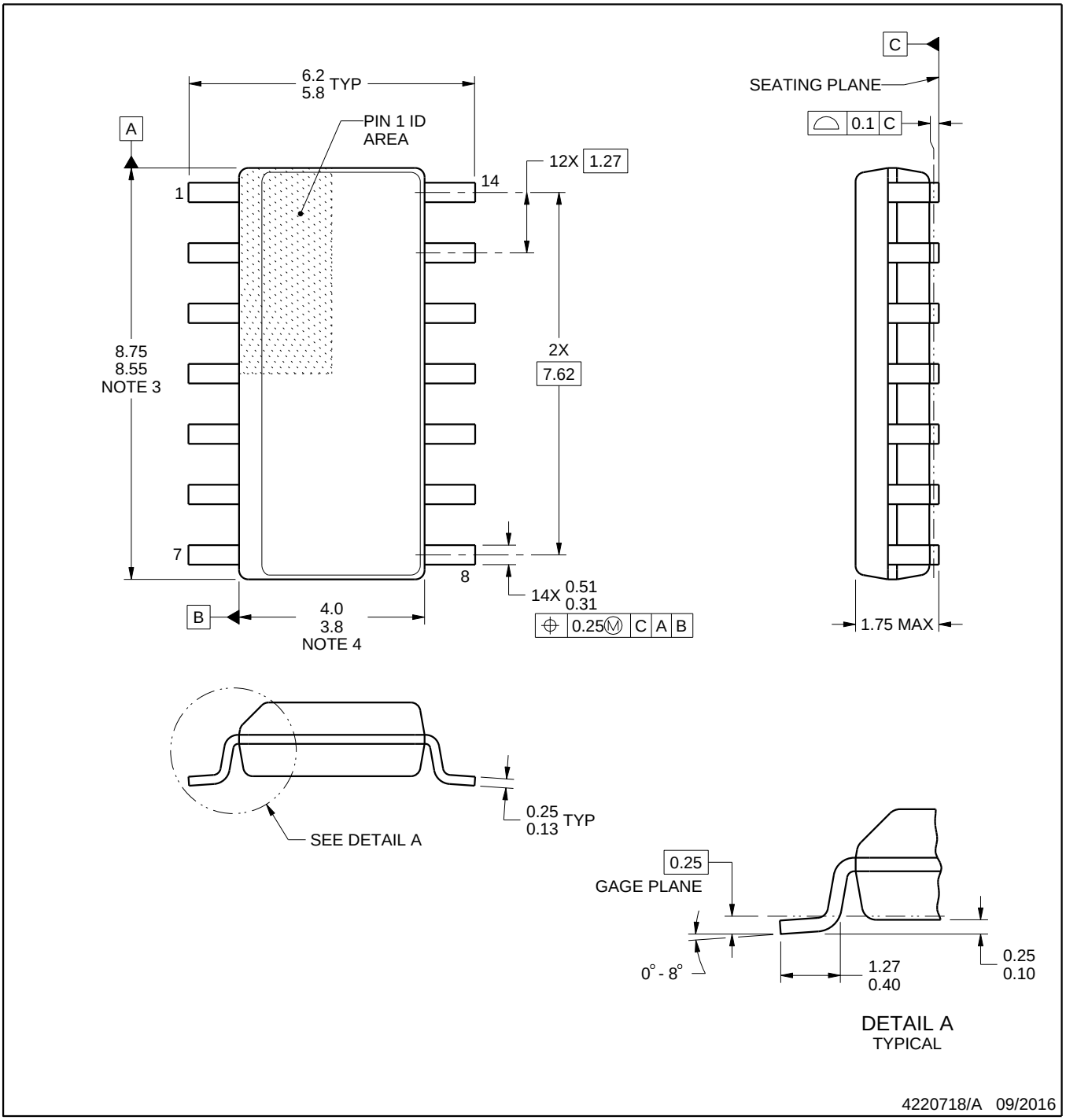


PACKAGE OUTLINE

D0014A

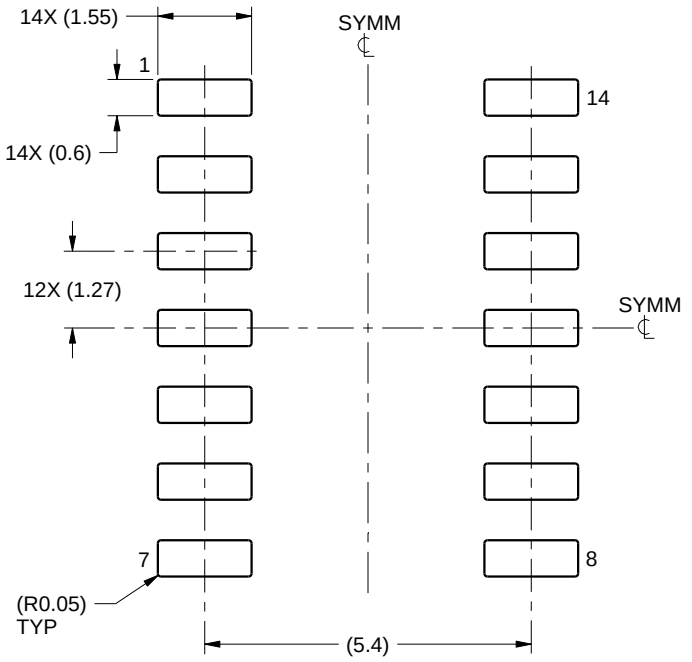
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

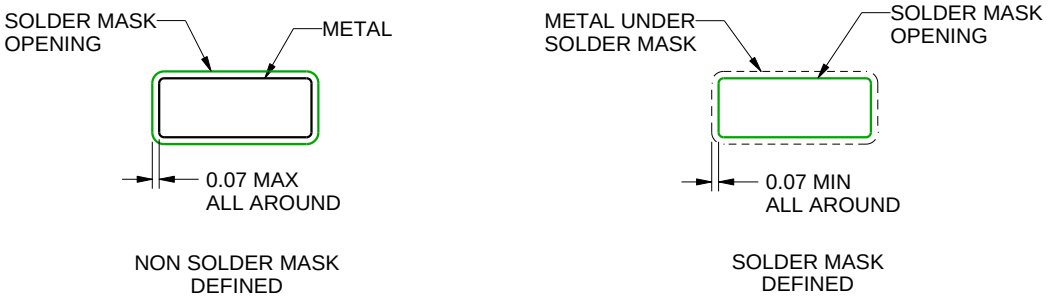


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

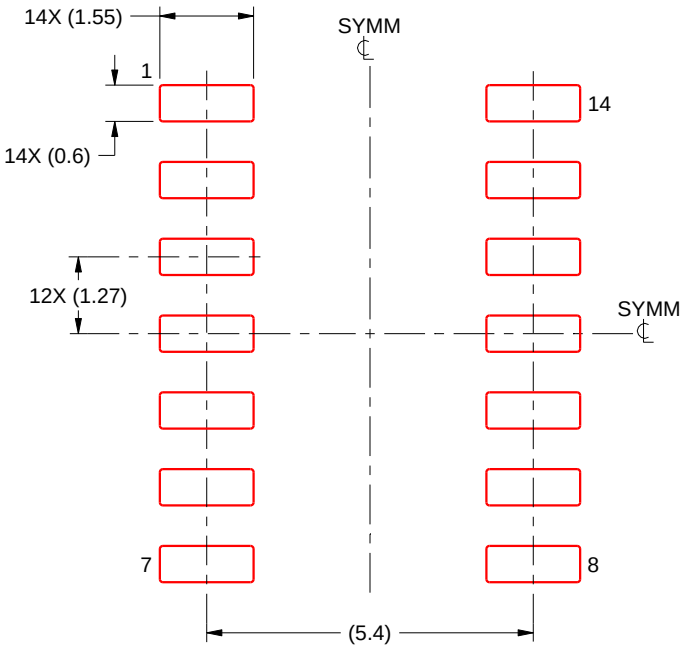
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

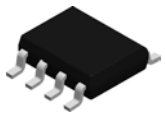


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

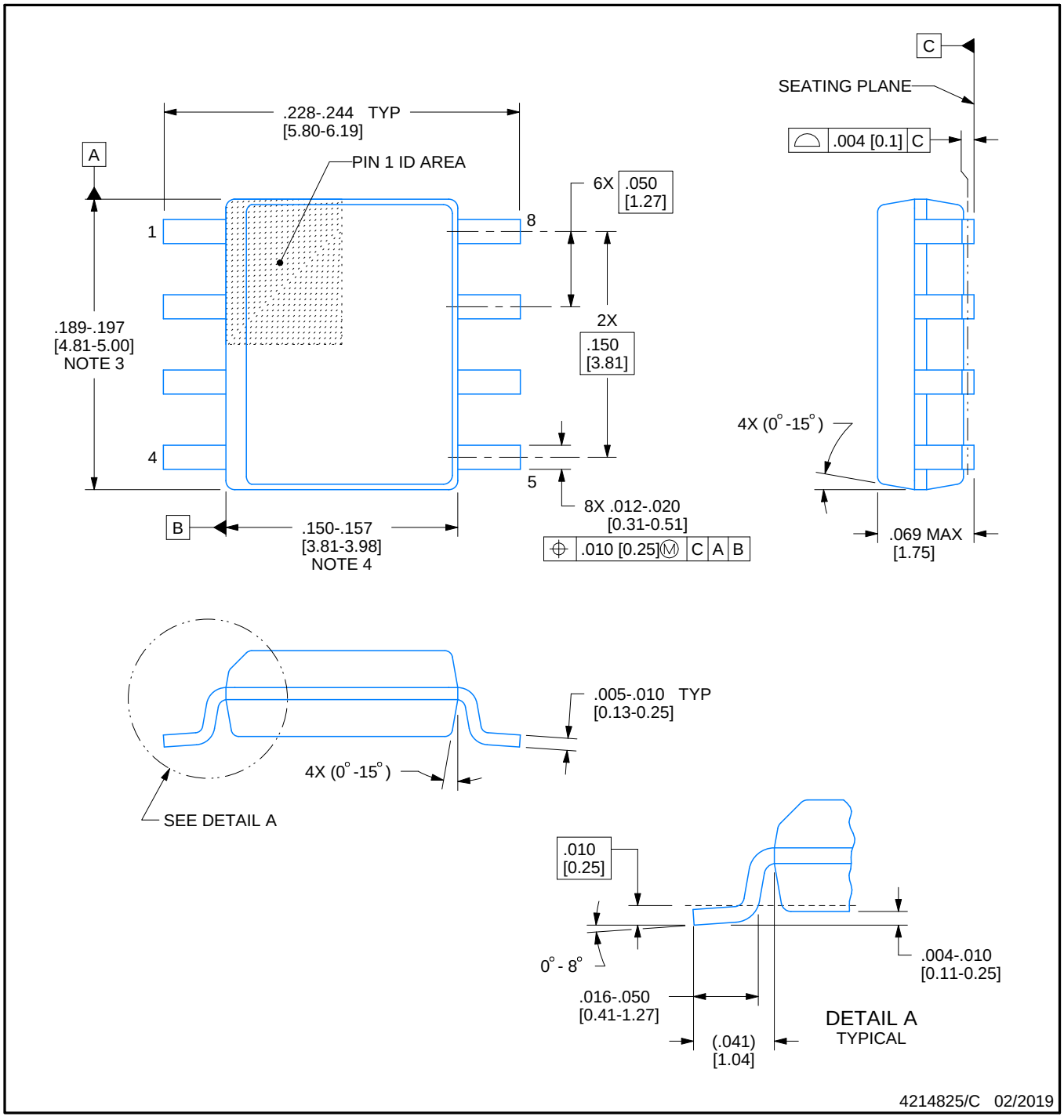


PACKAGE OUTLINE

D0008A

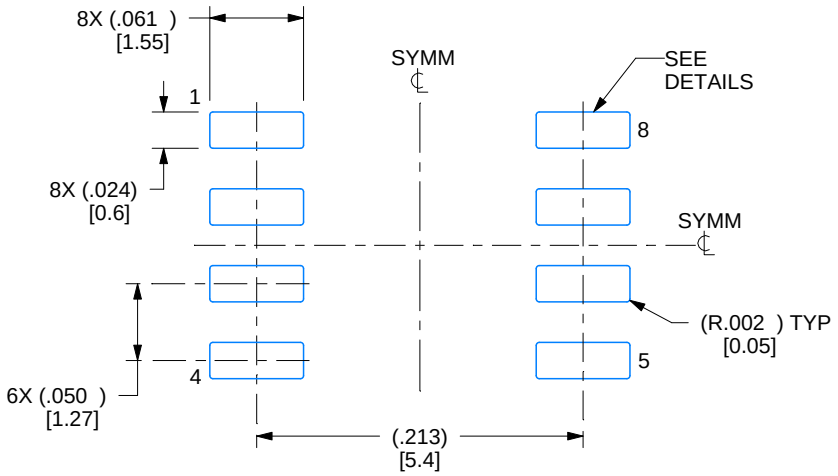
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

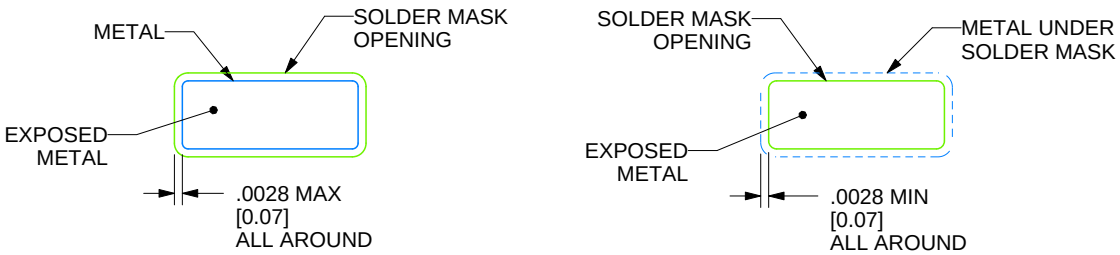


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

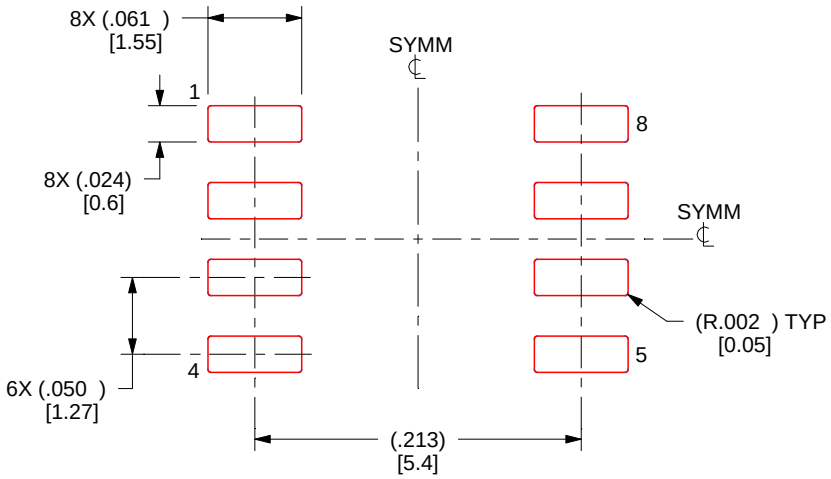
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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