# OPA857 超低噪声、宽带、可选反馈电阻互阻抗放大器

## 1 特性

- 内部中级基准电压
- 伪差分输出电压
- 宽动态范围
- 闭环互阻抗带宽：
  - 125MHz（5kΩ 互阻抗增益，1.5pF 外部寄生电容）
  - 105MHz（20kΩ 互阻抗增益，1.5pF 外部寄生电容）
- 超低输入引入电流噪声（Brickwall 滤波器带宽 = 135MHz）：15nA$_{RMS}$（20kΩ 互阻抗）
- 超短过载恢复时间：< 25ns
- 内部输入保护二极管
- 电源：
  - 电压：2.7V 至 3.6V
  - 电流：23.4mA
- 扩展级温度范围：-40°C 至 +85°C

## 2 应用

- 光电二极管监控
- 高速 I/V 转换
- 光学放大器
- 计算机轴向断层 (CAT) 扫描仪前端

## 3 说明

OPA857 是一款针对光电二极管监控应用的宽频带、快速过驱恢复、快速稳定、超低噪声互感抗 放大器。借助于可选反馈电阻，OPA857 简化了高性能光系统的设计。极快速过载恢复时间和内部输入保护提供了最佳组合，以便在最大限度地减少恢复时间的同时，保护信号链的剩余部分。两个可选的互阻抗增益配置可实现当代互阻抗放大器应用所需要的高动态范围和 灵活性。OPA857 采用 3mm × 3mm 超薄型四方扁平无引线 (VQFN) 封装。

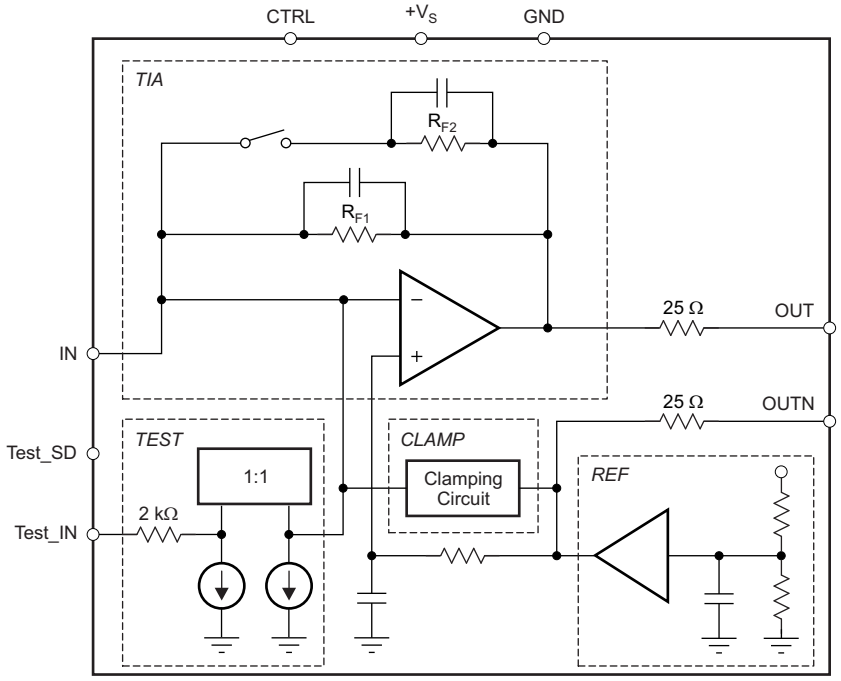
此器件可在 -40°C 至 +85°C 的整个工业级温度范围内额定运行。

器件信息(1)

| 器件名称 | 封装 | 封装尺寸 |
|---|---|---|
| OPA857 | VQFN (16) | 3mm x 3mm |

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。

功能方框图



# 目录



## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision C (April 2014) to Revision D** **Page**

- 已更改 特性 要点 ... 1
- 已将第二个应用要点中的“精密” 更改为 “高速” ... 1
- Changed pin configuration drawing and pin functions table ... 4
- Changed Handling Ratings table to ESD Ratings and moved storage temperature to Absolute Maximum Ratings ... 5
- Changed *Supply Input Voltage* min value from 3.0 to 2.7 in Recommended Operating Conditions ... 5
- Changed VOUT unit from $V_P$ to $V_{PP}$ in Electrical Charateristics condition line ... 6
- Changed all *AC Performance* values except *Closed-Loop Output Impedance* ... 6
- Changed test conditions for *Equivalent Input-Referred Current Noise* parameter in Electrical Characteristics ... 6
- Deleted *Operating Voltage* from Electrical Characteristics; already in Recommended Operating Conditions ... 7
- Deleted *Temperature Range* from Electrical Characteristics; already in Recommended Operating Conditions ... 7
- Changed all plots in Typical Characteristics section except figures 17, 35, and 36 ... 8
- Changed 4.5 kΩ and 18.2 kΩ to 5 kΩ and 20 kΩ, respectively, in first paragrpah of *Overview* section ... 14
- Changed text in *Transimpedance Amplifier (TIA) Block* section ... 15
- Changed text in *Reference Voltage (REF) Block* section ... 15
- Changed text in *Integrated Test Structure (TEST) Block* section ... 15
- Changed Table 2 values ... 17
- Added *Test Mode* section ... 17
- Changed *Application Information* section ... 18
- Changed Figure 50; updated pin names ... 24

**Changes from Revision B (January 2014) to Revision C** **Page**

- 更改了文档格式以满足新的数据表标准；增加了*处理额定值*和*器件和文档支持*部分，移动现有部分 ... 1
- Changed OUTN to OUT in *Output Voltage Swing* parameter test conditions ... 6
- Changed Functional Block Diagram ... 14

**Changes from Revision A (December 2013) to Revision B** **Page**

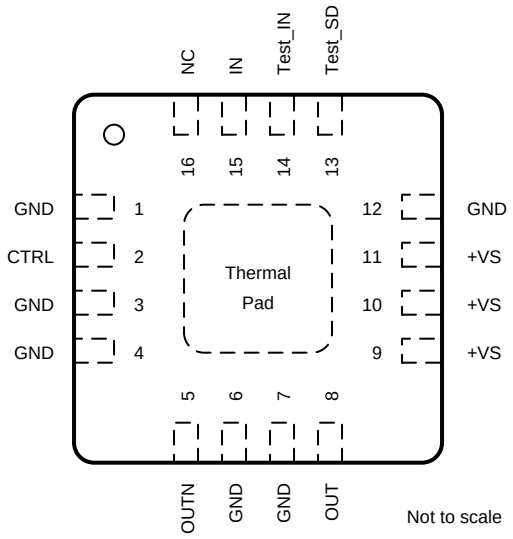
- 文档状态更改为生产数据 ..... 1
- 已更改*带宽*特性要点的两个分项的 互阻抗 值 ..... 1
- 已将*扩展级温度范围* 特性 要点更改为：-40°C 至 +85°C ..... 1
- 已将*说明*部分最后一句中的温度范围更改为“-40°C 至 +85°C” ..... 1
- 已更改首页图 ..... 1
- Added pages 2 through end of document ..... 4

**Changes from Original (December 2013) to Revision A** **Page**

- 文档状态更改为产品预览 ..... 1
- 删除第 1 页后的全部页面 ..... 1
- 已删除第四个 应用 要点 ..... 1
- 已更改*说明*部分的第一句话：已添加“针对光电二极管监控 应用” ..... 1
- 已更改*说明*部分的第一句话 ..... 1

# 5 Pin Configuration and Functions

**RGT Package**
**16-Pin VQFN**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CTRL | 2 | I | Control pin for transimpedance gain.<br>GND, logic 0 = 5-kΩ internal resistance; $+V_S$, logic 1 = 20-kΩ internal resistance. |
| GND | 1, 3, 4, 6, 7, 12 | I | Ground |
| IN | 15 | I | Input |
| NC | 16 | — | Not connected |
| OUT | 8 | O | Signal output |
| OUTN | 5 | O | Common-mode voltage output reference |
| Test_IN | 14 | I | Test mode input. Connect to $+V_S$ during normal operation. |
| Test_SD | 13 | I | Test mode enable. Connect to GND for normal operation, and connect to $+V_S$ to enable test mode. |
| $+V_S$ | 9, 10, 11 | I | Supply voltage |

# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply voltage, $V_{S–}$ to $V_{S+}$ | | 3.8 | V |
| | Input and output voltage, $V_{IN}$, $V_{OUT}$ pins | ($V_{S–}$) – 0.7 | ($V_{S+}$) + 0.7 | |
| | Differential input voltage | | 1 | |
| Current | Output current | | 50 | mA |
| | Input current, $V_{IN}$ pin | | 10 | |
| Continuous power dissipation | | See Thermal Information table | | |
| Temperature | Maximum junction, $T_J$ | | 150 | °C |
| | Maximum junction, $T_J$ (continuous operation, long-term reliability) | | 140 | |
| | Operating free-air, $T_A$ | –40 | 85 | |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{SS}$ | Supply input voltage | 2.7 | 3.3 | 3.6 | V |
| $T_J$ | Operating junction temperature | –40 | | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | OPA857 RGT (VQFN) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 67.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 91.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 41.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 41.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | 23.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

at $T_A$ = 25°C[1], $V_S$ = 3.3 V, $V_{S+}$ – $V_{S–}$ = 3.3 V, $C_{Source}$ = 1.5 pF, $V_{OUT}$ = 0.5 $V_{PP}$ (differential), $R_L$ = 500-Ω differential, single-ended input, pseudo-differential output, and input and output referenced to midsupply (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | TEST LEVEL[2] |
|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | | |
| | Small-signal bandwidth | CTRL = 1, $T_A$ = –40°C to +85°C | | 105 | | MHz | C |
| | | CTRL = 0, $T_A$ = –40°C to +85°C | | 125 | | MHz | C |
| SR | Slew rate (differential) | $V_{OUT}$ = 1-V step | | 215 | | V/µs | C |
| $t_S$ | Settling time to 1% | $V_{OUT}$ = 0.5-V step, CTRL = 0, $T_A$ = 25°C | | 8 | | ns | B |
| | | $V_{OUT}$ = 0.5-V step, CTRL = 1, $T_A$ = 25°C | | 8 | | ns | B |
| | Settling time to 0.001% | $V_{OUT}$ = 0.5-V step, CTRL = 0 | | 600 | | ns | C |
| | | $V_{OUT}$ = 0.5-V step, CTRL = 1 | | 700 | | ns | C |
| HD2 | Second-harmonic distortion | $V_{OUT}$ = 0.5 $V_{PP}$, f = 10 MHz, $R_F$ = 5 kΩ, $T_A$ = 25°C | | –80 | | dBc | C |
| | | $V_{OUT}$ = 0.5 $V_{PP}$, f = 10 MHz, $R_F$ = 20 kΩ, $T_A$ = 25°C | | –83 | | dBc | C |
| HD3 | Third-harmonic distortion | $V_{OUT}$ = 0.5 $V_{PP}$, f = 10 MHz, $R_F$ = 5 kΩ, $T_A$ = 25°C | | –88 | | dBc | C |
| | | $V_{OUT}$ = 0.5 $V_{PP}$, f = 10 MHz, $R_F$ = 20 kΩ, $T_A$ = 25°C | | –83 | | dBc | C |
| | Equivalent input-referred current noise | CTRL = 0, using 135-MHz brickwall filter | | 25 | | $nA_{RMS}$ | C |
| | | CTRL = 1, using 135-MHz brickwall filter | | 15 | | $nA_{RMS}$ | C |
| | Overdrive recovery time | $I_{IN}$ = 2x overload, CTRL = 1, settling to 1% of final value | | 25 | | ns | B |
| | Closed-loop output impedance | f = 1 MHz (differential) | | 50 | | Ω | C |
| **DC PERFORMANCE** | | | | | | | |
| | Transimpedance gain | CTRL = 1 into 500 Ω[3][4] | | 18.2 | | kΩ | C |
| | | CTRL = 0 into 500 Ω[3][4] | | 4.5 | | kΩ | C |
| | Transimpedance gain error | $T_A$ = 25°C, $R_F$ = 20 kΩ and $R_F$ = 5 kΩ | | ±1% | ±15% | | A |
| $V_{OO}$ | Output offset voltage | $T_A$ = +25°C | | ±1 | ±5 | mV | A |
| | | $T_A$ = –40°C to +85°C[5] | | | ±6 | mV | B |
| | Output offset voltage drift | $T_A$ = –40°C to +85°C[5] | | | ±15 | µV/°C | C |
| $V_{ICR}$ | Common-mode voltage range | $T_A$ = 25°C, OUTN | 1.78 | 1.83 | 1.88 | V | A |
| **INPUT** | | | | | | | |
| | Input pin capacitance | | | 2 | | pF | C |
| **OUTPUT** | | | | | | | |
| | Output voltage swing | OUT, $T_A$ = 25°C | 0.6 | | 1.9 | V | A |
| | | $T_A$ = –40°C to +85°C[5] | | | 1.9 | V | B |
| | Output current drive (for linear operation) | OUT, differential 50-Ω between OUT and OUTN | | +5 | | mA | C |
| | | | | –20 | | mA | C |

(1) Junction temperature = ambient for 70°C specifications.
(2) Test levels: **(A)** 100% tested at 25°C. Overtemperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(3) See the *Application and Implementation* section for details on loading and effective transimpedance gain.
(4) Note that the effective transimpedance gain is reduced to 18.2 kΩ and 4.5 kΩ, respectively, with a 500-Ω load resulting from the internal series resistance on OUT and OUTN.
(5) Junction temperature = ambient at low temperature; junction temperature = ambient + 3.5°C for overtemperature specifications.

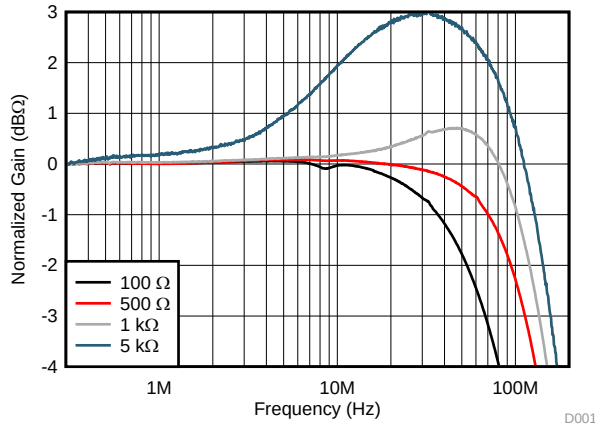
## Electrical Characteristics (接下页)

at $T_A$ = 25°C[1], $V_S$ = 3.3 V, $V_{S+} – V_{S–}$ = 3.3 V, $C_{Source}$ = 1.5 pF, $V_{OUT}$ = 0.5 $V_{PP}$ (differential), $R_L$ = 500-Ω differential, single-ended input, pseudo-differential output, and input and output referenced to midsupply (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | TEST LEVEL[2] |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| | Quiescent operating current | CTRL = 0, $T_A$ = 25°C | 20.5 | 23.4 | 26.3 | mA | A |
| | | CTRL = 0, $T_A$ = –40°C to +85°C[5] | 20.0 | | 26.8 | mA | B |
| | | CTRL = 1, $T_A$ = 25°C | 20.5 | 23.4 | 26.3 | mA | A |
| | | CTRL = 1, $T_A$ = –40°C to +85°C[5] | 20.0 | | 26.8 | mA | B |
| PSRR | Power-supply rejection ratio | At dc, $T_A$ = 25°C | 70 | 80 | | dB | A |
| | | f = 10 MHz, $T_A$ = –40°C to +85°C[5] | 15 | 18 | | dB | B |
| **LOGIC LEVEL (CTRL)** | | | | | | | |
| $V_{IH}$ | High-level input voltage | | 2 | | | V | A |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V | A |
| | High-level control pin input bias current | | | | 1 | µA | A |
| | Low-level control pin input bias current | | | | 1 | µA | A |

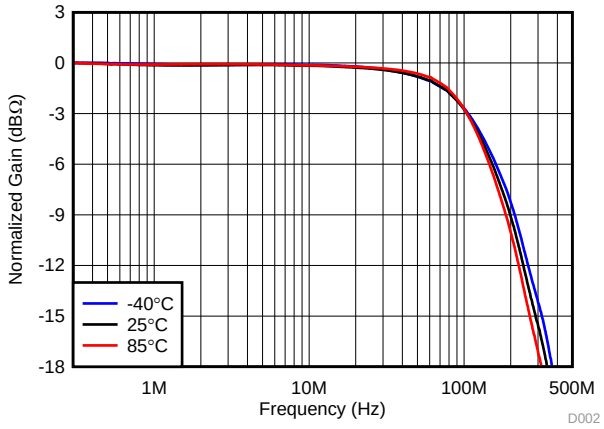
## 6.6 Typical Characteristics

At $T_A$ = 25°C, $C_S$ = 1.5 pF, and $R_L$ = 500-Ω differential between OUT and OUTN (unless otherwise noted).



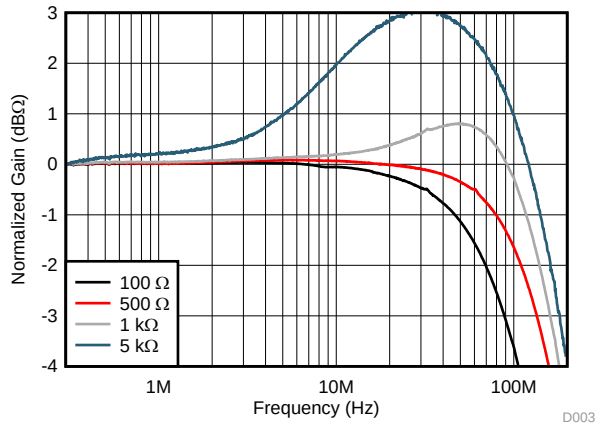

$T_Z$ Gain = 20 kΩ

**图 1. Frequency Response vs Load Resistance**



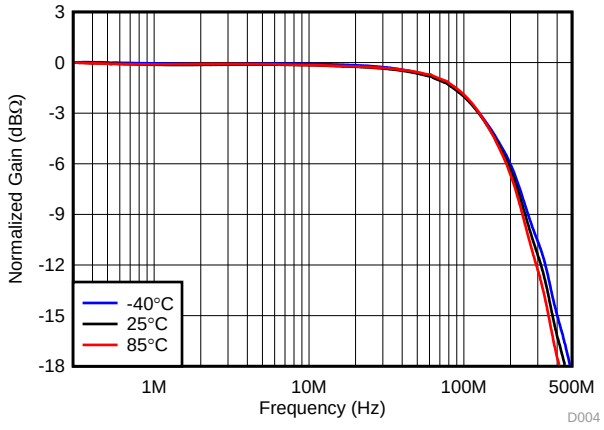

$T_Z$ Gain = 20 kΩ

**图 2. Frequency Response vs Temperature**



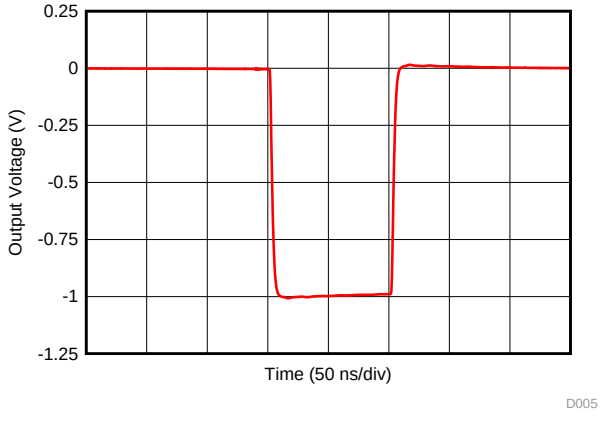

$T_Z$ Gain = 5 kΩ

**图 3. Frequency Response vs Load Resistance**



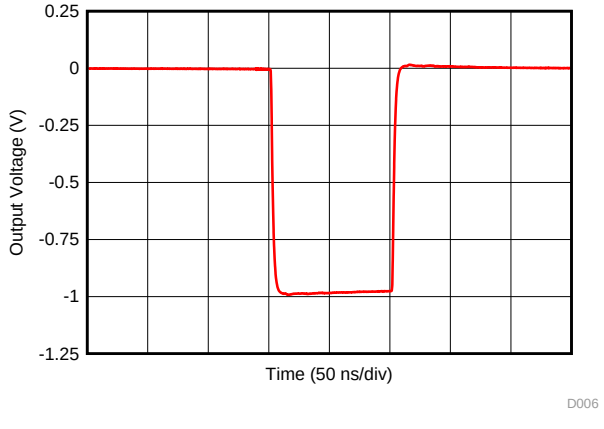

$T_Z$ Gain = 5 kΩ

**图 4. Frequency Response vs Temperature**




$T_Z$ Gain = 20 kΩ

**图 5. 1-$V_{PP}$ Pulse Response**




$T_Z$ Gain = 5 kΩ

**图 6. 1-$V_{PP}$ Pulse Response**

## Typical Characteristics (接下页)

At $T_A$ = 25°C, $C_S$ = 1.5 pF, and $R_L$ = 500-Ω differential between OUT and OUTN (unless otherwise noted).

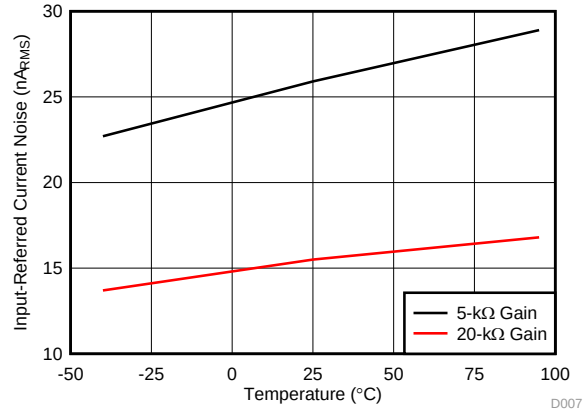



**图 7. RMS Input-Referred Current Noise vs Temperature**

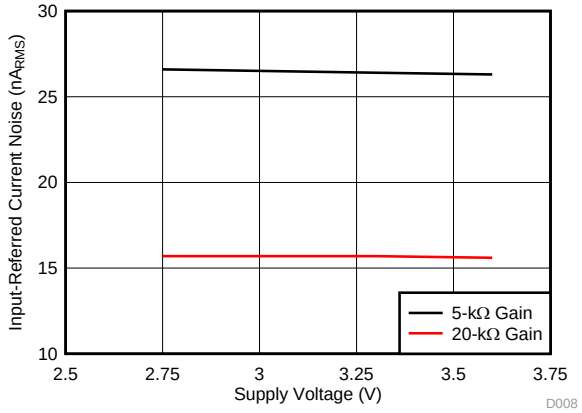



**图 8. RMS Input-Referred Current Noise vs Supply Voltage**

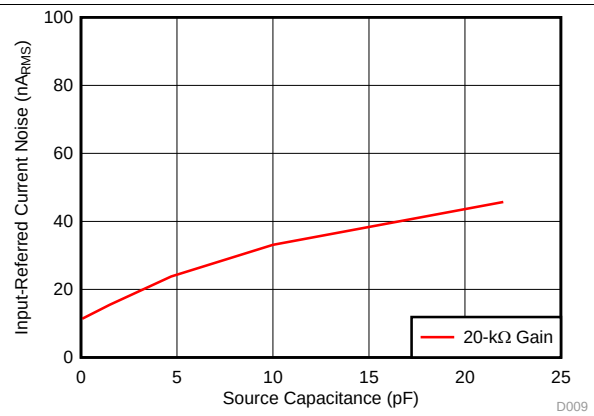



**图 9. RMS Input-Referred Current Noise vs Capacitance**

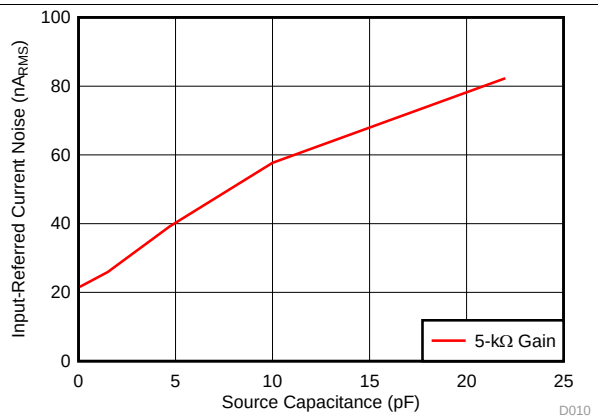
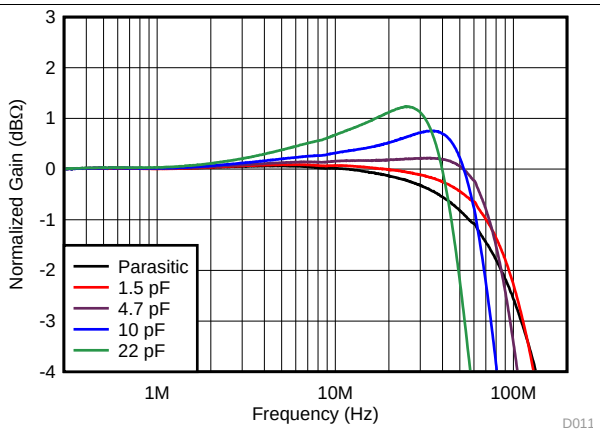
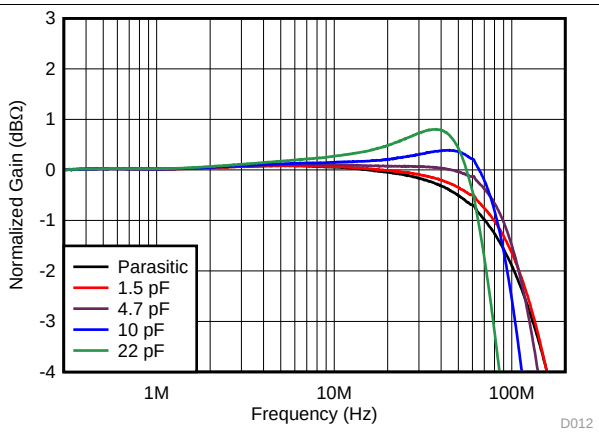



**图 10. Gain RMS Input-Referred Current Noise vs Input Capacitance**




$T_Z$ Gain = 20 kΩ

**图 11. Gain Frequency Response vs Input Capacitance**

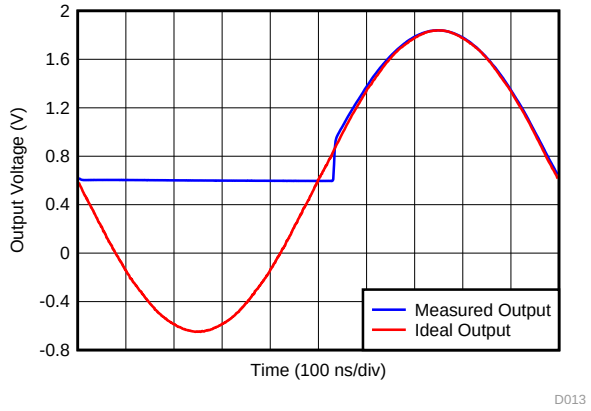



$T_Z$ Gain = 5 kΩ

**图 12. Gain Frequency Response vs Input Capacitance**

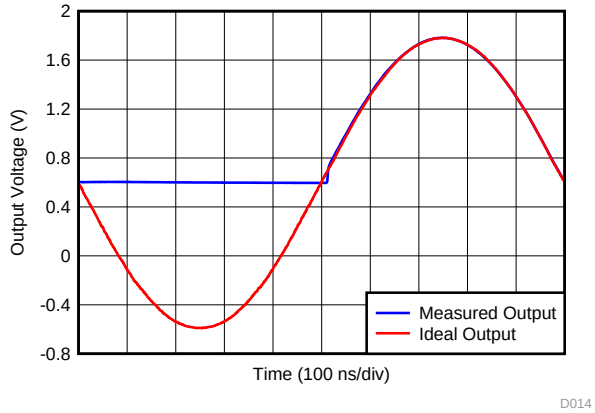
## Typical Characteristics (接下页)

At $T_A$ = 25°C, $C_S$ = 1.5 pF, and $R_L$ = 500-Ω differential between OUT and OUTN (unless otherwise noted).



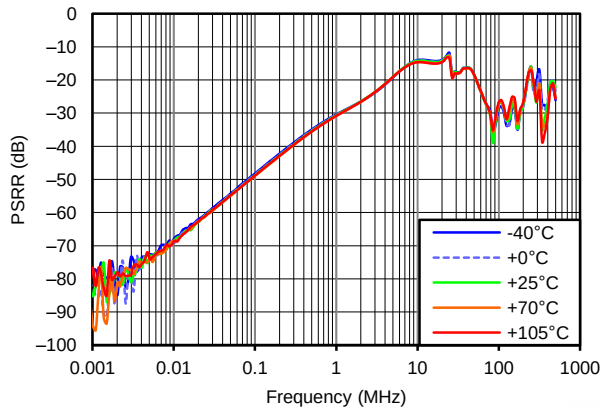

$T_Z$ Gain = 20 kΩ

**图 13. 2x Overdrive Recovery**



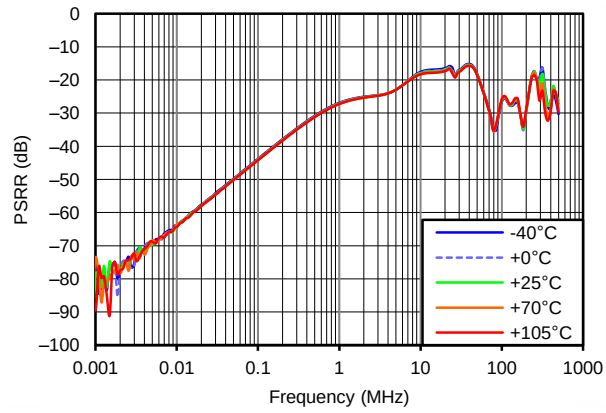

$T_Z$ Gain = 5 kΩ

**图 14. 2x Overdrive Recovery**




$T_Z$ Gain = 20-kΩ

**图 15. Power-Supply Rejection Ratio vs Frequency**




$T_Z$ Gain = 5 kΩ

**图 16. Power-Supply Rejection Ratio vs Frequency**

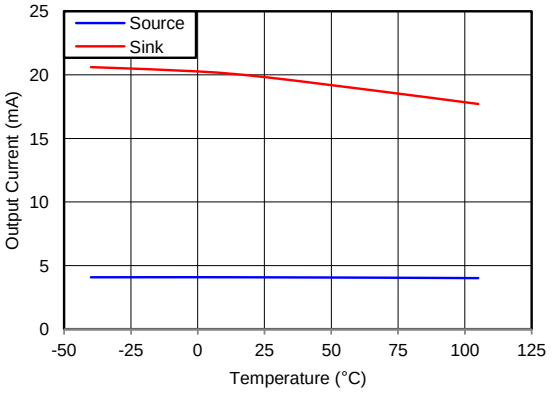
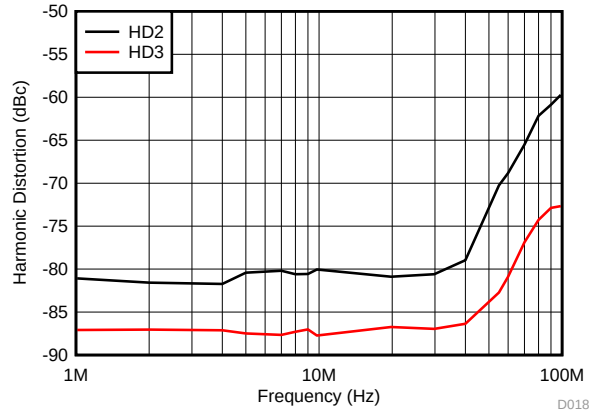



**图 17. Output Current vs Temperature**

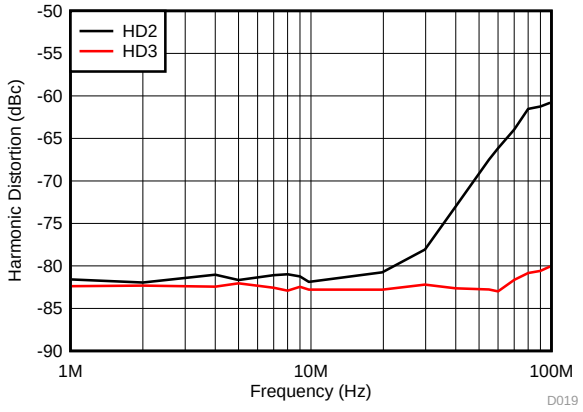



$T_Z$ Gain = 5 kΩ, $R_{LOAD}$ = 500 Ω

**图 18. Harmonic Distortion vs Frequency**

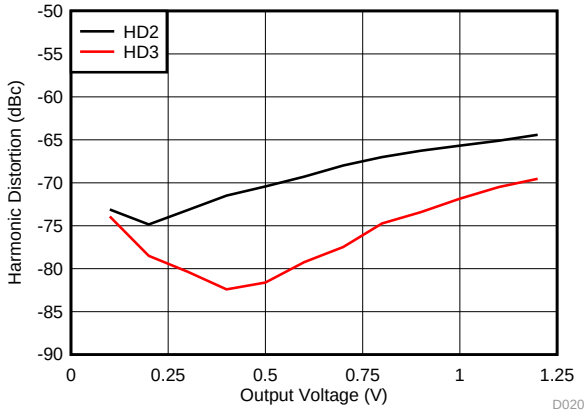
## Typical Characteristics (接下页)

At $T_A$ = 25°C, $C_S$ = 1.5 pF, and $R_L$ = 500-Ω differential between OUT and OUTN (unless otherwise noted).



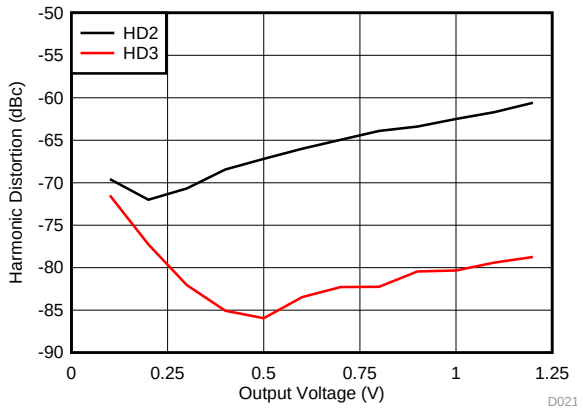

$T_Z$ Gain = 20 kΩ, $R_{LOAD}$ = 500 Ω

**图 19. Harmonic Distortion vs Frequency**



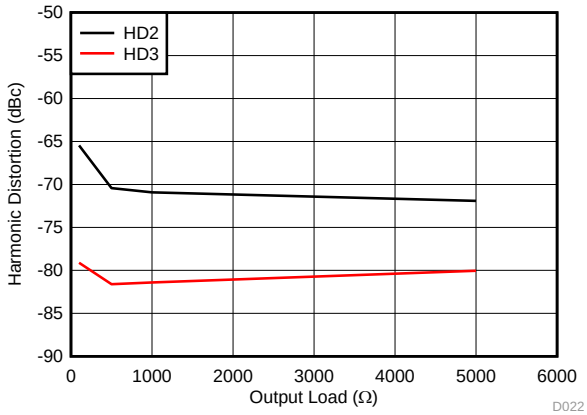

$T_Z$ Gain = 5 kΩ, $R_{LOAD}$ = 500 Ω, f = 50 MHz

**图 20. Harmonic Distortion vs Output Voltage**



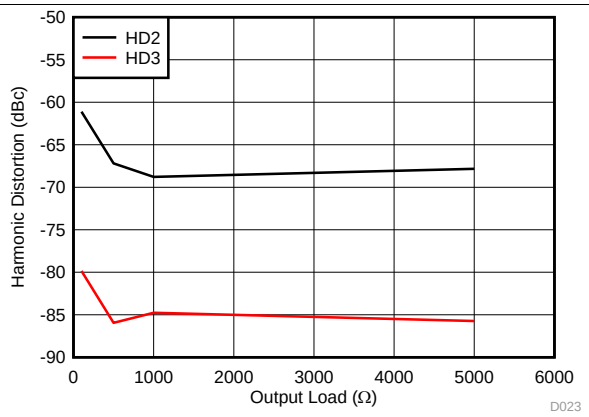

$T_Z$ Gain = 20 kΩ, $R_{LOAD}$ = 500 Ω, f = 50 MHz

**图 21. Harmonic Distortion vs Output Voltage**



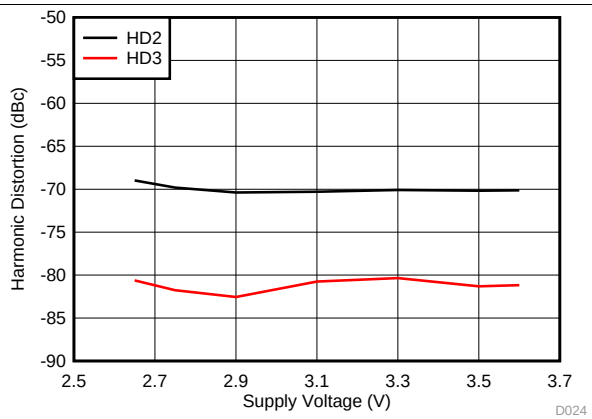

$T_Z$ Gain = 5 kΩ, f = 50 MHz

**图 22. Harmonic Distortion vs $R_{LOAD}$**




$T_Z$ Gain = 20 kΩ, f = 50 MHz

**图 23. Harmonic Distortion vs $R_{LOAD}$**

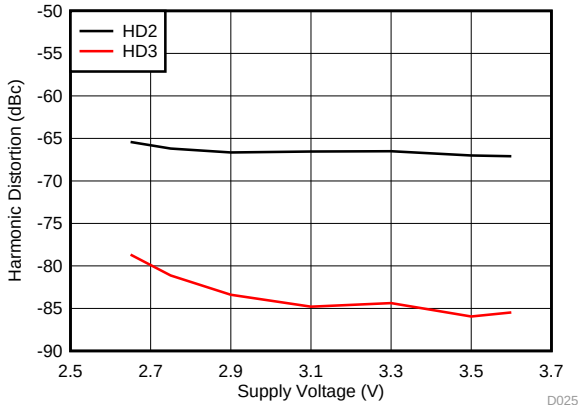



$T_Z$ Gain = 5 kΩ, $T_A$ = 25°C, $R_{LOAD}$ = 500 Ω, f = 50 MHz

**图 24. Harmonic Distortion vs Supply Voltage**

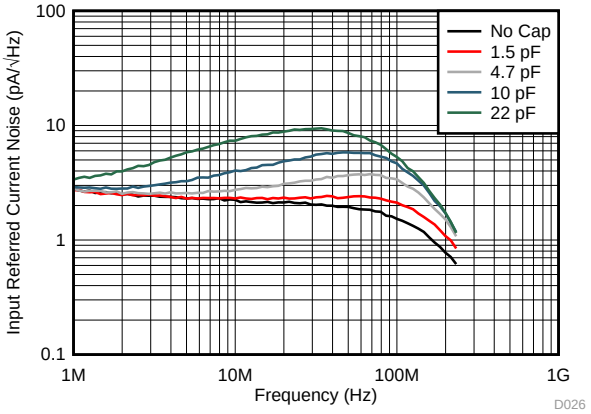
## Typical Characteristics (接下页)

At $T_A$ = 25°C, $C_S$ = 1.5 pF, and $R_L$ = 500-Ω differential between OUT and OUTN (unless otherwise noted).



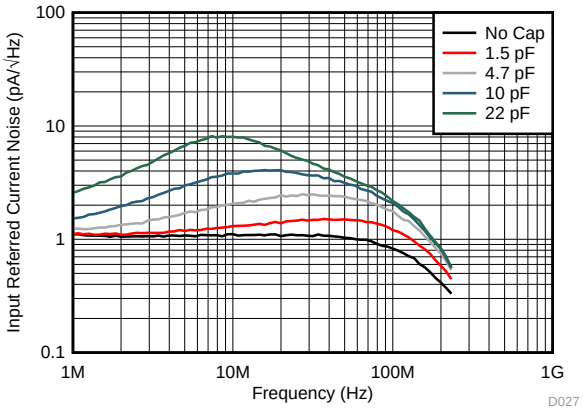

$T_Z$ Gain = 20 kΩ, $T_A$ = 25°C, $R_{LOAD}$ = 500 Ω, f = 50 MHz

**图 25. Harmonic Distortion vs Supply Voltage**



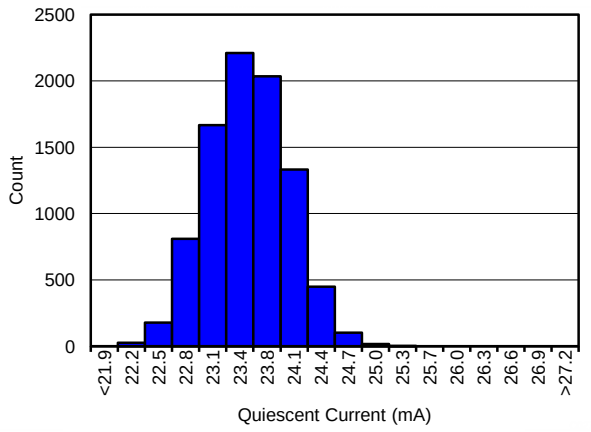

$T_Z$ Gain = 5 kΩ

**图 26. Input-Referred Current Noise Density vs Frequency**



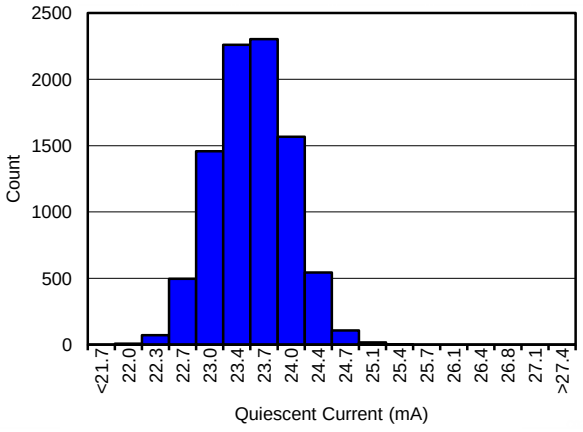

$T_Z$ Gain = 20 kΩ

**图 27. Input-Referred Current Noise Density vs Frequency**




$T_Z$ Gain = 20 kΩ

**图 28. $I_Q$ Histogram**




$T_Z$ Gain = 5 kΩ

**图 29. $I_Q$ Histogram**

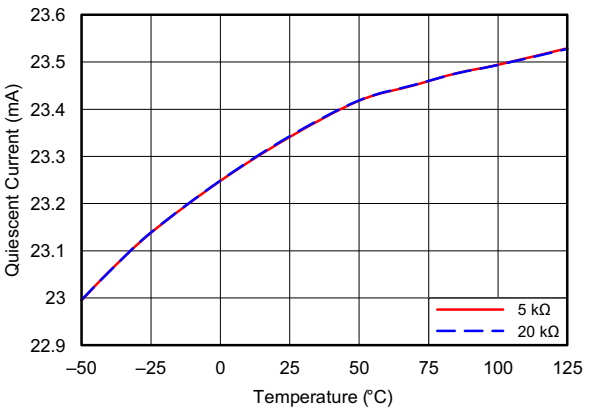



**图 30. Quiescent Current vs Temperature**

## Typical Characteristics (接下页)

At $T_A$ = 25°C, $C_S$ = 1.5 pF, and $R_L$ = 500-Ω differential between OUT and OUTN (unless otherwise noted).

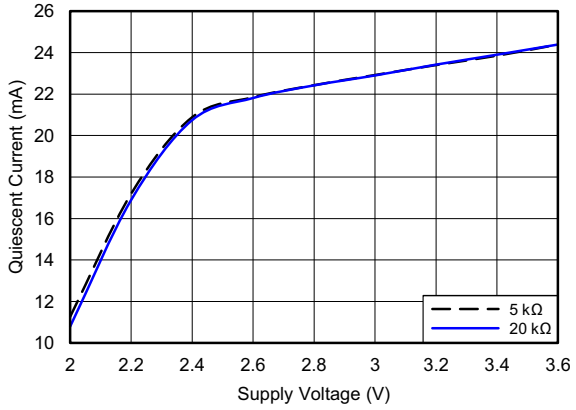
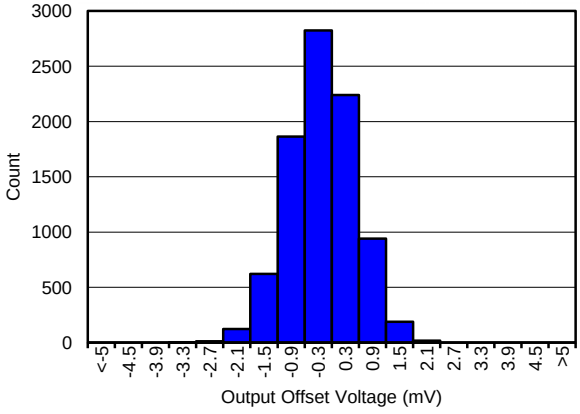
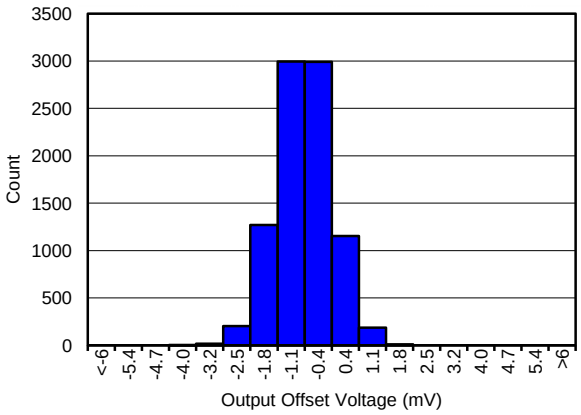



**图 31. Quiescent Current vs Supply Voltage**




$T_Z$ Gain = 5 kΩ

**图 32. Differential $V_{OSO}$ Histogram**




$T_Z$ Gain = 20 kΩ

**图 33. Differential $V_{OSO}$ Histogram**

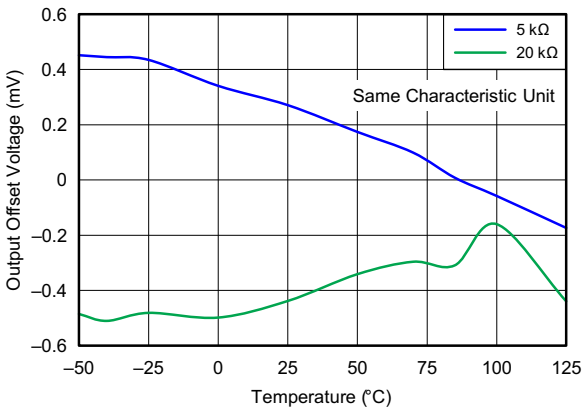



**图 34. Output Offset Voltage vs Temperature**

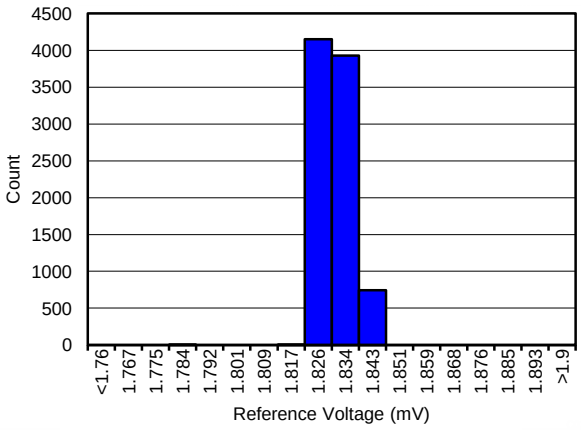



**图 35. Reference Voltage ($V_{OUTN}$) Distribution Histogram**

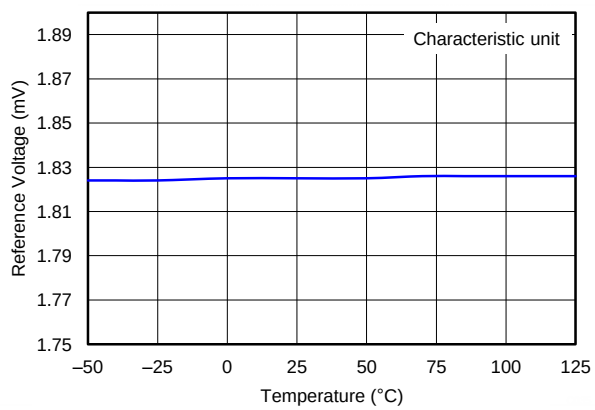



**图 36. Reference Voltage ($V_{OUTN}$) vs Temperature**

# 7 Detailed Description

## 7.1 Overview

The OPA857 provides a unique combination of low-noise, high-bandwidth, and high-transimpedance gain. The amplifier is optimized to achieve greater than 100-MHz bandwidth on either the 5-kΩ or 20-kΩ transimpedance gain for the lowest possible RMS noise on the output for a targeted low input capacitance of 1.5 pF. Note that this 1.5-pF capacitance includes the board parasitic; thus, great attention must be placed on minimizing stray capacitance in the layout. This value is selected because the device is expected to be driven by a photodiode with biasing high enough to include the photodiode capacitance contribution between approximately 0.5 pF and 0.7 pF, leaving between 0.8 pF to 1 pF for the external parasitic.

The OPA857 is a dedicated transimpedance amplifier with a pseudo-differential output. A block diagram is provided in the Functional Block Diagram section.

There are four distinct blocks in this diagram: a transimpedance amplifier (TIA), a reference voltage (REF), a test structure (TEST), and an internal clamping circuit (CLAMP).

The TIA block of the Functional Block Diagram includes two selectable gain configurations: $R_{F1}$ and $R_{F2}$. For a 500-Ω load, including the GND alternatives resulting from the internal 25-Ω series resistor on each output, the resulting gain is 4.5 kΩ or 18.2 kΩ. The TIA block is designed to provide excellent bandwidth (> 100 MHz) in both gain configurations with the lowest possible RMS noise over the entire bandwidth. This level of performance is achieved by minimizing the noise gain peaking at higher frequencies. The noise gain peaking resulting from feedback and source capacitance is the main noise contributor in high-speed transimpedance amplifiers.

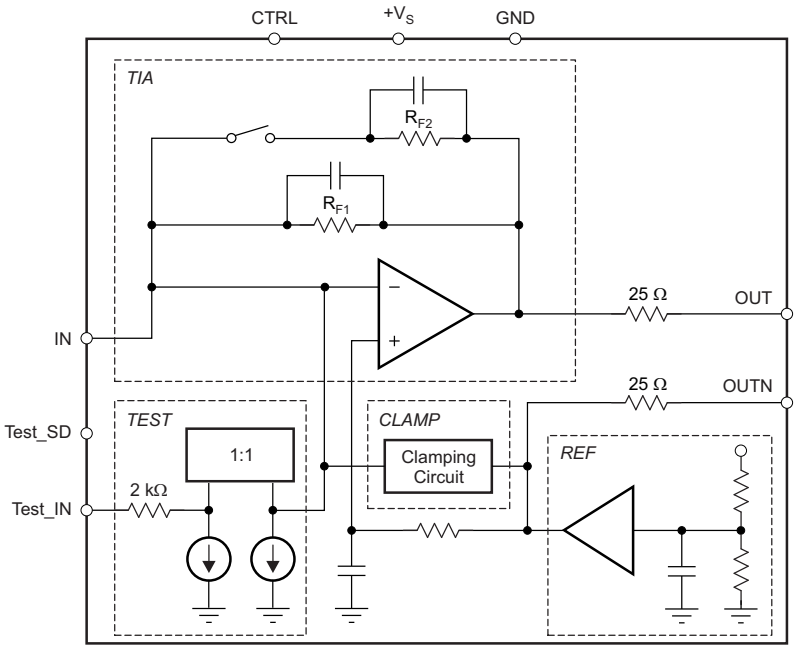
The reference voltage block of the Functional Block Diagram has several purposes: this block provides an adequate dc reference voltage to the input, and provides a dc reference at the output (thus allowing the dc-coupled solution to interface to a fully-differential signal chain). The CMRR provided by the fully-differential signal chain reduces any feedthrough from the OPA857 power supply, thereby increasing the PSRR of the amplifier.

The test structure block is available on the pinout, but the main purpose of this structure is to allow the device characterization to proceed as smoothly as possible.

The internal clamping circuit block and ESD diodes on the IN pin are used for internal protection and to make sure that the amplifier can recover quickly after saturation.

These blocks are each described in further detail in the *Feature Description* section.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Transimpedance Amplifier (TIA) Block

The amplifier of the TIA block has a class-A output stage, which limits its usable swing from the common-mode voltage of 1.83 V to the negative rail. Because the internal protection allows excellent overdrive recovery, the negative swing cannot go closer than 0.6 V to the rail. The resulting output dynamic range of the OPA857 on a 3.3-V supply is 1.2 V. This 1.2-V swing corresponds to a maximum input current of 60 µA in the high-gain configuration, and 240 µA in the low-gain configuration. A 25-Ω series resistor between the internal output of the TIA block and OUT (pin 8) limits the amplifier load during short-circuit conditions. A similar 25-Ω series resistor also exists between the output of the reference voltage amplifier and OUTN (pin 5). The internal resistors on OUT and OUTN reduce the overall gain of the OPA857. With a 500-Ω differential load, the attenuation resulting from the load is 0.83 dB, which affects the overall transimpedance gain. Because of the load attenuation, the 20-kΩ transimpedance gain is reduced to an effective 18.2 kΩ, while the 5-kΩ internal resistor gain is reduced to an effective 4.5-kΩ internal resistor.

### 7.3.2 Reference Voltage (REF) Block

The reference output voltage is set to be 5/9th of the power supply. Thus, for a single 3.3-V supply, the reference voltage is 1.83 V. A wideband amplifier with low output impedance to high frequencies is used in the reference voltage block. The amplifier output drives two paths: the first path drives the output (OUTN) through a 25-Ω series resistor, while the second path drives the noninverting input of the TIA block. The output from the second path is filtered through an RC filter in order to reduce the noise contribution from the reference block.

### 7.3.3 Integrated Test Structure (TEST) Block

In order to evaluate the low input capacitance condition on the input of the OPA857, simply evaluate the OPA857 performance without the photodiode. An integrated voltage-to-current conversion is implemented and can be accessed with the use of Test_SD (pin 13) and Test_IN (pin 14). This V-to-I converter structure is represented in 图 37. If required, a capacitor can be added to IN (pin 15) to match the target input capacitance during normal operation with an external photodiode. The test structure in 图 37 allows for the evaluation of the OPA857 as a TIA using standard lab equipment, such as function generators and network analyzers.

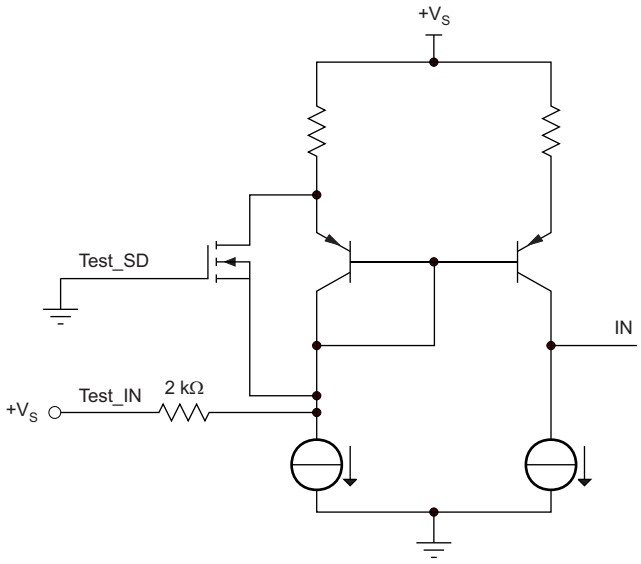



**图 37. Internal V-to-I Converter**

When using a photodiode, make sure that this source is turned off completely. This test structure is not intended to be used as a output dc-control voltage.

## Feature Description (接下页)

### 7.3.4 Internal Clamping Circuit (CLAMP) Block

The OPA857 is built using a very high-speed, complementary, BICMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings(1) table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in 图 38.

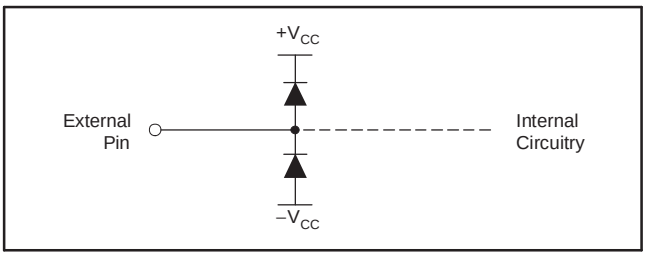



**图 38. Internal ESD Protection**

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Use additional external low-capacitance protection where higher currents are possible.

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Gain Control

The device transimpedance gain is controlled with the CTRL pin. Setting the CTRL pin high results in selecting the high-gain configuration. Setting the CTRL pin low results in selecting the low-gain configuration, as described in 表 1.

**表 1. Gain Control Logic Table**

| GAIN | CTRL (Pin 2) |
|---|---|
| 5 kΩ | Logic 0 (GND) |
| 20 kΩ | Logic 1 ($+V_S$) |

### 7.4.2 Test Mode

The OPA857 operates in normal mode when the input is driven by a photodiode. In test mode, the test structure described in the *Integrated Test Structure (TEST) Block* section is used to emulate a photodiode using a voltage input. 表 2 describes how to configure the OPA857 in each mode.

**表 2. Mode Configuration**

| MODE | Test_IN PIN CONNECTED TO | Test_SD PIN CONNECTED TO |
|---|---|---|
| Normal mode | $+V_S$ | GND |
| Test mode | AC-coupled input using a series cap or dc-coupled signal on a 2.1-V (approx) offset voltage | $+V_S$ |

Set an adequate dc voltage at the input to make sure that the output is operating within normal operation. At minimum, the output of the TIA block must be set to 5/9th of the supply voltage in preparation for a pulse configuration. For sine-wave operation, as required when measuring a frequency response, set the dc voltage on the OUT pin to allow the full sine-wave amplitude and avoid clipping. In such a case, the OUT pin voltage is set lower than 5/9th of the supply voltage.

Note that the 2-kΩ internal resistance used for the V-to-I conversion is not trimmed and can vary ±15% with process. Therefore, the source must be capable of sourcing both dc and ac voltages to make sure that the output voltage swing is compliant with the class-A output stage of the TIA block. Any change in the test circuit configuration (such as gain change) requires a new calibration of the internal V-to-I converter.

Again if a photodiode is used, the internal V-to-I converter must be shut off completely. Failure to do so results in degraded performance and higher than normal quiescent current.

# 8 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The OPA857 is a transimpedance amplifier offering two selectable gains. This device is used in conjunction with a photodiode at its input. The output is pseudo differential and may or may not require the use of a fully differential amplifier, depending on the analog-to-digital converter (ADC) used for implementation.

The OPA857 requires a photodiode to be connected to the positive bias voltage because the output voltage can only swing down from the reference voltage (1.85 V for a 3.3-V supply) to ground.

## 8.2 Typical Application

### 8.2.1 TIA With Associated Signal Chain

图 39 presents a complete end-to-end receive signal chain for an optical input. It includes a high-speed photodiode, the OPA857, a THS4541 fully-differential amplifier, and a 16-bit, 160-MSPS, high-speed ADC. For the complete wide-bandwidth, optical front-end reference design, go to http://www.ti.com/tool/TIDA-00725.

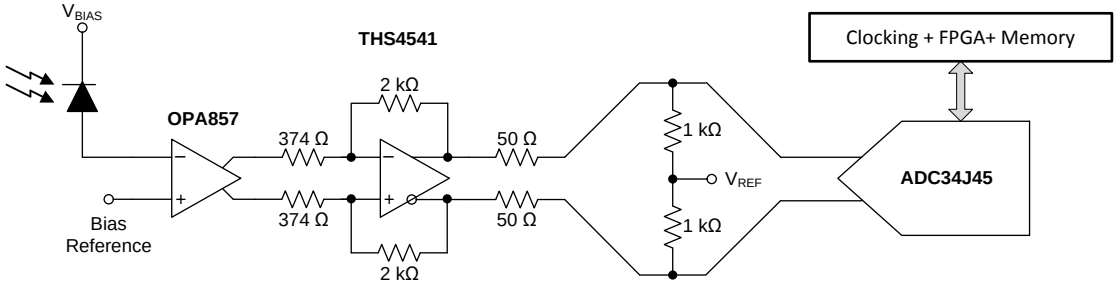



**图 39. TIA With Associated Signal Chain**

## Typical Application (接下页)

### 8.2.1.1 Design Requirements

For this example, use the values listed in 表 3 for the input parameters.

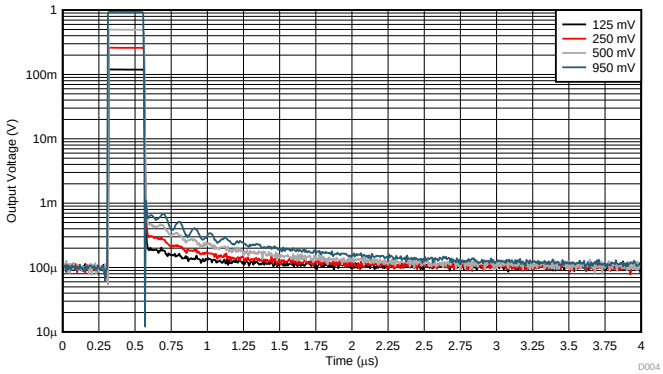
**表 3. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Supply voltage | 5-V external supply |
| Analog bandwidth | 120 MHz |
| ADC sampling rate | 160 MSPS |
| Maximum system gain | 100 kΩ |
| Programmable transimpedance gain | 5 kΩ / 20 kΩ |
| Maximum signal swing | 1 $V_{PP}$ |
| Noise performance | ≥ 60-dB SNR |
| Averaged noise performance | < 10-$\mu V_{RMS}$ |

### 8.2.1.2 Detailed Design Procedure

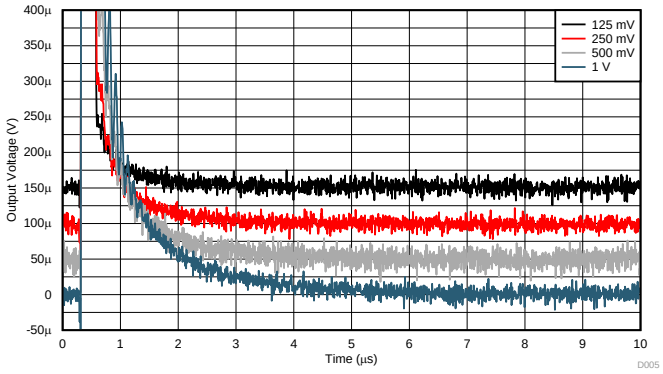
1. Use a high-speed, low input capacitance photodiode, such as the NR7500 or NR8300, as the front-end optical sensor. Take care during layout to minimize parasitic capacitance added because of the PCB.
2. Bias the photodiode with the cathode connected to a positive supply, and the anode connected to IN pin of the OPA857. These connections make sure that the photodiode sources an output current that results in the OPA857 output swinging down below the reference voltage = (5 / 9) × 3.3 V = 1.83 V.
3. Disable the OPA857 test mode by setting Test_IN = $+V_S$ and Test_SD = GND. The transimpedance gain is selected by setting CTRL = $+V_S$ (gain = 20 kΩ) or CTRL = GND (gain = 5 kΩ).
4. The THS4541 is configured in a gain of 5 V/V in order to achieve a maximum signal transimpedance gain of 100 kΩ. It is important to carefully select the value of the RG gain resistors for the THS4541.
5. Setting RG very low increases the resistive loading on the previous OPA857 output stage, and reduces the bandwidth of the OPA857.
6. Setting $R_G$ very high results in a large value of feedback resistance, $R_F$, on the THS4541 in order to achieve the desired 5V/V gain. $R_F$ interacts with the input capacitance of the THS4541 to create a zero in the noise-gain response of the amplifier, and if not properly compensated, results in reduced phase-margin and potential instability.
7. A value of $R_G$ = 374 Ω was selected that results in a total differential load of 798 Ω on the OPA857. The resultant $R_F$ = 2 kΩ.
8. The response to an optical pulsed input is shown in 图 40 to 图 43. To prevent signal reflections between the THS4541 output and the ADC34J45 input, the signal is doubly terminated through 50-Ω resistors. If the THS4541 and ADC34J45 are physically close together on the PCB, then the double-termination is eliminated, which increases the overall gain of the signal chain without affecting the transient response of the system. These results were verified, and the complete data is available in reference design TIDA-00725.
9. An optional antialiasing filter can be added between the THS4541 and the ADC34J45 to reduce system noise caused by aliasing.

### 8.2.1.3 Application Curves



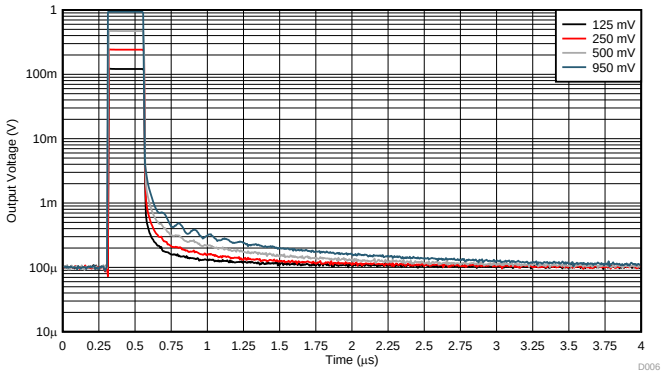

$T_Z$ Gain = 20 kΩ

**图 40. Pulse Response vs Output Voltage**



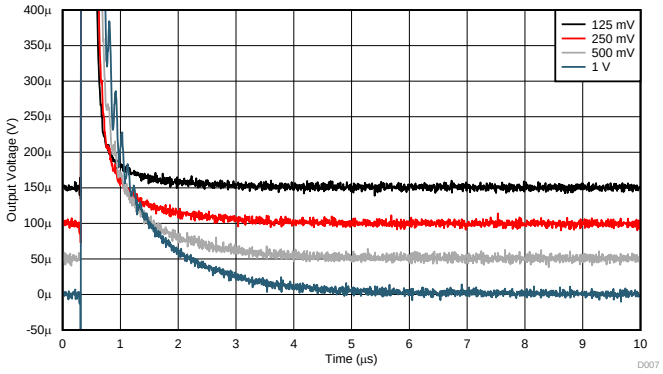

$T_Z$ Gain = 20 kΩ

**图 41. Long-Term Settling Response vs Output Voltage**




$T_Z$ Gain = 5 kΩ

**图 42. Pulse Response vs Output Voltage**




$T_Z$ Gain = 5 kΩ

**图 43. Long-Term Settling Response vs Output Voltage**

### 8.2.2 Extending Transimpedance Bandwidth

At the core of the OPA857 is an ultrawide bandwidth op amp. One of the highlights of the OPA857 is the relatively small change in the transimpedance bandwidth as a function of the internal gain selected; 130 MHz (gain = 5 kΩ) and 105 MHz (gain = 20 kΩ). Theoretically, for a four times increase in gain, the bandwidth should reduce by two times; however, as observed in the case of the OPA857, the results do not follow theory. For more information on the various factors that contribute to an amplifier frequency-response performance when configured as a TIA, see What You Need To Know About Transimpedance Amplifiers – Part 1 on the TI E2E Community website at e2e.ti.com. This blog also contains a reference to an excel calculator to simplify TIA designs when using discrete opamps. The OPA857 is unique in displaying this type of behavior because the CTRL logic controls an internal switch in the amplifier core that recompensates the amplifier open-loop gain characteristic depending upon the logic level. In this application, it it shown how the closed-loop transimpedance bandwidth can be increased to greater than 250 MHz. The circuit used for this test is shown in 图 44. An external feedback resistor, $R_F$, is added in parallel to the internal transimpedance gain resistors of the OPA857. This resistor has the effect of reducing the overall transimpedance gain, but with increased bandwidth.

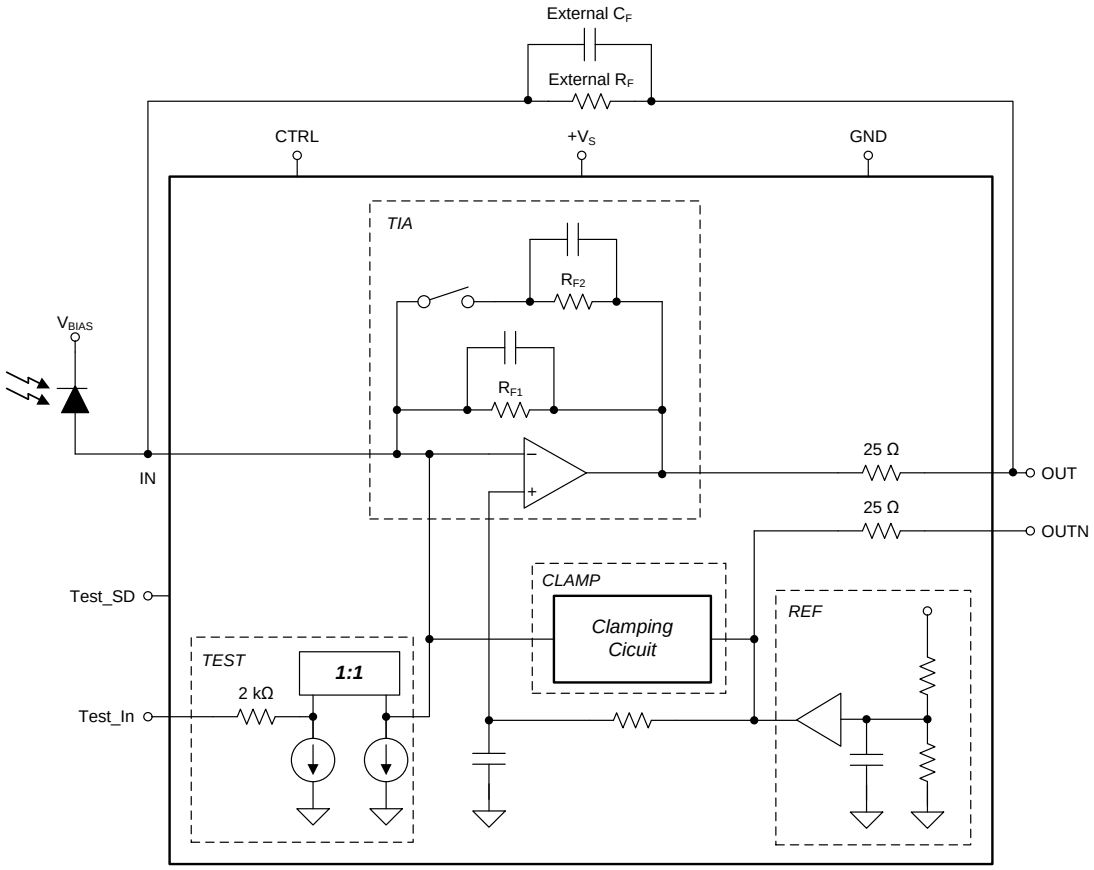



**图 44. Extending Transimpedance Bandwidth**

#### *8.2.2.1 Design Requirements*

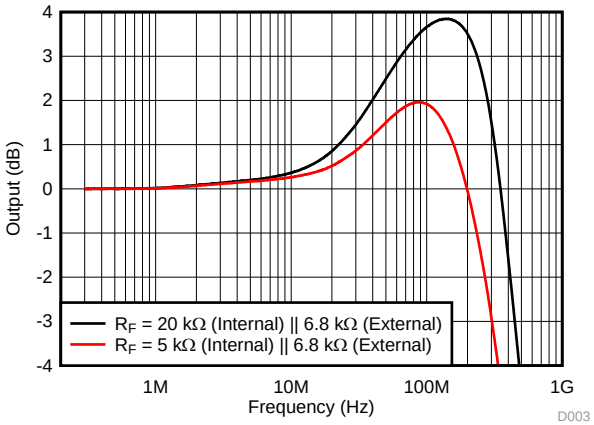
For this example, use the values listed in 表 4 for the input parameters.

**表 4. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Supply voltage | 3.3 V |
| Output swing | 500 $mV_{PP}$ |
| Differential output load | 500 kΩ and 1 kΩ |
| Target bandwidth | 250 MHz |
| Effective transimpedance gain | 5 kΩ |

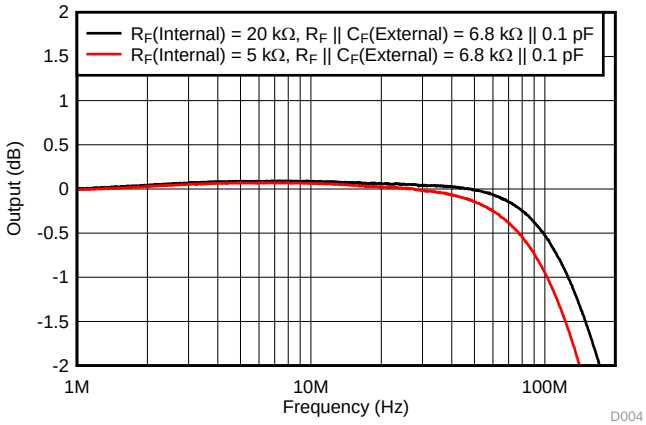
### 8.2.2.2 Application Curves

图 45 shows the frequency response with a feedback resistance of 6.8 kΩ and an output load of 500 Ω. The large amount of peaking indicates a low phase-margin and potential instability. Next, a 0.1-pF feedback capacitor, $C_F$, is added in parallel to the 6.8-kΩ $R_F$. Both $R_F$ and $C_F$ interact to create pole in the noise gain curve that counteracts the effect of the zero caused by $R_F$, and the total input capacitance at pin IN of the OPA857. The input capacitance is caused by the opamps inherent input capacitance, the photodiode capacitance, and the parasitic input capacitance from the PCB. The pole zero cancellation increases the phase margin, as is evident in the reduced peaking shown in 图 46. In 图 47, an output load of 1 kΩ was used, along with an $R_F$ = 6.8 kΩ and $C_F$ = 0.1 pF. The reduced load helps to increase the op amp open-loop gain, which in turn increases the closed-loop bandwidth of the OPA857 circuit.



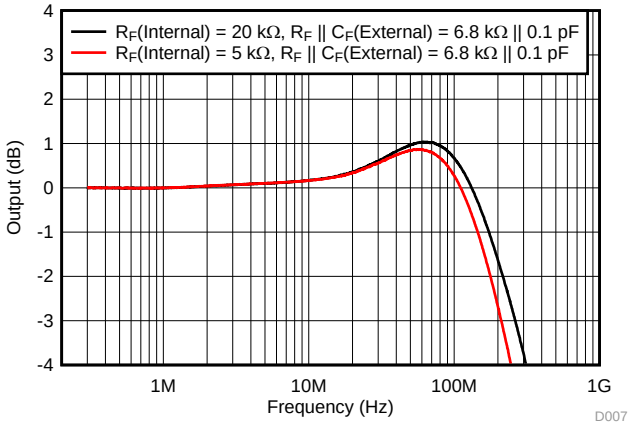

$R_F$ = 6.8 kΩ

**图 45. Frequency Response With External Feedback**




$R_F$ = 6.8 kΩ, $C_F$ = 0.1 pF

**图 46. Frequency Response With External Feedback**




$R_F$ = 6.8 kΩ, $C_F$ = 0.1 pF

**图 47. Frequency Response With External Feedback**

# 9 Power-Supply Recommendations

Use a linear power supply with good PSRR. For a good, high-frequency, power-supply bypass, use a ceramic capacitor connected as close as possible to the $+V_S$ pin.

# 10 Layout

## 10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA857 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a. **Minimize parasitic capacitance** to any ac ground for all signal I/O pins. Parasitic capacitance on the inverting input pin can cause instability. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

b. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1-µF decoupling capacitors, as shown in 图 48. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors. An optional supply decoupling capacitor (0.1 µF) across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Use larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequencies, on the main supply pins. These capacitors can be placed somewhat farther from the device and can be shared among several devices in the same area of the PC board.

c. **Careful selection and placement of external components preserves the high-frequency performance of the OPA857.** Use very low reactance type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good high-frequency performance. Again, keep the leads and PC board traces as short as possible. Never use wirewound type resistors in a high-frequency application.

d. **Connections to other wideband devices** on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.

e. **Do not socket a high-speed part such as the OPA857.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the OPA857 onto the board.

## 10.2 Layout Example

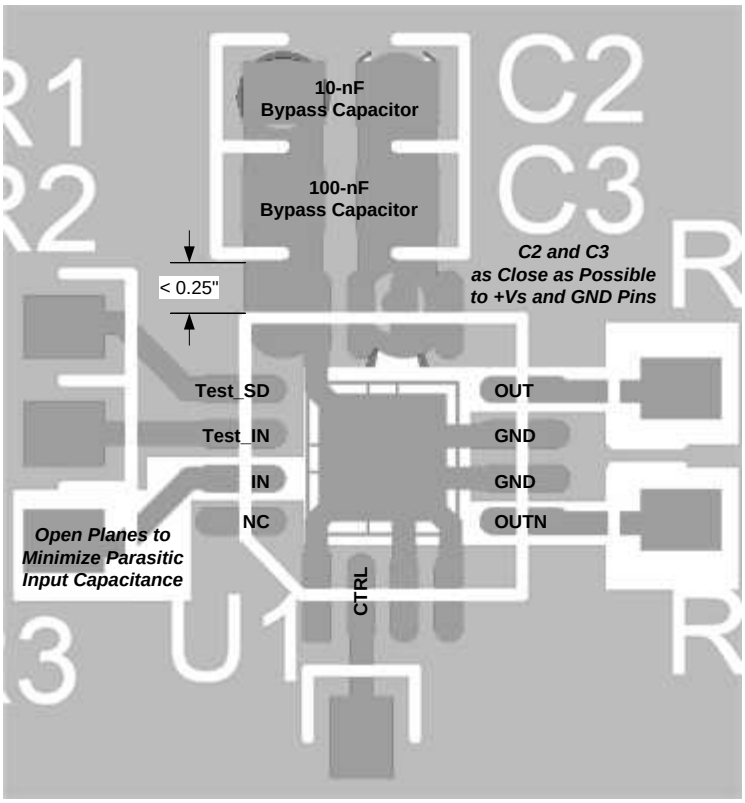



**图 48. Layout Example**

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 开发支持

#### *11.1.1.1 评估模块*

评估模块 (EVM) 可与 OPA857 配套使用，帮助评估初始电路性能。此固定装置的相关摘要信息显示在表 5 中。

**表 5. EVM 订购信息**

| 产品 | 封装 | 订购号 | 文献编号 |
|---|---|---|---|
| OPA857IRGT | RGT | OPA857EVM | SBOU138 |

在德州仪器 (TI) 网站 (www.ti.com) 上，可通过 OPA857 产品文件夹获取 EVM。

#### *11.1.1.2 Spice 模型*

分析模拟电路和系统的性能时，使用 spice 模型对电路性能进行计算机仿真非常有用。这一点对于互阻抗应用尤为确切，在此类 应用 中，寄生电容和电感可能对电路性能产生重大影响。OPA857 的 spice 模型可从 OPA857 产品文件夹中的仿真模型下获取。利用这些模型可以有效预测各种运行条件下的交流小信号和瞬态特性。不过，这些模型在预测谐波失真方面的效果并不如意。

## 11.2 文档支持

### 11.2.1 相关文档

相关文档如下：

- *《OPA857EVM 评估模块》*（文献编号：SBOU138）
- *《高速放大器互阻抗注意事项》*（文献编号：SBOA122）
- *《高带宽光学前端参考设计》*（文献编号：TIDUAZ1）
- *《扩展 OPA857 互阻抗带宽的参考设计》*（文献编号：TIDUBX7）
- 通过以下文档可以直观地学习如何补偿互阻抗放大器：
  *《互阻抗放大器须知 – 第 1 部分》*（作者：Cherian；2016 年）

## 11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

## 11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 机械、封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| OPA857IRGTR | Active | Production | VQFN (RGT) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA857 |
| OPA857IRGTR.B | Active | Production | VQFN (RGT) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA857 |
| OPA857IRGTT | Active | Production | VQFN (RGT) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA857 |
| OPA857IRGTT.B | Active | Production | VQFN (RGT) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA857 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

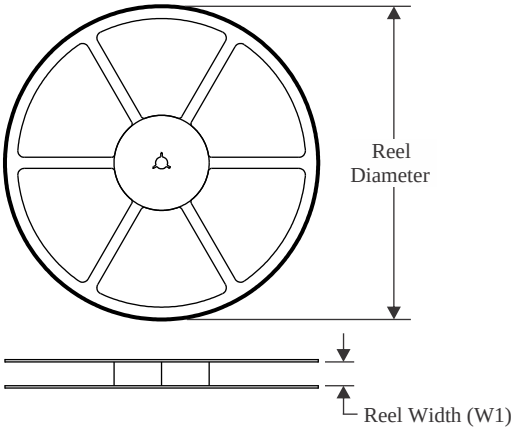
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

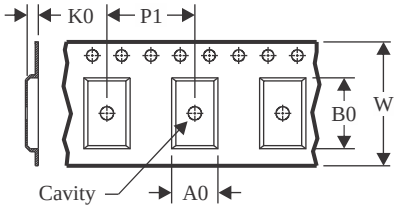
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

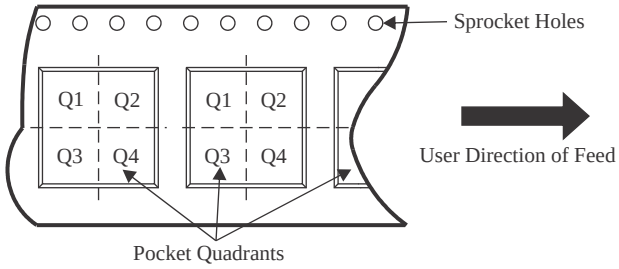



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

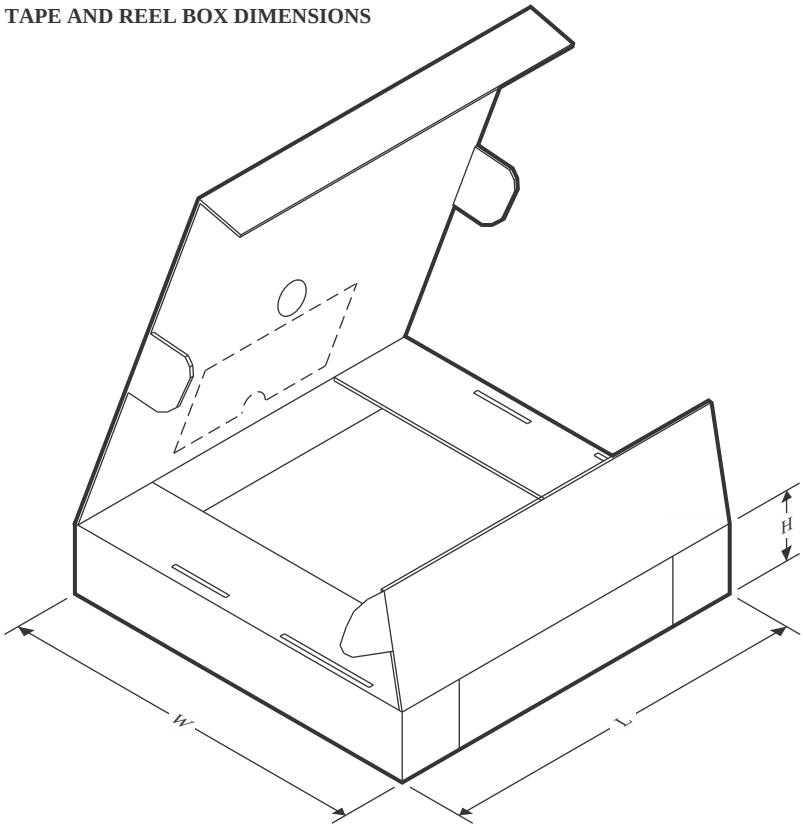
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA857IRGTR | VQFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| OPA857IRGTT | VQFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

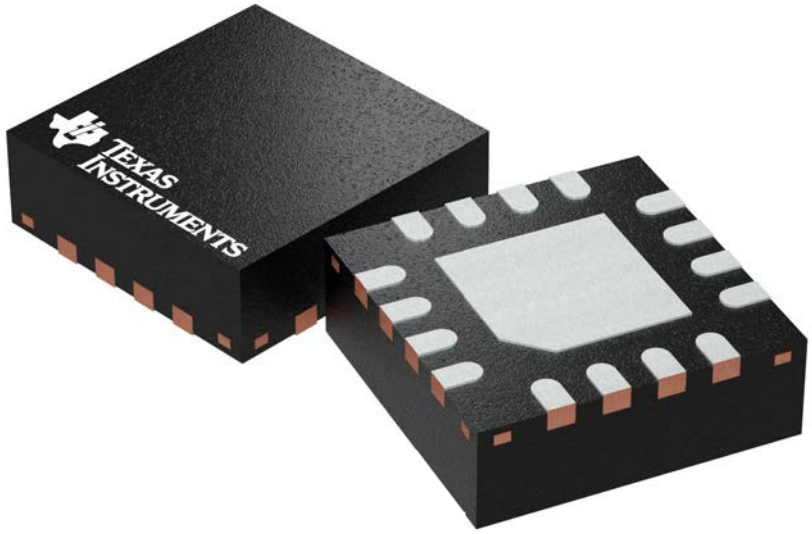



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA857IRGTR | VQFN | RGT | 16 | 3000 | 346.0 | 346.0 | 33.0 |
| OPA857IRGTT | VQFN | RGT | 16 | 250 | 210.0 | 185.0 | 35.0 |

# RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



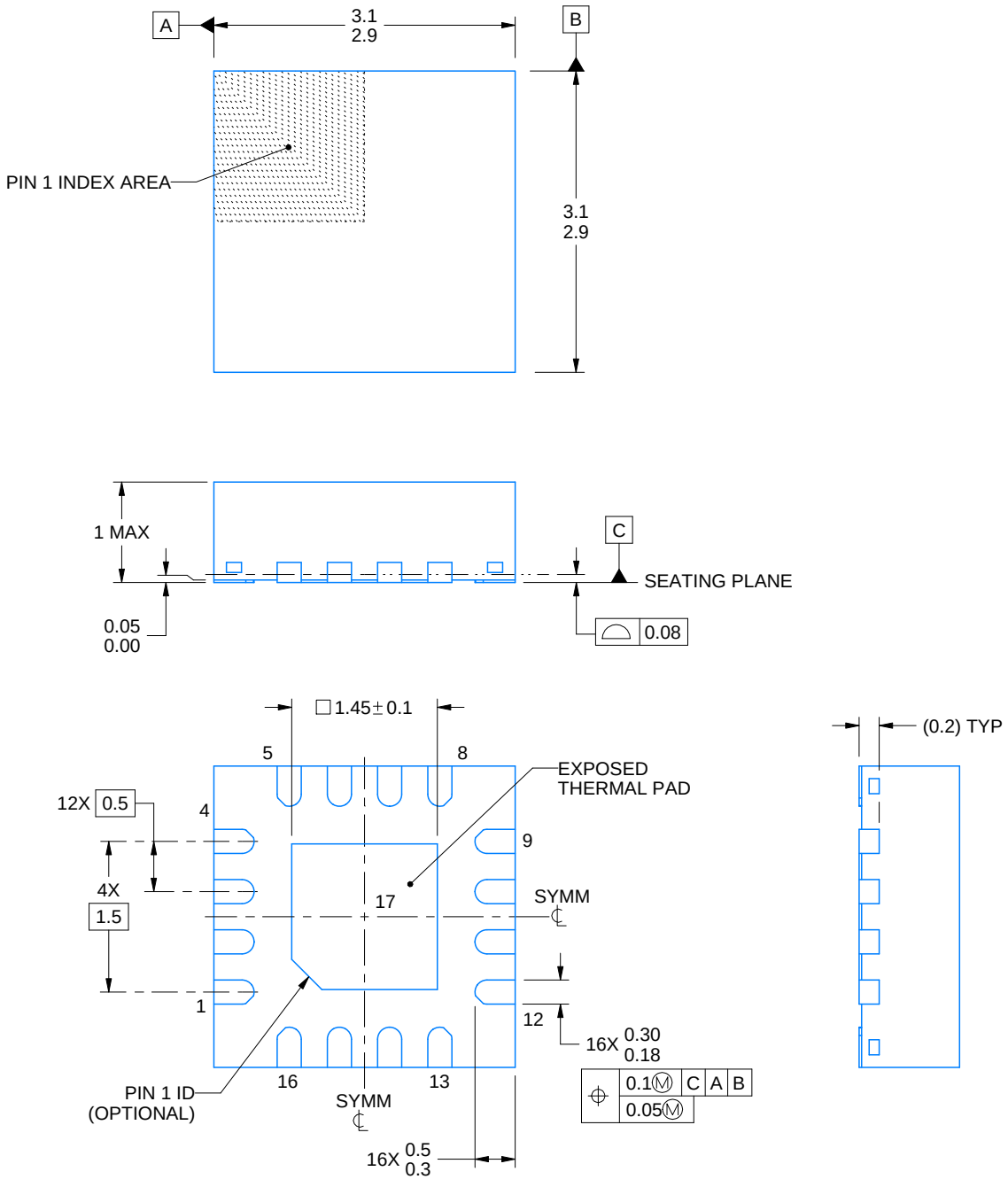

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# RGT0016A

# PACKAGE OUTLINE

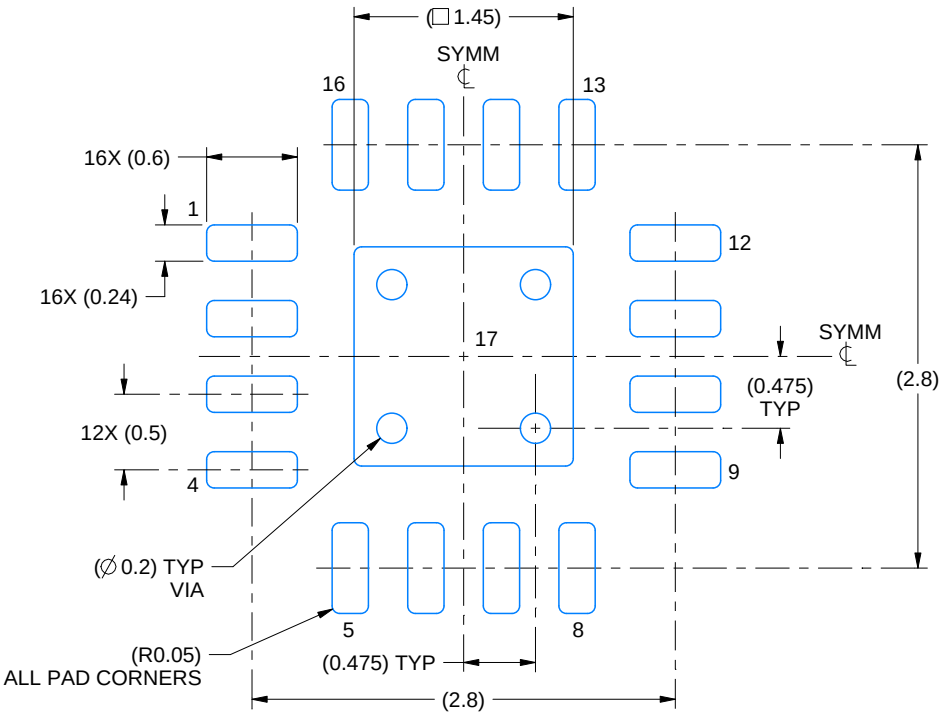
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

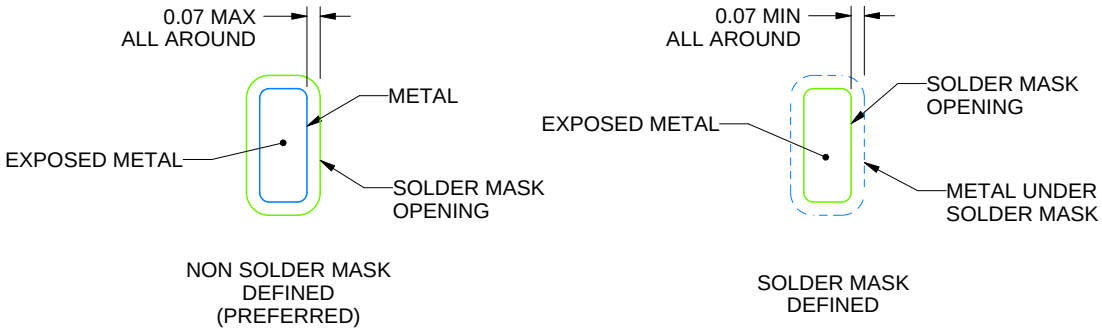



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X




SOLDER MASK DETAILS

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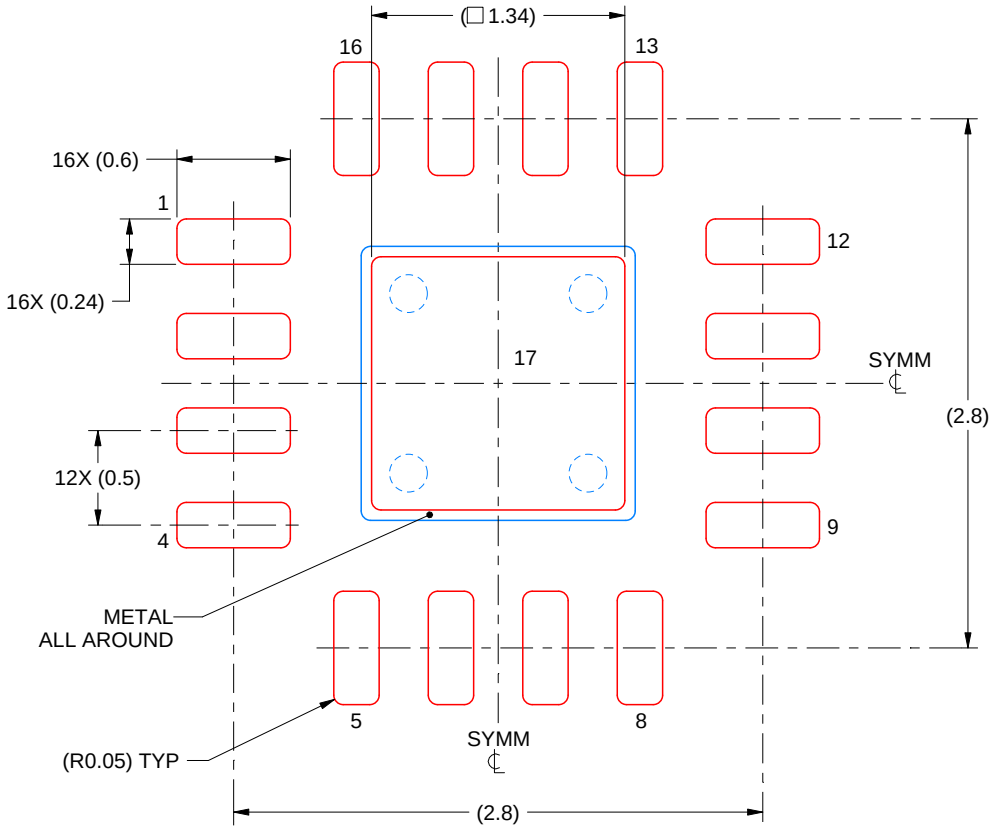
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月