# PCA9306 双路双向 I²C 总线和 SMBus 电压电平转换器

## 1 特性

- 适用于混合模式 I²C 应用中 SDA 和 SCL 线路的 2 位双向转换器
- 与 I²C 和 SMBus 兼容
- 小于 1.5ns 的最大传播延迟，适应标准模式和快速模式 I²C 器件和多个控制器
- 可实现以下电压之间的电压电平转换
  - 1.2V $V_{REF1}$ 和 1.8V、2.5V、3.3V 或 5V $V_{REF2}$
  - 1.8V $V_{REF1}$ 和 2.5V、3.3V 或 5V $V_{REF2}$
  - 2.5V $V_{REF1}$ 和 3.3V 或 5V $V_{REF2}$
  - 3.3V $V_{REF1}$ 和 5V $V_{REF2}$
- 在无方向引脚的情况下提供双向电压转换
- 输入和输出端口之间 3.5Ω 的低导通电阻提供更少的信号失真
- 漏极开路 I²C I/O 端口（SCL1、SDA1、SCL2 和 SDA2）
- 5V 耐压 I²C 和 I/O 端口可支持混合模式信号操作
- 针对 EN 为低电平的高阻抗 SCL1、SDA1、SCL2 和 SDA2 引脚
- 无闭锁操作可在 EN 为低电平时实现隔离
- 采用直通引脚排列以简化印刷电路板布线
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 带电器件模型 (C101)

## 2 应用

- I²C、SMBus、PMBus、MDIO、UART、低速 SDIO、GPIO 和其他双信号接口
- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 工业自动化

## 3 说明

PCA9306 器件是一款采用使能 (EN) 输入的双路双向 I²C 和 SMBus 电压电平转换器，可在 1.2V 至 3.3V $_{REF1}$ 和 1.8V 至 5.5V $_{REF2}$ 的范围内工作。

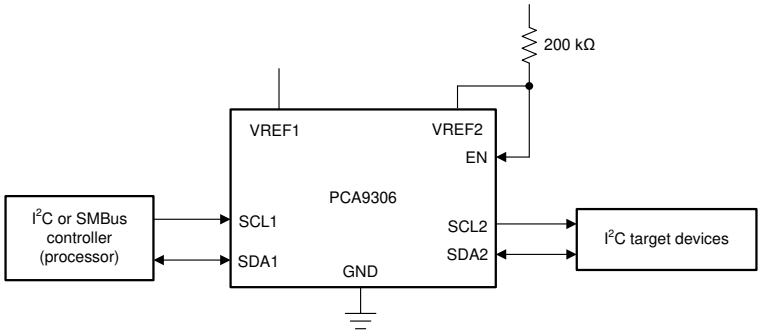
PCA9306 器件可以在 1.2V 到 5V 之间实现双向电压转换而无须使用方向引脚。此开关具有低导通状态电阻 ($R_{ON}$)，可以在最短传播延迟情况下建立连接。当 EN 为高电平时，转换器开关打开，并且 SCL1 和 SDA1 I/O 被分别连接至 SCL2 和 SDA2 I/O，从而实现端口间的双向数据流。当 EN 为低电平时，转换器开关关闭，在端口之间存在一个高阻态。

除了电压转换，PCA9306 器件还可用于将 400kHz 的总线与 100kHz 的总线隔离，方法是在快速模式通信过程中控制 EN 引脚以断开较慢总线的连接。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) |
|---|---|---|
| PCA9306 | SSOP (8) | 2.95mm x 4mm |
| | VSSOP (8) | 2.3mm x 3.1mm |
| | X2SON (8) | 1.4mm x 1mm |
| | DSBGA (8) | 1.98mm x 0.98mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。




简化版应用示意图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision N (October 2021) to Revision O (September 2023)** — **Page**

- 将“器件信息”表更改为*封装信息*表 ..... 1
- Changed the *Thermal Information* table values for the DQE package ..... 6

**Changes from Revision M (April 2019) to Revision N (October 2021)** — **Page**

- 将提到 I2C 的旧术语实例全局更改为控制器和目标 ..... 1
- Changed the *Thermal Information* table values for the DCT and DCU packages ..... 6
- Changed the MIN and MAX values of $V_{IK}$ in the *Electrical Characteristics* table ..... 6
- Changed $t_{PHL}$ to show the package values in the *Switching Characteristics AC Performance (Translating Down) (EN = 3.3 V)* table ..... 7
- Changed $t_{PHL}$ to show the package values in the *Switching Characteristics AC Performance (Translating Down) (EN = 2.5 V)* table ..... 7
- Changed $t_{PHL}$ to show the package values in the *Switching Characteristics AC Performance (Translating Up) (EN = 3.3 V)* table ..... 7
- Changed $t_{PHL}$ to show the package values in the *Switching Characteristics AC Performance (Translating Up) (EN = 2.5 V)* table ..... 7

**Changes from Revision L (April 2016) to Revision M (April 2019)** — **Page**

- Changed the DQE package family From: VSSON to X2SON ..... 4
- Added new section to *Overview* ..... 10
- Changed the labels in 图 9-4. The red curve is > 2 V, the black curve is ≤ 2 V. ..... 20

**Changes from Revision K (October 2014) to Revision L (April 2016)** — **Page**

- 将“导通状态连接”更改为“导通状态电阻” ..... 1
- 删除了机器模型 ESD 等级 ..... 1
- 在*说明*部分最后一句的“100kHz”后增加了“总线” ..... 1


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- 更改了 *器件信息* 表中的封装尺寸 ..... 1
- Replaced pinout diagrams ..... 4
- Added I/O column to the *Pin Functions* table ..... 4
- Deleted RVH package from *Pin Configuration and Functions* section ..... 4
- Moved $T_{stg}$ from *Handling Ratings* to *Absolute Maximum Ratings* ..... 5
- Added a note following the *Electrical Characteristics* table ..... 6
- Added 图 7-1 to the *Parameter Measurement Information* section ..... 9
- Changed 图 7-2 ..... 9
- Changed "repeater" to "level shifter" in second paragraph of the *Overview* section ..... 10
- Deleted the last row of the Design Requirements table. ..... 18
- Corrected equation from $f_{knee}$= 0.5 / RT (10% – 80%) to $f_{knee}$= 0.5 / RT (10% – 90%) ..... 19

**Changes from Revision J (October 2010) to Revision K (December 2012)** **Page**

- 添加了 *引脚配置和功能* 部分、*处理等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 ..... 1

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## 5 Pin Configuration and Functions

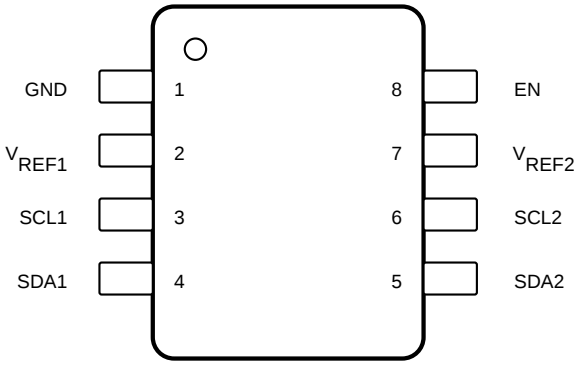



图 5-1. DCT Package 8-Pin SSOP (Top View)




图 5-2. DCU Package 8-Pin VSSOP (Top View)

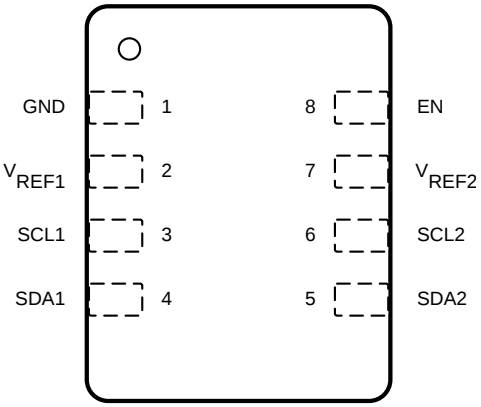



图 5-3. DQE Package 8-Pin X2SON (Top View)

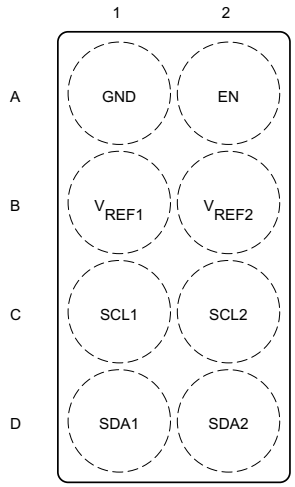



图 5-4. YZT Package 8-Pin DSBGA (Top View)

表 5-1. Pin Functions

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | DCT, DCU, DQE | YZT | | |
| EN | 8 | A2 | I | Switch enable input |
| GND | 1 | A1 | — | Ground, 0 V |
| SCL1 | 3 | C1 | I/O | Serial clock, low-voltage side |
| SCL2 | 6 | C2 | I/O | Serial clock, high-voltage side |
| SDA1 | 4 | D1 | I/O | Serial data, low-voltage side |
| SDA2 | 5 | D2 | I/O | Serial data, high-voltage side |
| $V_{REF1}$ | 2 | B1 | I | Low-voltage-side reference supply voltage for SCL1 and SDA1 |
| $V_{REF2}$ | 7 | B2 | I | High-voltage-side reference supply voltage for SCL2 and SDA2 |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) see (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{REF1}$ | DC reference voltage range | | –0.5 | 7 | V |
| $V_{REF2}$ | DC reference bias voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_{I/O}$ | Input/output voltage range(2) | | –0.5 | 7 | V |
| | Continuous channel current | | | 128 | mA |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $T_{j(max)}$ | Maximum junction temperature | | | 125 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-0011, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{I/O}$ | Input/output voltage | SCL1, SDA1, SCL2, SDA2 | 0 | 5.5 | V |
| $V_{REF1}$ (1) | Reference voltage | | 0 | 5.5 | V |
| $V_{REF2}$ (1) | Reference voltage | | 0 | 5.5 | V |
| EN | Enable input voltage | | 0 | 5.5 | V |
| $I_{PASS}$ | Pass switch current | | | 64 | mA |
| $T_A$ | Operating ambient temperature | | –40 | 85 | °C |

(1) To support translation, $V_{REF1}$ supports 1.2 V to $V_{REF2}$ - 0.6 V. $V_{REF2}$ must be between $V_{REF1}$ + 0.6 V to 5.5 V. See 节 9.2 for more information.

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## 6.4 Thermal Information

| THERMAL METRIC(1) | | PCA9306 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DCT | DCU | DQE | YZT | |
| | | 8 PINS | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 254.1 | 275.5 | 299.3 | 125.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 148.6 | 127.1 | 166.9 | 1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 168.8 | 186.9 | 188.30 | 62.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 70.1 | 65.7 | 18.0 | 3.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 167.4 | 185.9 | 187.4 | 62.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating ambient temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | | $I_I$ = –18 mA, | EN = 0 V | | -1.2 | | 0 | V |
| $I_{IH}$ | Input leakage current | | $V_I$ = 5 V, | EN = 0 V | | | | 5 | μA |
| $C_{i(EN)}$ | Input capacitance | | $V_I$ = 3 V or 0 | | | | 11 | | pF |
| $C_{io(off)}$ | Off capacitance | SCLn, SDAn | $V_O$ = 3 V or 0, | EN = 0 V | | | 4 | 6 | pF |
| $C_{io(on)}$ | On capacitance | SCLn, SDAn | $V_O$ = 3 V or 0, | EN = 3 V | | | 10.5 | 12.5 | pF |
| $R_{ON}$ (2) | On-state resistance | SCLn, SDAn | $V_I$ = 0 | $I_O$ = 64 mA | EN = 4.5 V | | 3.5 | 5.5 | Ω |
| | | | | | EN = 3 V | | 4.7 | 7 | |
| | | | | | EN = 2.3 V | | 6.3 | 9.5 | |
| | | | $V_I$ = 0 | $I_O$ = 15 mA | EN = 1.5 V | | 25.5 | 32 | |
| | | | $V_I$ = 2.4 V(3) | $I_O$ = 15 mA | EN = 4.5 V | 1 | 6 | 15 | |
| | | | | | EN = 3 V | 20 | 60 | 140 | |
| | | | $V_I$ = 1.7 V(3) | $I_O$ = 15 mA | EN = 2.3 V | 20 | 60 | 140 | |

(1) All typical values are at $T_A$ = 25°C.
(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two terminals.
(3) Measured in current sink configuration only (See 图 7-1)


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## 6.6 Switching Characteristics AC Performance (Translating Down) (EN = 3.3 V)

over recommended operating ambient temperature range, EN = 3.3 V, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0, $V_M$ = 1.15 V (unless otherwise noted) (see 图 7-1).

| PARAMETER(1) | FROM (INPUT) | TO (OUTPUT) | Package | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | SCL2 or SDA2 | SCL1 or SDA1 | | 0 | 0.8 | 0 | 0.6 | 0 | 0.3 | ns |
| $t_{PHL}$ | | | YZT, DQE | 0 | 1.2 | 0 | 1 | 0 | 0.5 | |
| | | | DCU, DCT | | | | | | 0.75 | |

(1) Translating down: the high-voltage side driving toward the low-voltage side

## 6.7 Switching Characteristics AC Performance (Translating Down) (EN = 2.5 V)

over recommended operating ambient temperature range, EN = 2.5 V, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0, $V_M$ = 0.75 V (unless otherwise noted) (see 图 7-1).

| PARAMETER(1) | FROM (INPUT) | TO (OUTPUT) | Package | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | SCL2 or SDA2 | SCL1 or SDA1 | | 0 | 1 | 0 | 0.7 | 0 | 0.4 | ns |
| $t_{PHL}$ | | | YZT, DQE | 0 | 1.3 | 0 | 1 | 0 | 0.6 | |
| | | | DCT, DCU | | | | | | 0.75 | |

(1) Translating down: the high-voltage side driving toward the low-voltage side

## 6.8 Switching Characteristics AC Performance (Translating Up) (EN = 3.3 V)

over recommended operating ambient temperature range, EN = 3.3 V, $V_{IH}$ = 2.3 V, $V_{IL}$ = 0, $V_T$ = 3.3 V, $V_M$ = 1.15 V, $R_L$ = 300 Ω (unless otherwise noted) (see 图 7-1).

| PARAMETER(1) | FROM (INPUT) | TO (OUTPUT) | Packages | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | SCL1 or SDA1 | SCL2 or SDA2 | | 0 | 0.9 | 0 | 0.6 | 0 | 0.4 | ns |
| $t_{PHL}$ | | | YZT, DQE | 0 | 1.4 | 0 | 1.1 | 0 | 0.7 | |
| | | | DCU, DCT | | 1.7 | | 1.4 | | 1.0 | |

(1) Translating up: the low-voltage side driving toward the high-voltage side

## 6.9 Switching Characteristics AC Performance (Translating Up) (EN = 2.5 V)

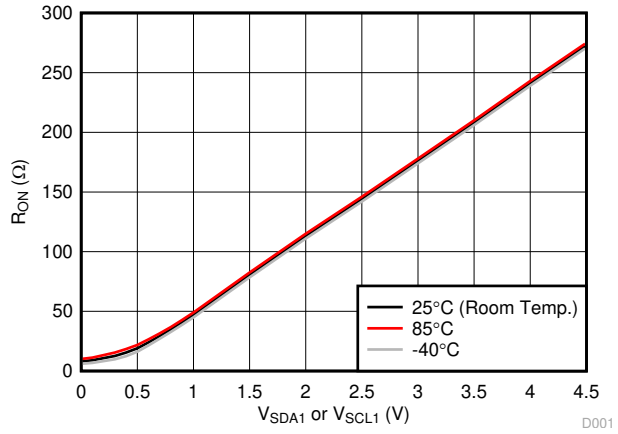
over recommended operating ambient temperature range, EN = 2.5 V, $V_{IH}$ = 2.3 V, $V_{IL}$ = 0, $V_T$ = 3.3 V, $V_M$ = 0.75 V, $R_L$ = 300 Ω (unless otherwise noted) (see 图 7-1).

| PARAMETER(1) | FROM (INPUT) | TO (OUTPUT) | Packages | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 15 pF | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | SCL1 or SDA1 | SCL2 or SDA2 | | 0 | 1 | 0 | 0.6 | 0 | 0.4 | ns |
| $t_{PHL}$ | | | YZT, DQE | 0 | 1.3 | 0 | 1.3 | 0 | 0.8 | |
| | | | DCT, DCU | | 2.1 | | 1.7 | | 1.3 | |

(1) Translating up: the low-voltage side driving toward the high-voltage side

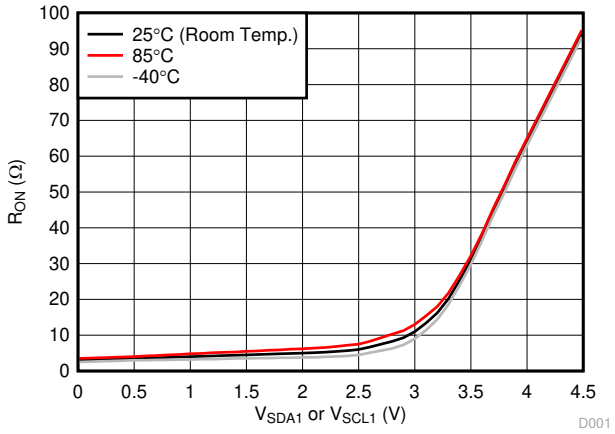
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## 6.10 Typical Characteristics



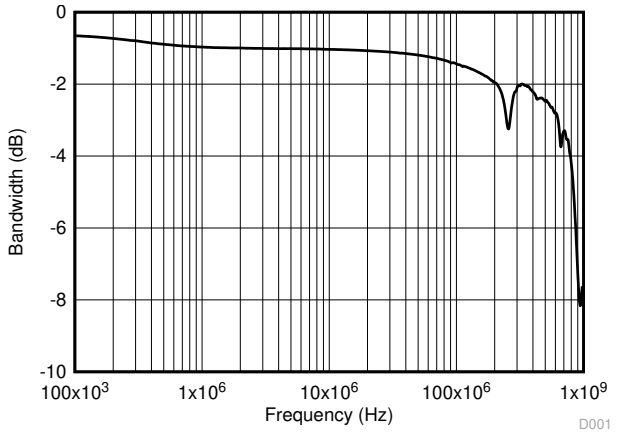

$V_{EN}$ = 1.5 V $I_I$ = 15 mA

**图 6-1. On-Resistance ($R_{ON}$) vs Input Voltage ($V_{SDA1}$ or $V_{SCL1}$)**




$V_{EN}$ = 4.5 V $I_I$ = 15 mA

**图 6-2. On-Resistance ($R_{ON}$) vs Input Voltage ($V_{SDA1}$ or $V_{SCL1}$)**

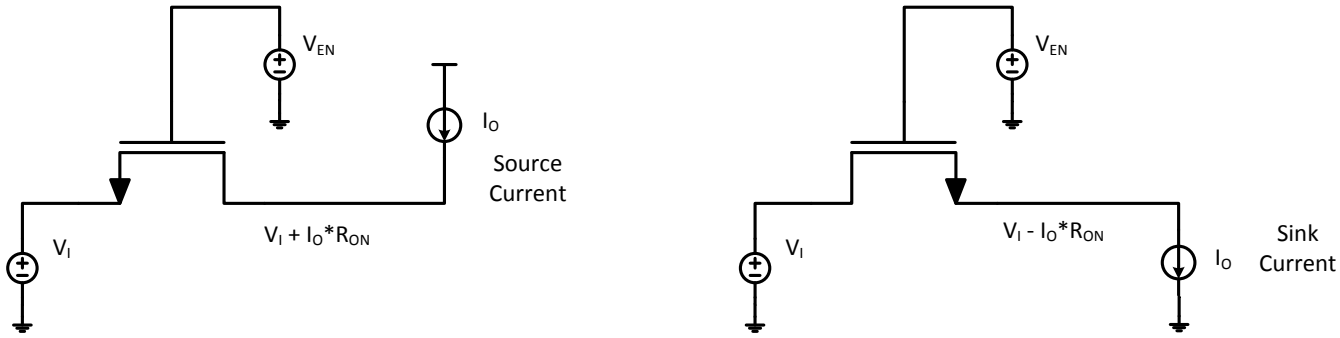



$V_{EN}$ = 2.5 V $V_{BIAS}$ = GND

**图 6-3. Typical Bandwidth of PCA9306**


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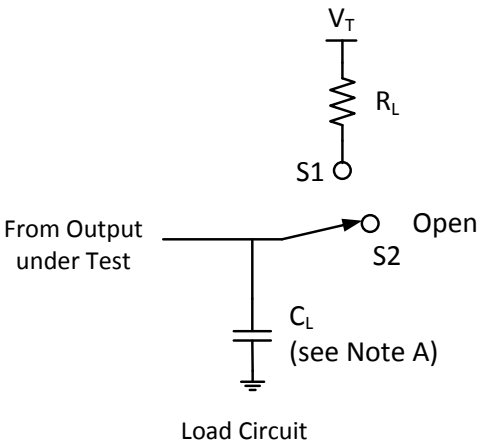
## 7 Parameter Measurement Information



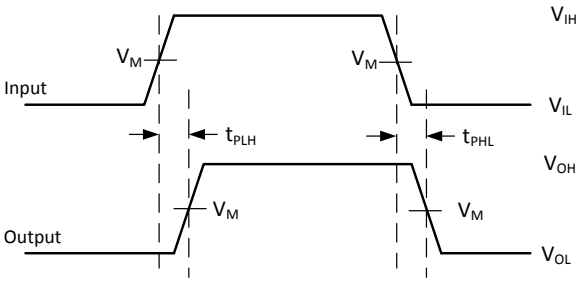

a) Current Source Configuration

b) Current Sink Configuration

**图 7-1. Current Source and Current Sink Configurations for $R_{ON}$ Measurements**




| USAGE | SWITCH |
|---|---|
| Translating up | S1 |
| Translating down | S2 |




NOTES: A. $C_L$ includes probe and jig capacitance
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω , $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

**图 7-2. Load Circuit for Outputs**

# 8 Detailed Description

## 8.1 Overview

The PCA9306 device is a dual bidirectional $I^2C$ and SMBus voltage-level translator with an enable (EN) input and operates without use of a direction pin. The voltage supply range for $V_{REF1}$ is 1.2 V to 3.3 V and the supply range for $V_{REF2}$ is 1.8 V to 5.5 V.

The PCA9306 device can also be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be disconnected by using the EN pin when the 400-kHz operation of the main bus is required. If the controller is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the level shifter.

In $I^2C$ applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. The capacitive load on both sides of the PCA9306 device must be taken into account when approximating the total load of the system, ensuring the sum of both sides is under 400 pF.

Both the SDA and SCL channels of the PCA9306 device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete-transistor voltage-translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less-ESD-resistant devices.

### 8.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as $V_{th}$, which appears multiple times throughout this document when discussing the NFET between $V_{REF1}$ and $V_{REF2}$. The value of $V_{th}$ is approximately 0.6 V at room temperature.

### 8.1.2 Correct Device Set Up

In a normal set up shown in 图 8-1, the enable pin and $V_{REF2}$ are shorted together and tied to a 200-kΩ resistor, and a reference voltage equal to $V_{REF1}$ plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.


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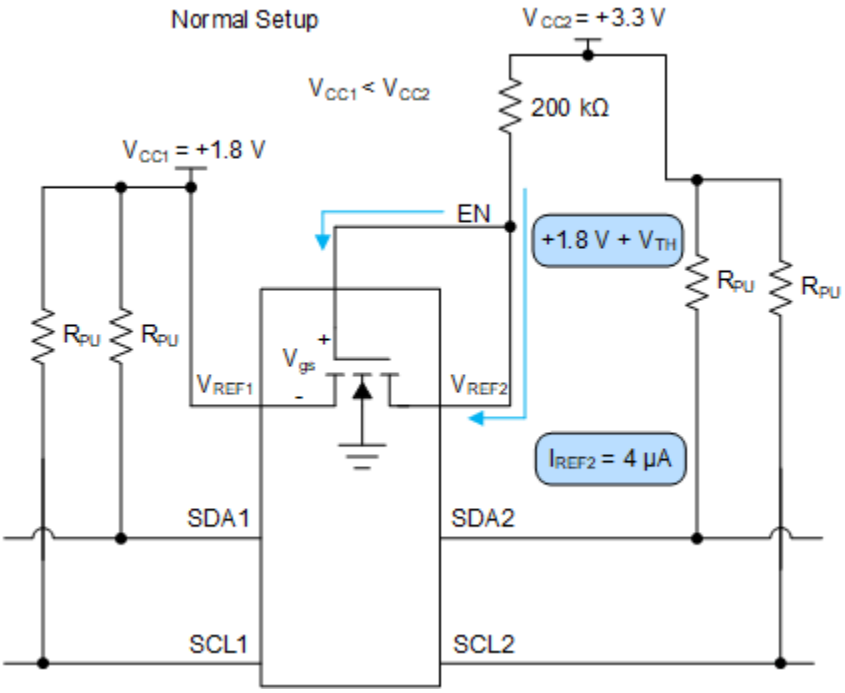



**图 8-1. Normal Setup**

Care should be taken to make sure $V_{REF2}$ has an external resistor tied between it and $V_{CC2}$. If $V_{REF2}$ is tied directly to the $V_{CC2}$ rail without a resistor, then there is no external resistance from the $V_{CC2}$ to $V_{CC1}$ to limit the current such as in 图 8-2. This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 6.1. The continuous channel current is larger with a higher voltage difference between $V_{CC1}$ and $V_{CC2}$.

图 8-2 shows an improper set up. If $V_{CC2}$ is larger than $V_{CC1}$ but less than $V_{th}$, the impedance between $V_{CC1}$ and $V_{CC2}$ is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when $V_{CC2}$ becomes larger than $V_{CC1}$ by $V_{th}$. During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

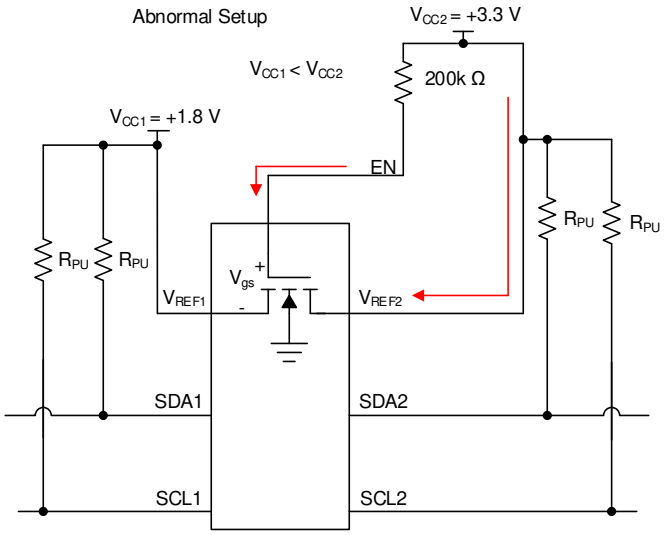



**图 8-2. Abnormal Setup**

### 8.1.3 Disconnecting an I2C target from the Main I2C Bus Using the EN Pin

PCA9306 can be used as a switch to disconnect one side of the device from the main I2C bus. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I2C bus which only supports fast mode (400 kHz) while other devices on the bus support fast mode plus (1 MHz). An example of this is displayed in 图 8-3.

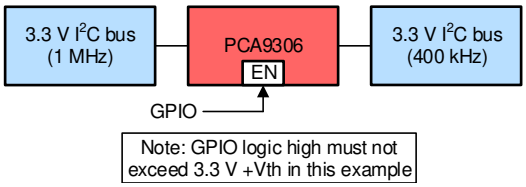



**图 8-3. Example of an I2C bus with multiple supported frequencies**

In this situation, if the controller is on the 1 MHz side then communicating at 1 MHz should not be attempted if PCA9306 were enabled. It needs to be disabled for PCA9306 to avoid possibly glitching state machines in devices which were designed to operate correctly at 400 kHz or slower. When PCA9306 is disabled, the controller can communicate with the 1 MHz devices without disturbing the 400 kHz bus. When the PCA9306 is enabled, communication across both sides at 400 kHz is acceptable.

### 8.1.4 Supporting Remote Board Insertion to Backplane with PCA9306

Another situation where PCA9306 is advantageous when using its enable feature is when a remote board with I2C lines needs to be attached to a main board (backplane) with an I2C bus such as in 图 8-4. If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line. Which could glitch an I2C device state machine causing the I2C bus to get stuck.

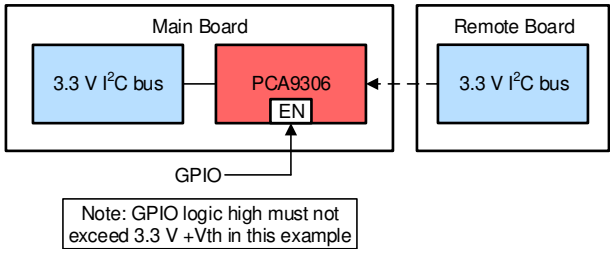



**图 8-4. An example of connecting a remote board to a main board (backplane)**

PCA9306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

### 8.1.5 Switch Configuration

PCA9306 has the capability of being used with its $V_{REF1}$ voltage equal to $V_{REF2}$. This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in 图 8-5 and translation mode is shown in 图 8-6.


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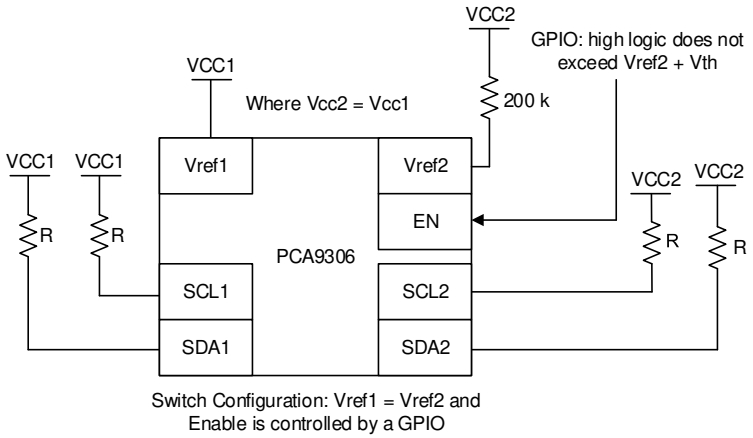



**图 8-5. Switch Configuration**

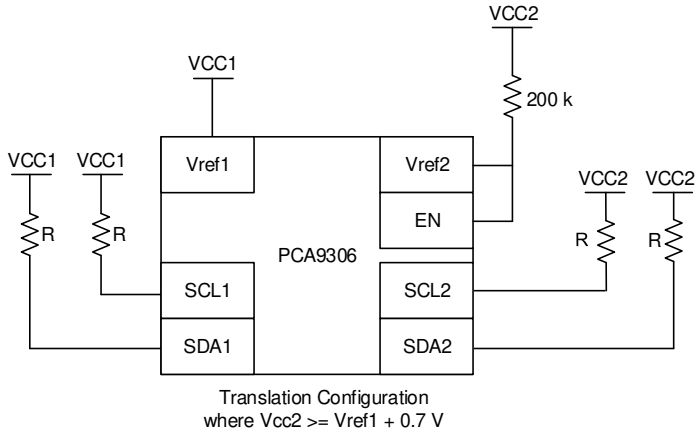



**图 8-6. Translation Configuration**

When PCA9306 is in the switch configuration ($V_{REF1}$ = $V_{REF2}$), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the PCA9306 has the same propagation delay from side one to two and side two to one. The propagation delays become lower when $V_{CC1}$/$V_{CC2}$ is larger. For example, the propagation delay at 1.8 V is longer than at 5 V in the switching configuration. When PCA9306 is in translation mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between $V_{CC2}$ and $V_{CC1}$ becomes.

### 8.1.6 Controller on Side 1 or Side 2 of Device

I2C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. PCA9306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the controller to be able to placed on either side of the device. 图 8-7 shows the controller on side two as opposed to the diagram on page 1 of this data sheet.

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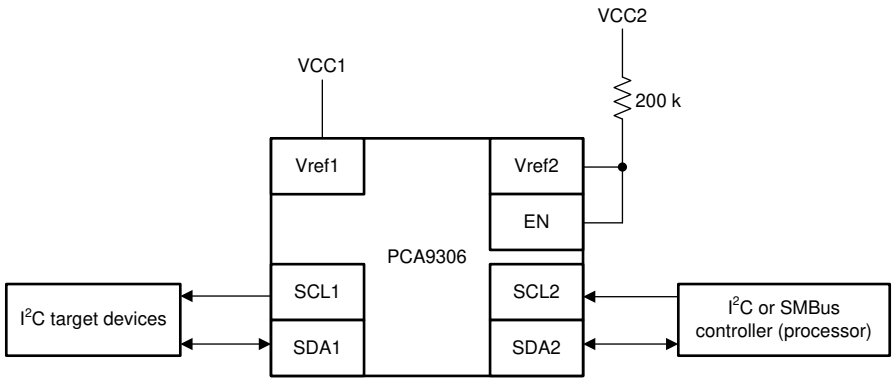



**图 8-7. Controller on side 2 of PCA9306**

### 8.1.7 LDO and PCA9306 Concerns

The $V_{REF1}$ pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO may lose its regulation because of the bias current from $V_{REF2}$ to $V_{REF1}$. If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the $V_{REF1}$ node (both external and parasitic). This results in an increase in voltage on the $V_{REF1}$ node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the $V_{REF1}$ node), then the $V_{REF1}$ voltage ends up stabilizing when $V_{gs}$ of the pass FET is equal to $V_{th}$. This means $V_{REF1}$ node voltage is $V_{CC2}$ - $V_{th}$. Note that any targets/controllers running off of the LDO now see the $V_{CC2}$ - $V_{th}$ voltage which may cause damage to those targets/controllers if they are not rated to handle the increased voltage.

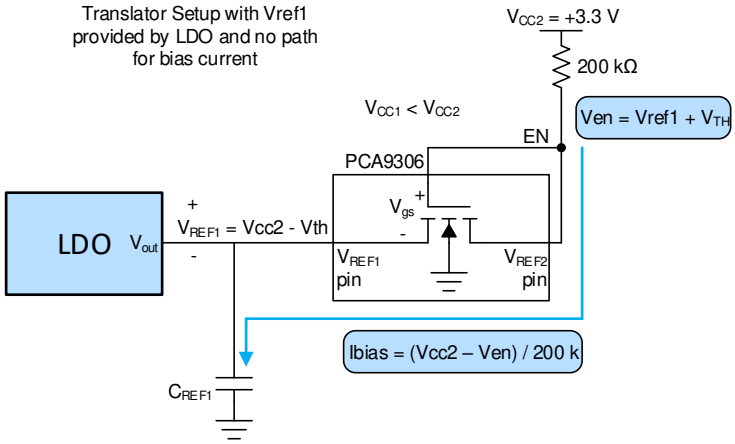



**图 8-8. Example of no leakage current path when using LDO**

To make sure the LDO does not lose regulation due to the bias current of PCA9306, a weak pull down resistor can be placed on $V_{REF1}$ to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by 方程式 4 where 0.75 gives about 25% margin for error incase bias current increases during operation.


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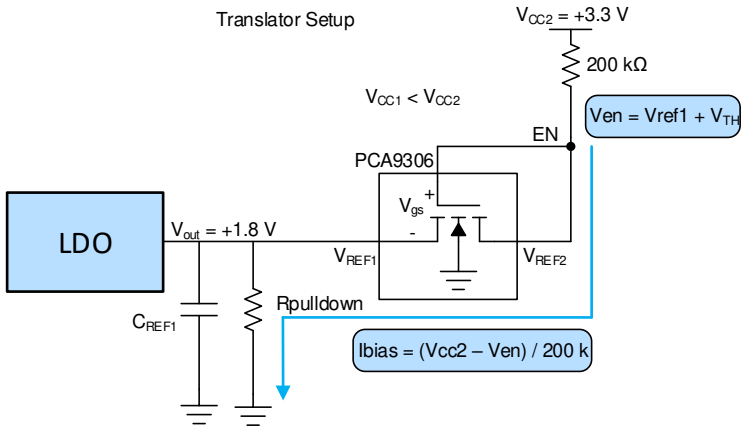



**图 8-9. Example with Leakage current path when using an LDO**

$$V_{en} = V_{REF1} + V_{th} \quad (1)$$

where

- $V_{th}$ is approximately 0.6 V

$$I_{bias} = (V_{CC2} - V_{en})/200k \quad (2)$$

$$R_{pulldown} = V_{OUT}/I_{bias} \quad (3)$$

$$\text{Recommended } R_{pulldown} = R_{pulldown} \times 0.75 \quad (4)$$

### 8.1.8 Current Limiting Resistance on $V_{REF2}$

The resistor is used to limit the current between $V_{REF2}$ and $V_{REF1}$ (denoted as $R_{CC}$) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = (V_{CC2} - V_{en})/R_{CC} : V_{en} = V_{REF1} + V_{th} \quad (5)$$

where

- $V_{th}$ is approximately 0.6V

Keep in mind $R_{CC}$ should not be sized low enough that $I_{CC}$ exceeds the absolute maximum continuous channel current specified in section 6.1 which is described in 方程式 6.

$$R_{CC}(min) \geqslant (V_{CC2} - V_{en})/0.128 : V_{en} = V_{REF1} + V_{th} \quad (6)$$

where

- $V_{th}$ is approximately 0.6V

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## 8.2 Functional Block Diagram

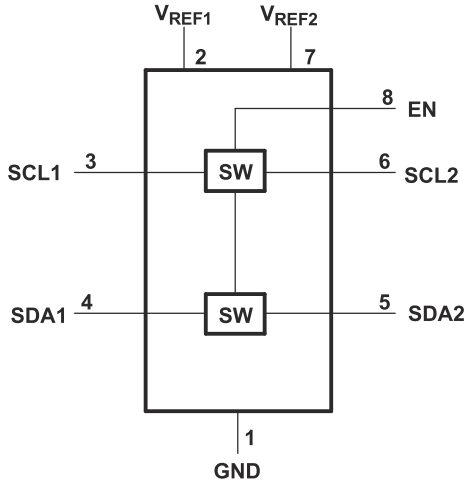



图 8-10. Block Diagram of PCA9306

## 8.3 Feature Description

### 8.3.1 Enable (EN) Pin

The PCA9306 device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In 图 9-1, the PCA9306 device is always enabled when power is applied to $V_{REF2}$. In 图 9-2, the device is enabled when a control signal from a processor is in a logic-high state.

### 8.3.2 Voltage Translation

The primary feature of the PCA9306 device is translating voltage from an $I^2C$ bus referenced to $V_{REF1}$ up to an $I^2C$ bus referenced to $V_{DPU}$, to which $V_{REF2}$ is connected through a 200-kΩ pullup resistor. Translation on a standard, open-drain $I^2C$ bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to $V_{REF1}$ and connecting pullup resistors from SCL2 and SDA2 to $V_{DPU}$. Information on sizing the pullup resistors can be found in the *Sizing Pullup Resistors* section.

## 8.4 Device Functional Modes

| INPUT EN(1) | TRANSLATOR FUNCTION |
|---|---|
| H | Logic Lows are propagated from one side to the other, Logic Highs blocked (independent pull up resistors passively drive the line high) |
| L | Disconnect |

(1) The SCL switch conducts if EN is ≥ 0.6 V higher than SCL1 or SCL2. The same is true of SDA.


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# 9 Application and Implementation

**备注**

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## 9.1 Application Information

### 9.1.1 General Applications of $I^2C$

As with the standard $I^2C$ system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode $I^2C$ devices in addition to SMBus devices. Standard-mode $I^2C$ devices only specify 3 mA in a generic $I^2C$ system where standard-mode devices and multiple controllers are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by $V_{REF1}$. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain ($V_{DPU}$) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

## 9.2 Typical Application

图 9-1 and 图 9-2 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

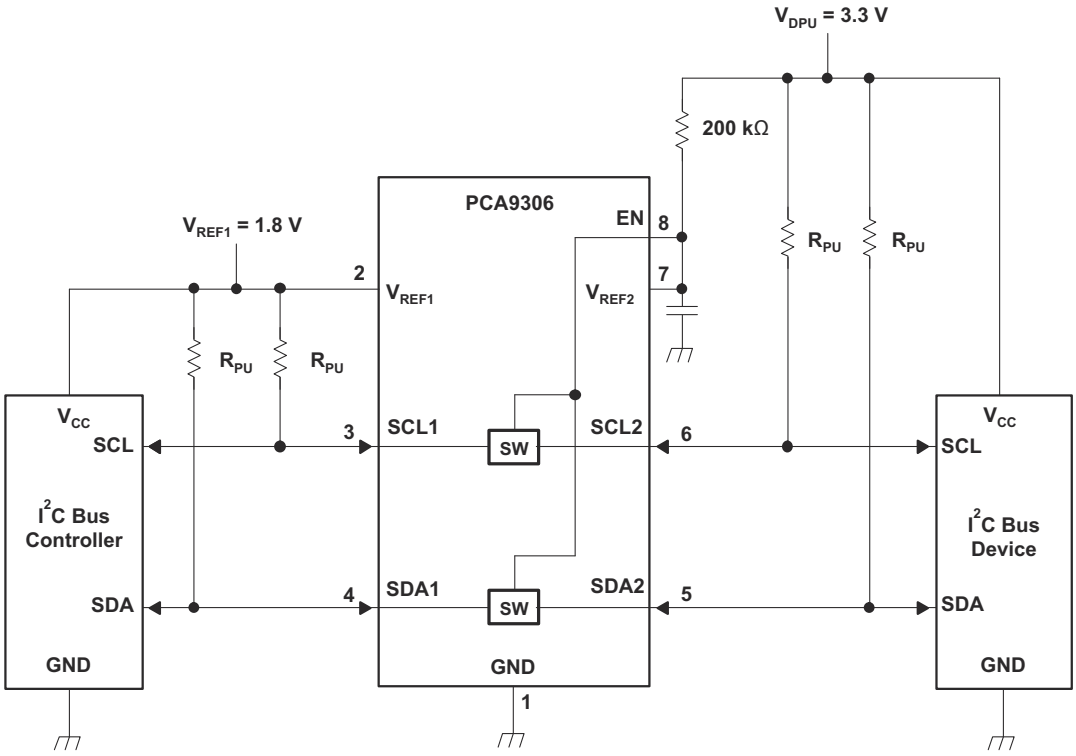



**图 9-1. Typical Application Circuit (Switch Always Enabled)**

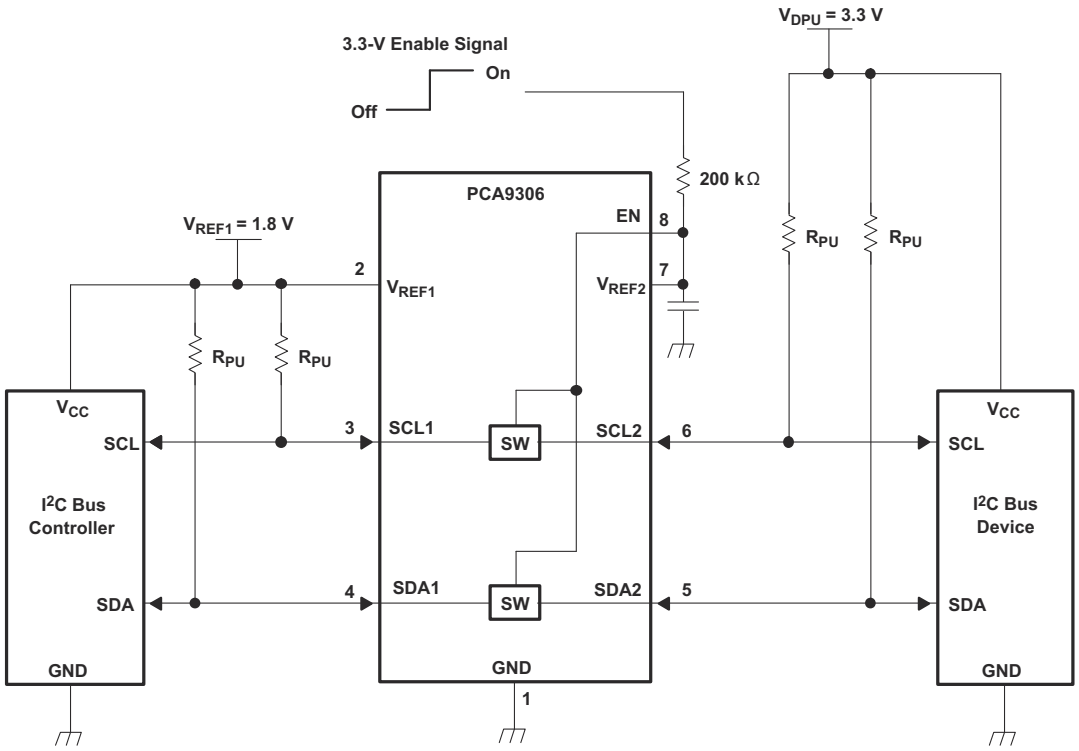



**图 9-2. Typical Application Circuit (Switch Enable Control)**

### 9.2.1 Design Requirements

| | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{REF2}$ | Reference voltage | $V_{REF1}$ + 0.6 | 2.1 | 5 | V |
| EN | Enable input voltage | $V_{REF1}$ + 0.6 | 2.1 | 5 | V |
| $V_{REF1}$ | Reference voltage | 1.2 | 1.5 | 4.4 | V |
| $I_{PASS}$ | Pass switch current | | 6 | | mA |
| $I_{REF}$ | Reference-transistor current | | 5 | | μA |

(1) All typical values are at $T_A$ = 25°C.

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Bidirectional Voltage Translation*

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to $V_{REF2}$ and both pins pulled to high-side $V_{DPU}$ through a pullup resistor (typically 200 kΩ). This allows $V_{REF2}$ to regulate the EN input. A 100-pF filter capacitor connected to $V_{REF2}$ is recommended. The $I^2C$ bus controller output can be push-pull or open-drain (pullup resistors may be required) and the $I^2C$ bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to $V_{DPU}$). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

#### *9.2.2.2 Sizing Pullup Resistors*

To get an estimate for the range of values that can be used for the pullup resistor, please refer to the application note SLVA689. 图 9-3 and 图 9-4 respectively show the maximum and minimum pullup resistance allowable by the $I^2C$ specification for standard-mode (100 kHz) and fast-mode (400 kHz) operation.


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#### 9.2.2.3 PCA9306 Bandwidth

The maximum frequency of the PCA9306 device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application.

图 6-3 shows a bandwidth measurement of the PCA9306 device using a two-port network analyzer.

However, this is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. As a rule of thumb, the frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the PCA9306 device, digital clock frequency of >100 MHz can be achieved.

The PCA9306 device does not provide any drive capability like the PCA9515 or PCA9517 series of devices. Therefore, higher-frequency applications require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the PCA9306 device is being driven by standard CMOS push-pull output driver. Ideally, it is best to minimize the trace length from the PCA9306 device on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum *practical* frequency component or the *knee* frequency ($f_{knee}$). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than $f_{knee}$ are insignificant in determining the shape of the signal.

To calculate $f_{knee}$:

$$f_{knee} = 0.5 / RT\ (10\% - 90\%) \quad (7)$$

$$f_{knee} = 0.4 / RT\ (20\% - 80\%) \quad (8)$$

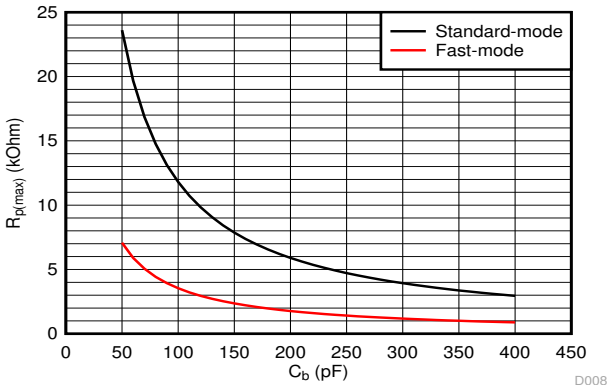
For signals with rise-time characteristics based on 10- to 90-percent thresholds, $f_{knee}$ is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20- to 80-percent thresholds, which is very common in many current device specifications, $f_{knee}$ is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that help maximize the performance of the device:

- Keep trace length to a minimum by placing the PCA9306 device close to the $I^2C$ output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

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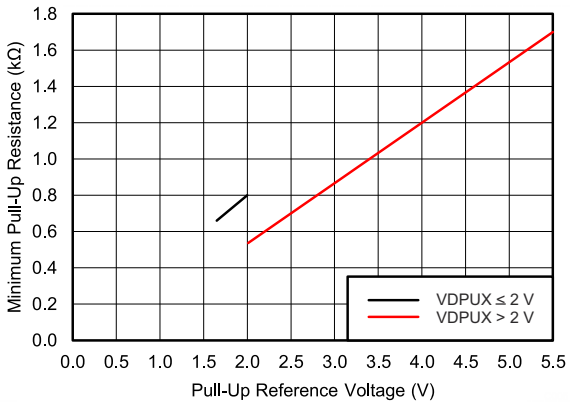
### 9.2.3 Application Curve




Standard mode ($f_{SCL}$ = 100 kHz, $t_r$ = 1 μs)

Fast mode ($f_{SCL}$ = 400 kHz, $t_r$ = 300 ns)

**图 9-3. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance ($C_b$)**




$V_{OL}$ = 0.2 x $V_{DPUX}$ , $I_{OL}$ = 2 mA when $V_{DPUX}$ ⩽ 2 V

$V_{OL}$ = 0.4 V, $I_{OL}$ = 3 mA when $V_{DPUX}$ > 2 V

**图 9-4. Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage ($V_{DPUX}$)**


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## 10 Power Supply Recommendations

For supplying power to the PCA9306 device, the $V_{REF1}$ pin can be connected directly to a power supply. The $V_{REF2}$ pin must be connected to the $V_{DPU}$ power supply through a 200-kΩ resistor. Failure to have a high-impedance resistor between $V_{REF2}$ and $V_{DPU}$ results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the PCA9306 must have the EN and VREF2 pins shorted and then pulled up to $V_{DPU}$ through a high-impedance resistor.

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# 11 Layout

## 11.1 Layout Guidelines

For printed-circuit board (PCB) layout of the PCA9306 device, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for $I^2C$ signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor should be placed as close to $V_{REF2}$ as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-kΩ resistor results in longer turnon and turnoff times for the PCA9306 device. These best practices are shown in 图 11-1.

For the layout example provided in 图 11-1, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power ($V_{CC}$) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to $V_{CC}$ or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in 图 11-1.

## 11.2 Layout Example

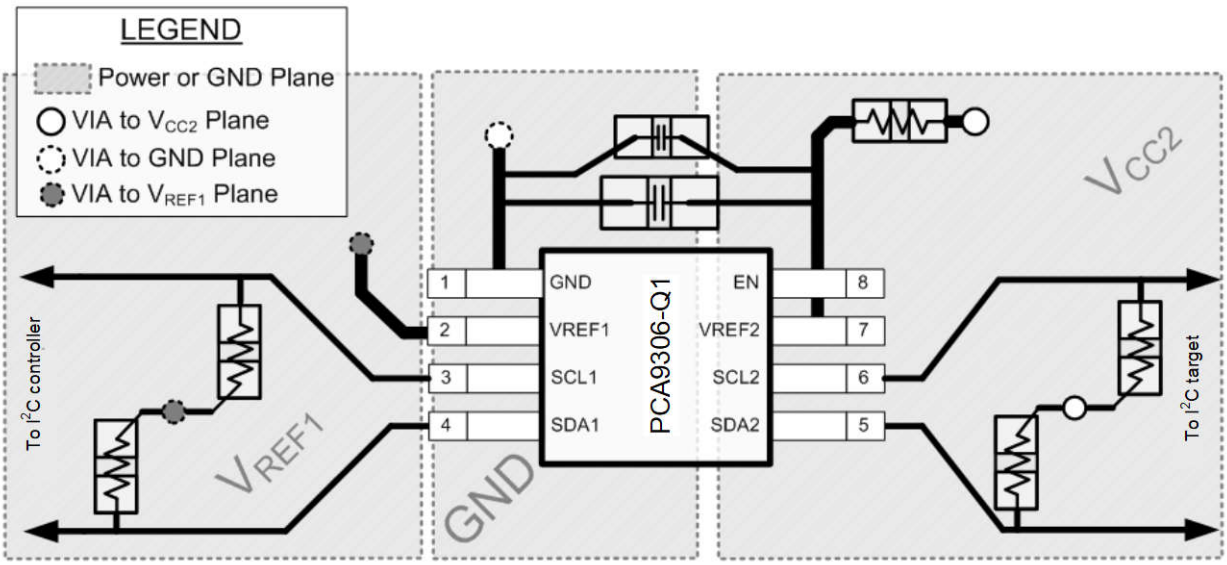



**图 11-1. PCA9306 Layout Example**


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# 12 Device and Documentation Support

## 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.2 支持资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PCA9306DCTR | Active | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 7BD (G, S, Y) |
| PCA9306DCTR.A | Active | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 7BD (G, S, Y) |
| PCA9306DCTT | Active | Production | SSOP (DCT) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 7BD (G, S, Y) |
| PCA9306DCTT.A | Active | Production | SSOP (DCT) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 7BD (G, S, Y) |
| PCA9306DCUR | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | (29O4, 7BDP, 7BDS, 7BDY) |
| PCA9306DCUR.A | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (29O4, 7BDP, 7BDS, 7BDY) |
| PCA9306DCUT | Active | Production | VSSOP (DCU) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | (29O4, 7BDP, 7BDS, 7BDY) |
| PCA9306DCUT.A | Active | Production | VSSOP (DCU) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (29O4, 7BDP, 7BDS, 7BDY) |
| PCA9306DQER | Active | Production | X2SON (DQE) \| 8 | 5000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (3M, 7F) |
| PCA9306DQER.A | Active | Production | X2SON (DQE) \| 8 | 5000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (3M, 7F) |
| PCA9306DQER.B | Active | Production | X2SON (DQE) \| 8 | 5000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (3M, 7F) |
| PCA9306YZTR | Active | Production | DSBGA (YZT) \| 8 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 7F |
| PCA9306YZTR.B | Active | Production | DSBGA (YZT) \| 8 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 7F |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF PCA9306 :**

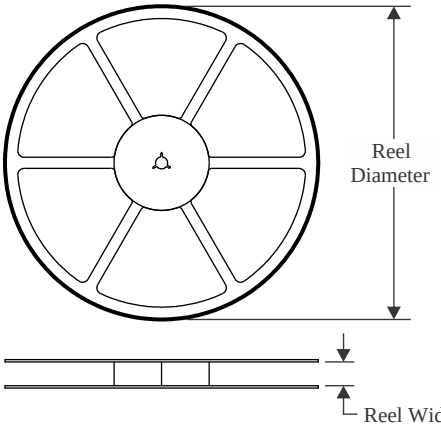
- Automotive : PCA9306-Q1

NOTE: Qualified Version Definitions:

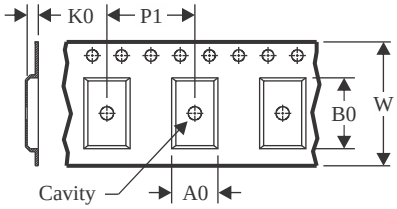
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

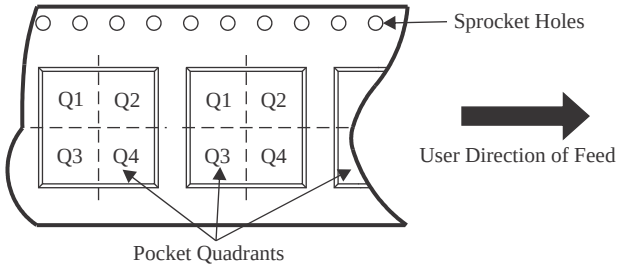



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

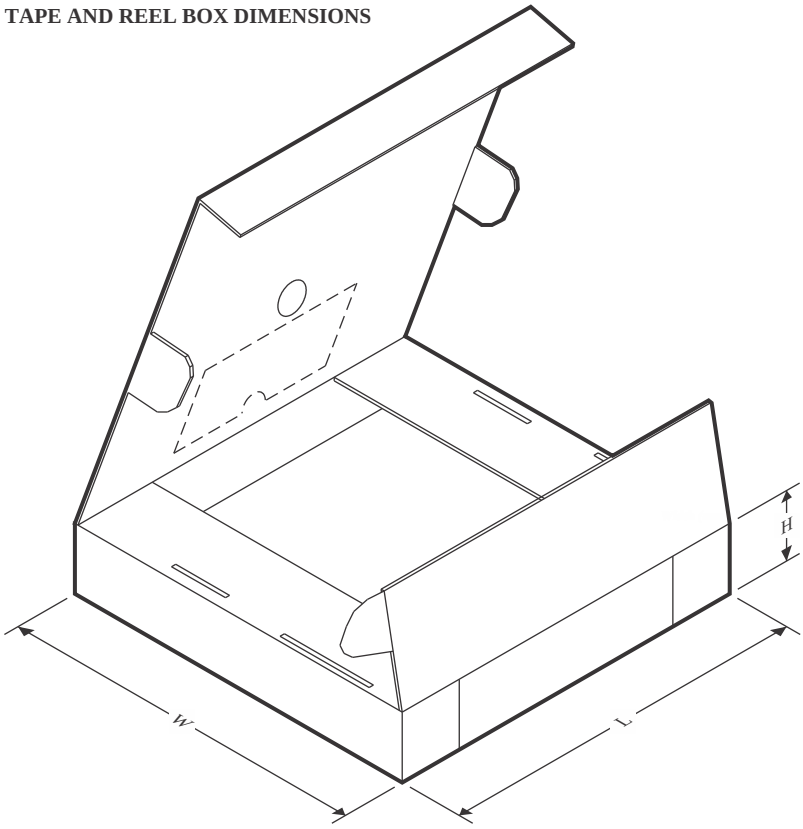
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCA9306DCTR | SSOP | DCT | 8 | 3000 | 177.8 | 12.4 | 3.45 | 4.4 | 1.45 | 4.0 | 12.0 | Q3 |
| PCA9306DCTT | SSOP | DCT | 8 | 250 | 177.8 | 12.4 | 3.45 | 4.4 | 1.45 | 4.0 | 12.0 | Q3 |
| PCA9306DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.0 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| PCA9306DCUT | VSSOP | DCU | 8 | 250 | 178.0 | 9.0 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| PCA9306DQER | X2SON | DQE | 8 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.5 | 4.0 | 8.0 | Q1 |
| PCA9306YZTR | DSBGA | YZT | 8 | 3000 | 180.0 | 8.4 | 1.02 | 2.02 | 0.75 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

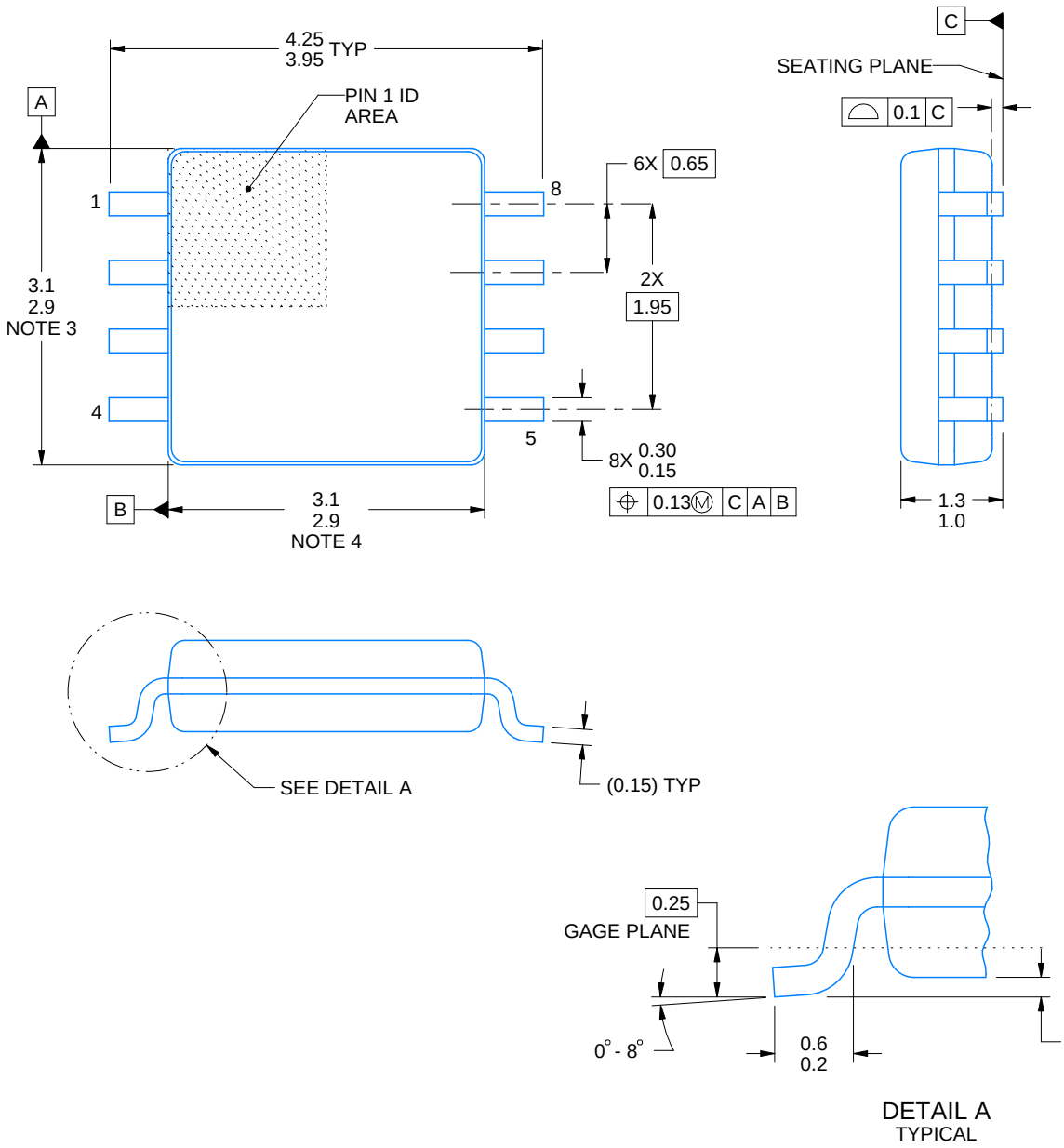
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PCA9306DCTR | SSOP | DCT | 8 | 3000 | 183.0 | 183.0 | 20.0 |
| PCA9306DCTT | SSOP | DCT | 8 | 250 | 183.0 | 183.0 | 20.0 |
| PCA9306DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 180.0 | 18.0 |
| PCA9306DCUT | VSSOP | DCU | 8 | 250 | 180.0 | 180.0 | 18.0 |
| PCA9306DQER | X2SON | DQE | 8 | 5000 | 184.0 | 184.0 | 19.0 |
| PCA9306YZTR | DSBGA | YZT | 8 | 3000 | 182.0 | 182.0 | 20.0 |

# PACKAGE OUTLINE

## DCT0008A

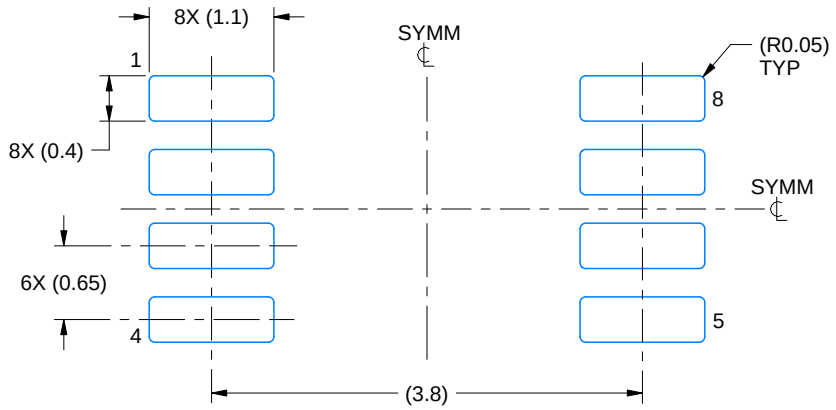
## SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE

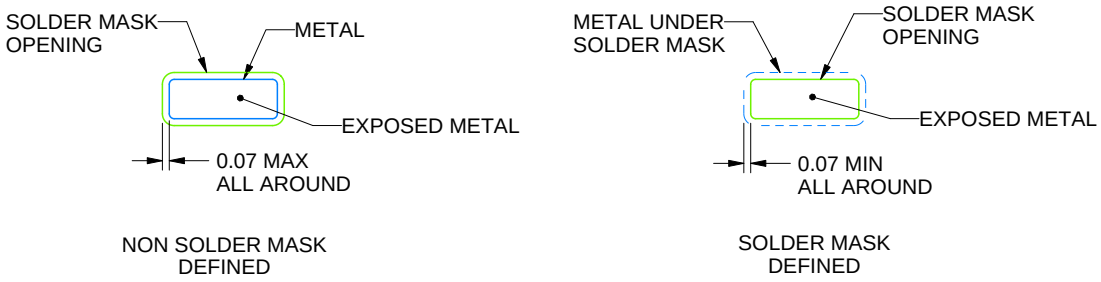



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

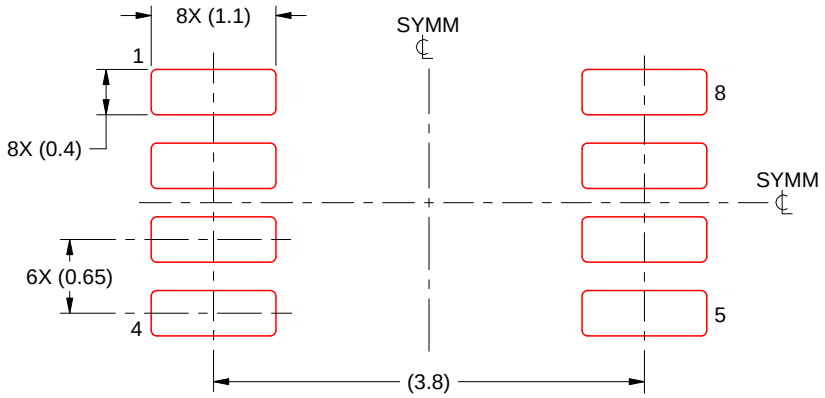



SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

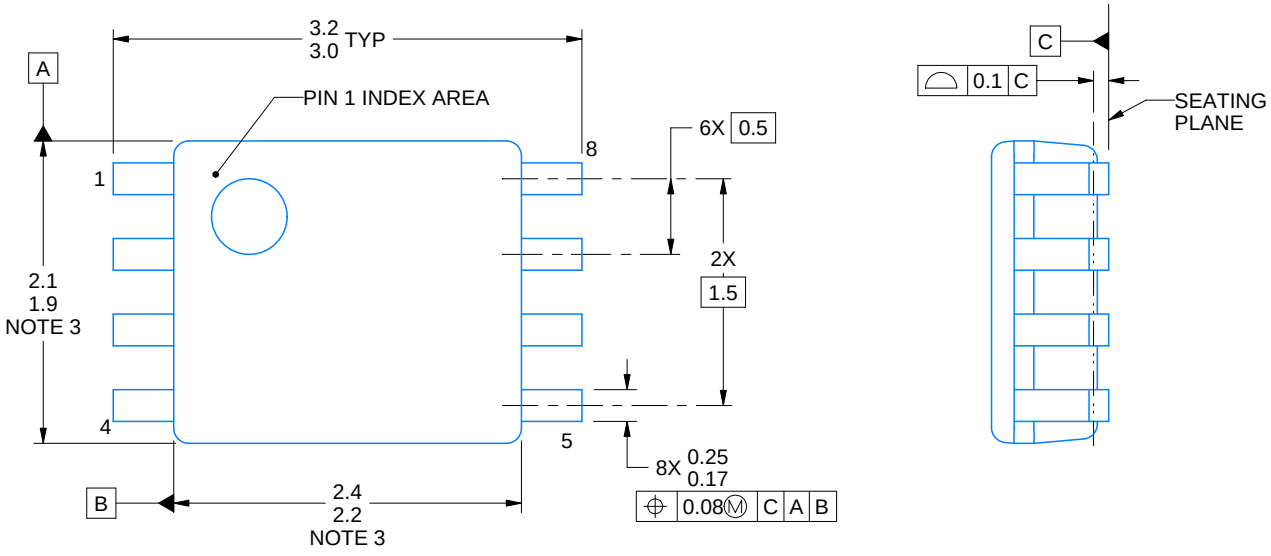
# DCU0008A

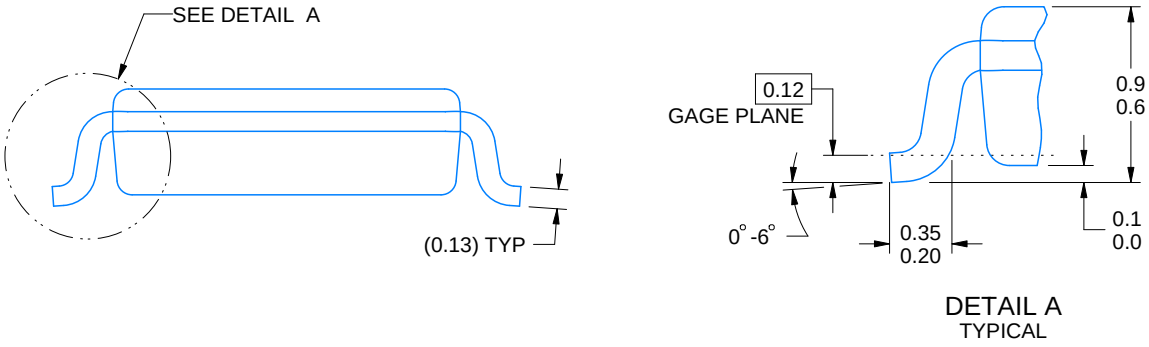


# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

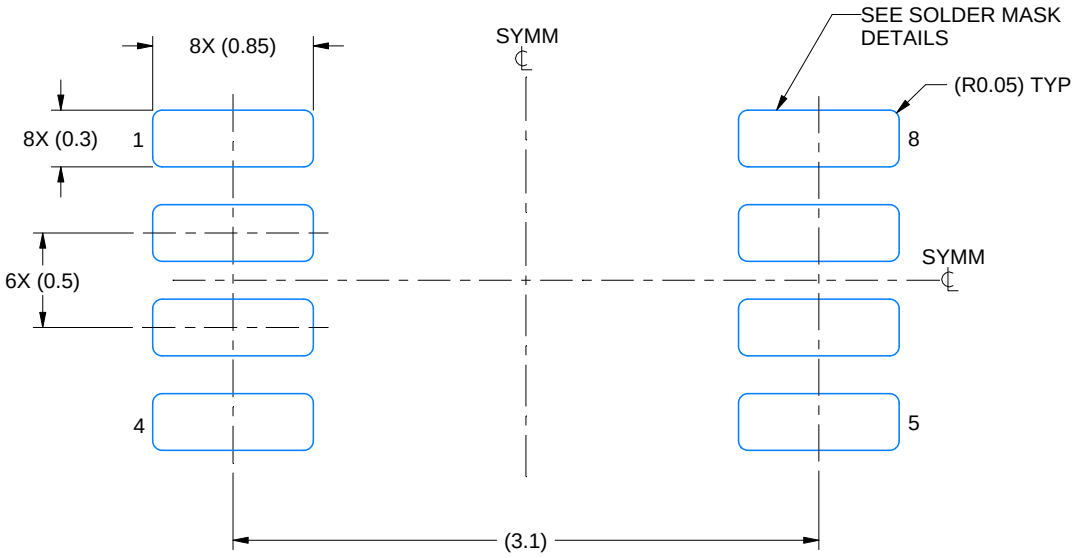


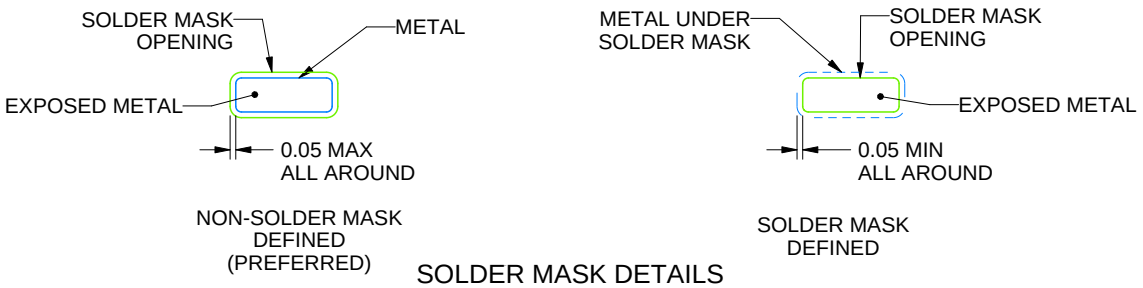

4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

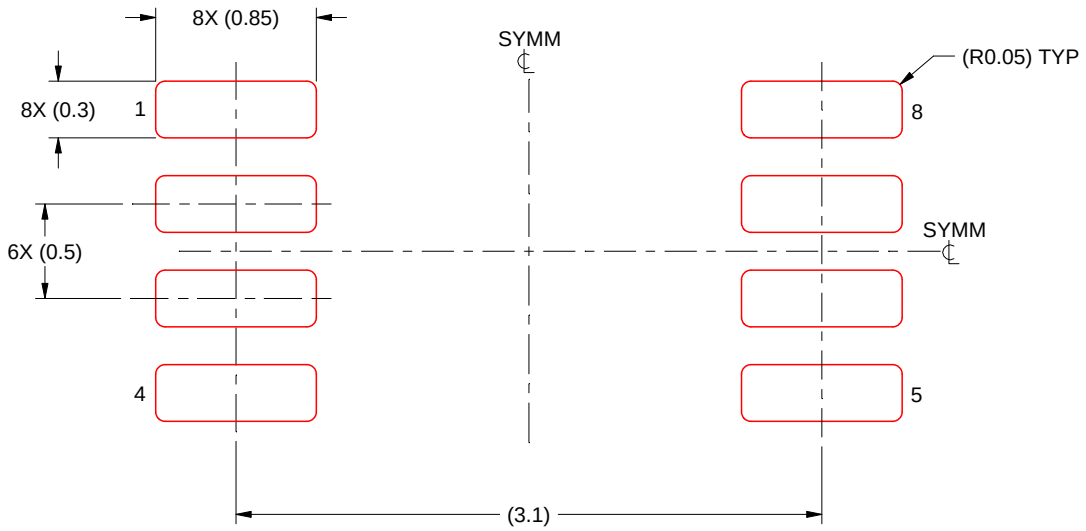



SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

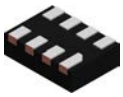
4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

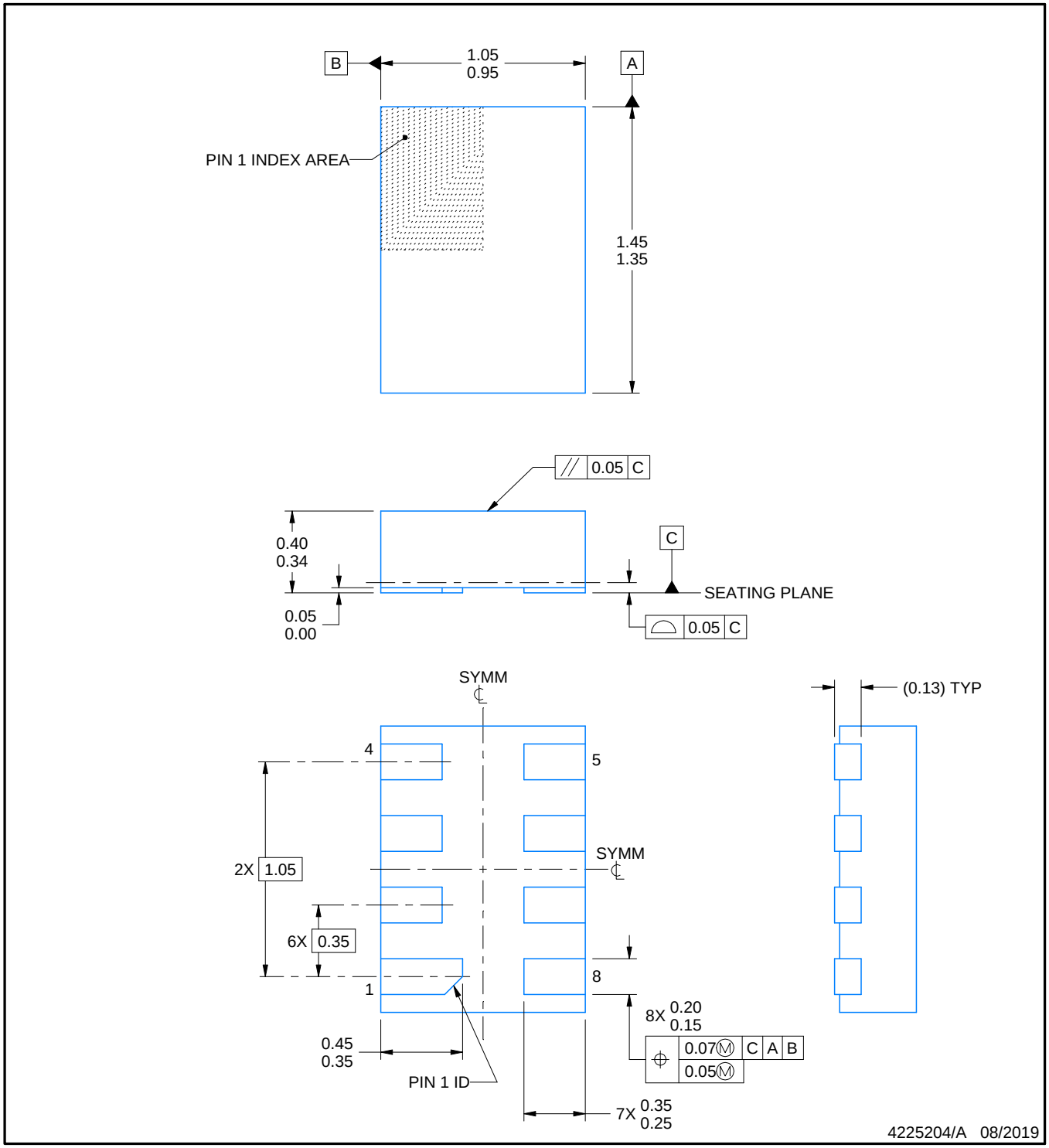
# PACKAGE OUTLINE

## DQE0008A



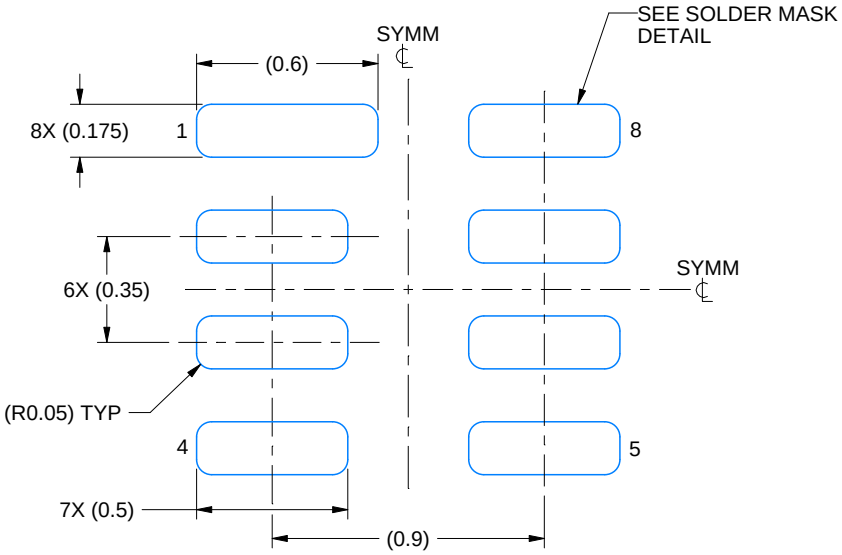
## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

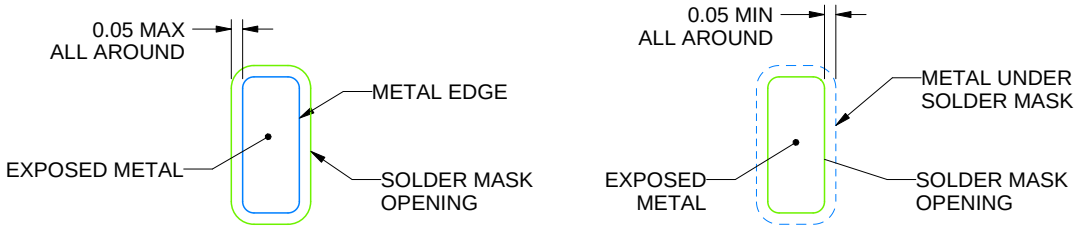



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

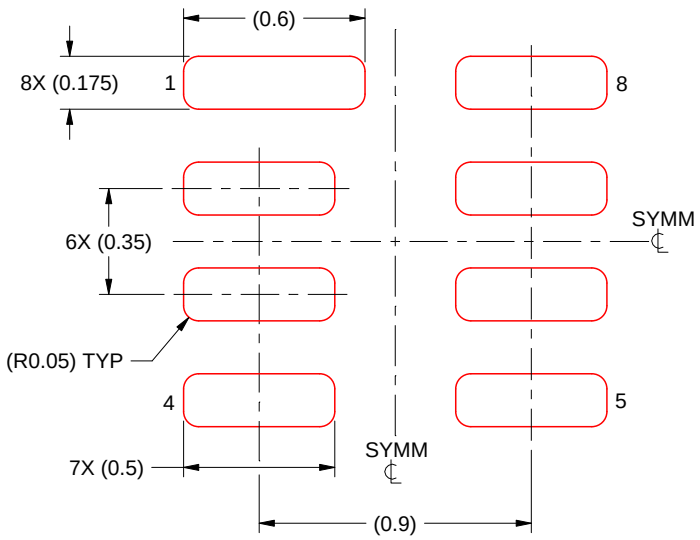



SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



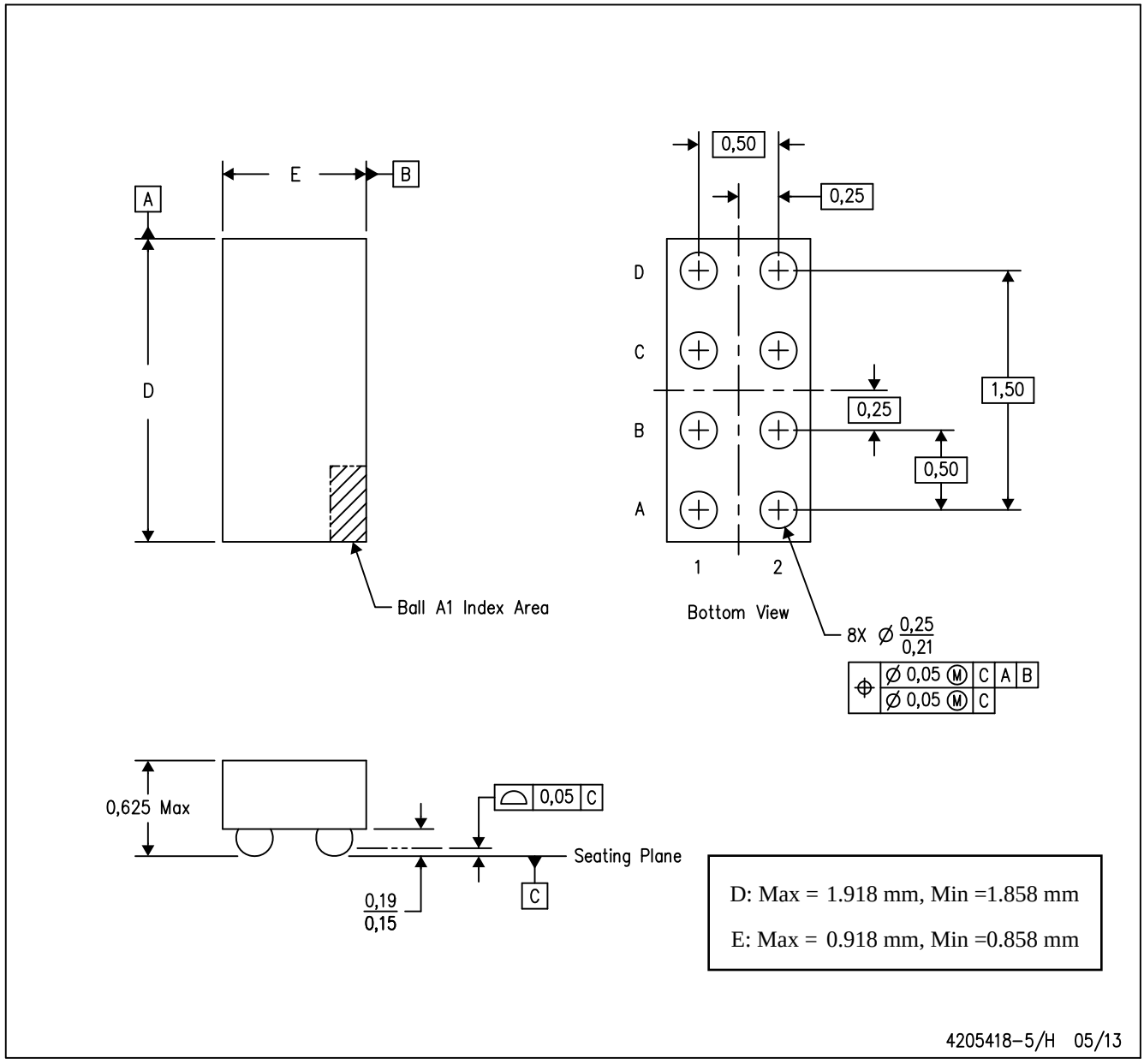

SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YZT (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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最后更新日期：2025 年 10 月