REF70 2ppm/°C 最大漂移、0.23ppm$_{p-p}$ 1/f 噪声精密电压基准

1 特性

- 低噪声支持精确测量：
  - 1/f 噪声（0.1Hz 至 10Hz）：0.23ppm$_{p-p}$
  - 10Hz 至 1kHz：0.35ppm$_{rms}$
- 低温度漂移系数：
  - 2ppm/°C（最大值，-40°C 至 125°C）
- 高准确度：±0.025%（最大值）
- 耐湿密封陶瓷封装 (LCCC)
- 出色的长期稳定性（1000 小时）：35ppm
- 低压降：400mV
- 适用于多种应用：
  - 高达 18V 的宽输入电压
  - 输出电流：±10mA
  - 电压选项：1.25V、2.5V、3V、3.3V、4.096V、5V
- 超灵活的解决方案：
  - 与 1µF 至 100µF 输出的低 ESR 电容器搭配使用时可保持稳定
  - 高 PSRR：1kHz 时为 107dB
  - 工作温度范围：−40°C 至 +125°C

2 应用

- 半导体测试设备
- 精密数据采集系统
- 精密称重秤
- 超声波扫描仪
- X 射线系统
- 工业仪表
- PLC 模拟 I/O 模块
- 现场发送器
- 电源监控

3 说明

REF70 是一系列高精度串联电压基准，具有业内超低的噪声 (0.23ppm$_{p-p}$)、非常低的温度漂移系数 (2ppm/°C) 和高精度 (±0.025%)。REF70 提供高 PSRR、低压降以及出色的负载和线路调节功能，有助于满足严格的瞬态要求。这种精度和特性的组合专门为测试和测量等应用而设计，这些应用需要与精密基准精确配对，并需要高分辨率数据转换器，例如 ADS8900B、ADS127L01 和 DAC11001A，从而在信号链中实现出色的性能。REF70 还适用于对噪声敏感的医疗应用，例如超声波和 X 射线，以帮助实现模拟前端的低噪声测量。

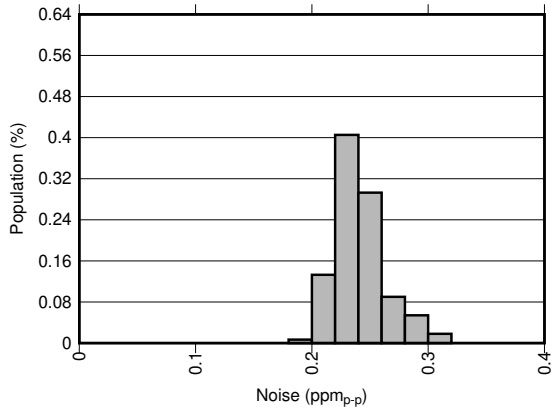
REF70 系列提供 VSSOP 和 LCCC 封装选项。LCCC (FKH) 封装是一种密封的陶瓷封装，可为需要长期稳定基准而无需校准的应用提供低的长期漂移。

REF70 可在 −40°C 至 +125°C 的宽温度范围内运行。凭借宽的温度范围，器件可在各种工业应用中运行。

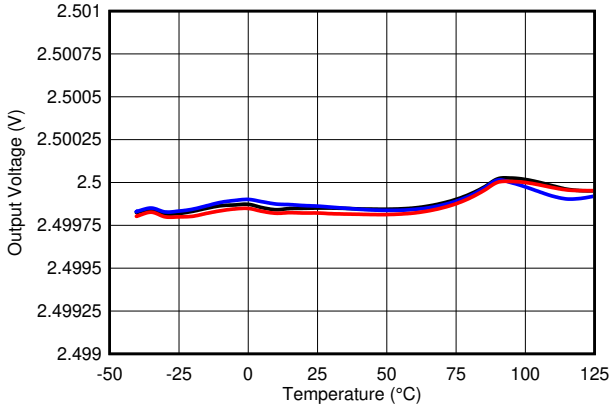
器件信息

器件名称	封装 (1)	封装尺寸（标称值）
REF70	LCCC (8)	5.00mm × 5.00mm
	VSSOP (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



0.1Hz 至 10Hz 电压噪声分布



输出电压与自然通风温度间的关系

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (March 2023) to Revision G (September 2023)	Page
• Update table to highlight REF7025 and REF7040 release in VSSOP package	4
• Added performance parameters for VSSOP package	8
• Added performance parameters for VSSOP package	11
• Changed 图 7-25 to longer duration (10000 hours)	15
• Added 图 7-27	15
• Changed 图 8-4 and 图 8-4, to longer duration (10000 hours)	21
• Changed 图 8-10, to highlight performance at different supply voltages	22
• Changed minimum ESR value from 10 mΩ to 1 mΩ	26
• Changed minimum ESR value from 10 mΩ to 1 mΩ	29

Changes from Revision E (July 2022) to Revision F (March 2023)	Page
• 向电压选项特性中添加换行符以提高可读性。	1
• 删除了 VSSOP 封装预发布脚注。	1
• Added footnote to indicate VSSOP package preview material	4
• Added performance parameters for VSSOP package	7
• Added performance graphs for VSSOP package devices	15
• Added solder shift histogram for VSSOP package	20
• Added long term stability details for VSSOP package	21
• Added thermal hysteresis details for VSSOP package	21
• Added layout details for VSSOP package	34

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Changes from Revision D (November 2021) to Revision E (July 2022) **Page**

- 根据文档反馈更新了“长期稳定性”特性文本，并根据执行的其他测试将数字从 28ppm 更新为 35ppm.....1
- 向“器件信息”表添加了针对 VSSOP 封装的脚注.....1
- Updated Long-term stability numbers to reflect latest evaluation results.....8
- Changed 图 7-25 to longer duration (4000 hours).....15
- Changed 图 8-4, to longer duration (4000 hours).....21

Changes from Revision C (September 2021) to Revision D (November 2021) **Page**

- Changed REF7012 status from Preproduction device to Released device.....4
- Changed REF7012 status to Released Device. Updated specifications to meet production release device.....7
- Added REF7030 Electrical Characteristics table.....9
- Added REF7033 Electrical Characteritics table.....10
- Added REF7012 Thermal Hysteresis figure.....15
- Added JEDEC standard details to follow for solder reflow profiles. Updated solder shift histogram plot.....20
- Added Thermal Hysteresis plots for REF7012 device 21

Changes from Revision B (April 2021) to Revision C (September 2021) **Page**

- 在第 1 页上向“特性”中添加了 1.25V 型号.....1
- In the Device Comparison Table, added the 1.25V variant and added foot notes to indicate which devices are released vs pre-production 4
- Changed Dropout voltage to min VIN = 2.75 V for VOUT < 2.5 V. 6
- Added Electrical Characteristics table for REF7012 (Product Preview).....7
- Changed V_{INMIN} from 3 V to V_{OUT} + V_{DO} 8
- Added Electrical Characteristics table for REF7040 (Product Preview).....11
- Added Electrical Characteristics table for REF7050 (Product Preview).....13
- Added to the notes above the Typical Characteristics plots, Vref = 2.5 V to the default conditions.....15
- Under Temperature Drift section of the Parameter Measurement Information, corrected the figure from Long Term Drift plot to Temperature Drift.....25

Changes from Revision A (December 2020) to Revision B (April 2021) **Page**

- 在标题和器件信息中将 REF7025 更改为更通用的 REF70 系列添加了 ADC 配套产品.....1
- Changed Figures 7-2 and 7-20, *Long-Term Stability (First 1000 Hours)*, to longer duration (2000 hours).....15
- Corrected typical shift from 0.021% to 0.009%.....20
- Changed Figure 8-3, *Long-Term Stability LCCC -1000 hours)*, to longer duration (2000 hours).....21
- Corrected Figure 8-5, *Thermal Hysteresis Distribution Cycle 2 (-40°C to 125°C)*, data and title.....21
- Reordered figures and paragraphs for better flow.....24
- Changed V_{REF} to $V_{REF(25°C)}$ in Equation 2.....25
- Added missing supply bypass capacitor value (10- µ F).....26
- Clarified piezoelectric contribution to noise and added links to resources.....29
- Added clarification on how to connect OUTF and OUTS in specific load current condition.....30
- Corrected part numbers and added links in Table 10-2, *Reference Op Amp Options* 31

Changes from Revision * (October 2020) to Revision A (December 2020) **Page**

- APL 到 RTM 发布.....1

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5 Device Comparison Table

PRODUCT		V_{OUT}
LCC package	VSSOP package	
REF7012QFKHT (1)	REF7012QDGKR (1)	1.25 V
REF7025QFKHT (1)	REF7025QDGKR (1)	2.5 V
REF7030QFKHT (1)	REF7030QDGKR 2	3.0 V
REF7033QFKHT (1)	REF7033QDGKR 2	3.3 V
REF7040QFKHT (1)	REF7040QDGKR (1)	4.096 V
REF7050QFKHT (1)	REF7050QDGKR 2	5.0 V

(1) This orderable is released to market.
(2) Samples available for the orderable upon request.

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6 Pin Configuration and Functions

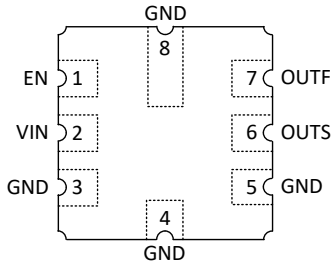


图 6-1. FKH Package
8-Pin LCCC
Top View

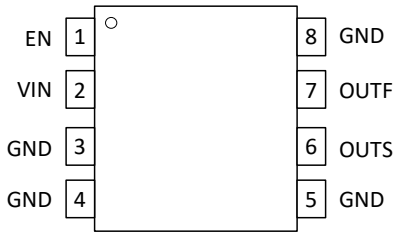


图 6-2. DGK Package
8-Pin VSSOP
Top View

表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	FKH	DGK		
EN	1	1	Input	Device enable control. Low level input disables the reference output and device enters shutdown mode. Device can be enabled by driving voltage > 1.6V. If the pin is left floating, the internal pull up will enable the device.
VIN	2	2	Power	Input supply voltage connection. Connect a minimum 0.1- μ F decoupling capacitor to ground for the best performance.
GND	3	3	Ground	Ground connection.
GND	4	4	Ground	Ground connection.
GND	5	5	Ground	Ground connection
OUTS	6	6	Input	Reference voltage output sense connection.
OUTF	7	7	Output	Reference voltage output force connection. Connect a output capacitor between 1- μ F to 100- μ F for the best performance.
GND	8	8	Ground	Ground connection.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	20	V
Enable voltage	EN	-0.3	VIN + 0.3	V
Output voltage	V_{OUT}	-0.3	6	V
Output short circuit current	I_{SC}		25	mA
Operating temperature range	T_A	-55	150	°C
Storage temperature range	T_{stg}	-65	170	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	± 1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input voltage	V_{OUT} + V_{DO} (1)		18	V
EN	Enable voltage	0		VIN	V
I_L	Output current	– 10		10	mA
T_A	Operating temperature	– 40	25	125	°C

(1) V_{DO} = Dropout voltage. For V_{OUT} < 2.5 V minimum VIN = 2.75 V

7.4 Thermal Information

THERMAL METRIC(1)		REF70xx		UNIT
		FKH (CERAMIC)	DGK (MSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.8	201.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.0	85.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.3	122.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	48.2	21.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.1	121.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	28.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 REF7012 Electrical Characteristics

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = 3 V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.025		0.025	%
	Output voltage accuracy	T_A = 25°C; DGK package		–0.05		0.05	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C				2	ppm/℃
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 85°C; DGK package				2	ppm/℃
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C; DGK package				4.2	ppm/℃
LINE AND LOAD REGULATION							
ΔV_O / ΔV_{IN}	Line regulation	2.75 V ≤ V_{IN} ≤ 18 V			4		ppm/V
		2.75 V ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C				30	
ΔV_O / ΔI_L	Load regulation	I_L = 0 mA to 10mA			5		ppm/mA
		I_L = 0 mA to 10mA, –40°C ≤ T_A ≤ 125°C				15	
		I_L = 0 mA to –10mA			15		
		I_L = 0 mA to –10mA, –40°C ≤ T_A ≤ 125°C				30	
NOISE							
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz			0.25		ppm_{p-p}
e_n	Output voltage noise	f = 10 Hz to 1 kHz			0.35		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 250h at 35°C – FKH package			15		ppm
		0 to 1000h at 35°C – FKH package			35		
	Long-term stability	0 to 250h at 35°C – DGK package			27		ppm
		0 to 1000h at 35°C – DGK package			37		
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – FKH package			18		ppm
		25°C, –40°C, 85°C, 25°C – FKH package			11		
		25°C, 0°C, 70°C, 25°C – FKH package			11		
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – DGK package			410		ppm
		25°C, –40°C, 85°C, 25°C – DGK package			35		
		25°C, 0°C, 70°C, 25°C – DGK package			33		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	–40℃ ≤ T_A ≤ 125℃		0.1			µF
C_{OUT}	Stable output capacitor range (1)	–40℃ ≤ T_A ≤ 125℃		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			2.75		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		4	6.5	mA
		–40°C ≤ T_A ≤ 125°C				7.5	mA
		T_A = 25°C	Shutdown mode		5	10	uA
		–40°C ≤ T_A ≤ 125°C				12	uA

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7.5 REF7012 Electrical Characteristics（续）

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = 3 V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{EN}	Enable pin voltage	Active mode (EN=1)	1.6			V
		Shutdown mode (EN=0)			0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18V		3.2	4	uA
		V_{IN} = V_{EN} = 18V, –40°C ≤ T_A ≤ 125°C			5	uA
I_{SC}	Short circuit current	V_{OUT} = 0V		30		mA

(1) ESR for the capacitor can range from 1 mΩ to 400 mΩ

7.6 REF7025 Electrical Characteristics

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	T_A = 25°C	–0.025		0.025	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C			2	ppm/℃
LINE AND LOAD REGULATION						
ΔV_O / ΔV_{IN}	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V		4		ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C			30	
ΔV_O / ΔI_L	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}		5		ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			10	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}		5		
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			15	
NOISE						
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz		0.23		ppm_{p-p}
e_n	Output voltage noise	f = 10 Hz to 1 kHz		0.35		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY						
	Long-term stability	0 to 250h at 35°C - FKH package		15		ppm
		0 to 1000h at 35°C - FKH package		35		
	Long-term stability	0 to 250h at 35°C – DGK package		35		ppm
		0 to 1000h at 35°C – DGK package		75		ppm
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – FKH package		180		ppm
		25°C, –40°C, 85°C, 25°C – FKH package		100		
		25°C, 0°C, 70°C, 25°C – FKH package		40		
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – DGK package		290		ppm
		25°C, –40°C, 85°C, 25°C – DGK package		50		
		25°C, 0°C, 70°C, 25°C – DGK package		45		
TURN ON TIME						
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF		0.5		ms
CAPACITIVE LOAD						

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7.6 REF7025 Electrical Characteristics（续）

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
C_{IN}	Stable input capacitor range	–40℃ ≤ T_A ≤ 125℃		0.1			µF
C_{OUT}	Stable output capacitor range (1)	–40℃ ≤ TA ≤ 125℃		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		4	6	mA
		–40°C ≤ T_A ≤ 125°C				6.5	mA
		T_A = 25°C	Shutdown mode		5	10	uA
		–40°C ≤ T_A ≤ 125°C				12	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18V			3.2	4	uA
		V_{IN} = V_{EN} = 18V, –40°C ≤ T_A ≤ 125°C				5	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C				250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C				400	mV
I_{SC}	Short circuit current	V_{OUT} = 0V			25		mA

(1) ESR for the capacitor can range from 1 mΩ to 400 mΩ

7.7 REF7030 Electrical Characteristics

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	T_A = 25°C	–0.025		0.025	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C			2	ppm/℃
LINE AND LOAD REGULATION						
ΔV_O / ΔV_{IN}	Line regulation	3.2 V ≤ V_{IN} ≤ 18 V		4		ppm/V
		3.2 V ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C			30	
ΔV_O / ΔI_L	Load regulation	I_L = 0 mA to 10mA, V_{IN} = 3.5 V		5		ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = 3.5 V, –40°C ≤ T_A ≤ 125°C			10	
		I_L = 0 mA to –10mA, V_{IN} = 3.5 V		5		
		I_L = 0 mA to –10mA, V_{IN} = 3.5 V, –40°C ≤ T_A ≤ 125°C			15	
NOISE						
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz		0.23		ppm_{p-p}
e_n	Output voltage noise	f = 10 Hz to 1 kHz		0.35		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY						
	Long-term stability	0 to 250h at 35°C - FKH package		15		ppm
		0 to 1000h at 35°C - FKH package		35		

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7.7 REF7030 Electrical Characteristics（续）

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – FKH package			180		ppm
		25°C, –40°C, 85°C, 25°C – FKH package			100		
		25°C, 0°C, 70°C, 25°C – FKH package			40		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	–40℃ ≤ T_A ≤ 125℃		0.1			µF
C_{OUT}	Stable output capacitor range (1)	–40℃ ≤ T_A ≤ 125℃		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		4	6	mA
		–40°C ≤ T_A ≤ 125°C				7	mA
		T_A = 25°C	Shutdown mode		5	10	uA
		–40°C ≤ T_A ≤ 125°C				12	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18V			3.2	4	uA
		V_{IN} = V_{EN} = 18V, –40°C ≤ T_A ≤ 125°C				5	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C				250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C				400	mV
I_{SC}	Short circuit current	V_{OUT} = 0V			25		mA

(1) ESR for the capacitor can range from 1 mΩ to 400 mΩ

7.8 REF7033 Electrical Characteristics

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	T_A = 25°C	–0.025		0.025	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C			2	ppm/℃
LINE AND LOAD REGULATION						
ΔV_O / ΔV_{IN}	Line regulation	3.5 V ≤ V_{IN} ≤ 18 V		4		ppm/V
		3.5 V ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C			30	
ΔV_O / ΔI_L	Load regulation	I_L = 0 mA to 10mA, V_{IN} = 3.8 V		5		ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = 3.8 V, –40°C ≤ T_A ≤ 125°C			10	
		I_L = 0 mA to –10mA, V_{IN} = 3.8 V		5		
		I_L = 0 mA to –10mA, V_{IN} = 3.8 V, –40°C ≤ T_A ≤ 125°C			15	

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7.8 REF7033 Electrical Characteristics（续）

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
NOISE							
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz			0.23		ppm_{p-p}
e_n	Output voltage noise	f = 10 Hz to 1 kHz			0.35		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 250h at 35°C - FKH package			15		ppm
		0 to 1000h at 35°C - FKH package			35		
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – FKH package			180		ppm
		25°C, –40°C, 85°C, 25°C – FKH package			100		
		25°C, 0°C, 70°C, 25°C – FKH package			40		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	–40℃ ≤ T_A ≤ 125℃		0.1			µF
C_{OUT}	Stable output capacitor range (1)	–40℃ ≤ T_A ≤ 125℃		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		4	6	mA
		–40°C ≤ T_A ≤ 125°C				7	mA
		T_A = 25°C	Shutdown mode		5	10	uA
		–40°C ≤ T_A ≤ 125°C				12	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18V			3.2	4	uA
		V_{IN} = V_{EN} = 18V, –40°C ≤ T_A ≤ 125°C				5	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C				250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C				400	mV
I_{SC}	Short circuit current	V_{OUT} = 0V			25		mA

(1) ESR for the capacitor can range from 1 mΩ to 400 mΩ

7.9 REF7040 Electrical Characteristics

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	T_A = 25°C	–0.025		0.025	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C			2	ppm/℃
LINE AND LOAD REGULATION						

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7.9 REF7040 Electrical Characteristics（续）

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
$\Delta V_O / \Delta V_{IN}$	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V			4		ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C				30	
$\Delta V_O / \Delta I_L$	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}			5		ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C				10	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}			5		
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C				15	
NOISE							
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz			0.23		ppm_{p-p}
e_n	Output voltage noise	f = 10 Hz to 1 kHz			0.35		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 250h at 35°C - FKH package			15		ppm
		0 to 1000h at 35°C - FKH package			35		
	Long-term stability	0 to 250h at 35°C – DGK package			35		ppm
		0 to 1000h at 35°C – DGK package			75		
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – FKH package			180		ppm
		25°C, –40°C, 85°C, 25°C – FKH package			100		
		25°C, 0°C, 70°C, 25°C – FKH package			40		
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C (cycle 1) – DGK package			290		ppm
		25°C, –40°C, 85°C, 25°C (cycle 1) – DGK package			50		
		25°C, 0°C, 70°C, 25°C (cycle 1) – DGK package			45		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	–40℃ ≤ T_A ≤ 125℃		0.1			µF
C_{OUT}	Stable output capacitor range (1)	–40℃ ≤ T_A ≤ 125℃		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		4	6	mA
		–40°C ≤ T_A ≤ 125°C				6.5	mA
		T_A = 25°C	Shutdown mode		5	10	uA
		–40°C ≤ T_A ≤ 125°C				12	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18V			3.2	4	uA
		V_{IN} = V_{EN} = 18V, –40°C ≤ T_A ≤ 125°C				5	uA

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7.9 REF7040 Electrical Characteristics（续）

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C			250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C			400	mV
I_{SC}	Short circuit current	V_{OUT} = 0V		25		mA

(1) ESR for the capacitor can range from 1 mΩ to 400 mΩ

7.10 REF7050 Electrical Characteristics

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	T_A = 25°C	–0.025		0.025	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C			2	ppm/℃
LINE AND LOAD REGULATION						
ΔV_O / ΔV_{IN}	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V		4		ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C			30	
ΔV_O / ΔI_L	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}		5		ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			10	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}		5		
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			15	
NOISE						
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz		0.23		ppm_{p-p}
e_n	Output voltage noise	f = 10 Hz to 1 kHz		0.35		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY						
	Long-term stability	0 to 250h at 35°C - FKH package		15		ppm
		0 to 1000h at 35°C - FKH package		35		
	Output voltage hysteresis (cycle 1)	25°C, –40°C, 125°C, 25°C – FKH package		180		ppm
		25°C, –40°C, 85°C, 25°C – FKH package		100		
		25°C, 0°C, 70°C, 25°C – FKH package		40		
TURN ON TIME						
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF		0.5		ms
CAPACITIVE LOAD						
C_{IN}	Stable input capacitor range	–40℃ ≤ T_A ≤ 125℃	0.1			µF
C_{OUT}	Stable output capacitor range (1)	–40℃ ≤ T_A ≤ 125℃	1		100	µF
POWER SUPPLY						
V_{IN}	Input voltage		V_{OUT} + V_{DO}		18	V

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7.10 REF7050 Electrical Characteristics（续）

Specifications are tested at T_A = 25°C, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, V_{IN} = V_{OUT} + 0.5V, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
I_Q	Quiescent current	T_A = 25°C	Active mode		4	6	mA
		–40°C ≤ T_A ≤ 125°C				6.5	mA
		T_A = 25°C	Shutdown mode		5	10	uA
		–40°C ≤ T_A ≤ 125°C				12	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18V			3.2	4	uA
		V_{IN} = V_{EN} = 18V, –40°C ≤ T_A ≤ 125°C				5	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C				250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C				400	mV
I_{SC}	Short circuit current	V_{OUT} = 0V			25		mA

(1) ESR for the capacitor can range from 1 mΩ to 400 mΩ

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7.11 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_L = 10 μF, C_{IN} = 0.1 μF, V_{REF} = 2.5 V (unless otherwise noted)

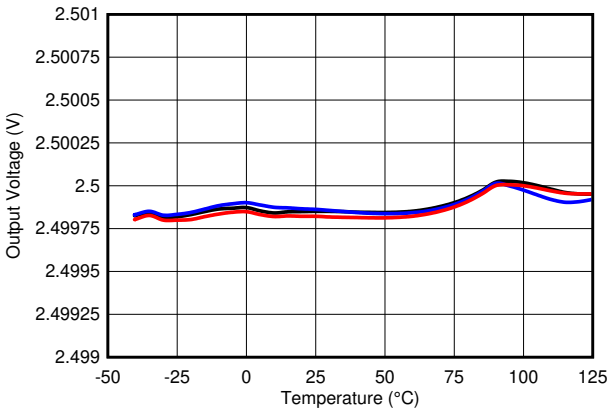


图 7-1. Output Voltage Vs Free-Air Temperature (REF7025QFKHR)

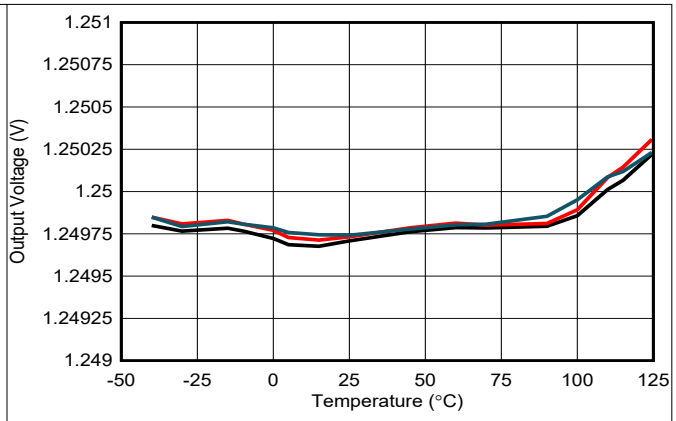


图 7-2. Output Voltage Vs Free-Air Temperature (REF7012QDGKR)

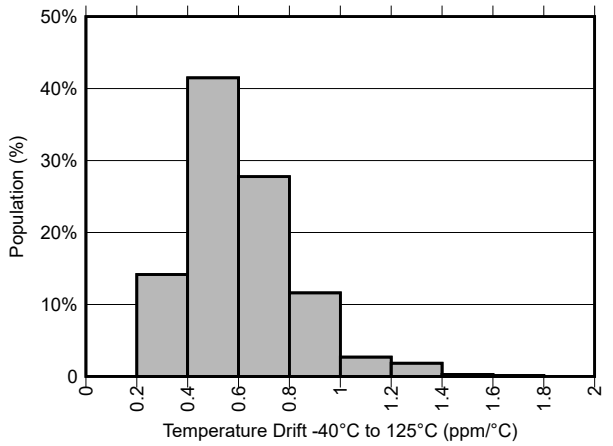


图 7-3. Temperature Drift Distribution (REF7025QFKHR)

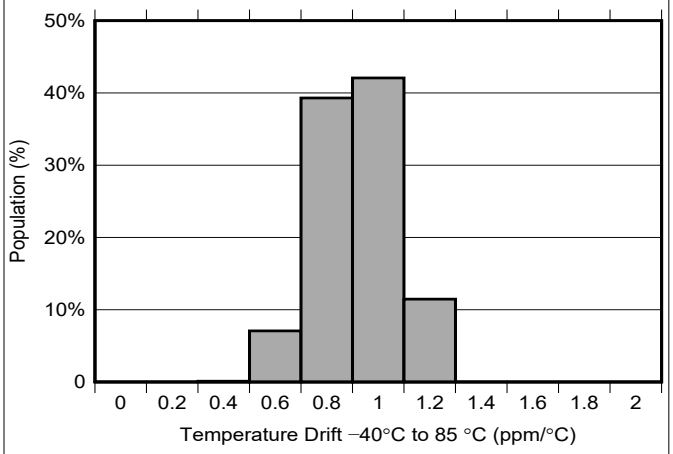


图 7-4. Temperature Drift Distribution (REF7012QDGKR)

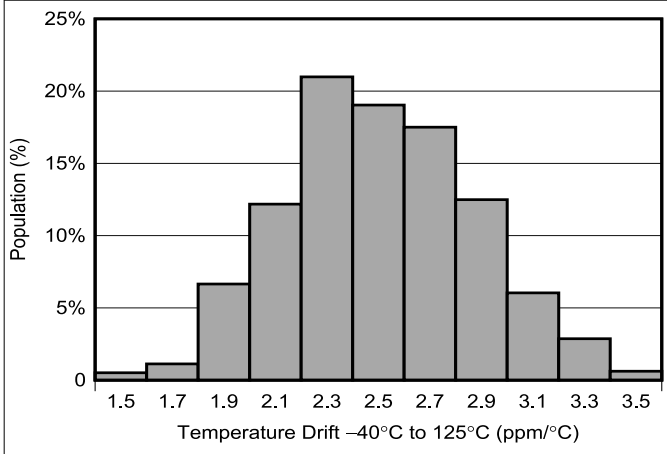


图 7-5. Temperature Drift Distribution (REF7012QDGKR)

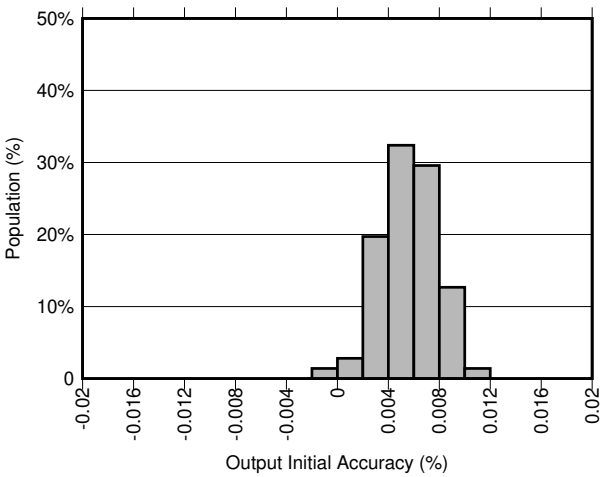


图 7-6. Accuracy Distribution (REF7025QFKHR)

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7.11 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF, V_{REF} = 2.5 V (unless otherwise noted)

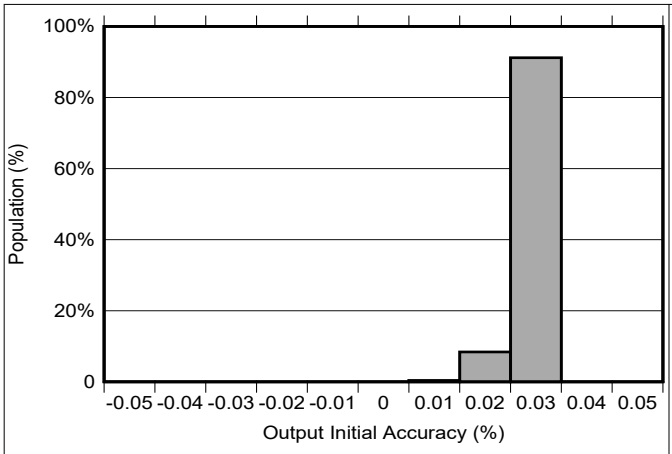


图 7-7. Accuracy Distribution (REF7012QDGKR)

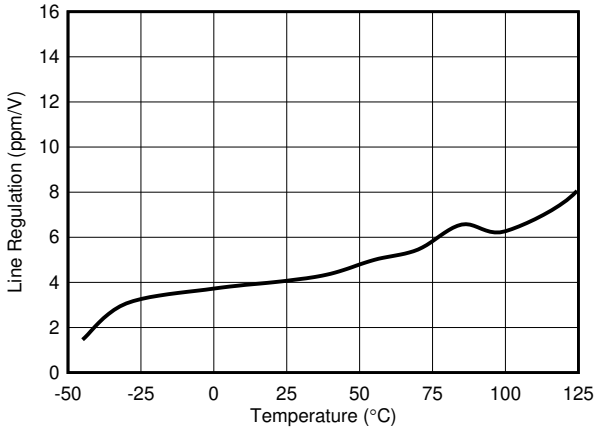


图 7-8. Line Regulation vs Temperature

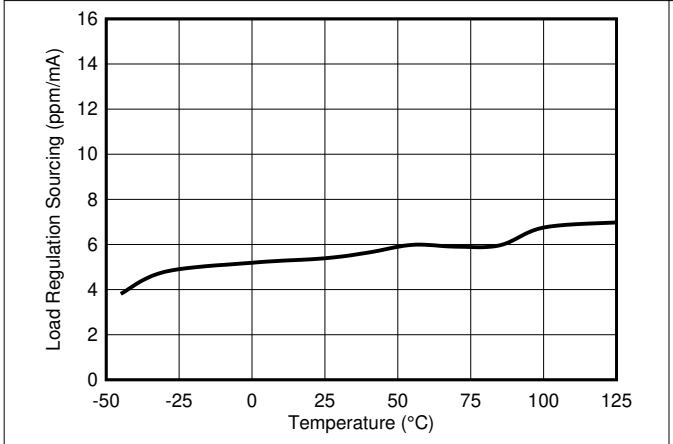


图 7-9. Load Regulation (Sourcing) vs Temperature

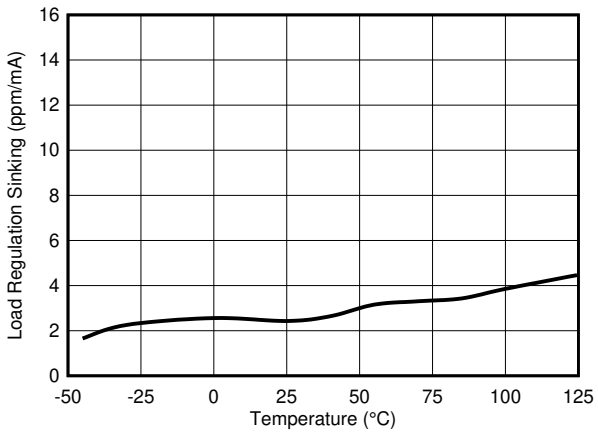


图 7-10. Load Regulation (Sinking) vs Temperature

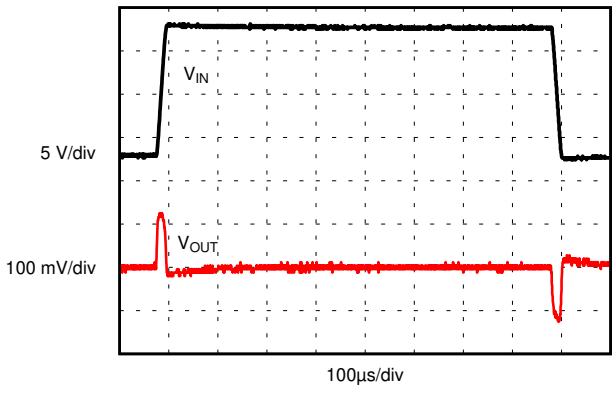


图 7-11. Line Regulation Response

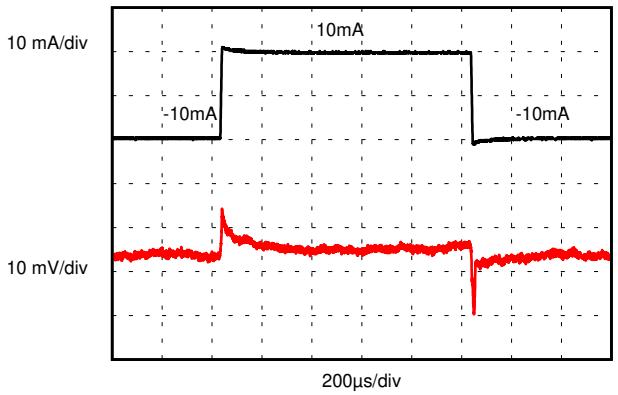


图 7-12. Load Transient Response (C_L = 1 µF)

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7.11 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF, V_{REF} = 2.5 V (unless otherwise noted)

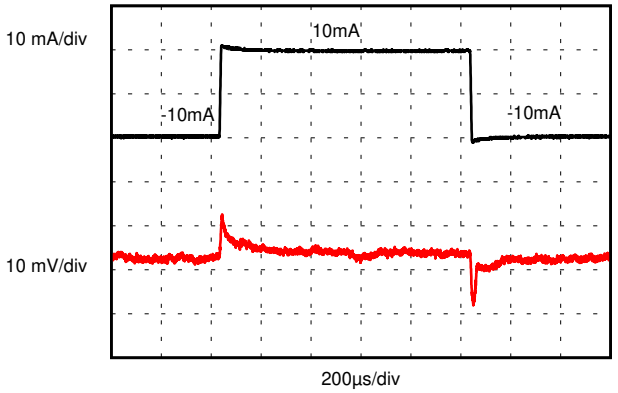


图 7-13. Load Transient Response (C_L = 10 µF)

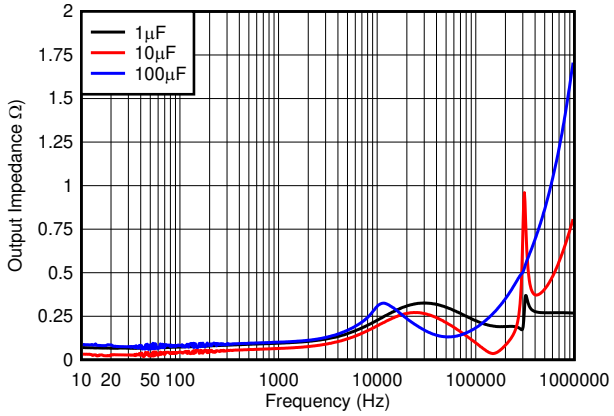


图 7-14. Output Impedance

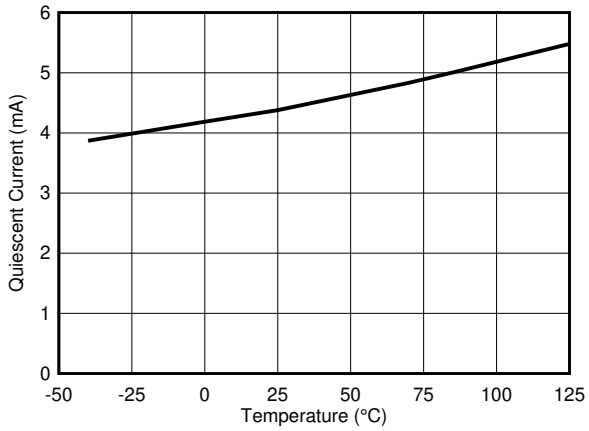


图 7-15. Quiescent Current vs Temperature

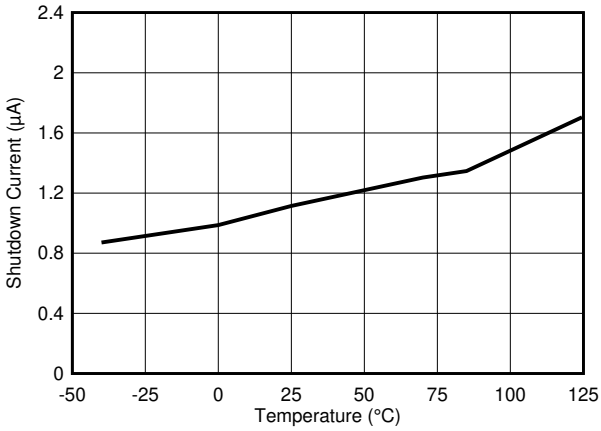


图 7-16. Shutdown Current vs Temperature

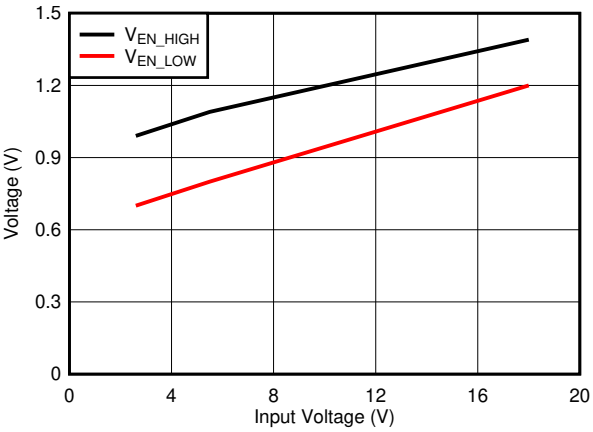


图 7-17. Enable Threshold vs V_{IN}

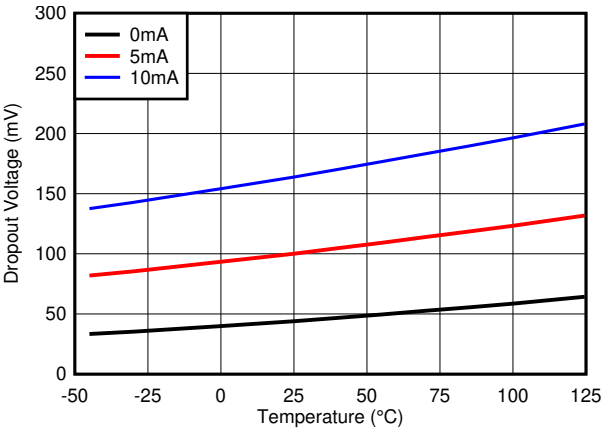


图 7-18. Dropout Voltage vs Temperature

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7.11 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF, V_{REF} = 2.5 V (unless otherwise noted)

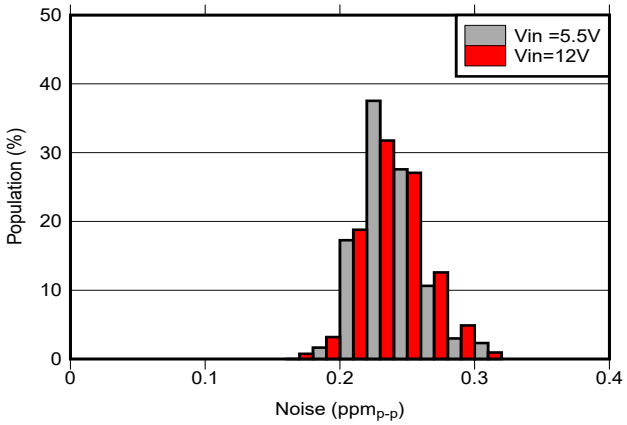


图 7-19. 0.1-Hz to 10-Hz Voltage Noise Distribution (300 units)

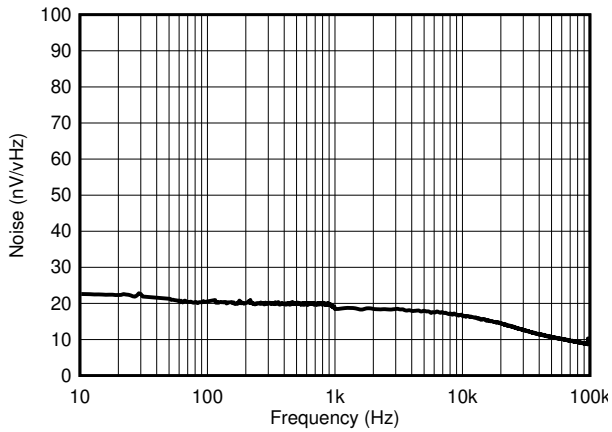


图 7-20. Noise Performance 10 Hz to 100 kHz

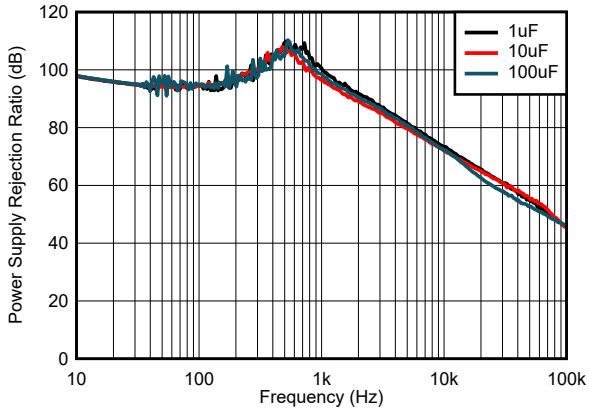


图 7-21. Power-Supply Rejection Ratio vs Frequency

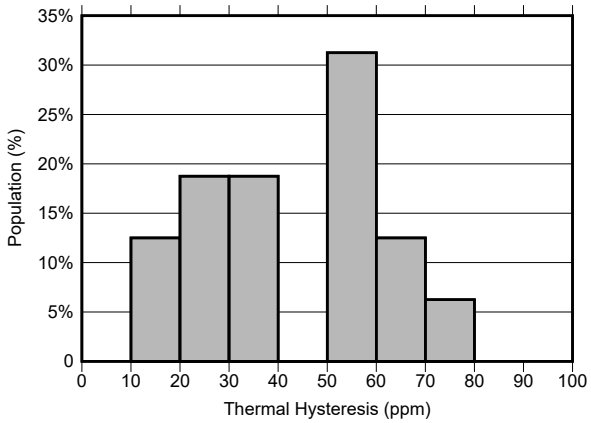


图 7-22. REF7025QFKHR Thermal Hysteresis Distribution (0°C to 70°C)

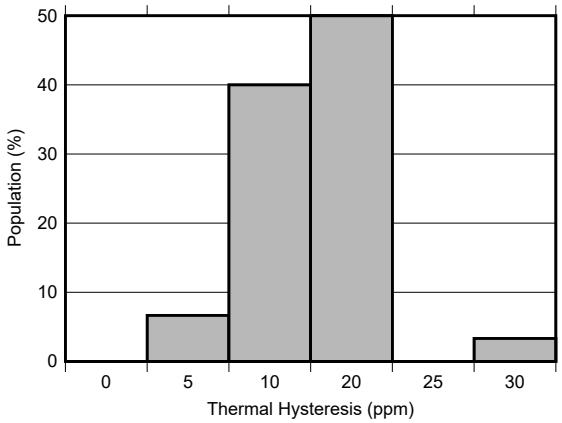


图 7-23. REF7012QFKHR Thermal Hysteresis Distribution (0°C to 70°C)

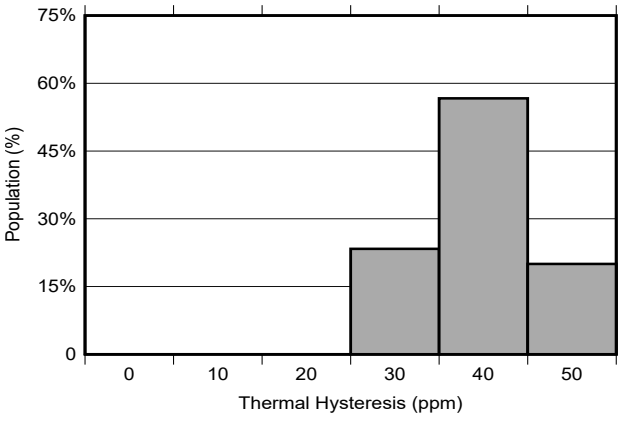


图 7-24. REF7012QDGKR Thermal Hysteresis Distribution (0°C to 70°C)

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7.11 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_L = 10 μF, C_{IN} = 0.1 μF, V_{REF} = 2.5 V (unless otherwise noted)

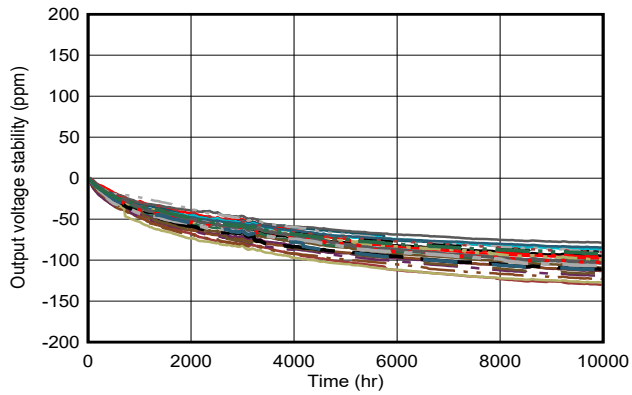


图 7-25. Long-Term Stability LCCC package (First 10000 Hours)

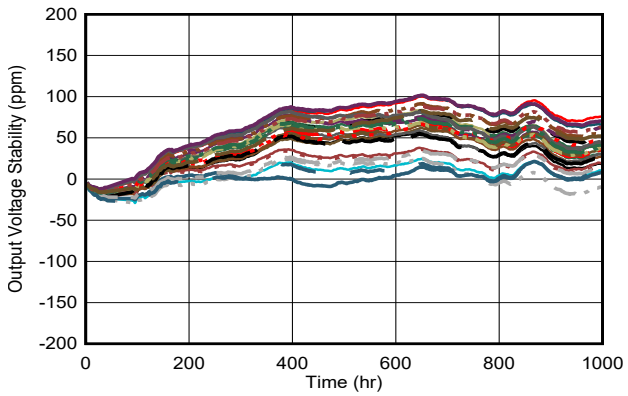


图 7-26. Long-Term Stability VSSOP package REF7012 (First 1000 Hours)

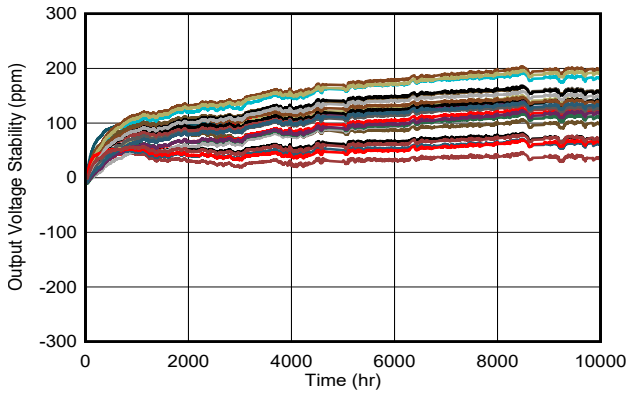


图 7-27. Long-Term Stability VSSOP package REF7025 (First 10000 Hours)

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF70 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated during soldering process. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error. In order to illustrate this effect, a total of 32 devices were soldered on two printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in 图 8-1. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm.

For recommended reflow profiles using 'Sn-Pb Eutectic Assembly' or 'Pb-Free Assembly' please refer JEDEC J-STD-020 standard.

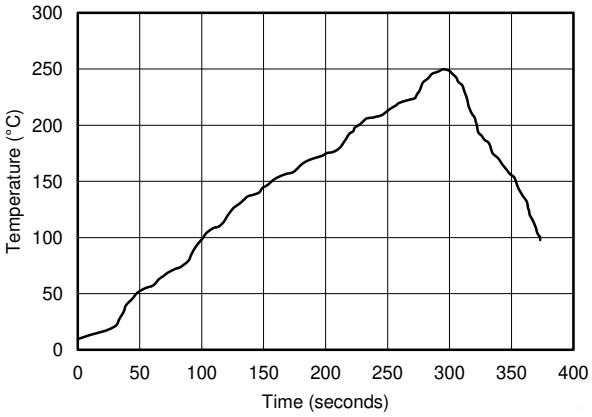


图 8-1. Reflow Profile

The reference output voltage is measured before and after the reflow process. Although all tested units exhibit very low shifts, higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the 图 8-2 and 图 8-3 display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize its exposure to thermal stress.

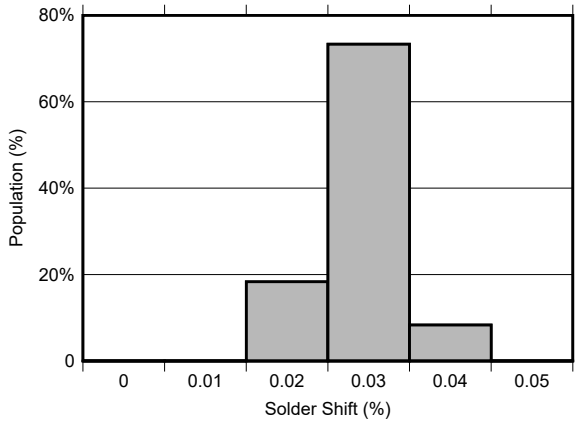


图 8-2. Solder Shift (LCCC Package)

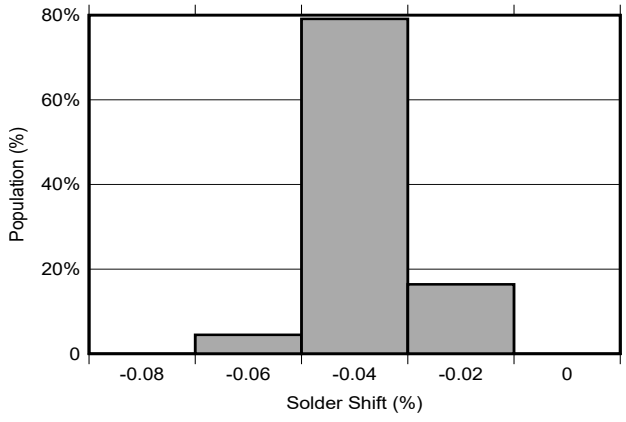


图 8-3. Solder Shift (VSSOP Package)

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8.2 Long-Term Stability

One of the key parameters of the REF70 references is long-term stability also known as long-term drift. The long-term stability value was tested in a typical setup that reflects standard PCB board manufacturing practices. The boards are made of standard FR4 material and the board does not have special cuts or grooves around the devices to relieve the mechanical stress of the PCB. The devices and boards in this test do not undergo high temperature burn in post-soldering prior to testing. These conditions reflect a real world use case scenario and common manufacturing techniques.

During the long-term stability testing, precautions are taken to ensure that only the long-term stability drift is being measured. The boards are maintained at 35°C in an oil bath. The oil bath ensures that the temperature is constant across the device over time compared to an air oven. The measurements are captured every 30 minutes with a calibrated 8.5 digit multimeter.

Typical long-term stability characteristic is expressed as a deviation over time. 图 8-4 shows the typical drift value for the REF70 in LCCC (FKH) package is 35 ppm from 0 to 1000 hours. It is important to understand that long-term stability is not ensured by design and that the value is typical. The REF70 will experience the highest drift in the initial 1000 hr. Subsequent deviation is typically lower than previous 1000 hr.

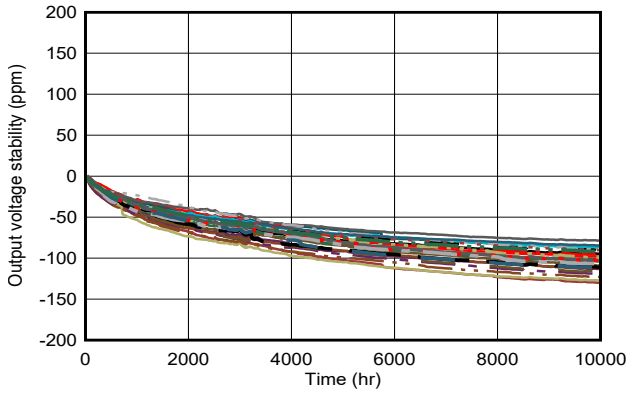


图 8-4. Long Term Stability LCCC -10000 hours (V_{OUT})

图 8-5 shows the typical drift value for the REF70 in VSSOP (DGK) package is 75 ppm from 0 to 1000 hours. It is important to understand that long-term stability is not ensured by design and that the value is typical. The REF70 will experience the highest drift in the initial 1000 hr.

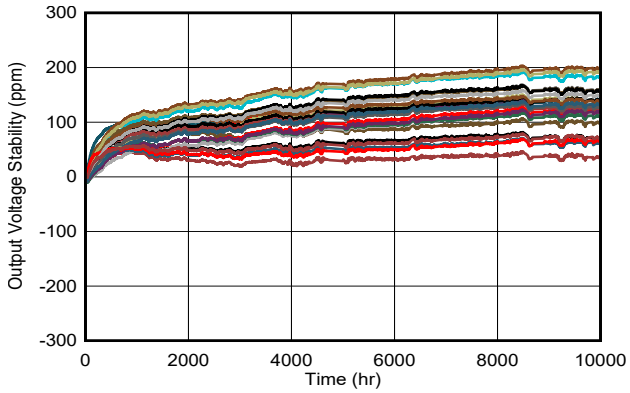


图 8-5. Long Term Stability VSSOP -10000 hours (V_{OUT})

8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF70 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling

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the device through the specified temperature range, and returning to 25°C. This can be seen in 图 8-6 to 图 8-8. Hysteresis can be expressed by 方程式 1:

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C.

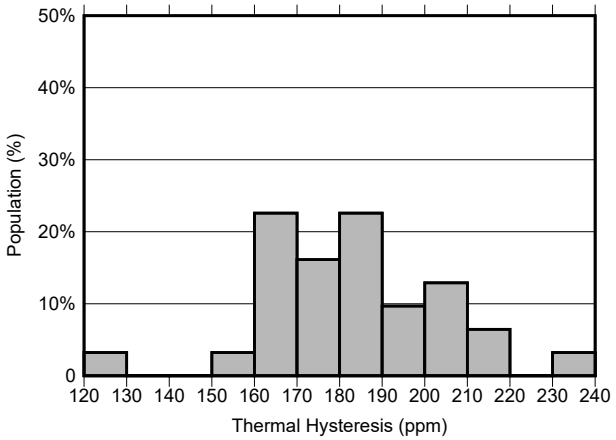


图 8-6. REF7025QFKHR Thermal Hysteresis Distribution (-40°C to 125°C)

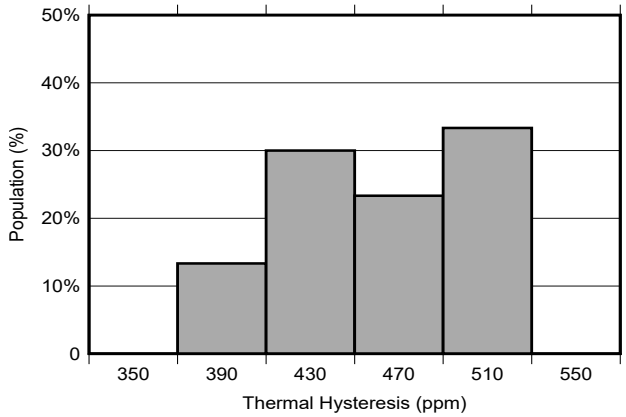


图 8-7. REF7012QDGKR Thermal Hysteresis Distribution (-40°C to 125°C)

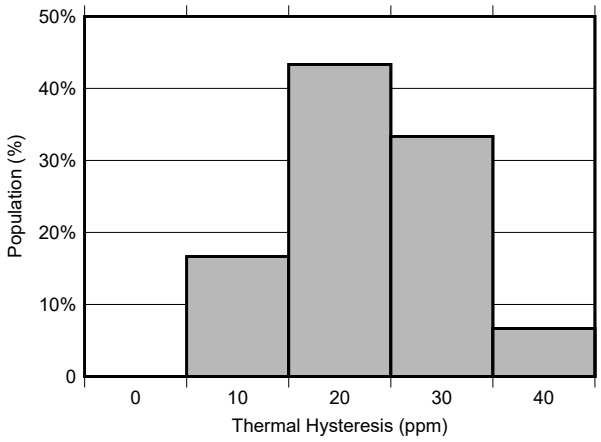


图 8-8. REF7012QFKHR Thermal Hysteresis Distribution (-40°C to 125°C)

8.4 Noise Performance

8.4.1 1/f Noise

1/f noise, also known as flicker noise, is a low frequency noise that affects the device output voltage which can affect precision measurements in ADCs. This noise increases proportionally with output voltage and operating temperature. It is measured by filtering the output from 0.1-Hz to 10-Hz. Since the 1/f noise is an extremely low

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value, the frequency of interest needs to be amplified and band-pass filtered. This is done by using a high-pass filter to block the DC voltage. The resulting noise is then amplified by a gain of 1000. The bandpass filter is created by a series of high-pass and low-pass filter that adds additional gain to make it more visible on a oscilloscope as shown in 图 8-9. 1/f noise must be tested in a Faraday cage enclosure to block environmental noise.

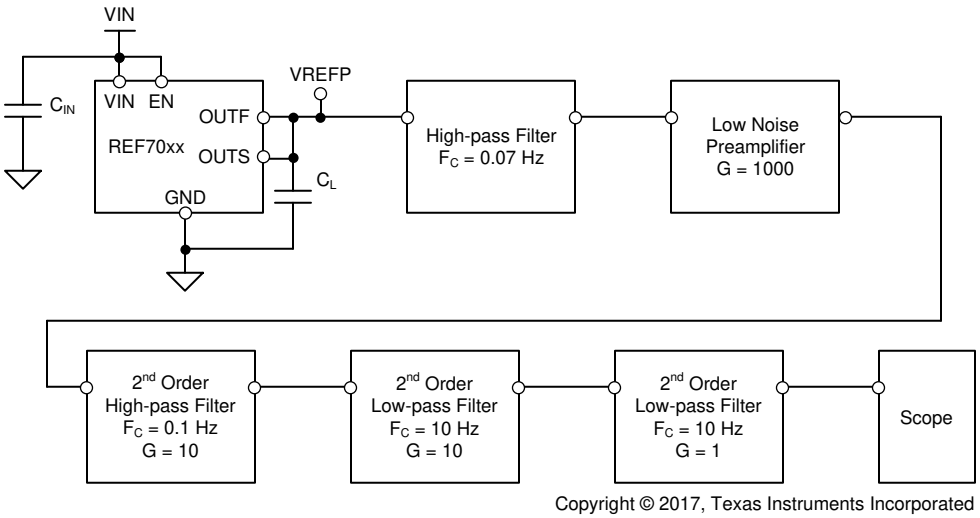


图 8-9. 1/f Noise Test Setup

Typical 1/f noise (0.1-Hz to 10-Hz) distribution can be seen in 图 8-10. The noise is measured at two different supply voltages. The REF70 noise performance is not impacted by supply voltage.

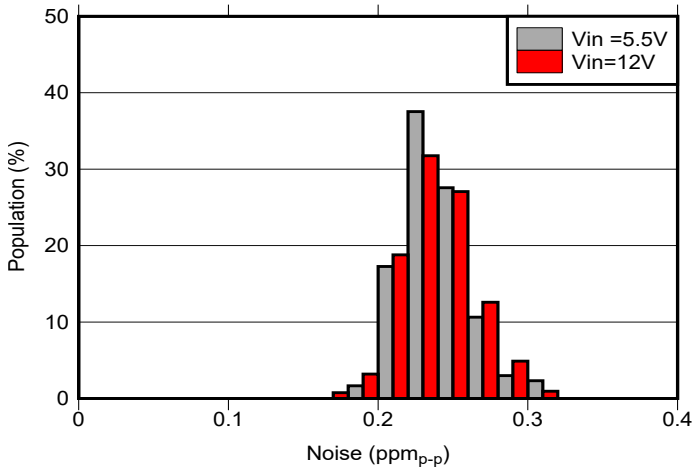


图 8-10. 0.1-Hz to 10-Hz Voltage Noise Distribution

The 1/f noise is in such a low frequency range that it is not practical to filter out which makes it a key parameter for ultra-low noise measurements. Noise sensitive designs must use the lowest 1/f noise for the highest precision measurements. 图 8-11 shows the effect of 1/f noise over 10s.

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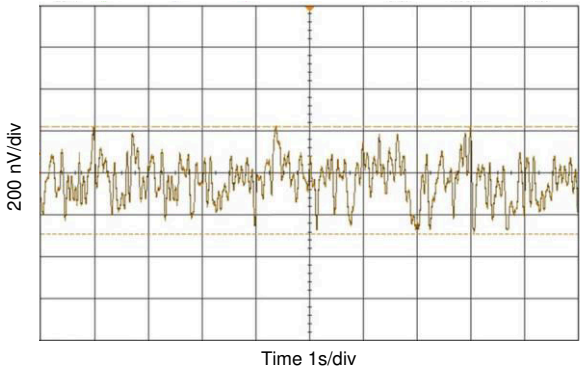


图 8-11. 0.1-Hz to 10-Hz Voltage Noise

8.4.2 Broadband Noise

Broadband noise is a noise that appears at higher frequency compared to 1/f noise. The broadband noise is usually flat and uniform over frequency as shown in 图 8-13. The broadband noise is measured by high-pass filtering the output of the REF70 and measuring the result on a spectrum analyzer as shown in 图 8-12. The DC component of the REF70 is removed by using a high-pass filter and then amplified. When measuring broadband noise, it is not necessary to have high gain in order to achieve maximum bandwidth.

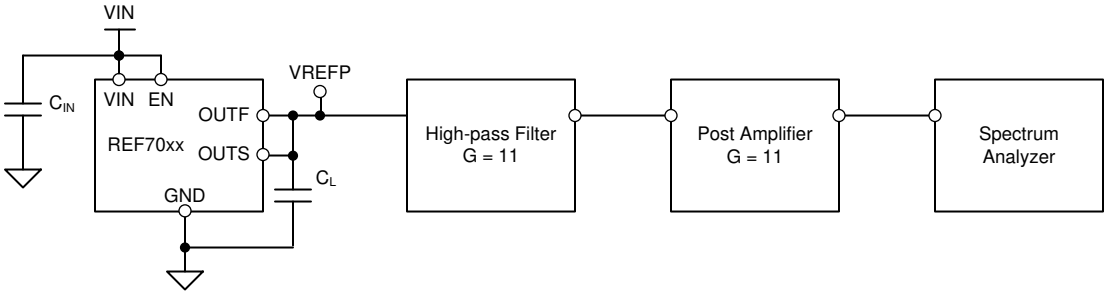


图 8-12. Broadband Noise Test Setup

For noise sensitive designs, a low-pass filter can be used to reduce broadband noise output noise levels by removing the high frequency components. When designing a low-pass filter special care must be taken to ensure the output impedance of the filter does not degrade ac performance. This can occur in RC low-pass filters where a large series resistance can impact the load transients due to output current fluctuations.

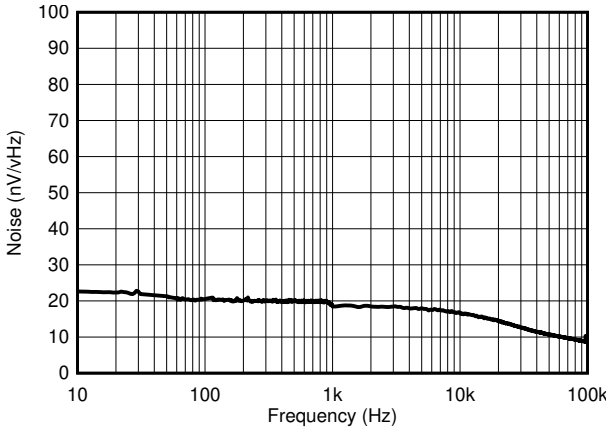


图 8-13. Noise Performance 10 Hz to 100 kHz

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8.5 Temperature Drift

The REF70 is designed and tested for a minimal output voltage temperature drift, which is defined as the change in output voltage over temperature. Every unit shipped is tested at multiple temperatures to ensure that the product meets data sheet specifications. The temperature coefficient is calculated using the box method in which a box is formed by the min/max limits for the nominal output voltage over the operating temperature range. REF70 has a low maximum temperature coefficient of 2 ppm/°C from –40°C to +125°C. This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Due to temperature curvature correction to achieve low-temperature drift, the temperature drift is expected to be non-linear. See *SLYT183* for more information on the box method. The box method equation is shown in 方程式 2:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}} \right) \times 10^6 \tag{2}$$

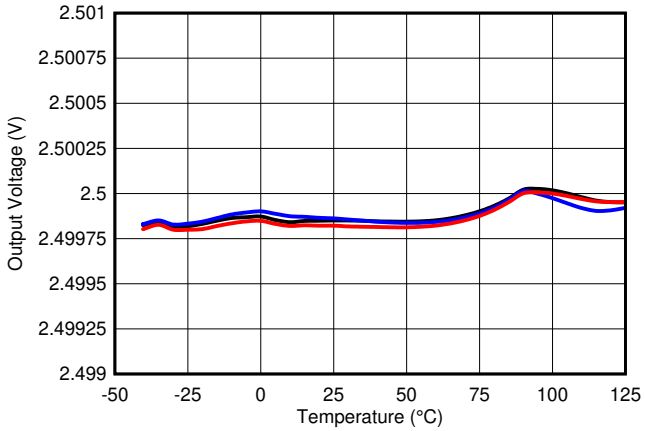


图 8-14. Output Voltage Vs Free-Air Temperature

8.6 Power Dissipation

The REF70 voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with 方程式 3:

$$T_J = T_A + P_D \times R_{\theta JA} \tag{3}$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

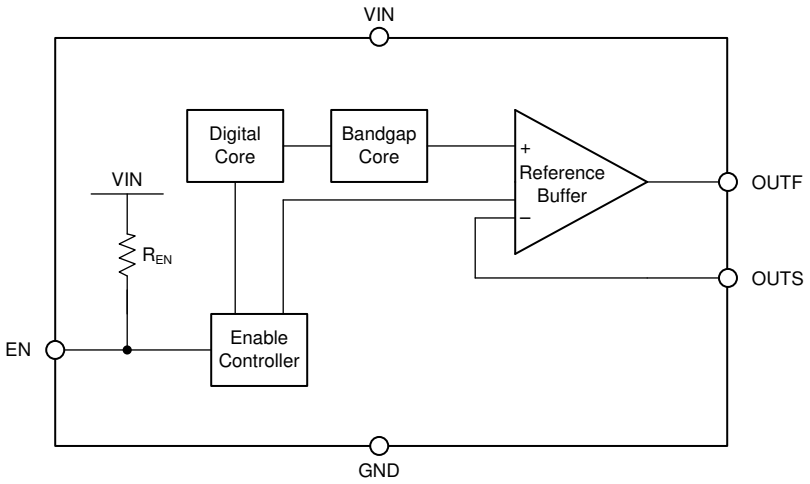
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9 Detailed Description

9.1 Overview

The REF70 is family of ultra low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The 节 9.2 is a simplified block diagram of the REF70 showing basic band-gap topology.

9.2 Functional Block Diagram



9.3 Feature Description

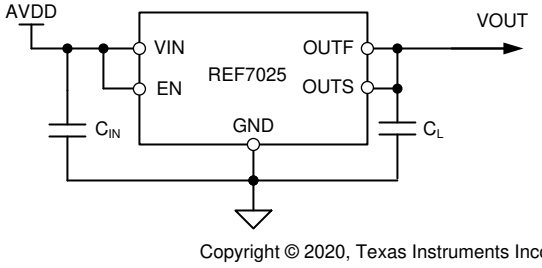
9.3.1 EN Pin

The EN pin of the REF70 has an internal 16 MΩ pull-up resistor (R_{EN}) to VIN. This allows the EN pin of the REF70 to be left floating. When the EN pin of the REF70 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF70 can be placed in shutdown mode by pulling the EN pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 12 µA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the 节 7.6 for logic high and logic low voltage levels.

9.4 Device Functional Modes

9.4.1 Basic Connections

图 9-1 shows the typical connections for the REF70. TI recommends a supply bypass capacitor (C_{IN}) ranging from 0.1- µF to 10- µF. A 1- µF to 100- µF output capacitor (C_L) must be connected from OUTF to GND. The equivalent series resistance (ESR) value of C_L must be 1 mΩ to 400 mΩ to ensure output stability.



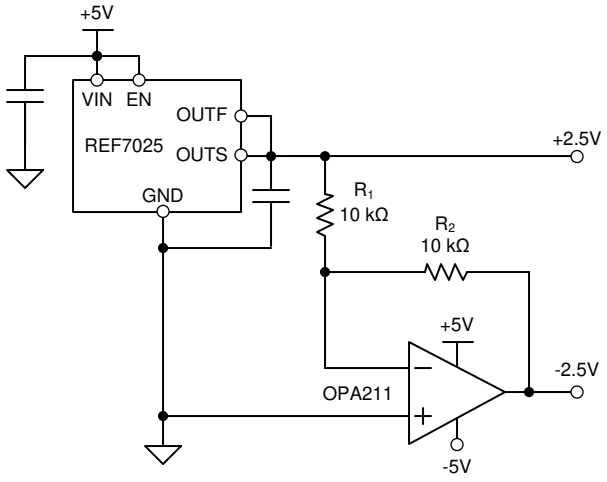
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图 9-1. Basic Connections

9.4.2 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF70 and OPA211 can be used to provide a dual-supply reference from a 5-V supply. 图 9-2 shows the REF70 used to provide a 2.5-V supply

reference voltage and -2.5V negative reference voltage. The low noise performance of the REF70 complements the low noise of the OPA211 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.



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图 9-2. The REF70 and OPA211 Create Positive and Negative Reference Voltages

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

This device is a natural fit for many precision applications and it can be connected to system components in various ways and thus there are many situations that this data sheet can not characterize in detail. Basic applications include positive/negative voltage reference and data acquisition systems. The table below shows the typical applications of REF70 and its companion data converters.

APPLICATION	DATA CONVERTER
Precision Data Acquisition	ADS124S08, ADS8900B, ADS1278, ADS1262, DAC80501, DAC8562
Industrial Instrumentation	ADS127L01, ADS8699, ADS1256, ADS1251, DAC9881, DAC8811, DAC1220, DAC80508
Semiconductor Test	ADS8598H, ADS131M08, ADS8686S, ADS8881, DAC11001A, DAC91001A, DAC7744
Power Monitoring, PLC Analog I/O	ADS131E04, ADS131A02,
Field Transmitters	ADS1247, ADS1220

10.2 Typical Applications

10.2.1 Typical Application: Basic Voltage Reference Connection

The circuit shown in 图 10-1 shows the basic configuration for the REF70 references. Connect bypass capacitors according to the guidelines in 节 10.2.1.2.1.

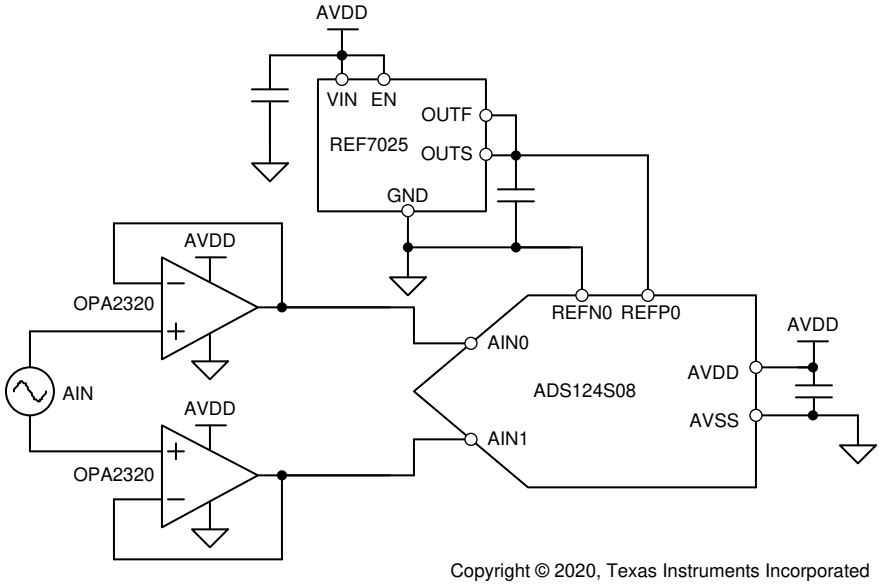


图 10-1. Basic Reference Connection

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10.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in 表 10-1 as the input parameters.

表 10-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5.5 V
Output voltage V_{OUT}	2.5 V
REF7025 input capacitor	10-µF
REF7025 output capacitor	10-µF

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Input and Output Capacitors

A 1 µF to 10 µF bypass capacitor should be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1 µF capacitor in parallel to reduce high frequency supply noise.

A low ESR capacitor of 1 µF to 100 µF must be connected to the output to improve stability and help filter out high frequency noise. Best performance and stability is attained with low-ESR output capacitors with an ESR from 1 mΩ to 400 mΩ. For very low noise applications, special care must be taken with X7R and other MLCC capacitors due to their piezoelectric effect. Mechanical vibration can transduce to voltage via the piezoelectric effect which appears as noise in the µV range, potentially dominating the noise of the REF70. More information on how the piezoelectric effect can be explored in systems can be found in Stress-induced outbursts: Microphonics in ceramic capacitors (Part 1) and Stress-induced outbursts: Microphonics in ceramic capacitors (Part 2). It is recommended that to use film capacitors for noise sensitive applications.

The transient startup response of the REF70 is shown in 图 10-2. The startup response of the REF70 family is dependent on the output capacitor. While larger capacitors will decrease the output noise, they will increase the startup response.

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10.2.1.2.1.1 Application Curve

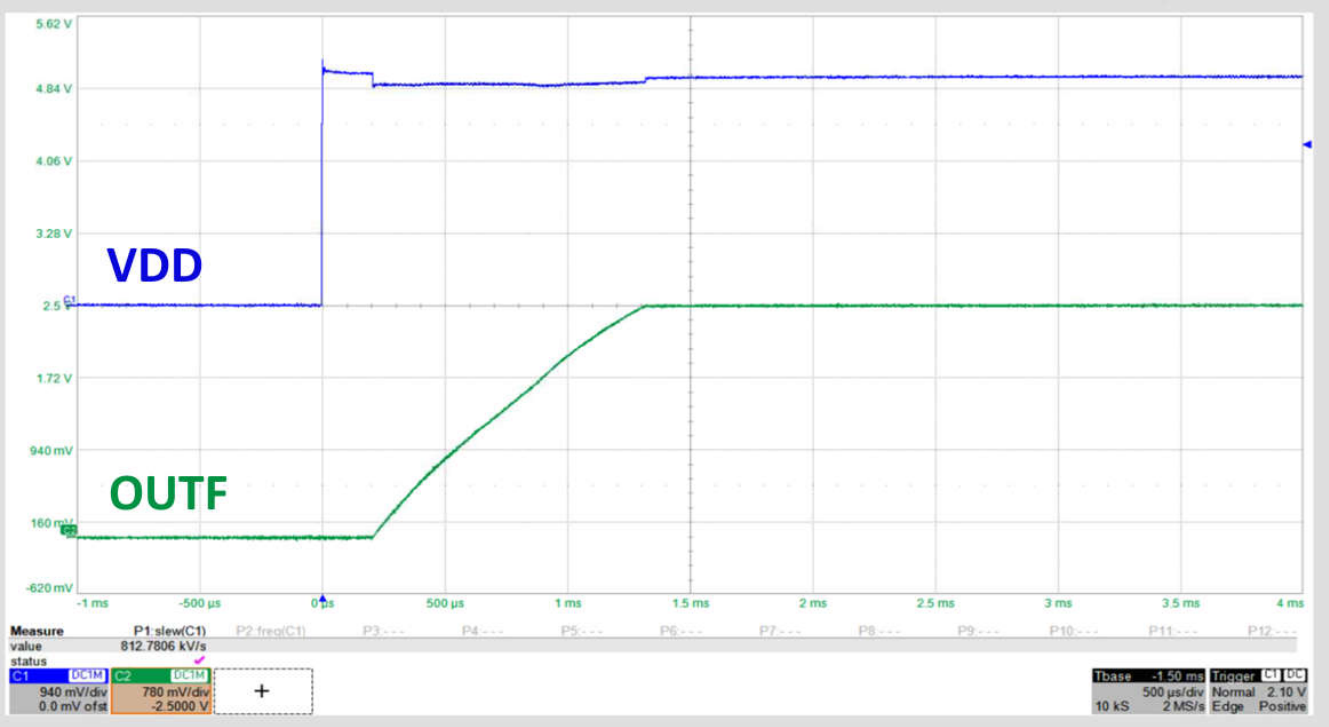


图 10-2. REF7025 Startup (C = 10 µF)

10.2.1.2.2 Force and Sense Connection

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 3000-mil long, 15-mil wide trace of 1-ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference must be mounted as close as possible to the load to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground. The REF70 has kelvin connection capabilities due to its output force (OUTF) and input sense (OUTS) connection as shown in Basic Reference Connection. The output force voltage will vary upwards from the internal V_{REF} voltage to ensure that at V_{OUT}, which is where the OUTF and OUTS connect at the point-of-load, the voltage will be precisely V_{REF}. The sense connection on the REF70 requires 4 mA due to its architecture.

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for V_{OUT} can simply be tied together close to the pins, and the device can be used in the same fashion as a normal 3-terminal reference.

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10.2.2 Typical Application: DAC Force and Sense Reference Drive Circuit

Certain DACs require external voltage references to operate properly. There are DACs that only require a positive voltage for operating in which the basic connection will work. For other DACs there can be a need a positive and negative reference voltage due to their bipolar output.

The circuit shown in 图 10-3 shows a DAC force and sense reference drive circuit for the DACx1001 using the REF70. This circuit takes advantage of the DACx1001 RCM circuit to remove the need of additional external resistors to make a negative reference due to the integrated precision resistors. This circuit requires additional buffers due to undesired series resistance on the reference input of the DAC.

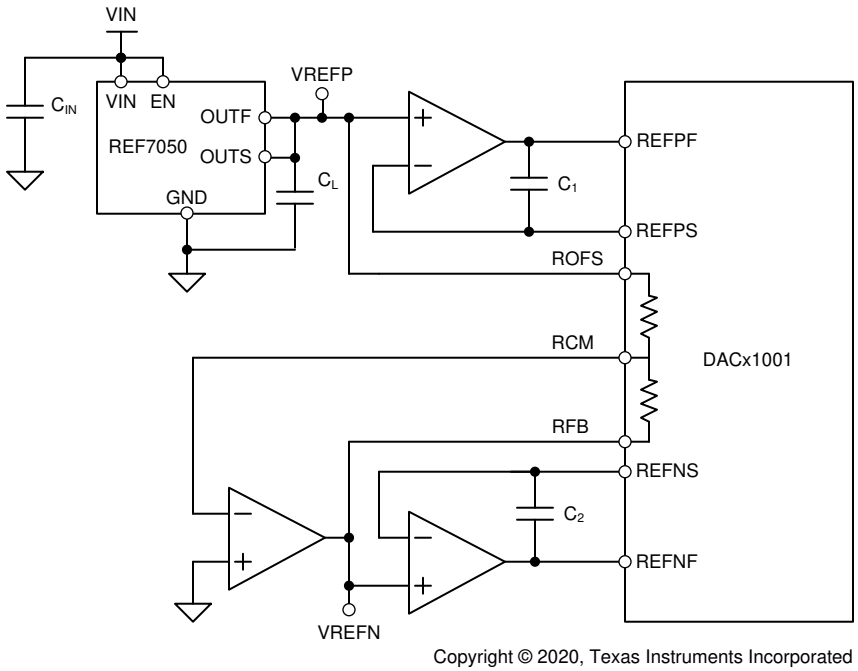


图 10-3. Basic Force and Sense Reference Drive Circuit Connections with DACx1001

10.2.2.1 Design Requirements

For this design example, use the reference op amp recommendation listed in 表 10-2 for the buffer circuit.

表 10-2. Reference Op Amp Options

SELECTION PARAMETERS	OP AMPS
Low voltage and current noise	OPA211, OPA827, OPA828
Low offset and drift	OPA189

The REF70 turn-on time is dependent on the output capacitor. In certain applications that require a fast turn-on can require a smaller output capacitor as shown in 图 10-4

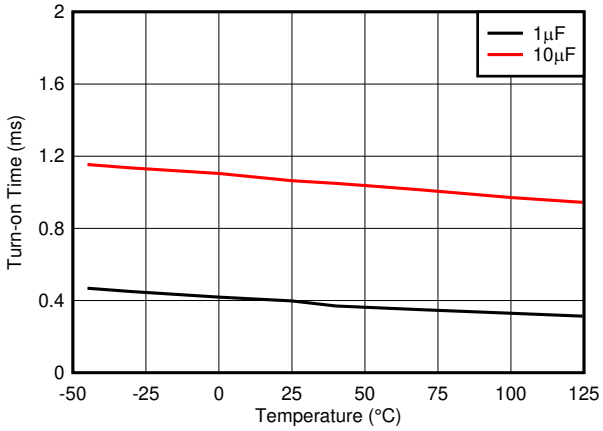


图 10-4. REF70 Turn-on Time

For DAC designs that do not have the RCM feature, use 图 10-5 as it in generates the negative reference circuit to create the VREFN. More details on this type of design can be found in *SBAA322*.

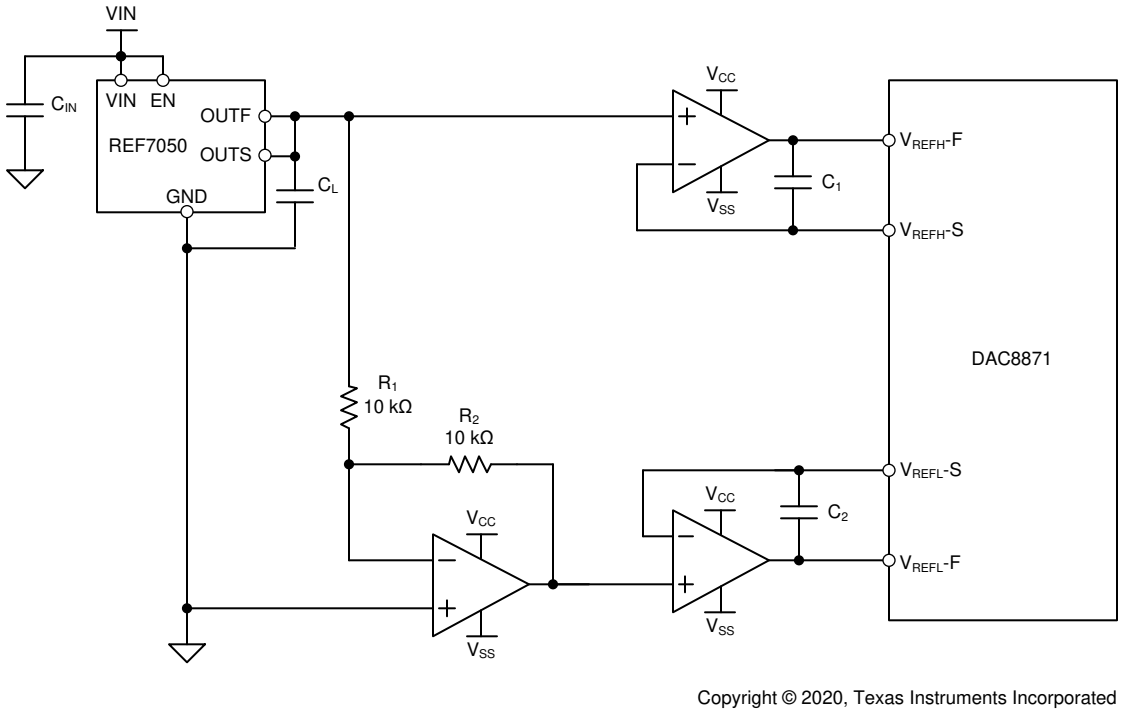


图 10-5. Basic Force and Sense Reference Drive Circuit Connections

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10.3 Power Supply Recommendation

The REF70 family of references features a low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage for 0-mA output current conditions. The dropout voltage will vary with the output current so refer to the dropout voltage to see typical dropout voltage requirements. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

During start-up the REF70 can experience moments of high input current due to the output capacitors. The input current can momentarily rise to I_{SC}.

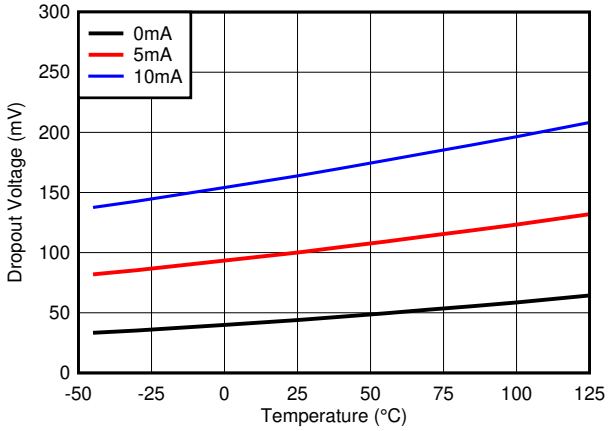


图 10-6. Dropout Voltage vs Temperature

10.4 Layout

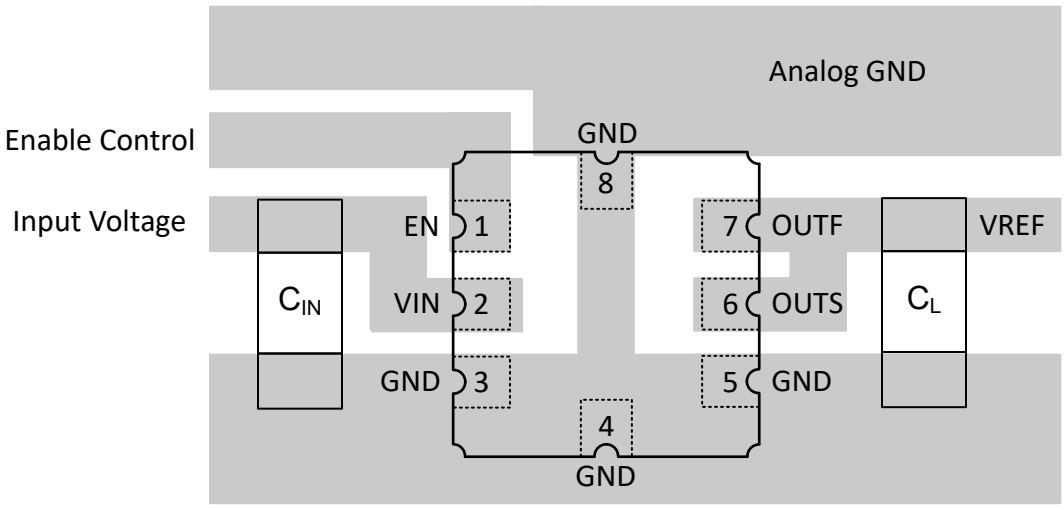
10.4.1 Layout Guidelines

图 10-7 and 图 10-8 illustrate an example of a PCB layout for a data acquisition system using the REF70. Some key considerations are:

- Connect low-ESR, 0.1- µ F ceramic bypass capacitors at V_{IN} of the REF70.
- Connect low-ESR, 1-uF to 100-uF capacitor at OUTF of the REF70.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

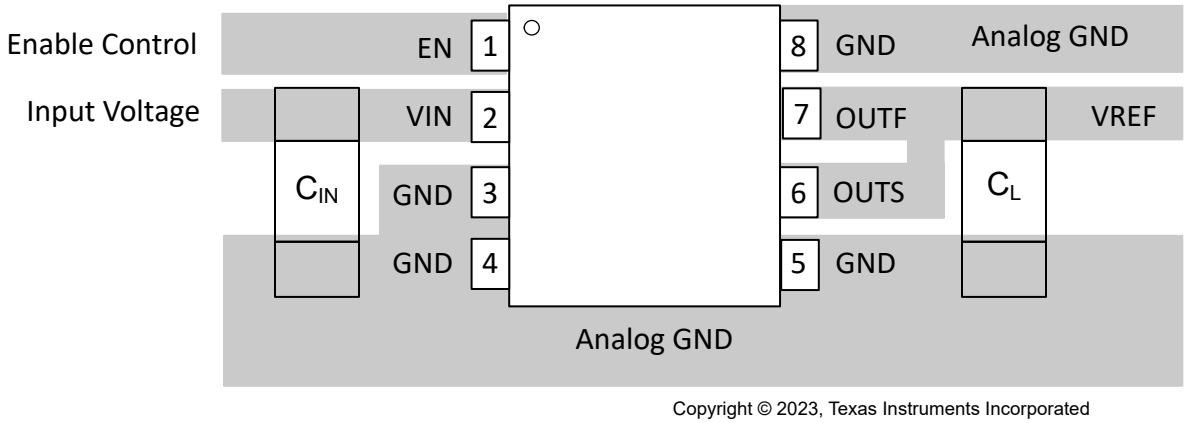
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10.4.2 Layout Example



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图 10-7. Layout Example FKH Package



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图 10-8. Layout Example DGK Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Voltage Reference Design Tips For Data Converters*
- Texas Instruments, *Voltage Reference Selection Basics*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF7012QDGKR	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2L1S
REF7012QDGKR.A	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2L1S
REF7012QFKHT	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF12FKH
REF7012QFKHT.A	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF12FKH
REF7025QDGKR	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TAS
REF7025QDGKR.A	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TAS
REF7025QFKHR	Active	Production	LCCC (FKH) | 8	4000 | LARGE T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF25FKH
REF7025QFKHT	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF25FKH
REF7025QFKHT.A	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF25FKH
REF7030QFKHT	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF30FKH
REF7030QFKHT.A	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF30FKH
REF7033QFKHT	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF33FKH
REF7033QFKHT.A	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF33FKH
REF7040QDGKR	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TDS
REF7040QDGKR.A	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TDS
REF7040QFKHT	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF40FKH
REF7040QFKHT.A	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF40FKH
REF7050QDGKR	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TES
REF7050QDGKR.A	Active	Production	VSSOP (DGK) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TES
REF7050QFKHT	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF50FKH
REF7050QFKHT.A	Active	Production	LCCC (FKH) | 8	250 | SMALL T&R	ROHS Exempt	Call TI	N/A for Pkg Type	-40 to 125	REF50FKH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

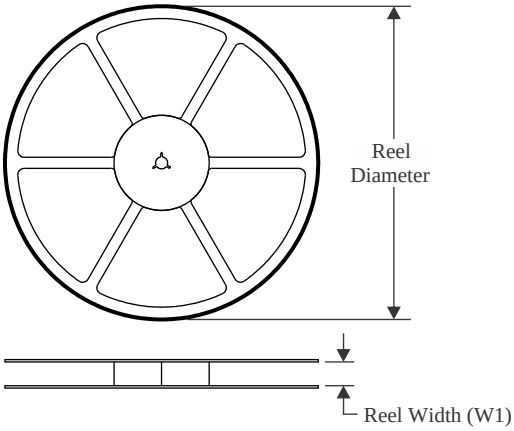
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

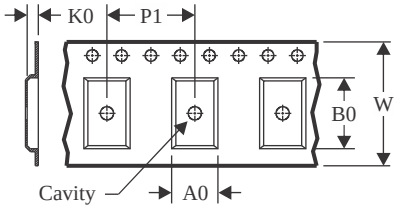
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

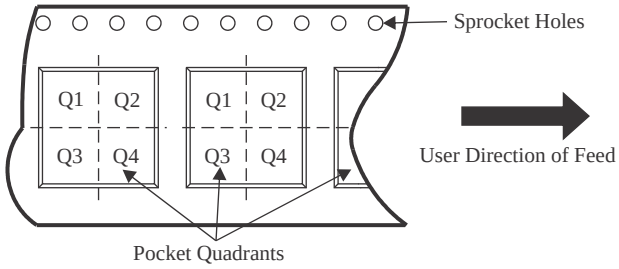


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

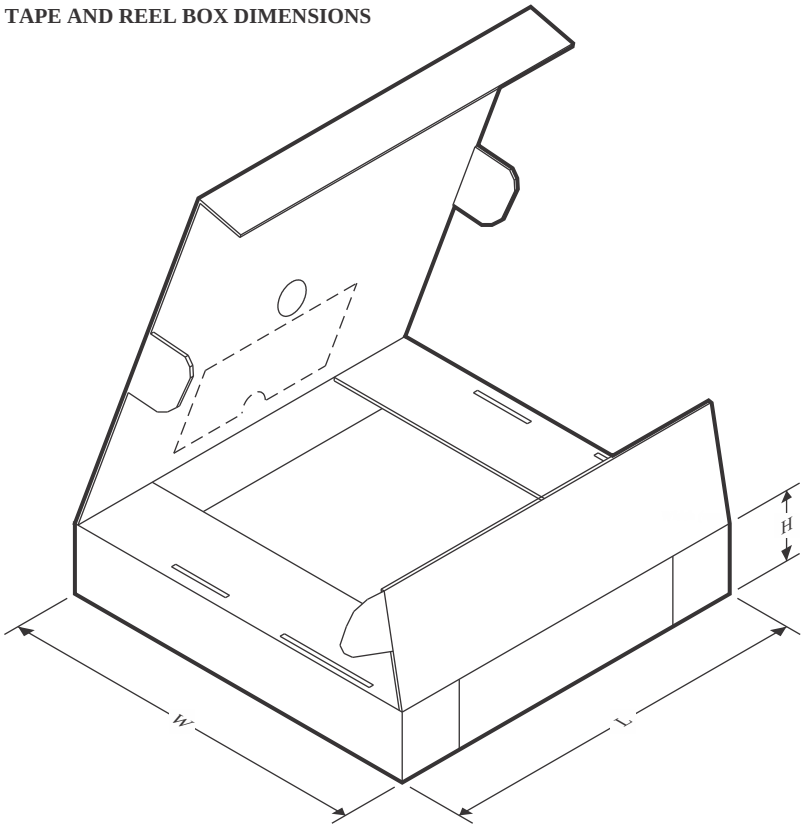
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF7012QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7012QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7025QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7025QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7030QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7033QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7040QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7050QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7050QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

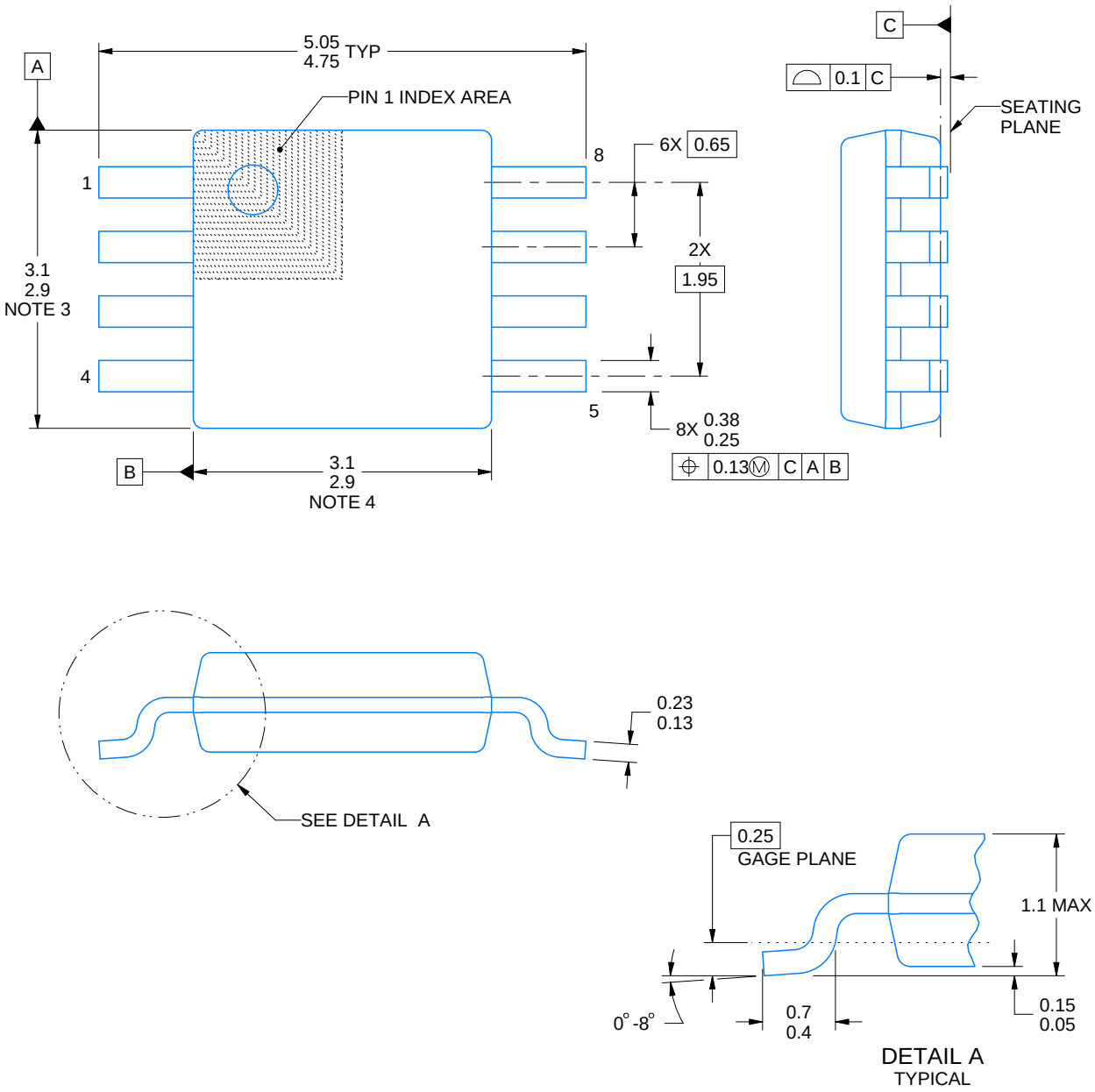
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF7012QDGKR	VSSOP	DGK	8	3000	353.0	353.0	32.0
REF7012QFKHT	LCCC	FKH	8	250	213.0	191.0	35.0
REF7025QDGKR	VSSOP	DGK	8	3000	353.0	353.0	32.0
REF7025QFKHT	LCCC	FKH	8	250	213.0	191.0	35.0
REF7030QFKHT	LCCC	FKH	8	250	213.0	191.0	35.0
REF7033QFKHT	LCCC	FKH	8	250	213.0	191.0	35.0
REF7040QDGKR	VSSOP	DGK	8	3000	353.0	353.0	32.0
REF7050QDGKR	VSSOP	DGK	8	3000	353.0	353.0	32.0
REF7050QFKHT	LCCC	FKH	8	250	213.0	191.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

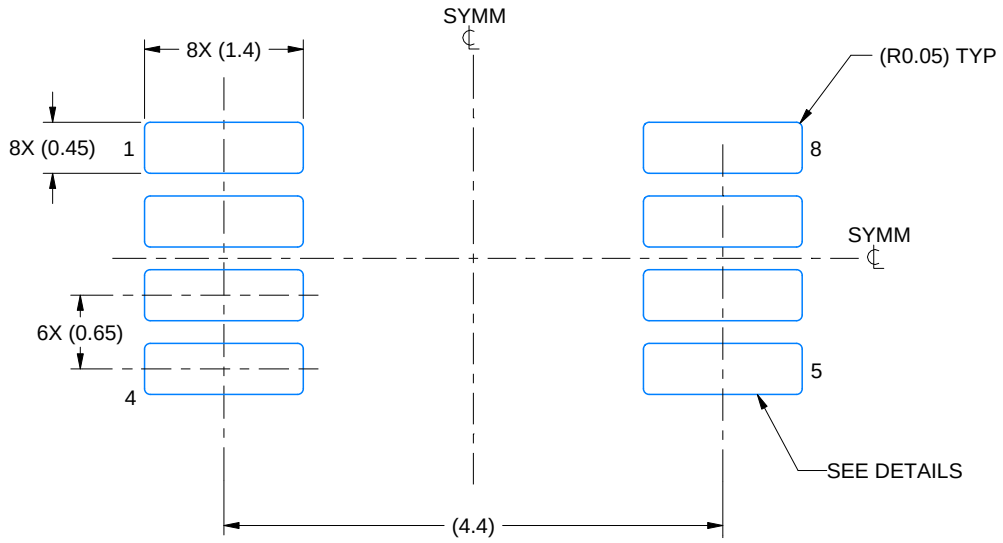
SMALL OUTLINE PACKAGE



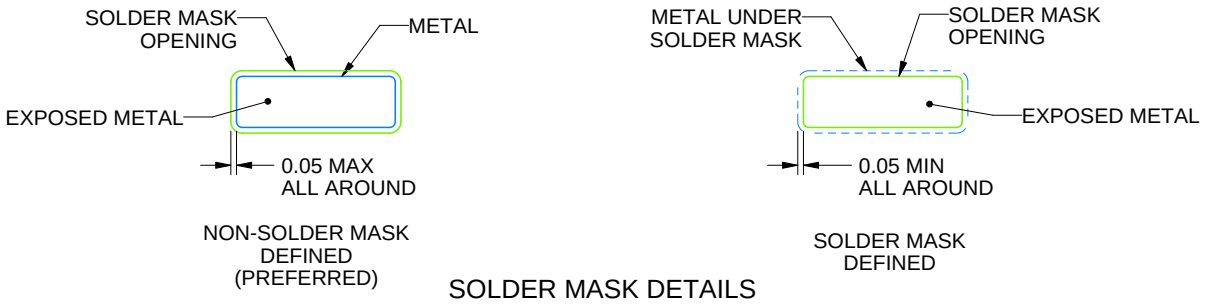
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

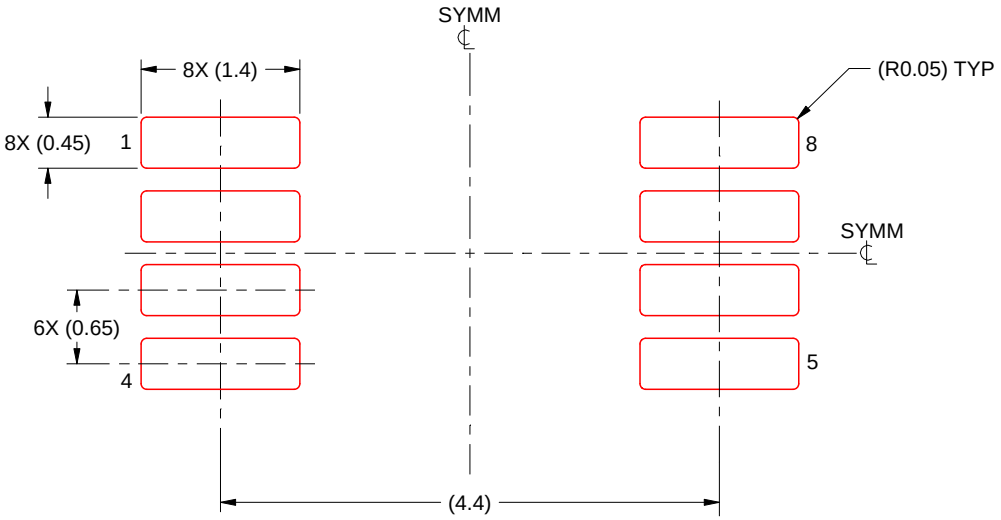


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



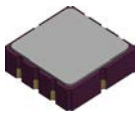
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

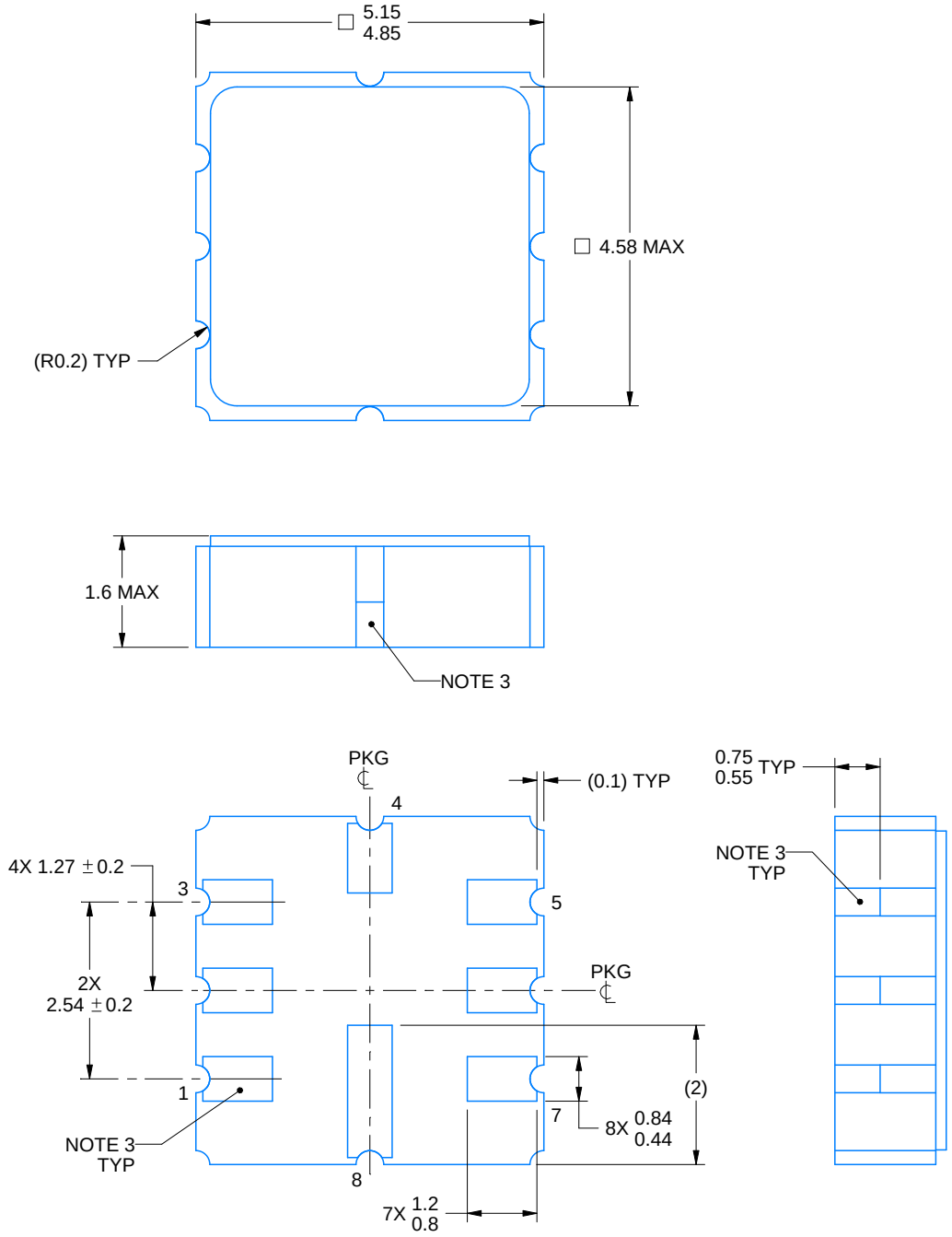
FKH0008A



PACKAGE OUTLINE

LCCC - 1.6 mm max height

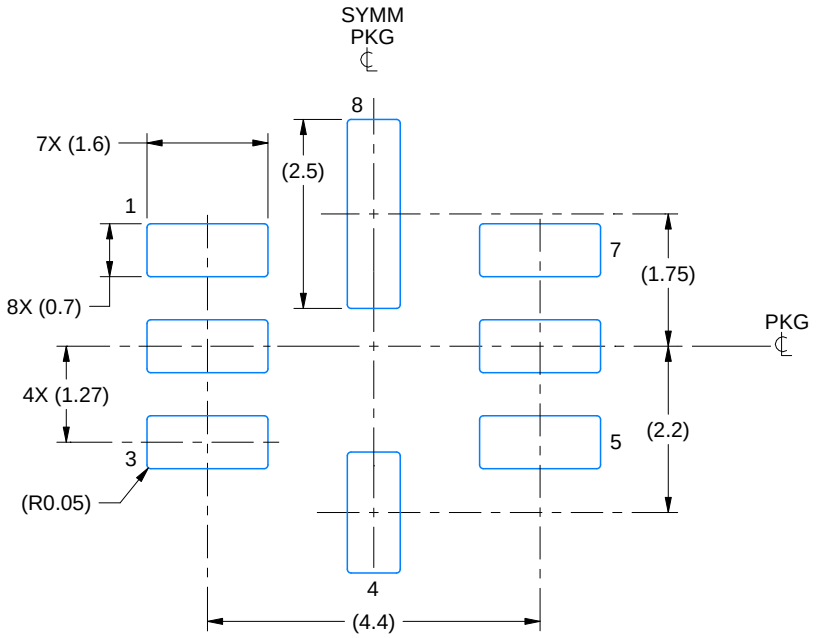
LEADLESS CERAMIC CHIP CARRIER



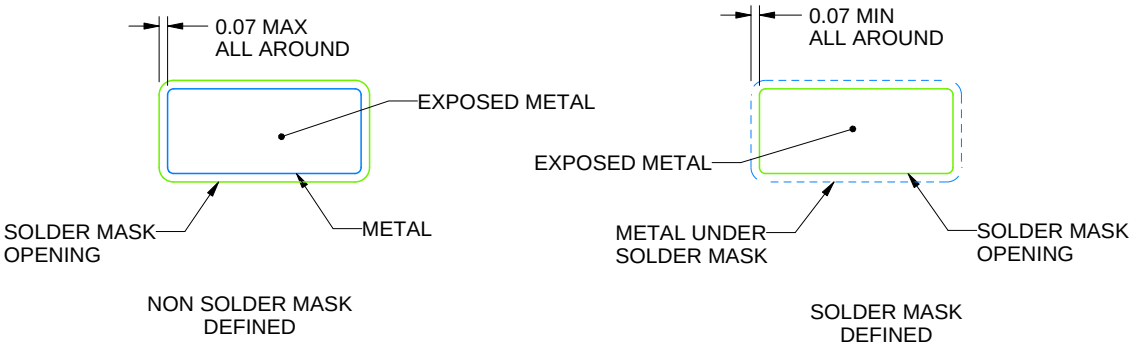
4222330/E 04/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. Terminals are gold plated.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS

4222330/E 04/2023

NOTES: (continued)

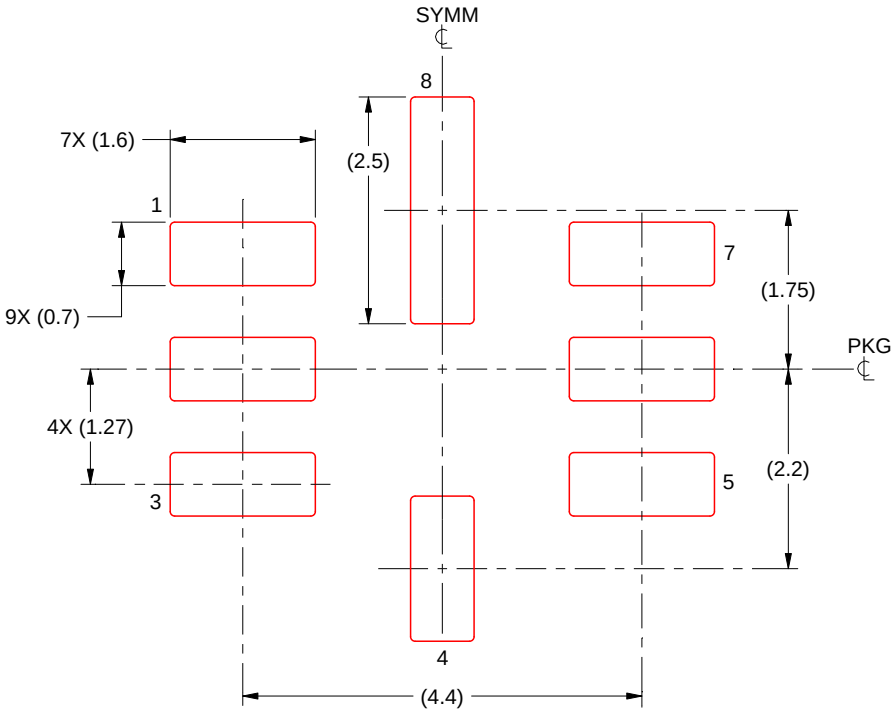
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

FKH0008A

LCCC - 1.6 mm max height

LEADLESS CERAMIC CHIP CARRIER



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:12X

4222330/E 04/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月