

SDLS077

**SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197,
SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197
50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES**

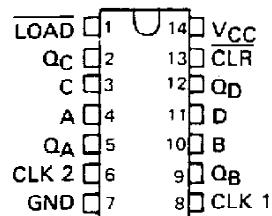
OCTOBER 1976—REVISED MARCH 1988

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output QA Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

TYPES	GUARANTEED		TYPICAL POWER DISSIPATION
	COUNT FREQUENCY CLOCK 1	CLOCK 2	
'196, '197	0-50 MHz	0-25 MHz	240 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	80 mW
'S196, 'S197	0-100 MHz	0-50 MHz	375 mW

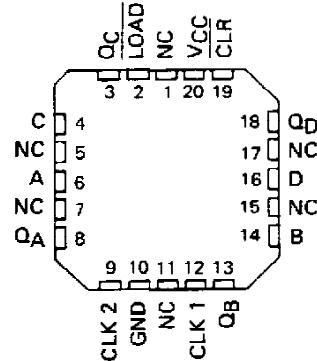
SN54196, SN54LS196, SN54S196,
SN54197, SN54LS197, SN54S197 . . . J OR W PACKAGE
SN74196, SN74197 . . . N PACKAGE
SN74LS196, SN74S196,
SN74LS197, SN74S197 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS196, SN54S196,
SN54LS197, SN54S197 . . . FK PACKAGE

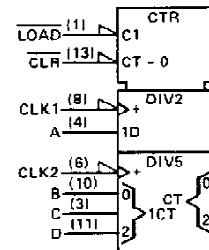
(TOP VIEW)



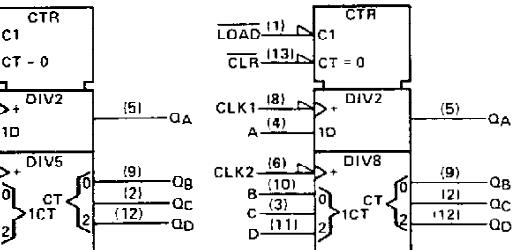
NC - No internal connection

logic symbols†

'196, 'LS196, 'S196



'197, 'LS197, 'S197



† These symbols are in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

**SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197,
SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197
50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES**

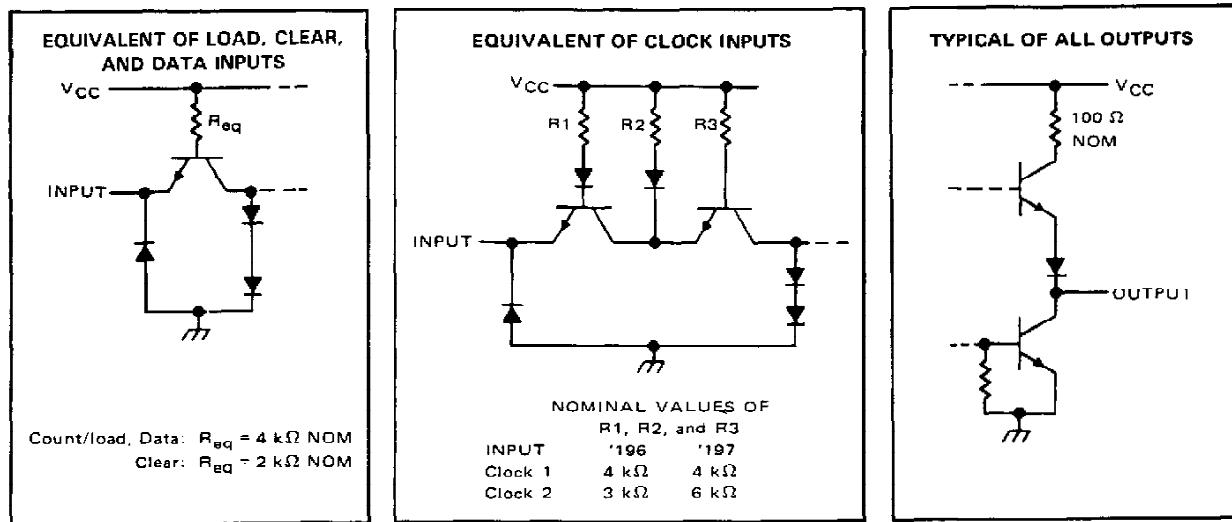
typical count configurations

'196, 'LS196, and 'S196 typical count configurations and function tables are the same as those for '176.
'197, 'LS197, and 'S197 typical count configurations and function tables are the same as those for '177.

logic diagrams

'196, 'LS196, and 'S196 logic diagrams are the same as those for '176.
'197, 'LS197, and 'S197 logic diagrams are the same as those for '177.

schematics of inputs and outputs



**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75205

SN54196, SN54197, SN74196, SN74197
50-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits	-55°C to 125°C
SN74196, SN74197 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the Clear and Load inputs.

recommended operating conditions

	SN54196, SN54197			SN74196, SN74197			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Count frequency	Clock-1 input	0	50	0	50		MHz
	Clock-2 input	0	25	0	25		
Pulse width, t_w	Clock-1 input	10		10			ns
	Clock-2 input	20		20			
	Clear	15		15			
	Load	20		20			
Input hold time, t_h (see Note 3)	High-level data	t_w (load)		t_w (load)			ns
	Low-level data	t_w (load)		t_w (load)			
Input setup time, t_{su} (see Note 3)	High-level data	10		10			ns
	Low-level data	15		15			
Count enable time, t_{en} (see Note 4)		20		20			ns
Operating free-air temperature, T_A	-55		125	0	70	"C	

NOTES: 3. Setup and hold times are with respect to the falling edge of the load input.

4. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

TEXAS

INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75266

**SN54196, SN54197, SN74196, SN74197
50-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54196, SN74196			SN54197, SN74197			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μ A	2.4	3.4		2.4	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA [¶]		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	Data, Load			40			40	μ A
	Clear, clock 1	V _{CC} = MAX, V _I = 2.4 V		80			80	
	Clock 2			120			80	
I _{IL} Low-level input current	Data, Load			-1.6			-1.6	mA
	Clear	V _{CC} = MAX, V _I = 0.4 V		-3.2			-3.2	
	Clock 1			-4.8			-4.8	
	Clock 2			-6.4			-3.2	
I _{OS} Short-circuit output current [§]	V _{CC} = MAX	SN54 [*]	-20	-57	-20	-57		mA
		SN74 [*]	-18	-57	-18	-57		
I _{CC} Supply current	V _{CC} = MAX, See Note 5		48	59		48	59	mA

NOTE 5: I_{CC} is measured with all inputs grounded and all outputs open.

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[¶]Not more than one output should be shorted at a time.

^{*}Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER #	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54196			SN54197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Clock 1	Q _A	C _L = 15 pF, R _L = 400 Ω , See Note 6	50	70		50	70		MHz
t _{PLH}	Clock 1	Q _A		7	12		7	12		ns
t _{PHL}				10	15		10	15		
t _{PLH}	Clock 2	Q _B		12	18		12	18		ns
t _{PHL}				14	21		14	21		
t _{PLH}	Clock 2	Q _C		24	36		24	36		ns
t _{PHL}				28	42		28	42		
t _{PLH}	Clock 2	Q _D		14	21		36	54		ns
t _{PHL}				12	18		42	63		
t _{PLH}	A, B, C, D	Q _A , Q _B , Q _C , Q _D		16	24		16	24		ns
t _{PHL}				25	38		25	38		
t _{PLH}	Load	Any		22	33		22	33		ns
t _{PHL}				24	36		24	36		
t _{PLH}	Clear	Any		25	37		25	37		ns

#f_{max} = maximum count frequency.

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

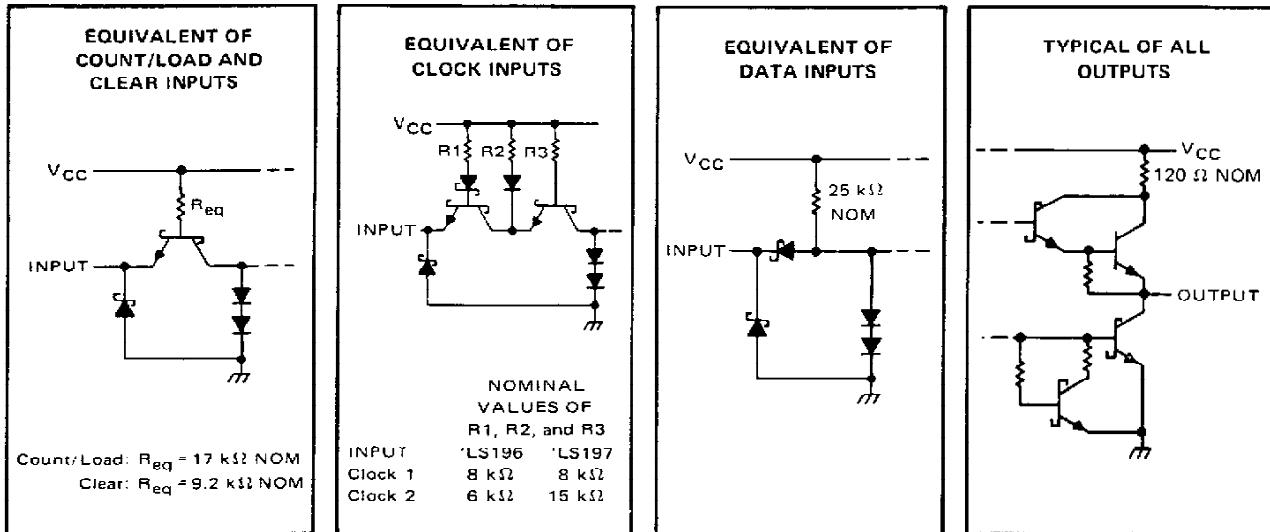
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that testing f_{max}, V_{IL} = 0.3 V.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 555012 • DALLAS, TEXAS 75285

SN54LS196, SN54LS197, SN74LS196, SN74LS197 30-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS196, SN54LS197			SN74LS196, SN74LS197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-400			-400	μA
I _{OL}	Low-level output current			4			8	mA
Count frequency	Clock-1 input	0	30	0	0	30		MHz
	Clock-2 input	0	15	0	0	15		
t _W	Clock-1 input	20		20				ns
	Clock-2 input	30		30				
	Clear	15		15				
	Load	20		20				
	High-level data	t _W (load)		t _W (load)		t _W (load)		ns
t _H	Low-level data	t _W (load)		t _W (load)		t _W (load)		
	High-level data	10		10				ns
t _{su}	Low-level data	15		15				
	High-level data	10		10				ns
t _{enable}	Low-level data	15		15				
	Clock 1	30		30				ns
	Clock 2	50		50				
T _A	Operating free-air temperature	-55	125		0	70	°C	

NOTES: 3. Setup and hold times are with respect to the falling edge of the load input.

4. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

SN54LS196, SN54LS197, SN74LS196, SN74LS197
30-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS196			SN74LS196			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2		2	2		2	V
V_{IL}	Low-level input voltage			0.7		0.7	0.8	0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$		-1.5		-1.5	-1.5	-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}^{\ddagger}$	0.25	0.4	0.25	0.4	0.35	V
I_I Input current at maximum input voltage	Data, Load	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$		0.1		0.1			
	Clear, clock 1			0.2		0.2			
	Clock 2 of 'LS196			0.4		0.4			
	Clock 2 of 'LS197			0.2		0.2			
I_{IH} High-level input current	Data, Load	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		20		20			
	Clear, clock 1			40		40			
	Clock 2 of 'LS196			80		80			
	Clock 2 of 'LS197			40		40			
I_{IL} Low-level input current	Data, Load	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.4		-0.4			
	Clear			-0.8		-0.8			
	Clock 1			-2.4		-2.4			
	Clock 2 of 'LS196			-2.8		-2.8			
	Clock 2 of 'LS197			-1.3		-1.3			
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-100	-20	-20	-100	-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 5		16	27	16	27	27	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

* Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.

NOTE 5: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER #	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS196			SN74LS197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 6	30	40		30	40		MHz
t_{PLH}	Clock 1	Q_A		8	15		8	15		ns
t_{PHL}	Clock 2	Q_B		13	20		14	21		
t_{PLH}	Clock 2	Q_C		16	24		12	19		
t_{PHL}	Clock 2	Q_D		22	33		23	35		
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D		38	57		34	51		
t_{PHL}	Load	Any		41	62		42	63		
t_{PLH}	Clear	Any		12	18		55	78		
t_{PHL}				30	45		63	95		
t_{PLH}				20	30		18	27		
t_{PHL}				29	44		29	44		
t_{PLH}				27	41		26	39		
t_{PHL}				30	45		30	45		
t_{PHL}				34	51		34	51		ns

f_{max} = maximum count frequency.

t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

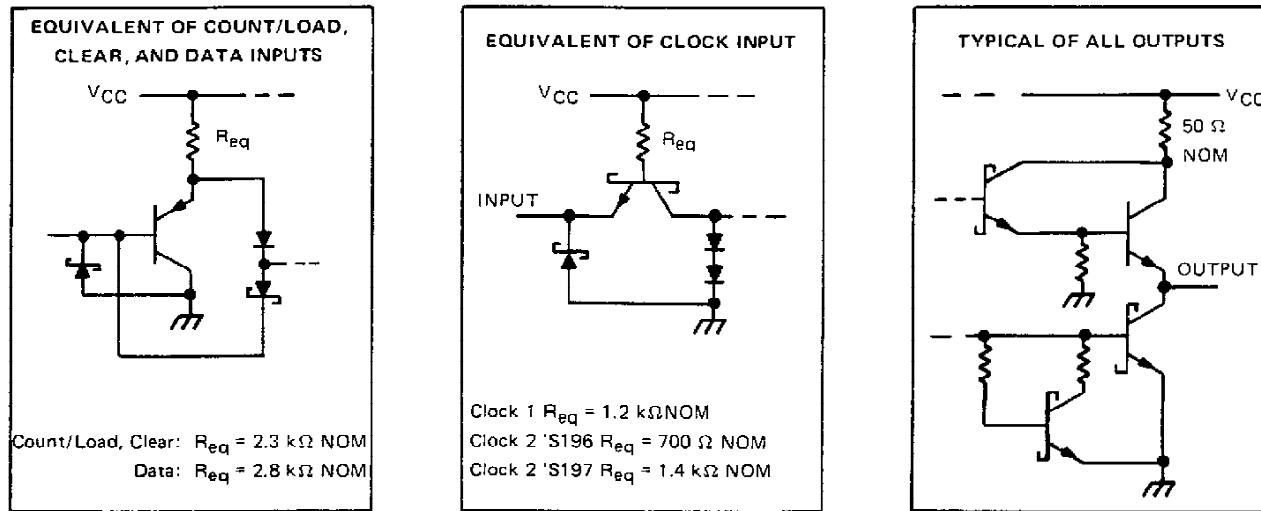
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$, and $V_{ref} = 1.3 \text{ V}$ (as opposed to 1.5 V).


**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54S196, SN54S197, SN74S196, SN74S197 100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S196, SN54S197 Circuits	-55°C to 125°C
SN74S196, SN74S197 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S196, SN54S197			SN74S196, SN74S197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1		mA
Low-level output current, I_{OL}			20			20		mA
Clock frequency	Clock-1 input	0	100		0	100		MHz
	Clock-2 input	0	50		0	50		
Pulse width, t_w	Clock-1 input	5			5			ns
	Clock-2 input	10			10			
	Clear	30			30			
	Load	5			5			
Input hold time, t_h (see Note 3)	High-level data	31			31			ns
	Low-level data	31			31			
Input setup time, t_{SU} (see Note 3)	High-level data	61			61			ns
	Low-level data	61			61			
Count enable time, t_{en} (see Note 4)		12			12			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

NOTES: 3. Setup and hold times are with respect to the falling edge of the load input.

4. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54S196, SN54S197, SN74S196, SN74S197
100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54S196, SN74S196			SN54S197, SN74S197			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}		2			2			V
V _{IL}				0.8			0.8	V
V _{IK}	V _{CC} = MIN, I _I = -18 mA				-1.2		-1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	54S	2.5	3.4	2.5	3.4		V
		74S	2.7	3.4	2.7	3.4		
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V				1		1	mA
I _{IH}	Clock 1, clock 2 All other inputs	V _{CC} = MAX, V _I = 2.7 V			150		150	μA
					50		50	
I _{IL}	Data, Load Clear Clock 1 Clock 2	V _{CC} = MAX, V _I = 0.5 V			-0.75		-0.75	mA
I _{OS} [§]	V _{CC} = MAX			-30	-110	-30	-110	mA
I _{CC}	V _{CC} = MAX, See Note 5	54S	75	110	75	110		mA
		74S	75	120	75	120		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ Q_A outputs are tested at I_{OL} = 20 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54S/74S loads.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 5: I_{CC} is measured with all input grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER #	(FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S196, SN74S196			SN54S197, SN74S197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Clock 1	Q _A		100	140		100	140		MHz
t _{PLH}	Clock 1	Q _A		5	10		5	10		ns
t _{PHL}	Clock 2	Q _B		6	10		6	10		
t _{PLH}	Clock 2	Q _C		5	10		5	10		ns
t _{PHL}	Clock 2	Q _D		8	12		8	12		
t _{PLH}	A,B,C,D	Q _A ,Q _B ,Q _C ,Q _D	R _L = 280 Ω, C _L = 15 pF, See Note 7	12	18		12	18		ns
t _{PHL}	Clock 2	Q _D		16	24		15	22		
t _{PLH}	Load	Any		5	10		18	27		ns
t _{PHL}	Load	Any		8	12		22	33		
t _{PLH}	Clear	Any		7	12		7	12		ns
t _{PHL}	Clear	Any		12	18		12	18		
t _{PLH}	Load	Any		10	18		10	18		ns
t _{PHL}	Load	Any		12	18		12	18		
t _{PLH}	Clear	Any		26	37		26	37		ns

#f_{max} = maximum count frequency.

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 7: Load circuit, input conditions, and voltage waveforms are the same as those shown in Section 1.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54196J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54196J
SN54196J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54196J
SN54197J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54197J
SN54197J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54197J
SNJ54196J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54196J
SNJ54196J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54196J
SNJ54197J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54197J
SNJ54197J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54197J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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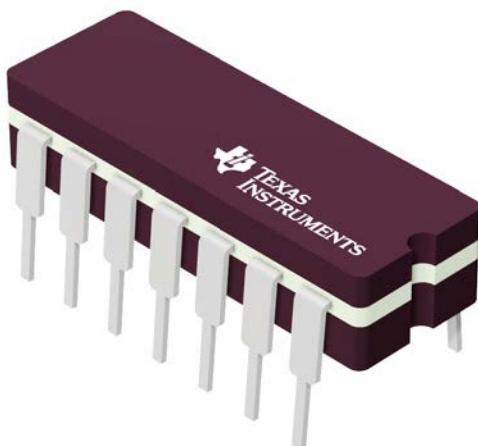
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

J 14

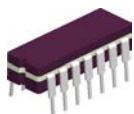
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

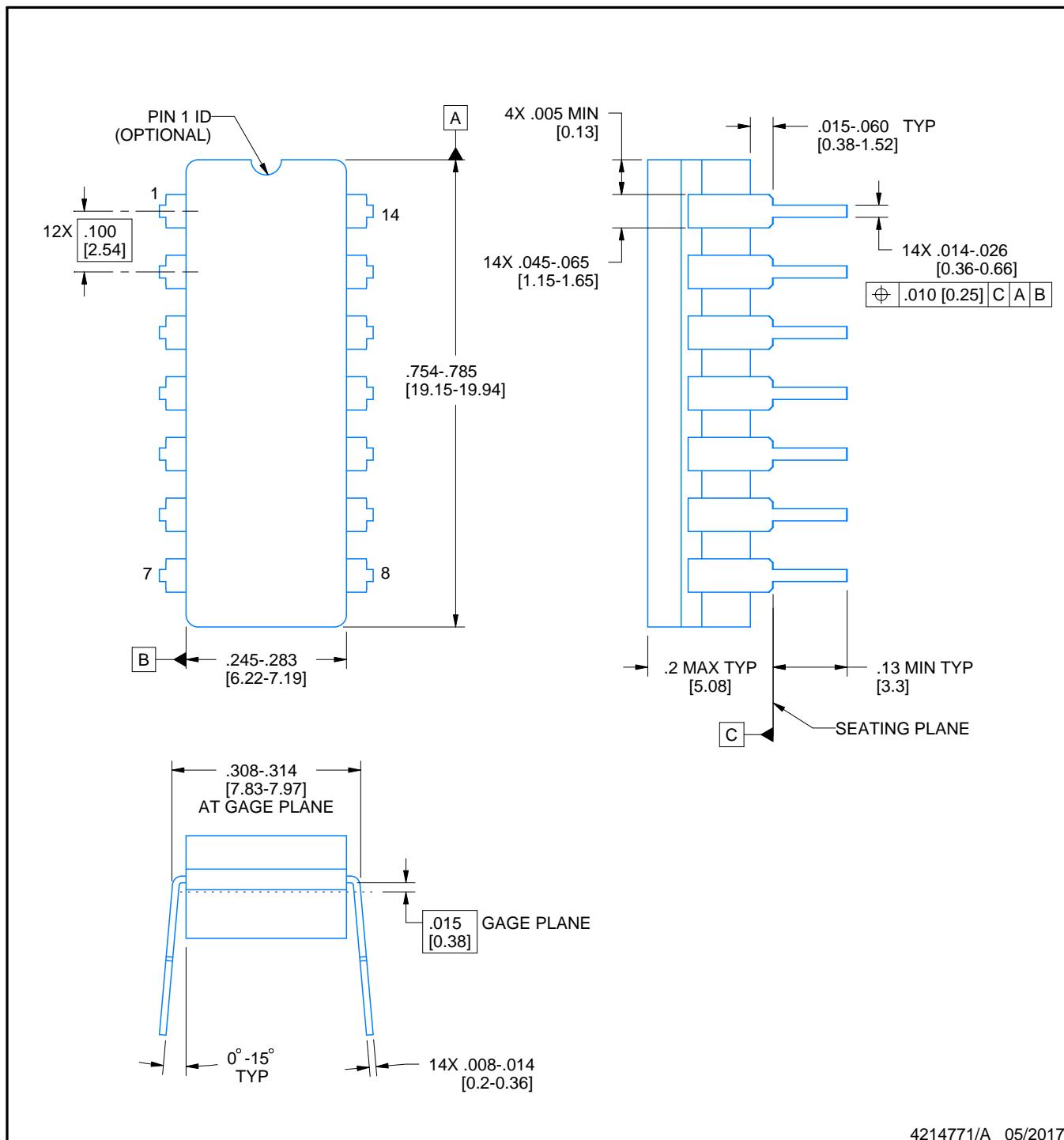


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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NOTES:

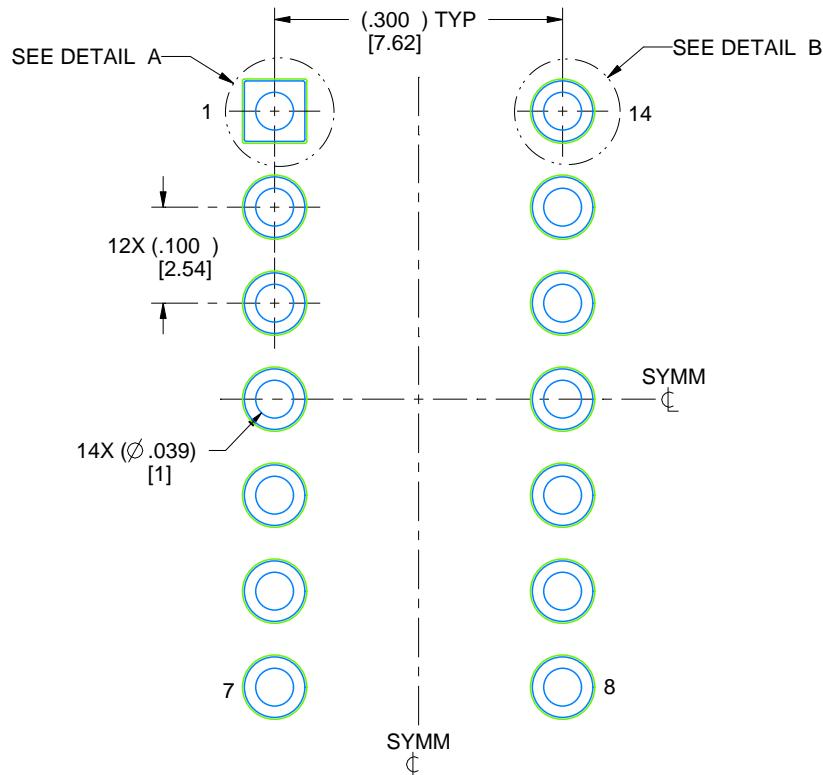
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

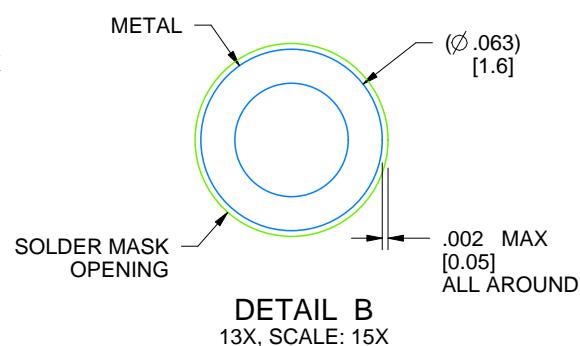
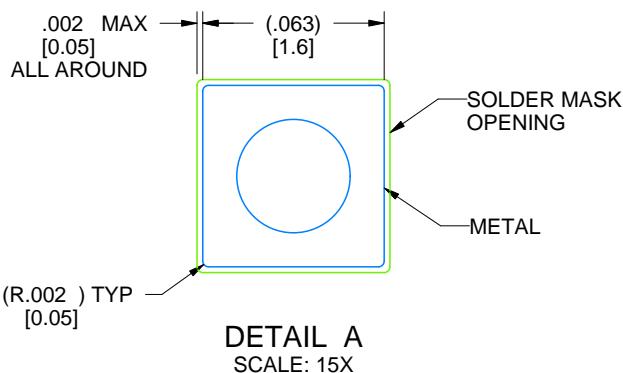
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

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