SNx4AHC273 具有清零功能的八路 D 类触发器

1 特性

- 工作范围为 2V 至 5.5V V_{CC}
- 包含 8 个具有单轨输出的触发器
- 直接清零输入
- 为每个触发器提供单独的数据输入
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 缓冲器和存储寄存器
- 移位寄存器
- 图形发生器
- 服务器
- PC 和笔记本电脑
- 网络交换机
- 存储器系统
- 数据库

3 说明

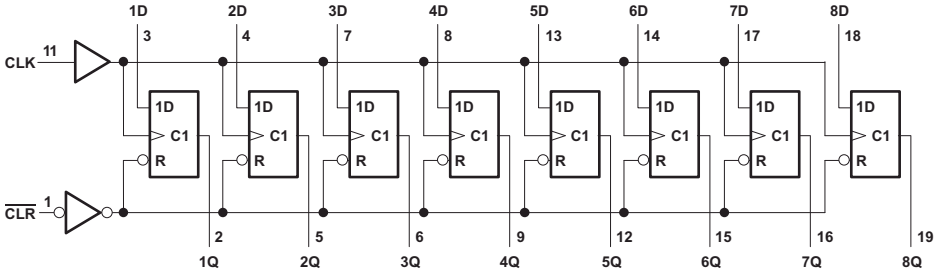
这些器件是正边沿触发式 D 类触发器，具有直接清零 ($\overline{CLR}$) 输入。

数据 (D) 输入上满足设置时间要求的信息被发送到时钟 (CLK) 脉冲正向边沿上的 Q 输出。时钟触发在一个特定电压电平下发生，并且不与正向脉冲的转换时间直接相关。当 CLK 处于高电平或低电平时，D 输入对输出无影响。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SNx4AHC273	N (PDIP , 20)	24.33mm x 9.4mm	25.40mm x 6.35mm
	DB (SSOP , 20)	7.2mm × 7.8mm	7.50mm x 5.30mm
	NS (SOP , 20)	12.60mm x 7.8mm	12.6mm x 5.30mm
	PW (TSSOP , 20)	6.50mm × 6.4mm	6.50mm x 4.40mm
	DGV (TVSOP , 20)	5.00mm x 6.4mm	5.00mm x 4.40mm
	DW (SOIC , 20)	12.80mm × 10.3mm	12.8mm x 7.5mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



简化版原理图

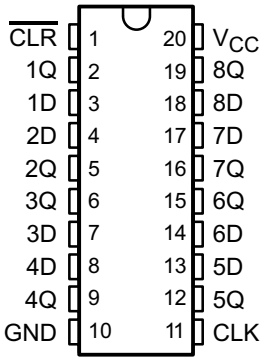
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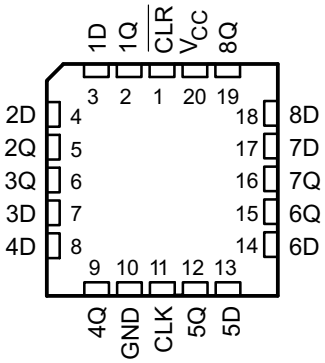
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4 引脚配置和功能

SN54AHC273 . . . J OR W PACKAGE
SN74AHC273 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC273 . . . FK PACKAGE
(TOP VIEW)



引脚		I/O	说明
编号	名称		
1	$\overline{CLR}$	I	清零引脚
2	1Q	O	1Q 输出
3	1D	I	1D 输入
4	2D	I	2D 输入
5	2Q	O	2Q 输出
6	3Q	O	3Q 输出
7	3D	I	3D 输入
8	4D	I	4D 输入
9	4Q	O	4Q 输出
10	GND	—	接地引脚
11	CLK	I	时钟管脚
12	5Q	O	5Q 输出
13	5D	I	5D 输入
14	6D	I	6D 输入
15	6Q	O	6Q 输出
16	7Q	O	7Q 输出
17	7D	I	7D 输入
18	8D	I	8D 输入
19	8Q	O	8Q 输出
20	VCC	—	电源引脚

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5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
V_I	输入电压范围(2)		-0.5	7	V
V_O	输出电压范围(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-20	mA
I_{OK}	输出钳位电流	V_O < 0 或 V_O > V_{CC}		±20	mA
I_O	持续输出电流	V_O = 0 至 V_{CC}		±25	mA
	通过 V_{CC} 或 GND 的持续电流			±75	mA
T_{stg}	贮存温度范围		-65	150	°C

(1) 应力超出*绝对最大额定值*下面列出的值可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，这并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准，所有引脚(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101，所有引脚(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN54AHC273		SN74AHC273		单位
			最小值	最大值	最小值	最大值	
V_{CC}	电源电压		2	5.5	2	5.5	V
V_{IH}	高电平输入电压	V_{CC} = 2V	1.5		1.5		V
		V_{CC} = 3V	2.1		2.1		
		V_{CC} = 5.5V	3.85		3.85		
V_{IL}	低电平输入电压	V_{CC} = 2V		0.5		0.5	V
		V_{CC} = 3V		0.9		0.9	
		V_{CC} = 5.5V		1.65		1.65	
V_I	输入电压		0	5.5	0	5.5	V
V_O	输出电压		0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 2V		-50		-50	μA
		V_{CC} = 3V ± 0.3V		-4		-4	mA
		V_{CC} = 5.5V ± 0.5V		-8		-8	
I_{OL}	低电平输出电流	V_{CC} = 2V		50		50	μA
		V_{CC} = 3V ± 0.3V		4		4	mA
		V_{CC} = 5.5V ± 0.5V		8		8	
Δt/Δv	输入转换上升和下降时间	V_{CC} = 3V ± 0.3V		100		100	ns/V
		V_{CC} = 5.5V ± 0.5V		20		20	

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在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		SN54AHC273		SN74AHC273		单位
		最小值	最大值	最小值	最大值	
T_A	自然通风条件下的工作温度范围	-55	125	-40	125	°C

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告，*CMOS 输入缓慢变化或悬空的影响* (SCBA004)。

5.4 热性能信息

热性能指标(1)		SN74AHC273						单位
		N	DW	NS	DB	PW	DGV	
		20 引脚						
$R_{\theta JA}$	结至环境热阻	53.9	81.1	79.4	98.7	116.8	118.1	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	38.8	48.9	45.9	60.4	58.5	33.4	
$R_{\theta JB}$	结至电路板热阻	34.7	53.8	46.9	56.9	78.7	59.6	
ψ_{JT}	结至顶部特征参数	26.9	19.5	19.1	21.6	12.6	1.1	
ψ_{JB}	结至电路板特征参数	34.7	53.1	46.5	53.5	77.9	58.9	
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	不适用	不适用	

(1) 有关新旧热指标的更多信息，请参阅 TI 应用报告 *IC 封装热指标* (SPRA953)。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			SN54AHC273		SN74AHC273		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = -50μA	2V	1.9			1.9		1.9		V
		3V	2.9			2.9		2.9		
		4.5V	4.4			4.4		4.4		
	I_{OH} = -4mA	3V	2.58			2.48		2.48		
	I_{OH} = -8mA	4.5V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50μA	2V			0.1		0.1		0.1	V
		3V			0.1		0.1		0.1	
		4.5V			0.1		0.1		0.1	
	I_{OL} = 4mA	3V			0.36		0.5		0.44	
	I_{OL} = 8mA	4.5V			0.36		0.5		0.44	
I_I	V_I = 5.5V 或 GND	0V 至 5.5V			±0.1		±1(1)		±1	μA
I_{CC}	V_I = V_{CC} 或 GND I_O = 0	5.5V			4		40		40	μA
C_i	V_I = V_{CC} 或 GND	5V		2.5	10				10	pF

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试（在 V_{CC} = 0V 时）。

5.6 时序要求，V_{CC} = 3.3V ± 0.3V

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

			SN54AHC273				SN74AHC273				单位
			T_A = 25°C		最小值	最大值	T_A = 25°C		最小值	最大值	
			最小值	最大值			最小值	最大值			
t_w	脉冲持续时间	$\overline{CLR}$ 为低电平	5		6		5		6		ns
		CLK 高电平或低电平	5		6.5		5		6.5		

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在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

			SN54AHC273				SN74AHC273				单位
			T_A = 25°C		最小值	最大值	T_A = 25°C		最小值	最大值	
			最小值	最大值			最小值	最大值			
t_{su}	设置时间	CLK ↑ 之前的数据	5.5		6.5		5.5		6.5		ns
		CLK ↑ 之前的 CLR	2.5		2.5		2.5		2.5		
t_h	保持时间，CLK ↑ 后的数据		1.5		2		1		1		ns

5.7 时序要求，V_{CC} = 5V ± 0.5V

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

			SN54AHC273				SN74AHC273				单位
			T_A = 25°C		最小值	最大值	T_A = 25°C		最小值	最大值	
			最小值	最大值			最小值	最大值			
t_w	脉冲持续时间	$\overline{CLR}$ 为低电平	5		5		5		5		ns
		CLK 高电平或低电平	5		5		5		5		
t_{su}	设置时间	CLK ↑ 之前的数据	4.5		4.5		4.5		4.5		ns
		CLK ↑ 之前的 CLR	2		2		2		2		
t_h	保持时间，CLK ↑ 后的数据		1.5		2		1		1		ns

5.8 开关特性，V_{CC} = 3.3V ± 0.3V

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN54AHC273		SN74AHC273		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
f_{max}			C_L = 15pF	75(1)	120(1)		65(1)		65		MHz
			C_L = 50pF	50	75		45		45		
t_{PHL}	$\overline{CLR}$	Q	C_L = 15pF		8.9(1)	13.6(1)	1(1)	16(1)	1	16	ns
t_{PLH}	CKL	Q	C_L = 15pF		8.7(1)	13.6(1)	1(1)	16(1)	1	16	ns
t_{PHL}					8.7(1)	13.6(1)	1(1)	16(1)	1	16	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50pF		11.4	17.1	1	19.5	1	19.5	ns
t_{PLH}	CLK	Q	C_L = 50pF		11.2	17.1	1	19.5	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	1	19.5	ns
$t_{sk(o)}$			C_L = 50pF			1.5(2)				1.5	ns

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。
(2) 对于符合 MIL-PRF-38535 标准的产品，此参数不适用。

5.9 开关特性，V_{CC} = 5V ± 0.5V

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN54AHC273		SN74AHC273		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
f_{max}			C_L = 15pF	120(1)	165(1)		100(1)		100		MHz
			C_L = 50pF	80	110		70		70		
t_{PHL}	$\overline{CLR}$	Q	C_L = 15pF		5.2(1)	8.5(1)	1(1)	10(1)	1	10	ns
t_{PLH}	CKL	Q	C_L = 15pF		5.8(1)	9(1)	1(1)	10.5(1)	1	10.5	ns
t_{PHL}					5.8(1)	9(1)	1(1)	10.5(1)	1	10.5	
t_{PHL}	$\overline{CLR}$	Q	C_L = 50pF		6.7	10.5	1	12	1	12	ns

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在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN54AHC273		SN74AHC273		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	CLK	Q	C_L = 50pF		7.3	11	1	12.5	1	12.5	ns
t_{PHL}					7.3	11	1	12.5	1	12.5	ns
$t_{sk(o)}$			C_L = 50pF			1(2)				1	ns

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。
(2) 对于符合 MIL-PRF-38535 标准的产品，此参数不适用。

5.10 噪声特性

V_{CC} = 5 V，C_L = 50pF，T_A = 25°C

参数		SN74AHC273			单位
		最小值	典型值	最大值	
$V_{OL(P)}$	安静输出，最大动态 V_{OL}		0.7		V
$V_{OL(V)}$	安静输出，最小动态 V_{OL}		-0.7		V
$V_{OH(V)}$	安静输出，最小动态 V_{OH}		4.7		V
$V_{IH(D)}$	高电平动态输入电压	3.5			V
$V_{IL(D)}$	低电平动态输入电压			1.5	V

5.11 工作特性

T_A = 25°C

参数		测试条件		典型值	单位
C_{pd}	功率耗散电容	无负载，	f = 1 MHz	31	pF

5.12 典型特性

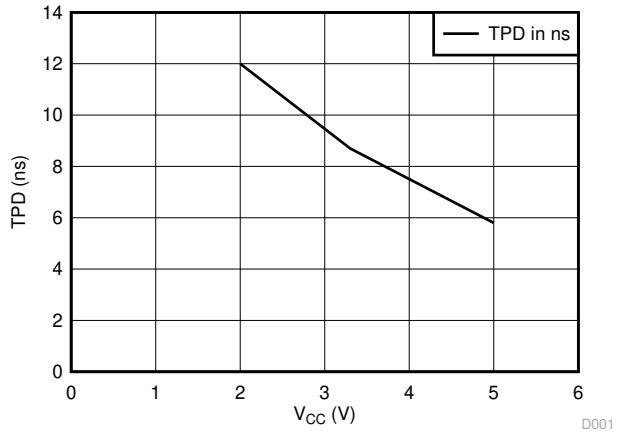


图 5-1. TPD 与 V_{CC} 间的关系

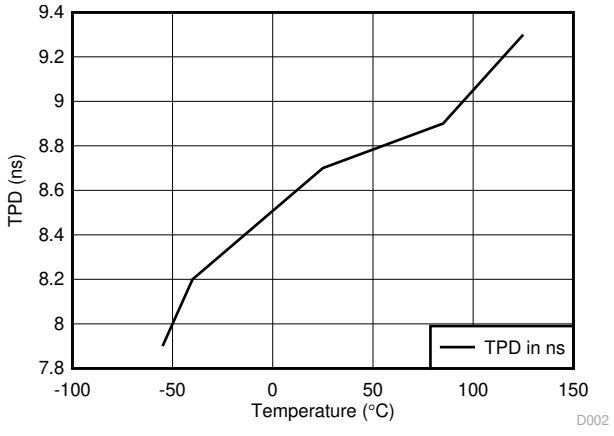
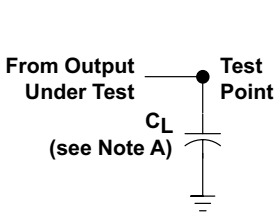
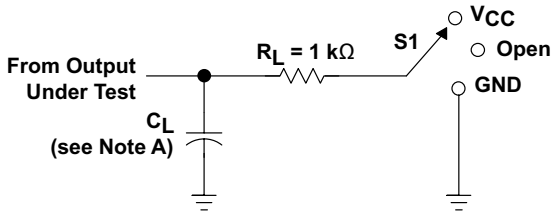


图 5-2. TPD 与温度间的关系

6 参数测量信息

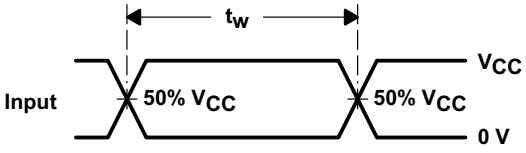


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

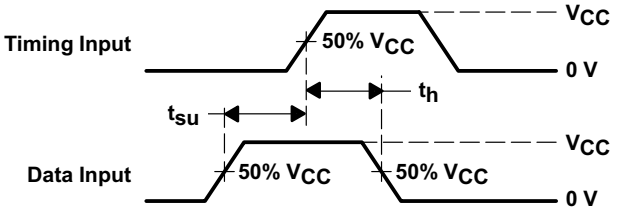


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

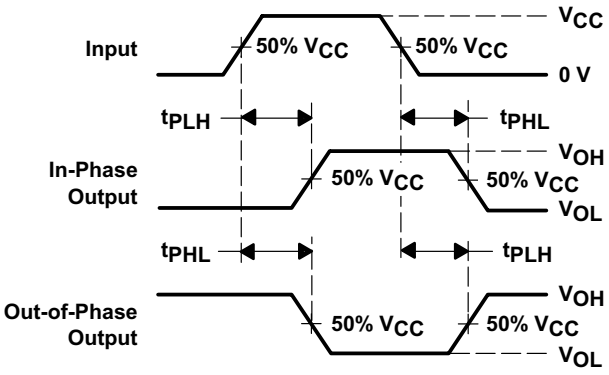
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



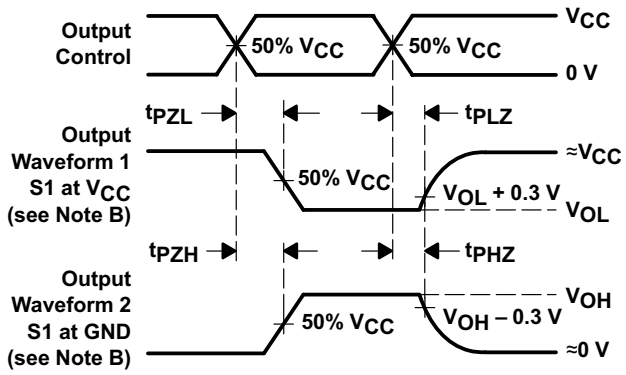
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. 负载电路和电压波形

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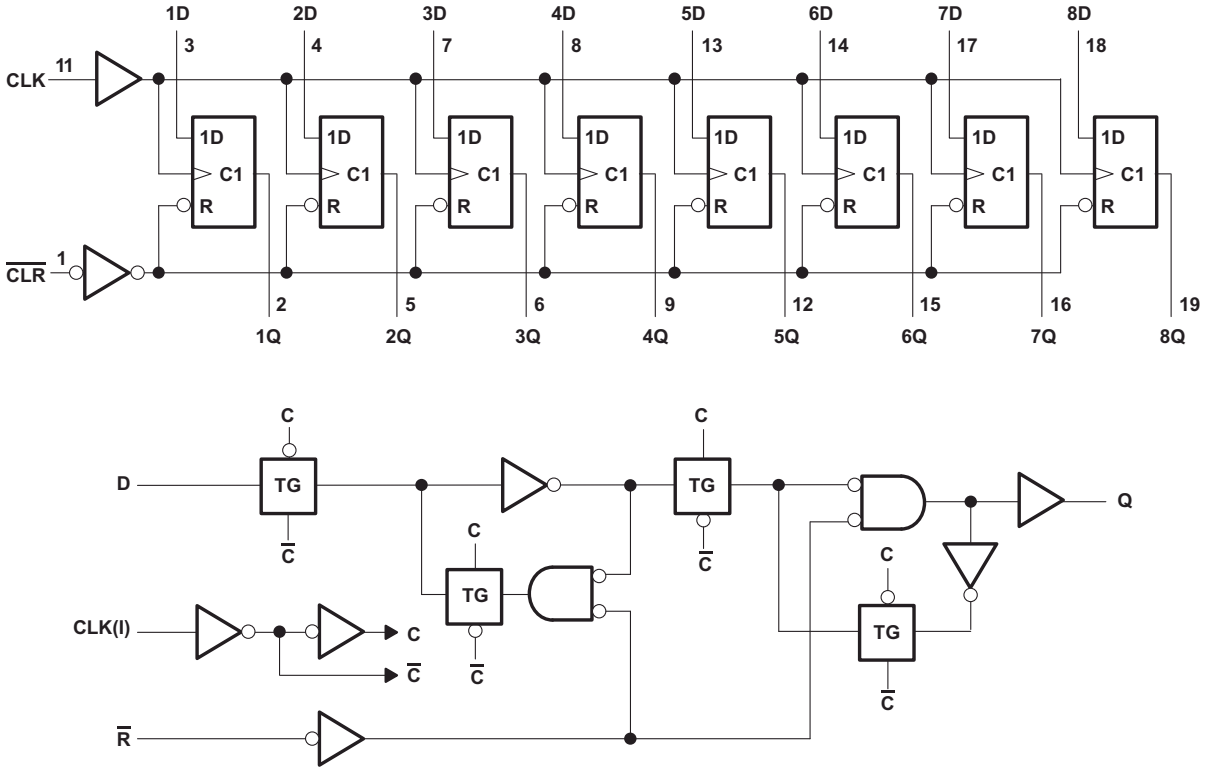
7 详细说明

7.1 概述

这些电路是正边沿触发式 D 类触发器，具有直接清零 ($\overline{CLR}$) 输入。数据 (D) 输入上满足设置时间要求的信息被发送到时钟 (CLK) 脉冲正向边沿上的 Q 输出。时钟触发在一个特定电压电平下发生，并且不与正向脉冲的转换时间直接相关。当 CLK 处于高电平或低电平时，D 输入对输出无影响。

输入可耐受 5V 电压并可由 5V 器件驱动。此特性允许在混合 5V 至 3.3V 系统环境中将这些器件用作降压转换器。

7.2 功能方框图



7.3 特性说明

- 宽工作电压范围
  - 可在 2V 至 5.5V 范围内工作
- 支持降压转换
  - 输入支持高达 5.5V 电压
- 慢速边沿速率可更大限度减少输出振铃

7.4 器件功能模式

表 7-1. 功能表

输入			输出
$\overline{CLR}$	CLK	D	Y
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

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8 应用和实施

8.1 应用信息

SNx4AHC273 是一款低驱动 CMOS 器件，可用于需要考虑输出振铃的多种应用。低驱动和慢速边沿速率将更大限度地减少输出上的过冲和下冲。在任何有效的 V_{CC} 下，输入可耐受 5.5V 电压。此特性使得该器件非常适合降压转换至 V_{CC} 电平。图 8-2 展示了该器件与更高驱动器件（如交流驱动）相比的振铃降低。

8.2 典型应用

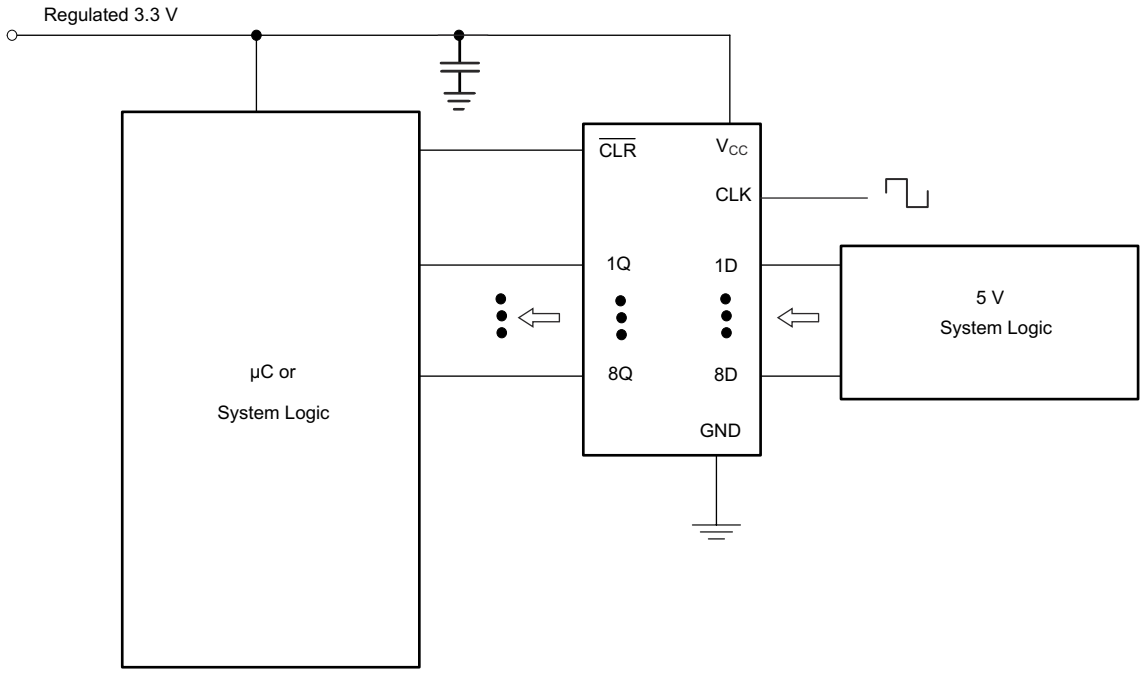


图 8-1. 特定应用原理图

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件
   - 上升时间和下降时间规格：请参阅 *节 5.3* 中的 ($\Delta t/\Delta V$)。
   - 指定的高电平和低电平：请参阅 *节 5.3* 表中的 (V_{IH} 和 V_{IL})。
   - 输入具有过压容限，允许它们在任何有效 V_{CC} 下高达 5.5V
2. 建议的输出条件
   - 每个输出的负载电流不应超过 25mA，该器件的总电流不应超过 75mA
   - 输出不应被拉至高于 V_{CC}

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8.2.3 应用曲线

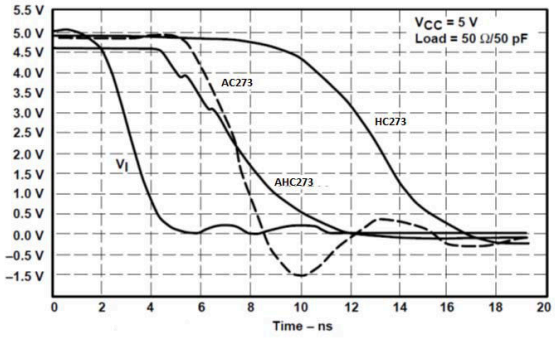


图 8-2. 开关特性比较

8.3 电源相关建议

电源可以是 *建议运行条件* 表中最小和最大电源电压额定值之间的任何电压。

每个 VCC 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 µf；如果有多个 VCC 引脚，则建议每个电源引脚使用 0.01 µf 或 0.022 µf。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µf 和 1 µf 通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，输入决不能悬空。

在许多情况下，数字逻辑器件的功能或部分功能未被使用（例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时）。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的运行状态。图 8-3 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应为任何特定未使用输入施加的逻辑电平取决于器件的功能。通常，将这些输入连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。浮动输出通常是可以接受的，除非该器件是收发器。

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8.4.2 布局示例

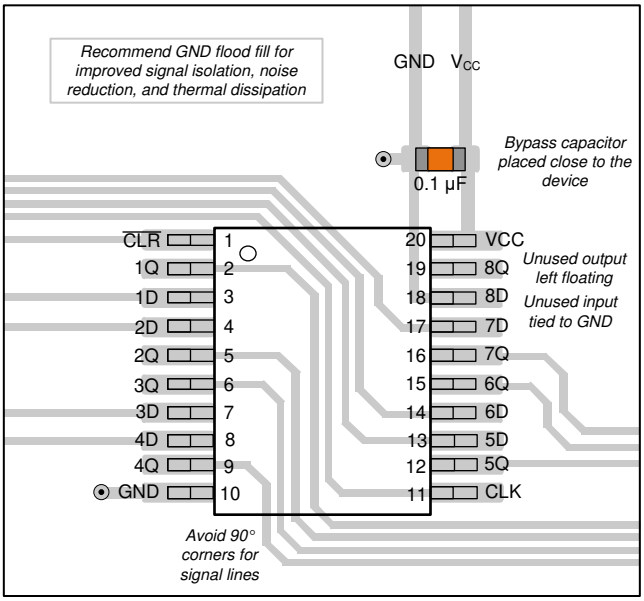


图 8-3. 布局图

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9 器件和文档支持

9.1 文档支持

9.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 9-1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
SN54AHC273	点击此处	点击此处	点击此处	点击此处	点击此处
SN74AHC273	点击此处	点击此处	点击此处	点击此处	点击此处

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

Changes from Revision I (March 2015) to Revision J (July 2024)	Page
• 向*器件信息* 表中添加了 NS 封装	1
• 更新了 R θ JA 值：PW 封装由 104.7 更新为 116.8，DW 封装由 81.8 更新为 81.1；更新了 PW 和 DW 封装的 R θ JC(top)、R θ JB、ΨJT、ΨJB 和 R θ JC(bot)，所有值均以 °C/W 为单位	5
• 更新了*布局示例* 图像	12

Changes from Revision H (July 2014) to Revision I (March 2015)	Page
• 将 V_{OH} 的测试条件 I_{OH} 从 mA 更改为 μA，以修复印刷错误	5

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9853001QRA	Last Time Buy	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9853001QR A SNJ54AHC273J
5962-9853001QSA	Last Time Buy	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9853001QS A SNJ54AHC273W
SN74AHC273DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273
SN74AHC273DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273
SN74AHC273DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273
SN74AHC273DGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273
SN74AHC273DGVR.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273
SN74AHC273DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	AHC273
SN74AHC273DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273
SN74AHC273DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273
SN74AHC273N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC273N
SN74AHC273N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC273N
SN74AHC273NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273
SN74AHC273NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273
SN74AHC273PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	HA273
SN74AHC273PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273
SN74AHC273PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273
SN74AHC273RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273
SNJ54AHC273J	Last Time Buy	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9853001QR A SNJ54AHC273J
SNJ54AHC273W	Last Time Buy	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9853001QS A SNJ54AHC273W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC273, SN74AHC273 :

- Catalog : SN74AHC273
- Automotive : SN74AHC273-Q1, SN74AHC273-Q1
- Military : SN54AHC273

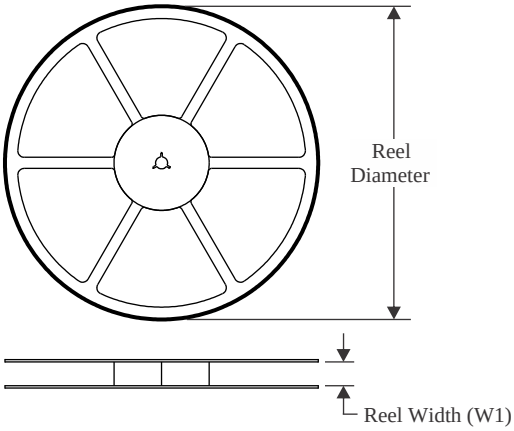
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

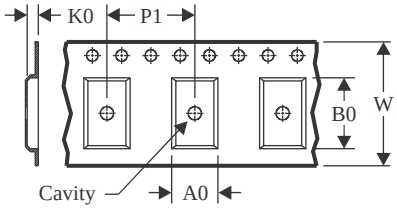
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

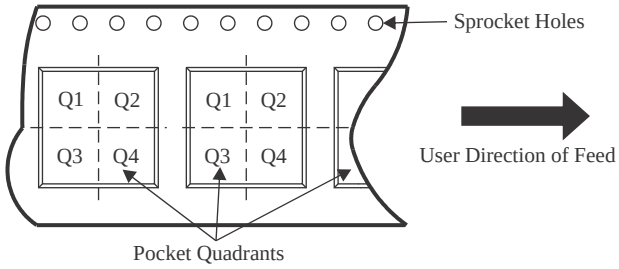


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

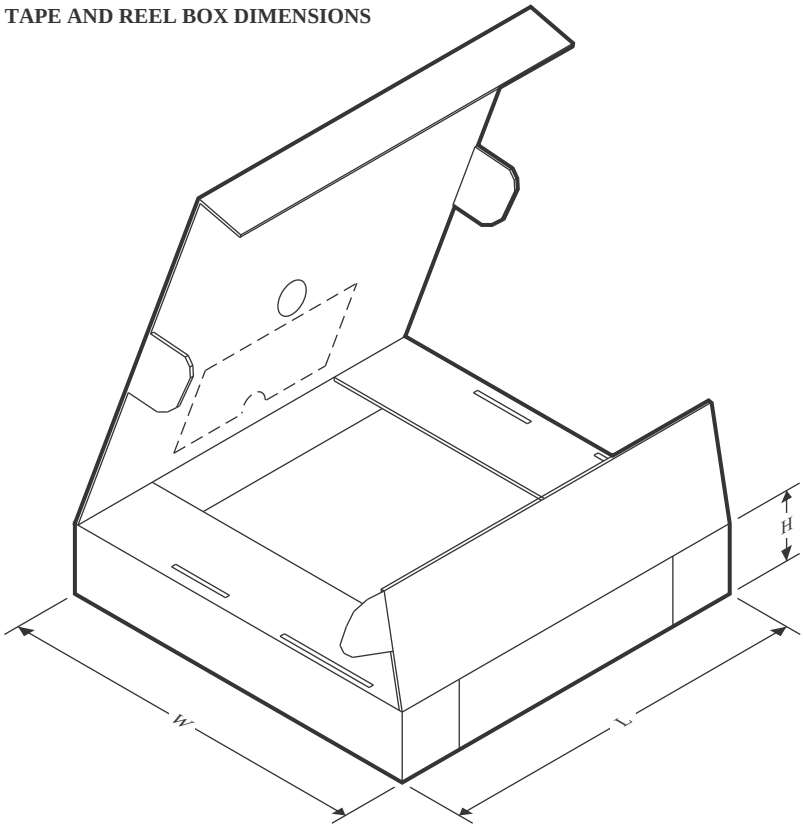
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC273DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHC273DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC273DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC273NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC273RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

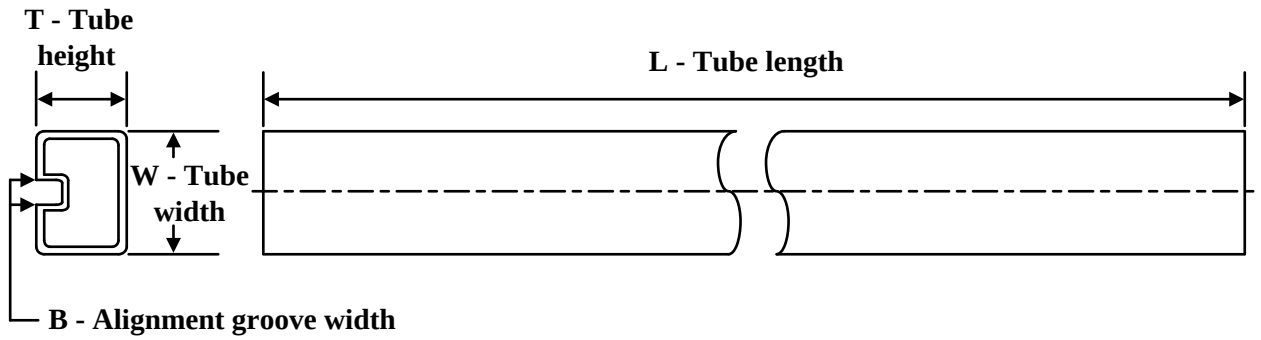
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC273DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHC273DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHC273DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74AHC273DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC273DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC273NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHC273PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC273RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

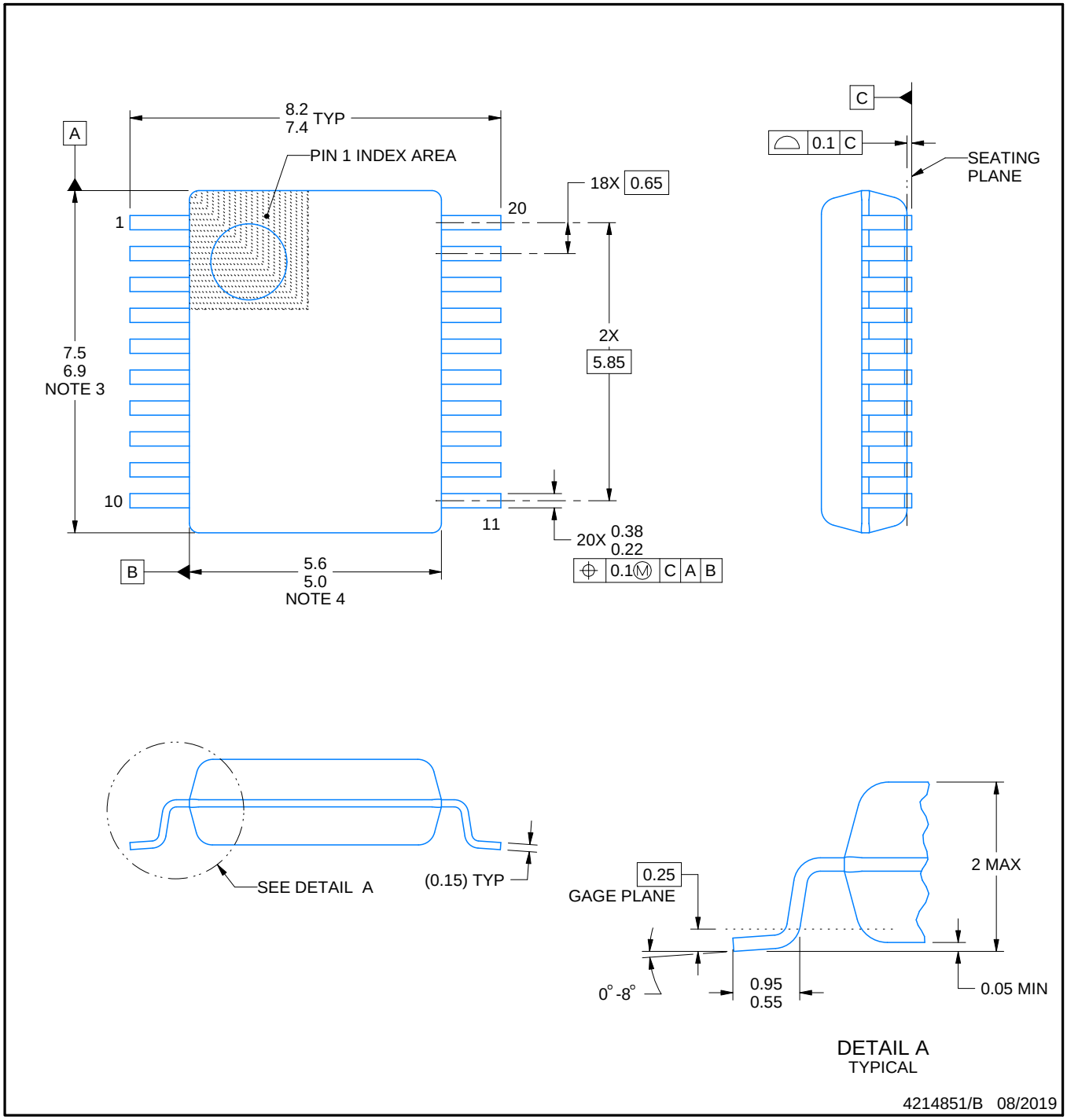
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9853001QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC273N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC273N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC273W	W	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DB0020A

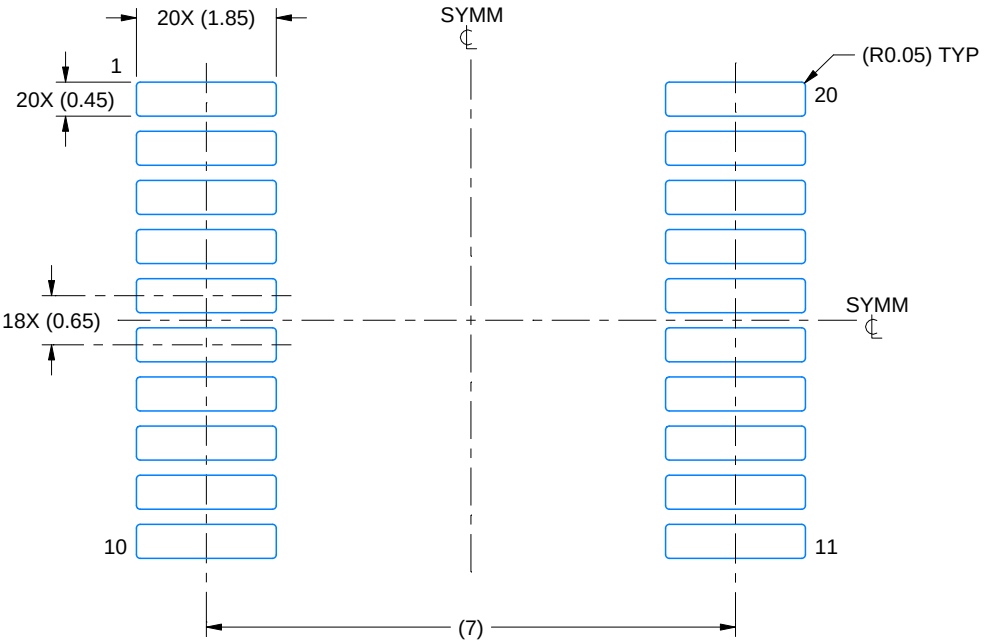
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

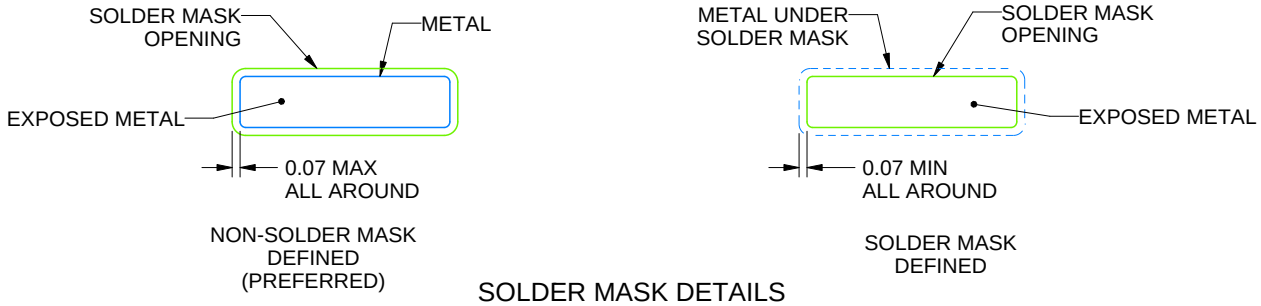


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

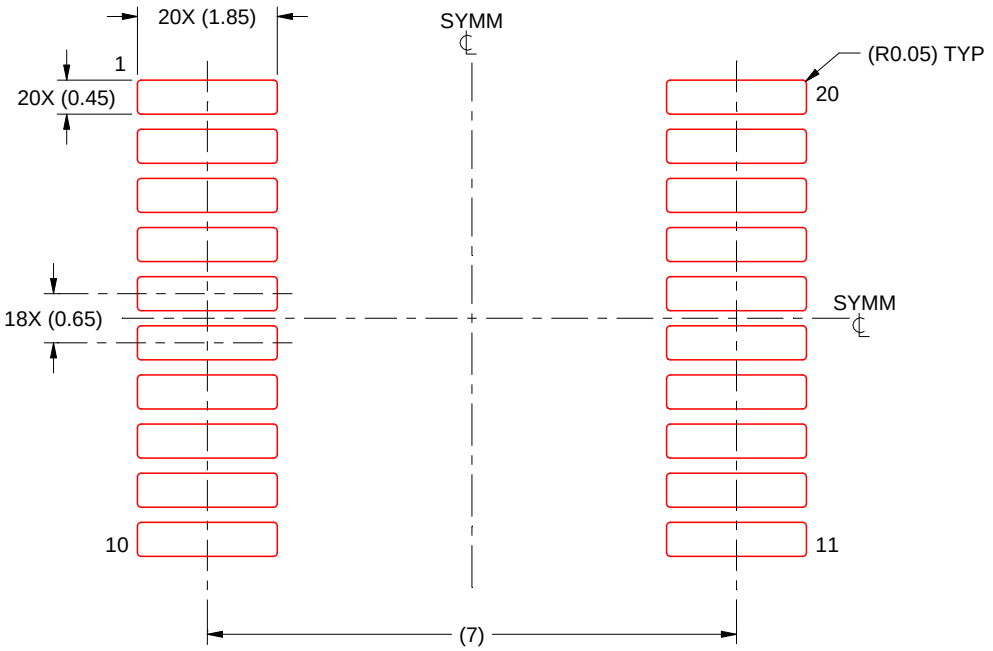
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

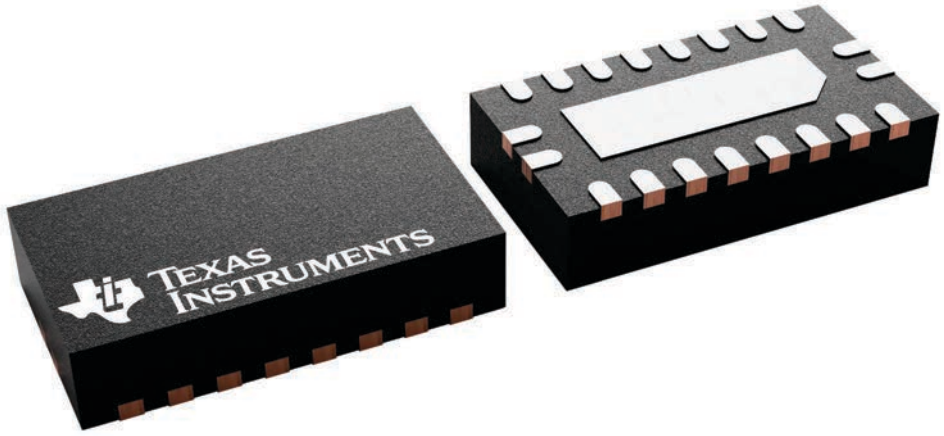
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

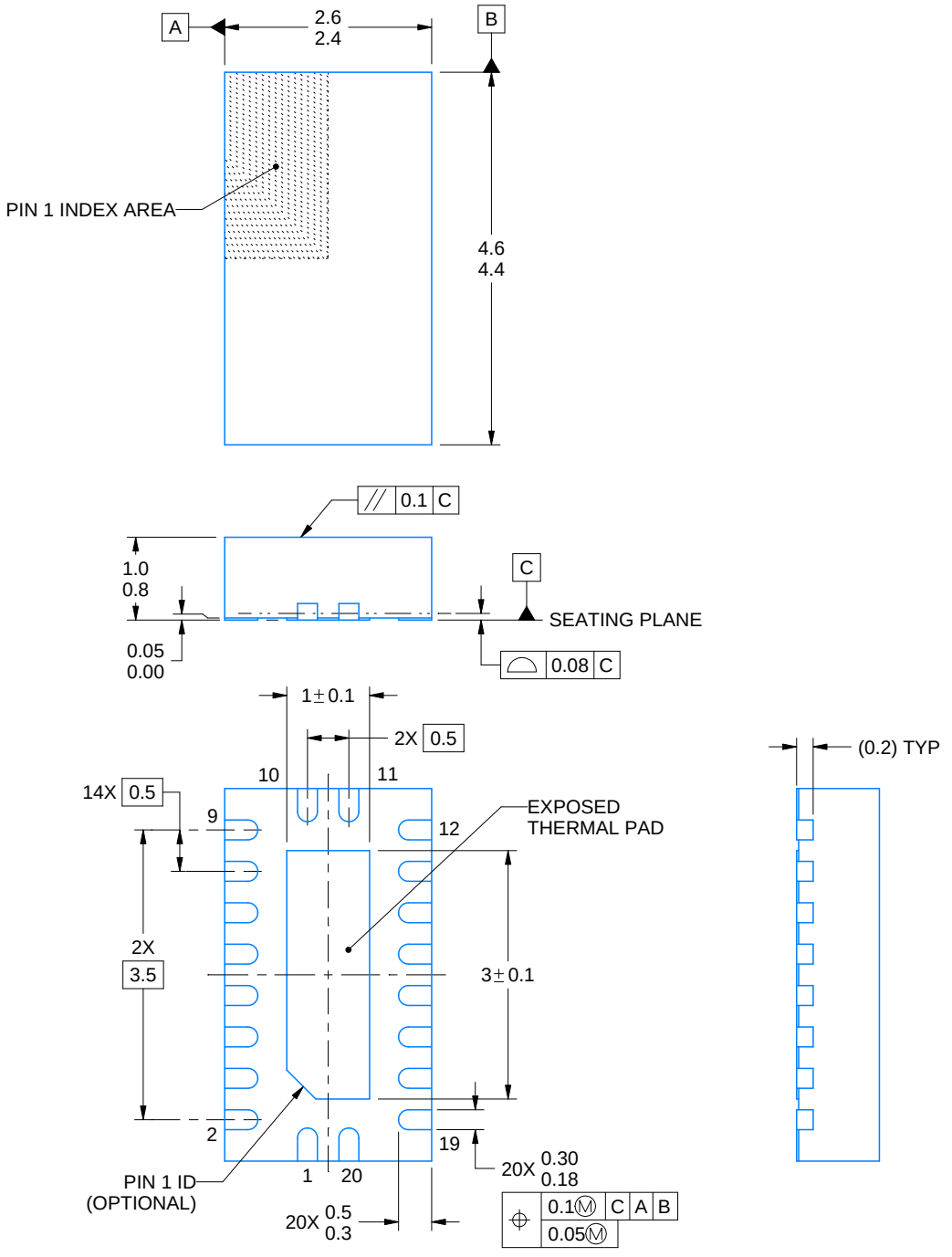


PACKAGE OUTLINE

RKS0020A

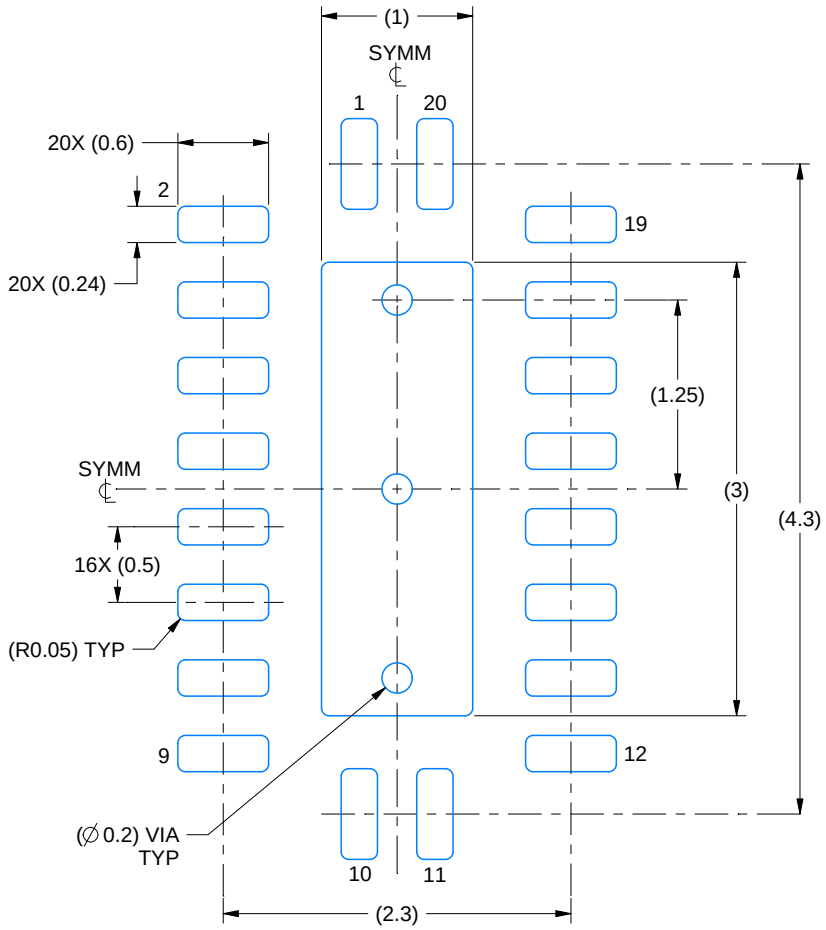
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

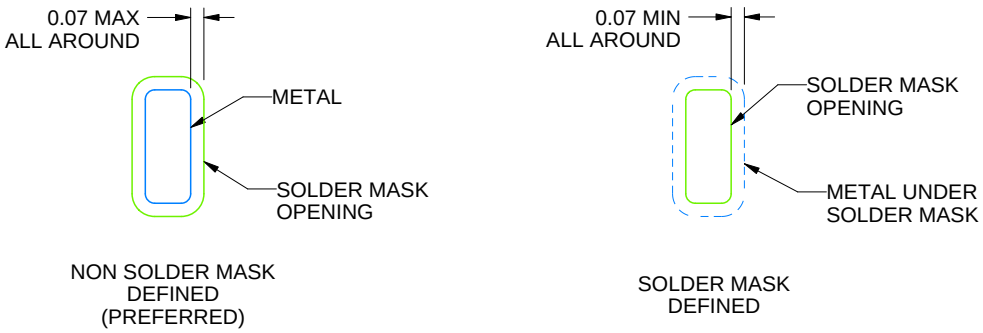


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

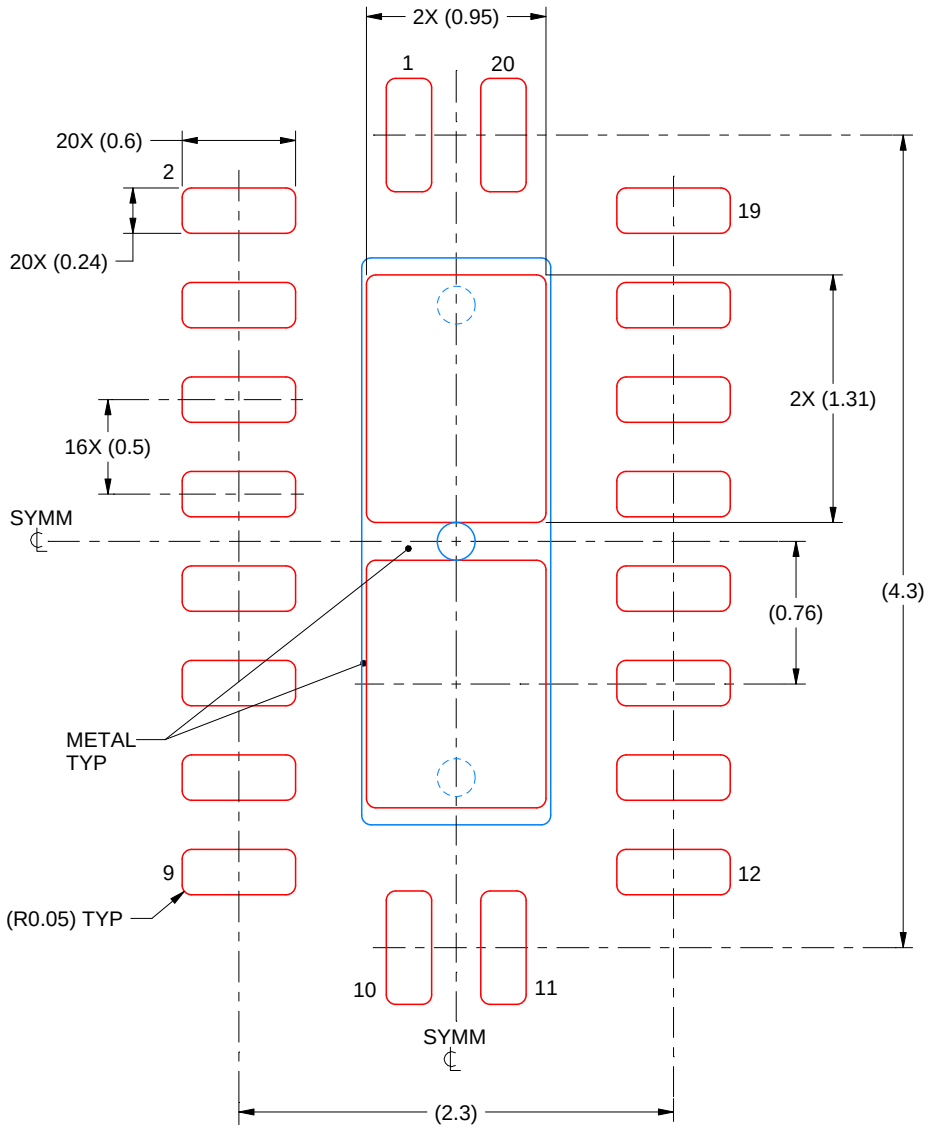


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

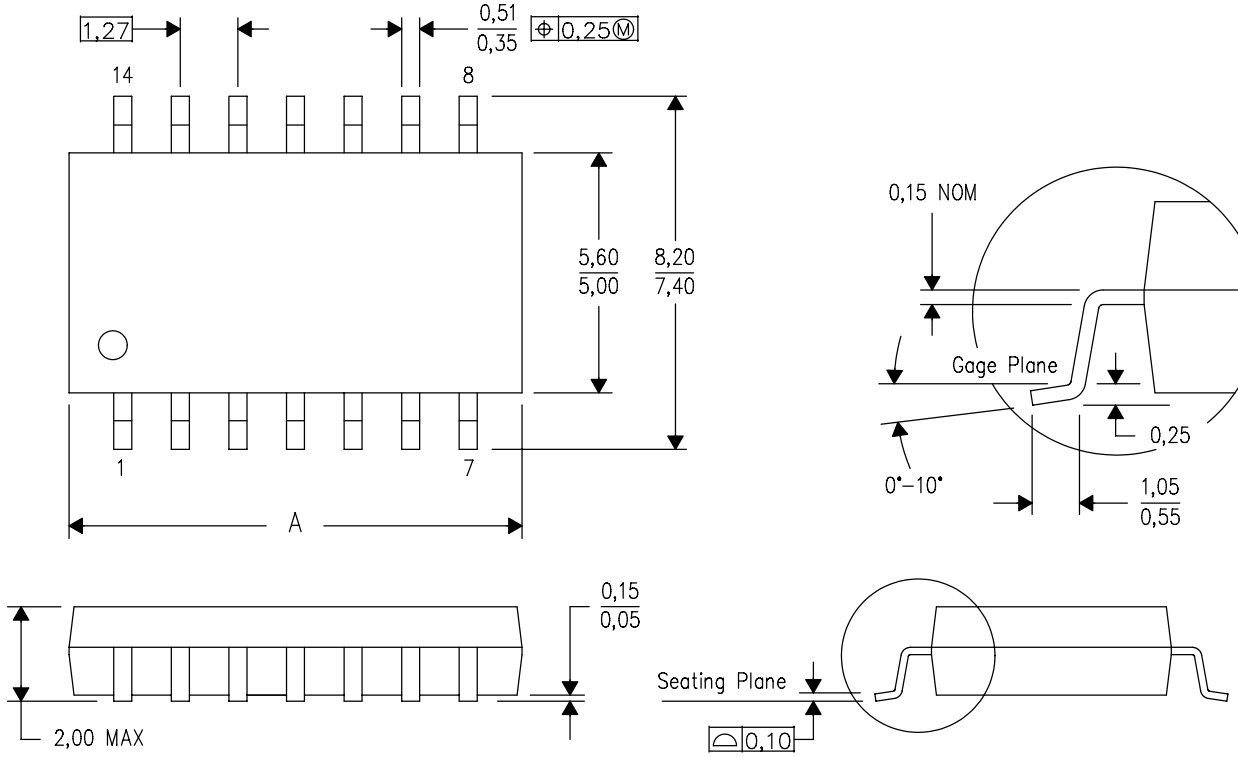
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

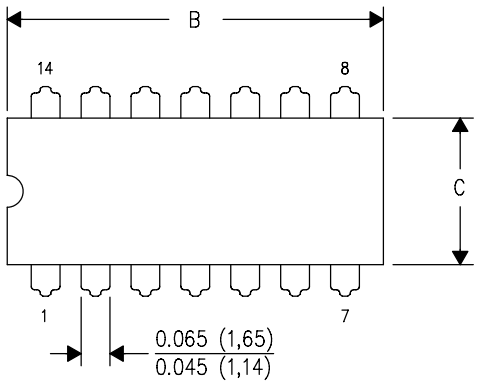
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

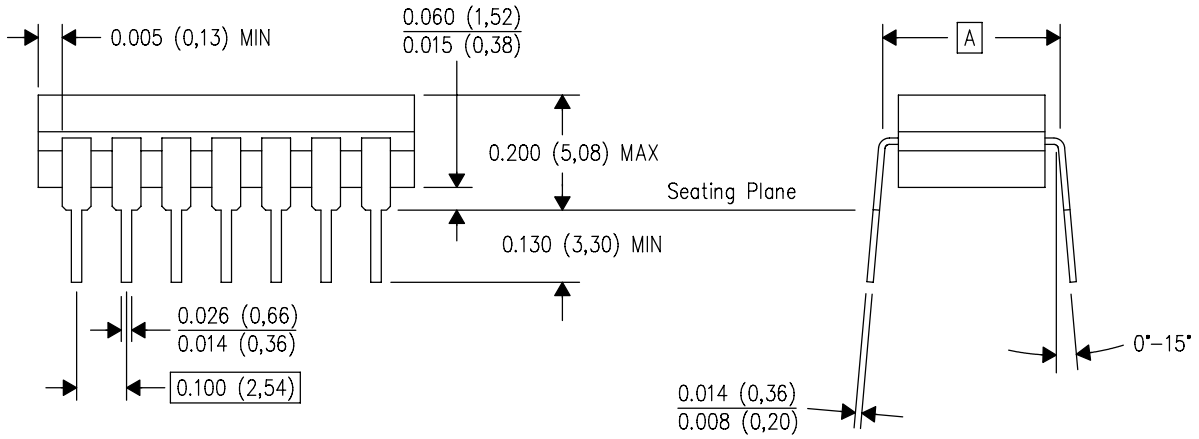
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

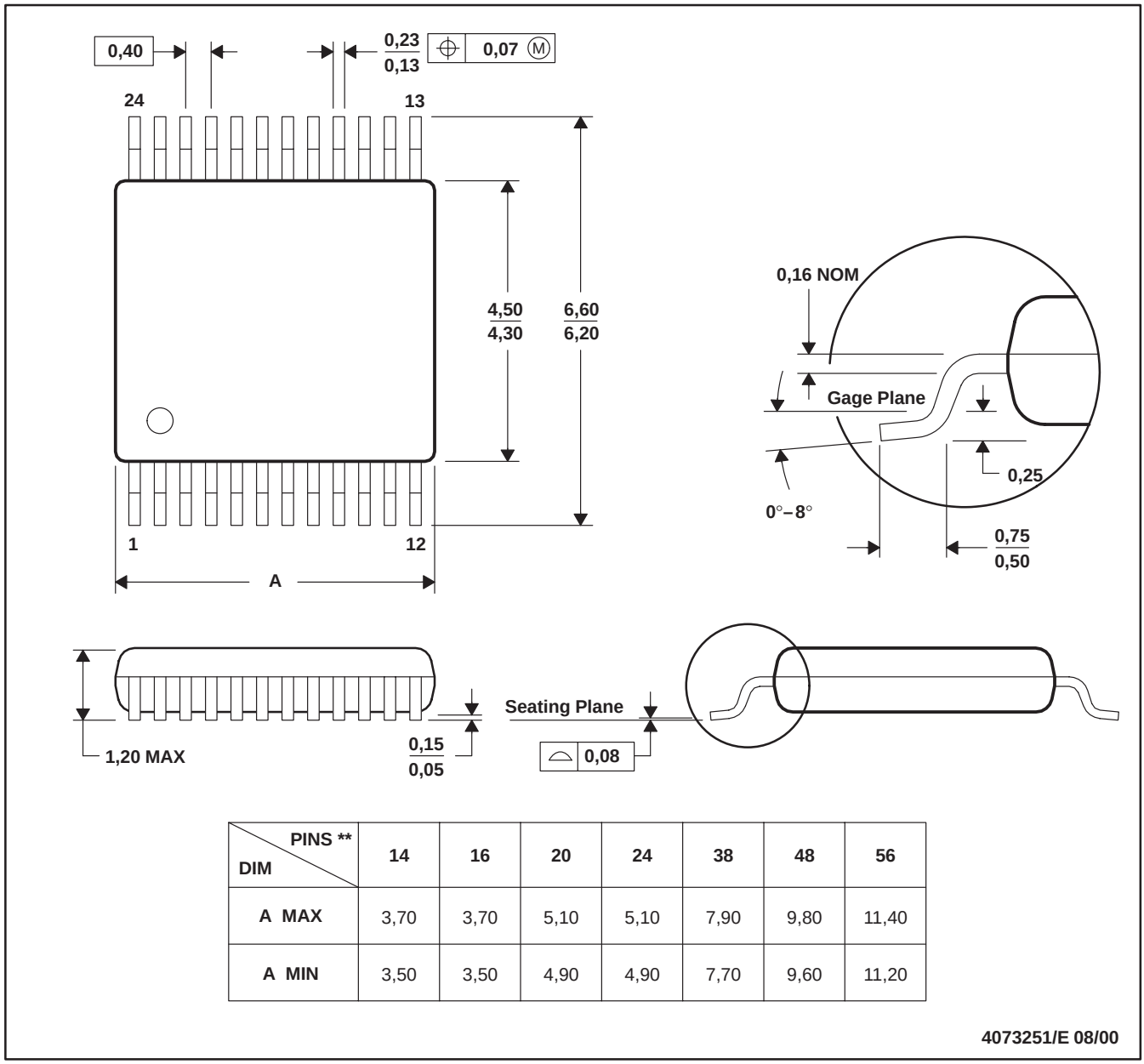


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

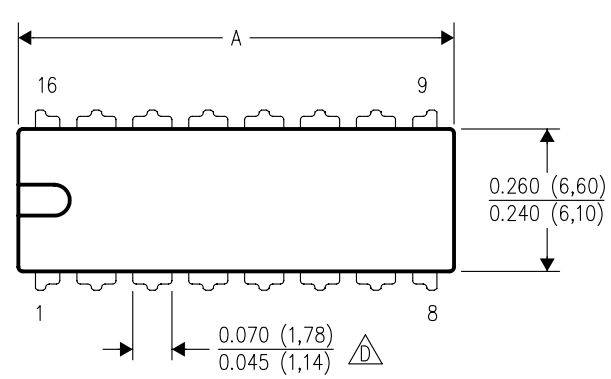
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

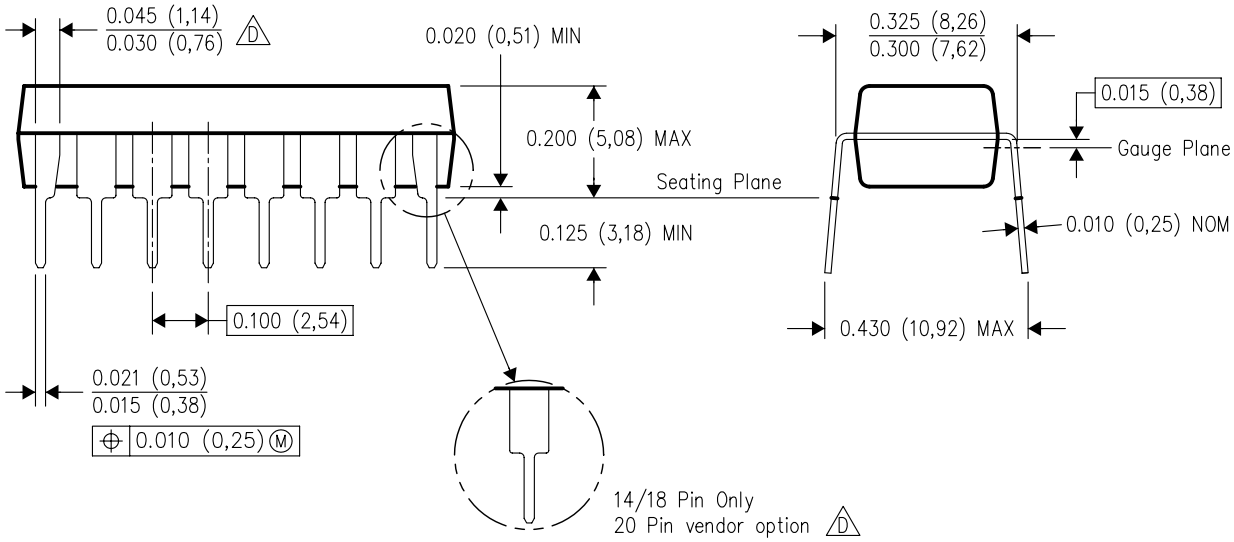
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

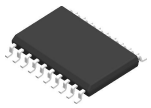


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

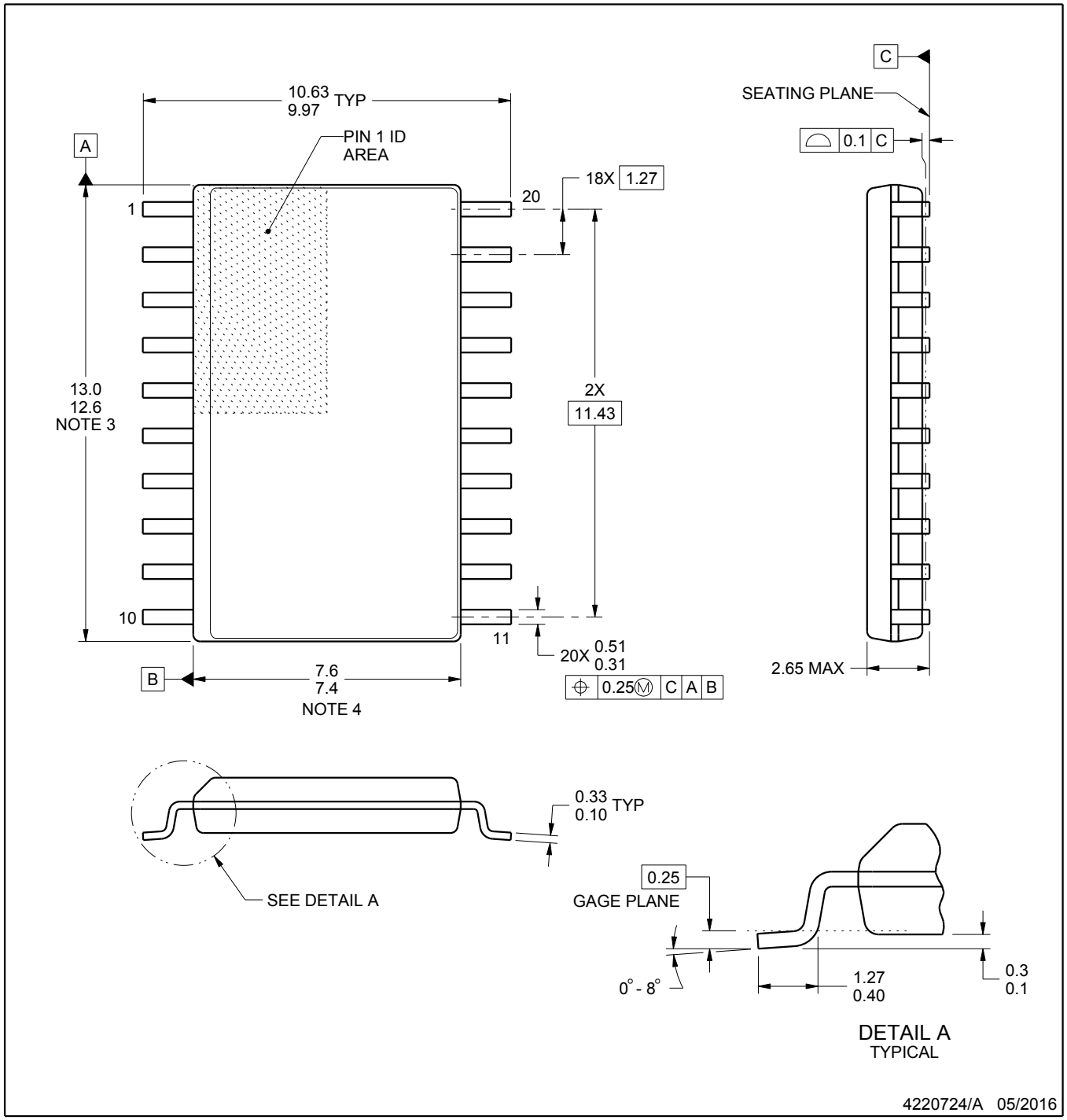


PACKAGE OUTLINE

DW0020A

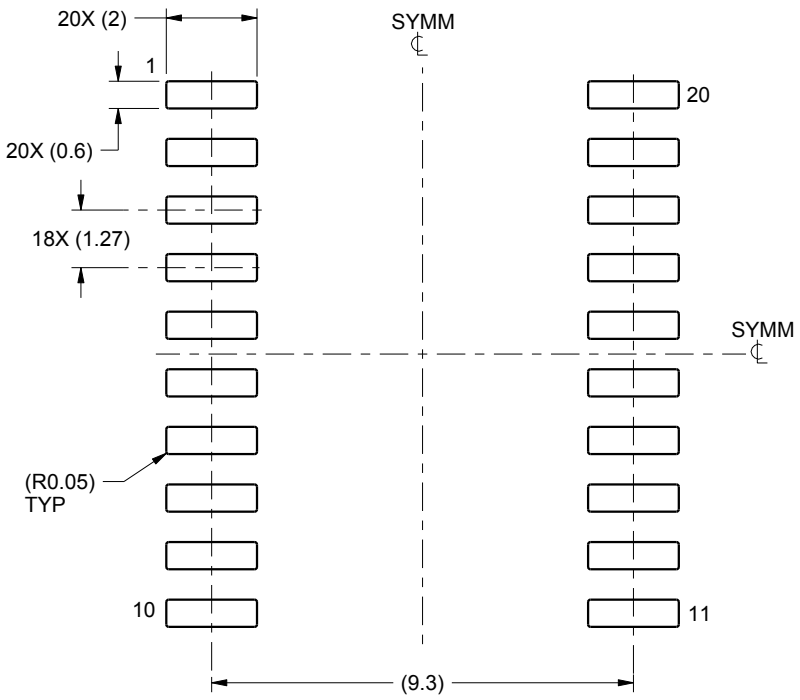
SOIC - 2.65 mm max height

SOIC

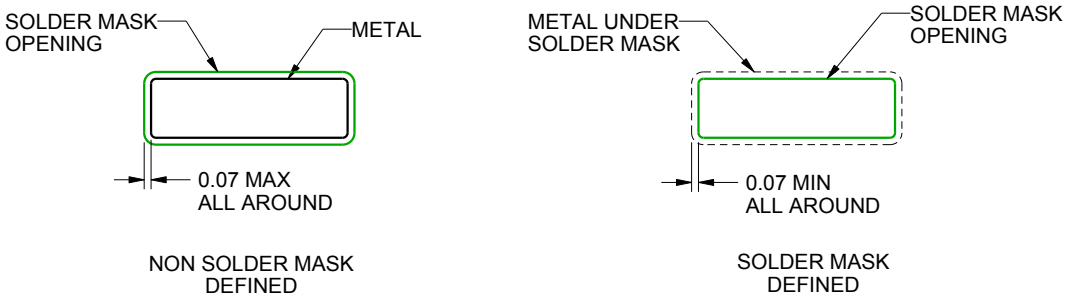


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

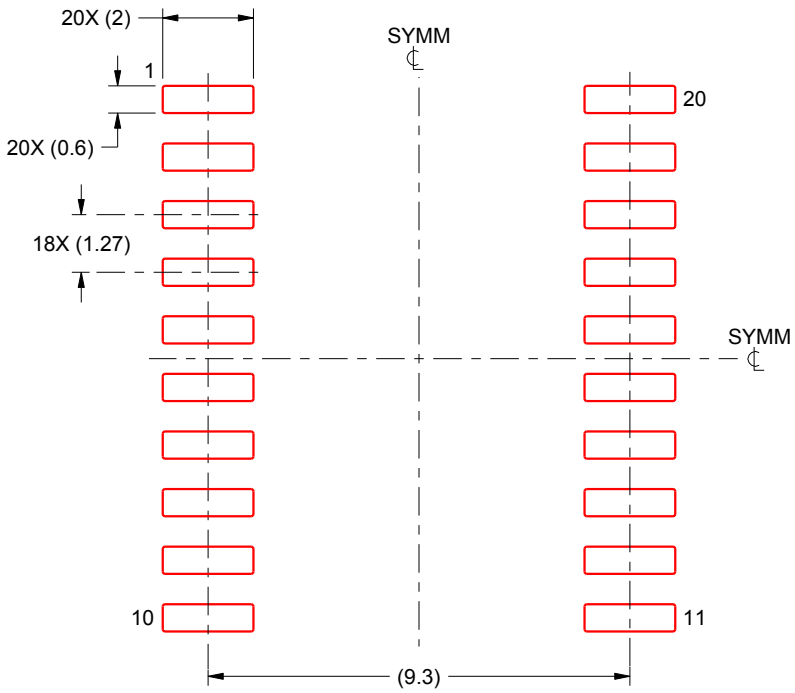


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



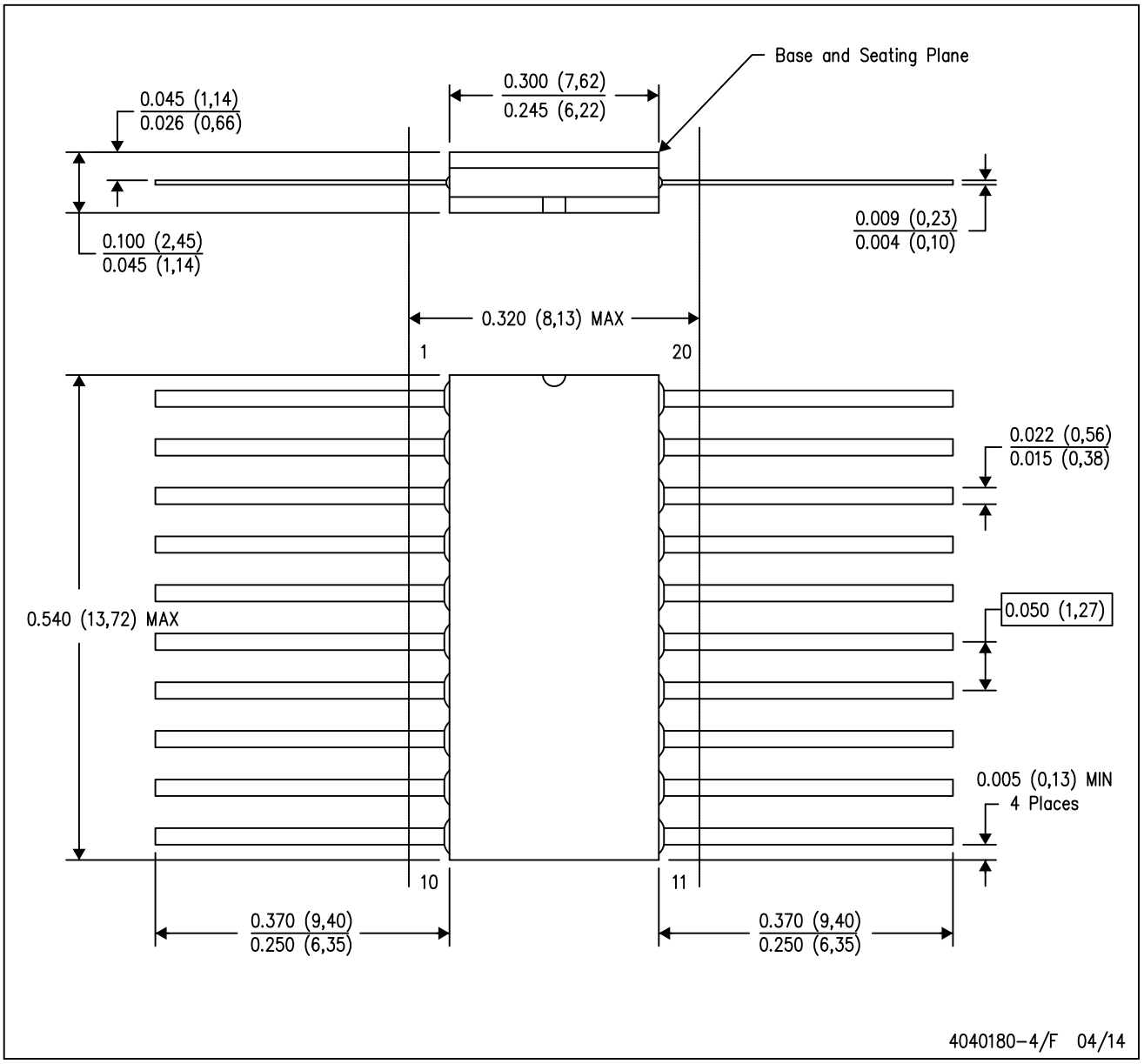
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



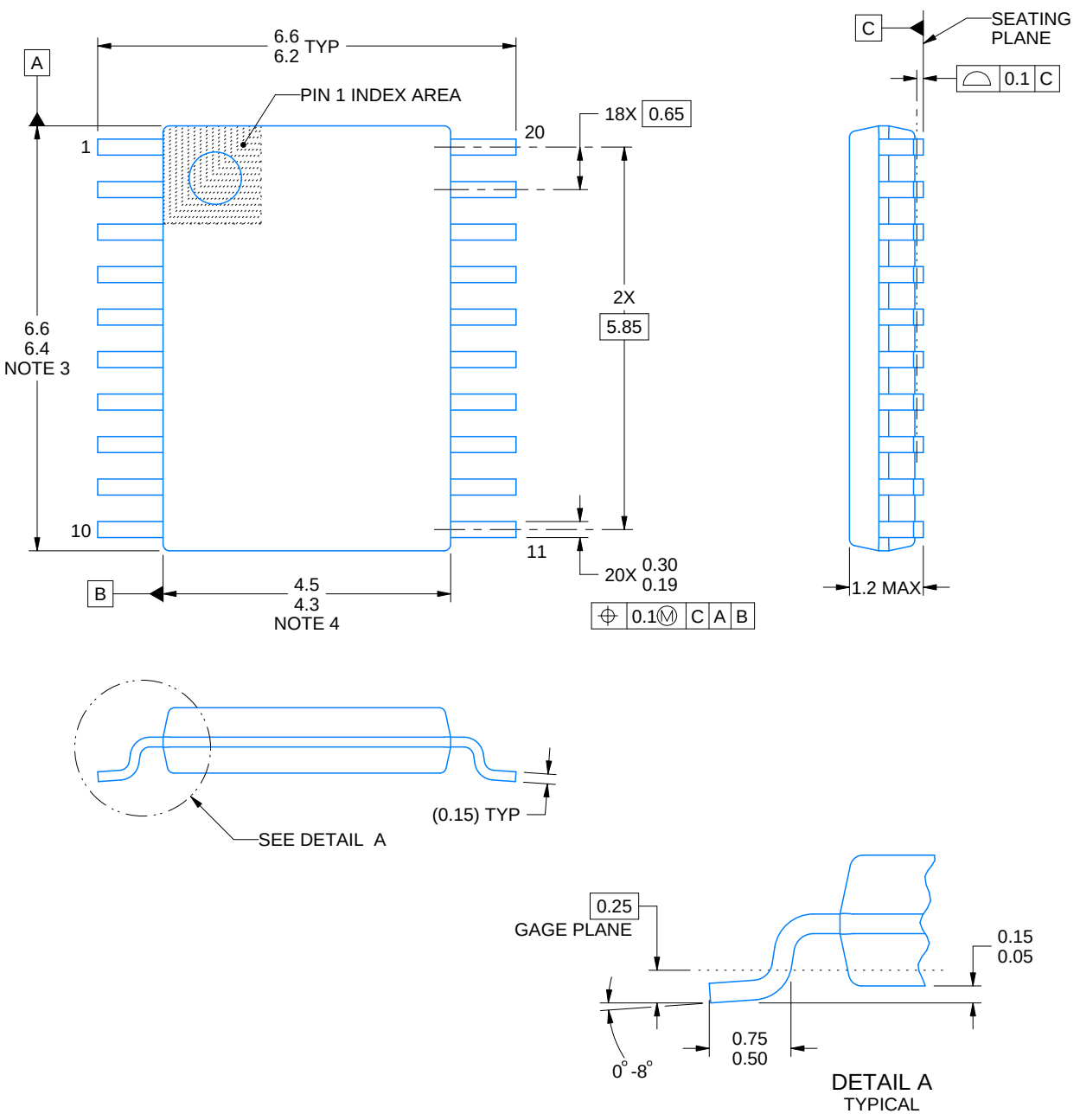
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

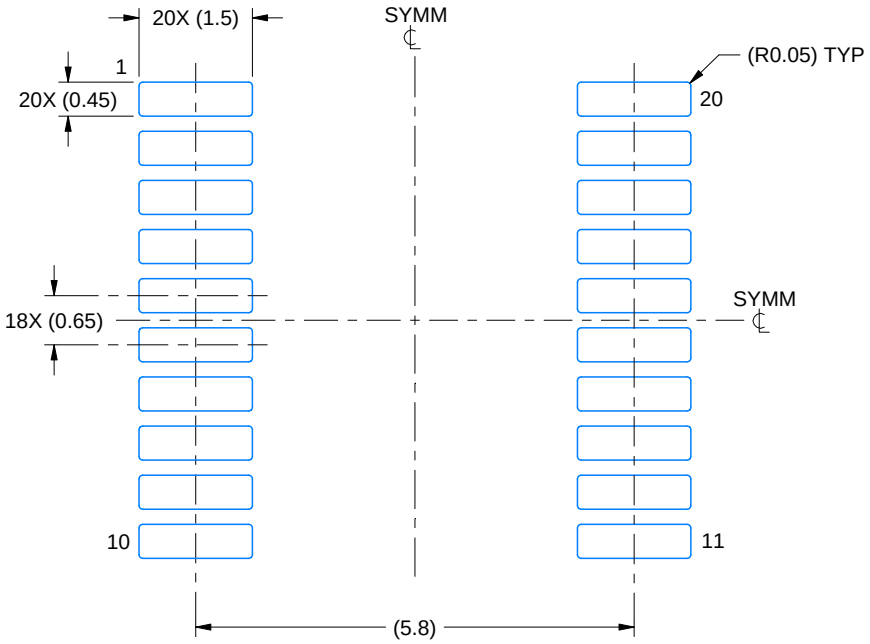
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

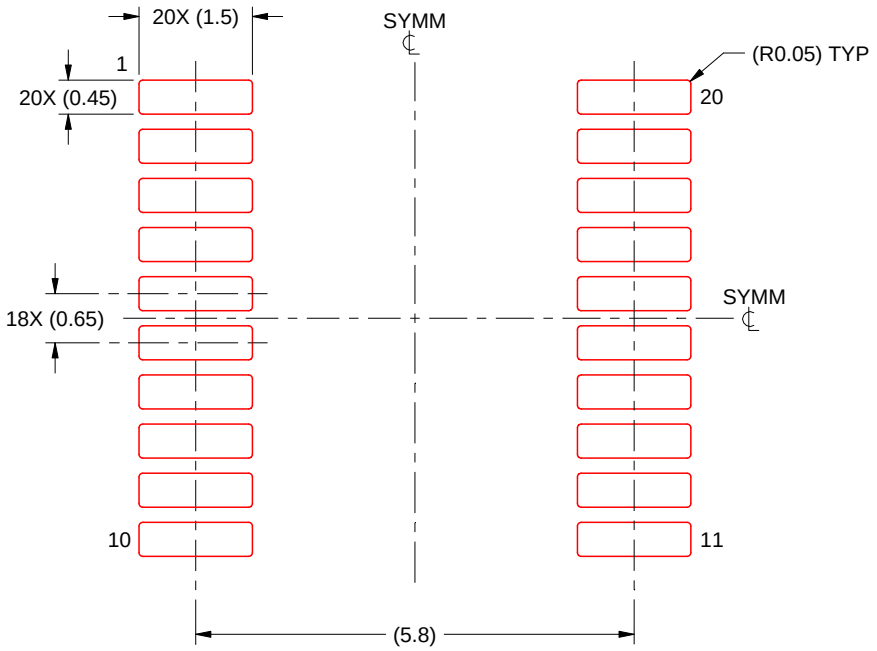


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

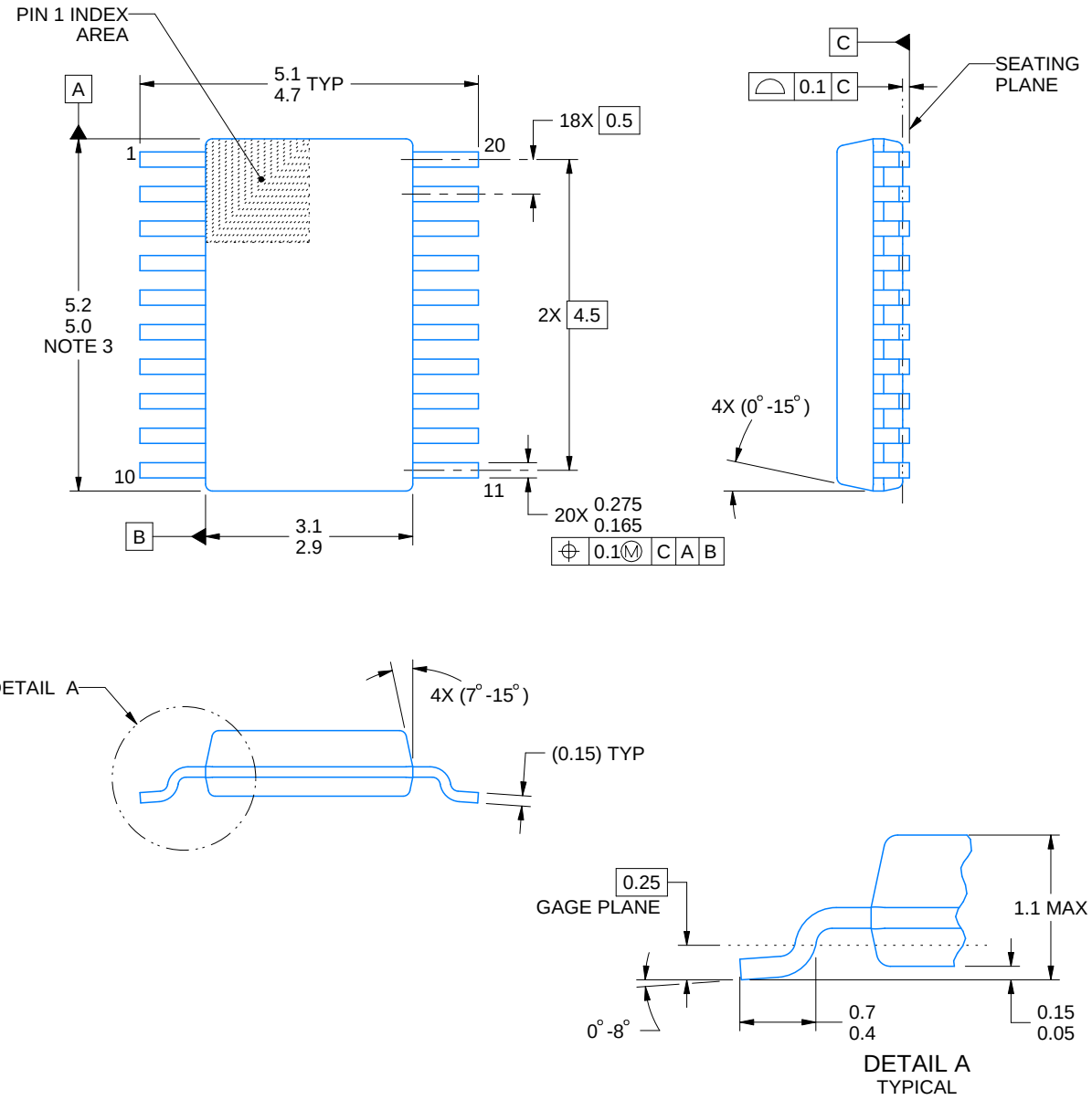
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

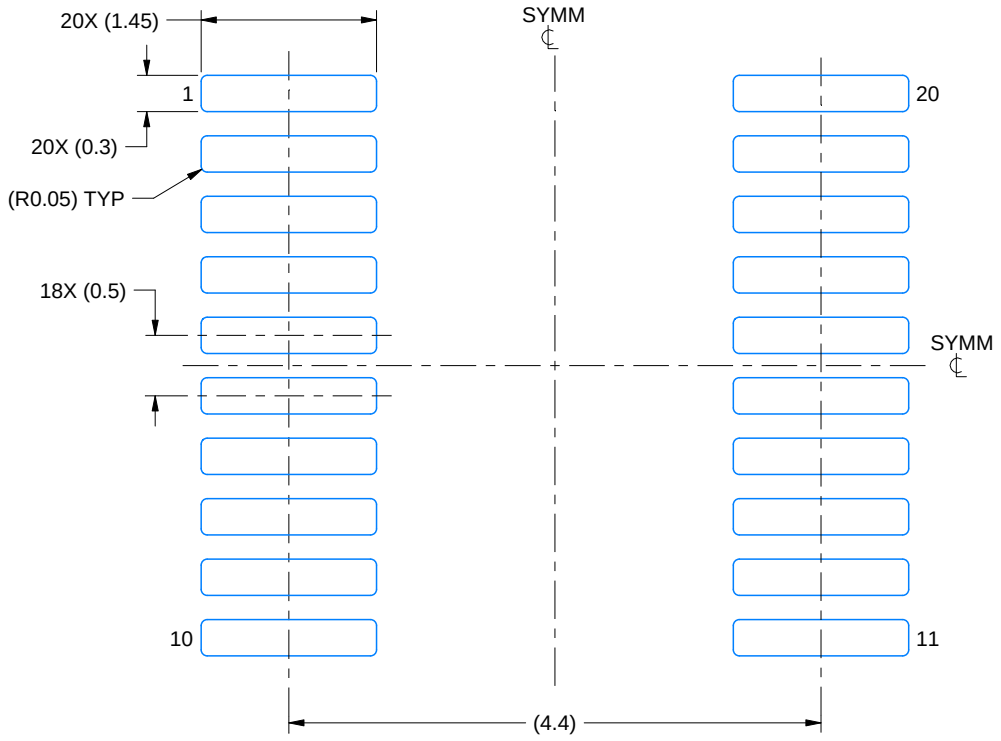
SMALL OUTLINE PACKAGE



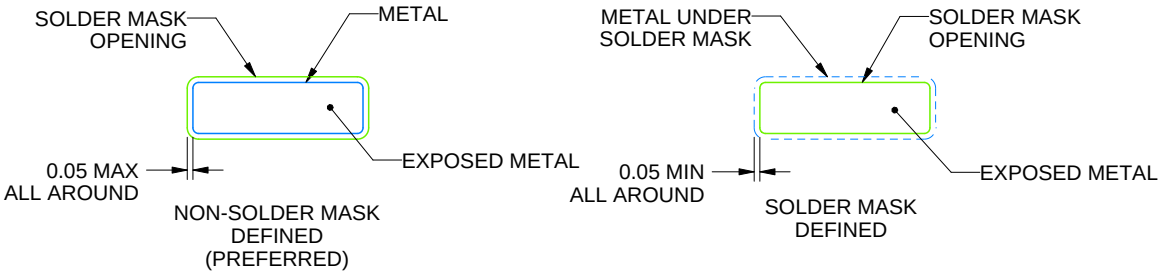
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

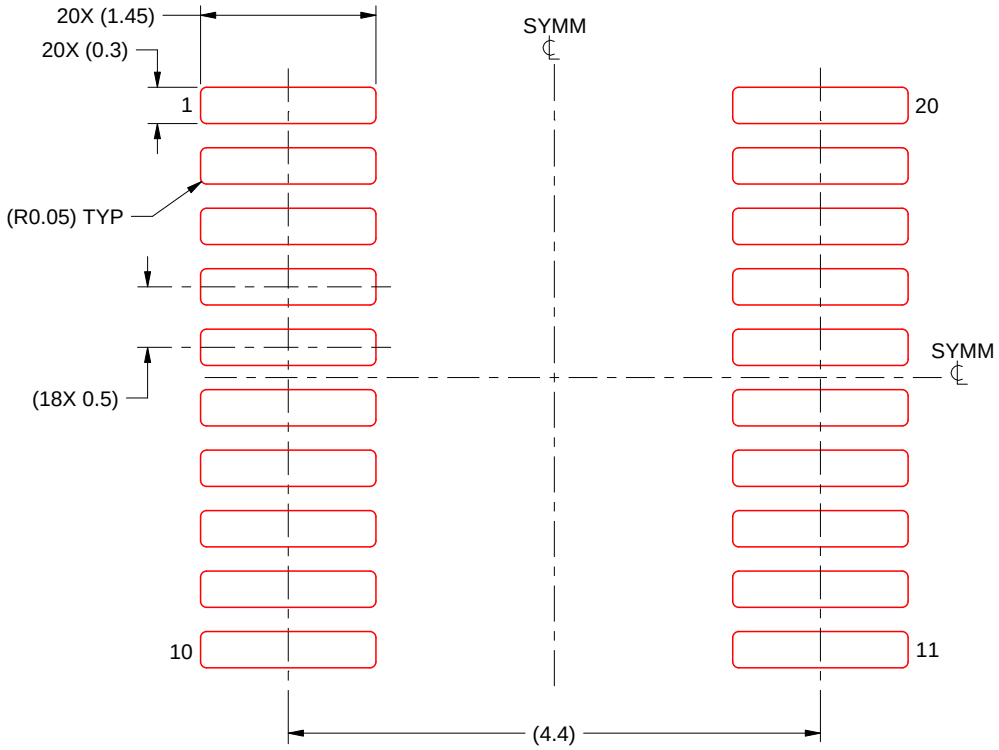


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月