

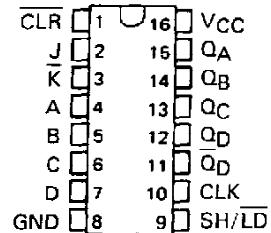
**SN54195, SN54LS195A, SN54S195,  
SN74195, SN74LS195A, SN74S195**  
**4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

MARCH 1974—REVISED MARCH 1988

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and  $\bar{K}$  Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High Performance:  
Accumulators/Processors  
Serial-to-Parallel, Parallel-to-Serial  
Converters

**SN54195, SN54LS195A, SN54S195 . . . J OR W PACKAGE**  
**SN74195 . . . N PACKAGE**  
**SN74LS195A, SN74S195 . . . D OR N PACKAGE**

(TOP VIEW)

**description**

These 4-bit registers feature parallel inputs, parallel outputs, J- $\bar{K}$  serial inputs, shift/load (SH/LD) control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

Parallel (broadside) load

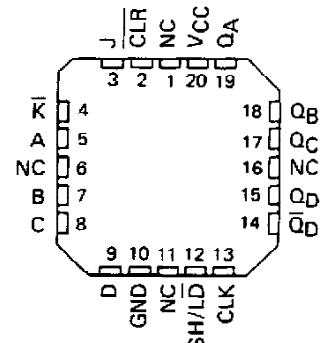
Shift (in the direction QA toward QD)

Parallel loading is accomplished by applying the four bits of data and taking SH/LD low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when SH/LD is high. Serial data for this mode is entered at the J- $\bar{K}$  inputs. These inputs permit the first stage to perform as a J- $\bar{K}$ , D-, or T-type flip-flop as shown in the function table.

The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

**SN54LS195, SN54S195 . . . FK PACKAGE**  
(TOP VIEW)



NC - No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'S195	105 MHz	350 mW

H = high level (steady state)  
L = low level (steady state)  
X = irrelevant (any input, including transitions)  
↑ = transition from low to high level  
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively  
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$  = the level of  $Q_A, Q_B, Q_C$ , or  $Q_D$ , respectively, before the indicated steady-state input conditions were established  
 $Q_{An}, Q_{Bn}, Q_{Cn}$  = the level of  $Q_A, Q_B$ , or  $Q_C$ , respectively, before the most-recent transition of the clock

**FUNCTION TABLE**

CLEAR	INPUTS				OUTPUTS				
	SHIFT/ LOAD	CLOCK	SERIAL	PARALLEL	$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\bar{Q}_D$
			J    K	A    B    C    D					
L	X	X	X    X	X    X    X    X	L	L	L	L	H
H	L	↑	X    X	a    b    c    d	a	b	c	d	$\bar{d}$
H	H	L	X    X	X    X    X    X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$\bar{Q}_{D0}$
H	H	↑	L    H	X    X    X    X	$Q_{A0}$	$Q_{A0}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	↑	L    L	X    X    X    X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	↑	H    H	X    X    X    X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	↑	H    L	X    X    X    X	$\bar{Q}_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$

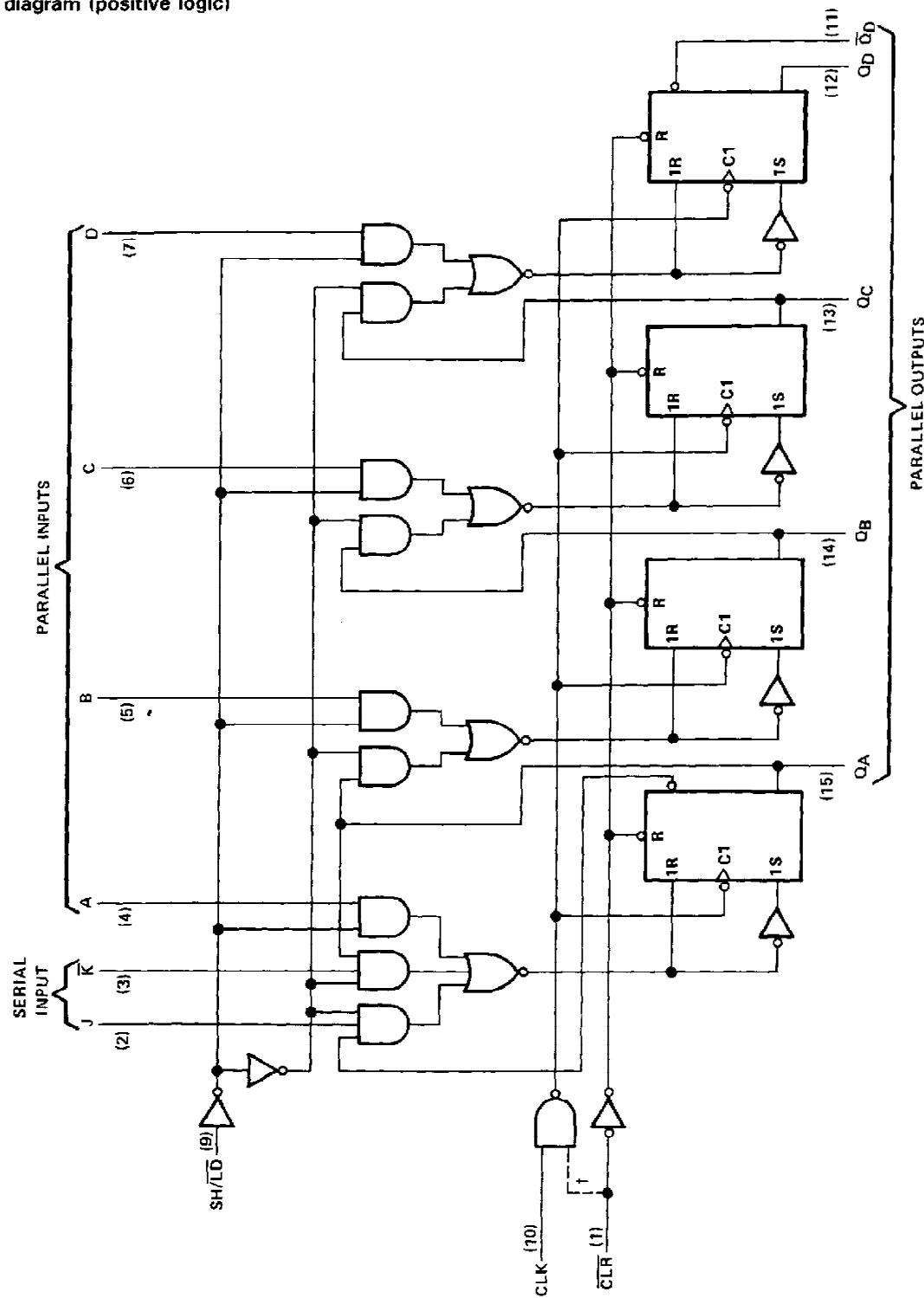
**PRODUCTION DATA** documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**SN54195, SN54LS195A, SN54S195,  
SN74195, SN74LS195A, SN74S195  
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

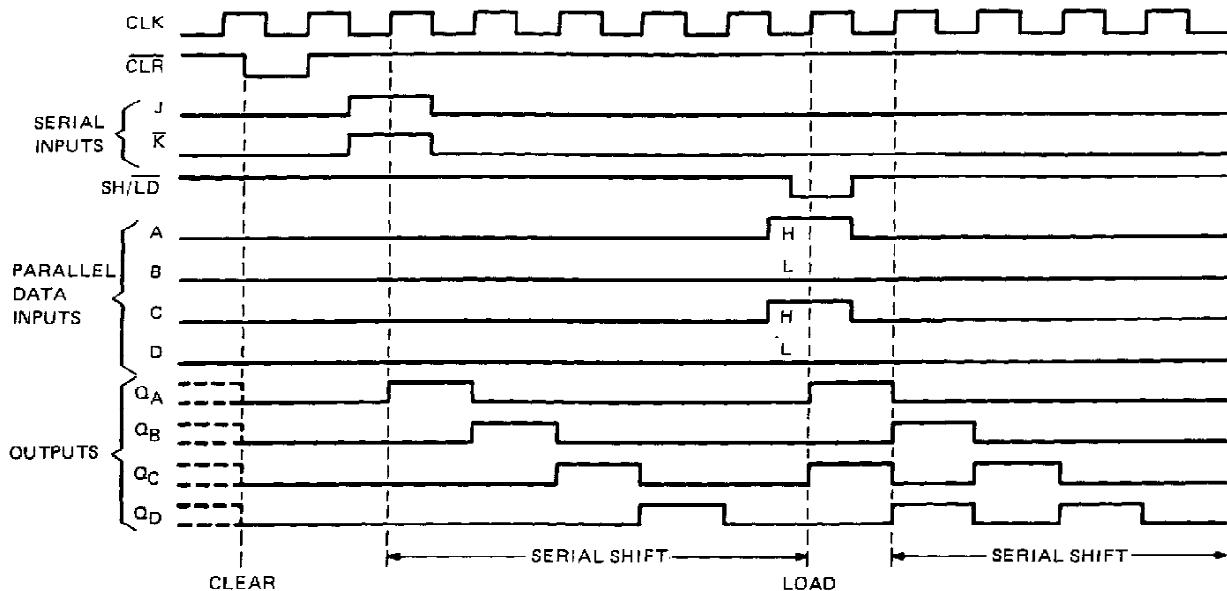
logic diagram (positive logic)



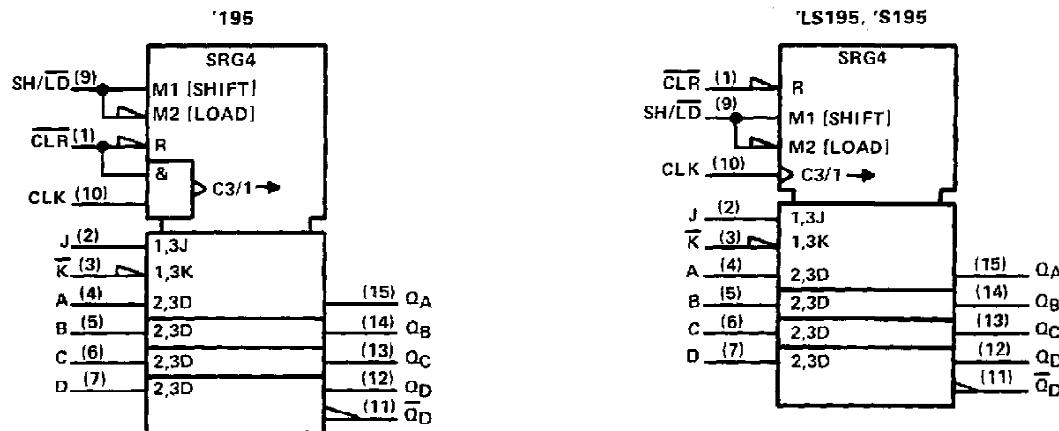
<sup>f</sup>This connection is made on '195 only.  
Pin numbers shown are for D, J, N, and W packages.

**SN54195, SN54LS195A, SN54S195,  
SN74195, SN74LS195A, SN74S195  
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

**typical clear, shift, and load sequences**



**logic symbols<sup>†</sup>**

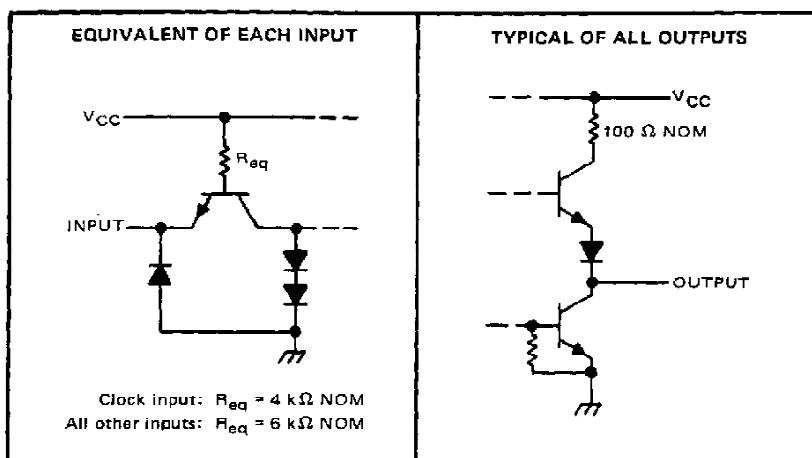


<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.  
Pin numbers are for D, J, N, and W packages.

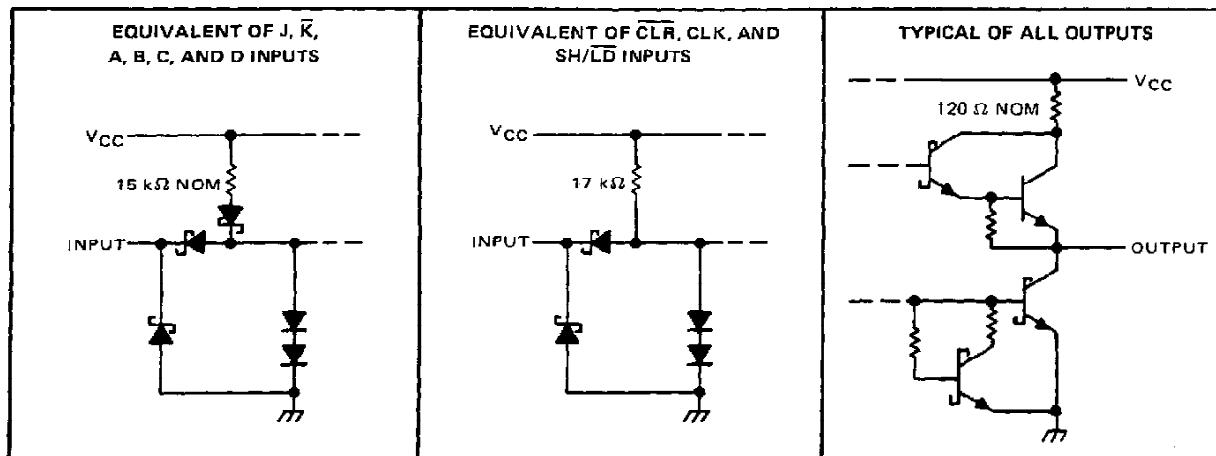
**SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195**  
**4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

**schematics of inputs and outputs**

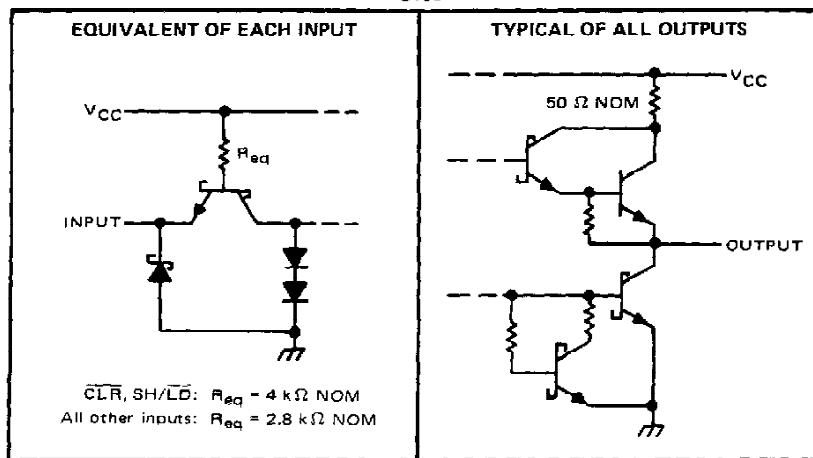
'195



'LS195A



'S195



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SN54195, SN74195  
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54195	-55°C to 125°C
SN74195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54195			SN74195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu A$
Low-level output current, $I_{OL}$			16			16	mA
Clock frequency, $f_{clock}$	0	30	0	0	30	0	MHz
Width of clock input pulse, $t_w(clock)$	16		16			ns	
Width of clear input pulse, $t_w(clear)$	12		12			ns	
Setup time, $t_{SU}$ (see Figure 1)	Shift/load	25	25				ns
	Serial and parallel data	20	20				
	Clear inactive-state	25	25				
Shift/load release time, $t_{release}$ (see Figure 1)			10			10	ns
Serial and parallel data hold time, $t_H$ (see Figure 1)	0		0			ns	
Operating free-air temperature, $T_A$	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IH}$ High-level input voltage		2			V
$V_{IL}$ Low-level input voltage			0.8		V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -800 \mu A$	2.4	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		1		mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$		40		$\mu A$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-1.6	mA
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	SN54195	-20	-57	mA
		SN74195	-18	-57	
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 2		39	63	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs,  $I_{CC}$  is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$ Maximum clock frequency	$C_L = 15 \text{ pF}$ , $R_L = 400 \Omega$ , See Figure 1	30	39		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear		19	30		ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock		14	22		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock		17	26		ns

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# SN54LS195A, SN74LS195A 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS195A	-55°C to 125°C
SN74LS195A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54LS195A	SN74LS195A			UNIT		
		MIN	NOM	MAX			
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$				-400		-400	$\mu$ A
Low-level output current, $I_{OL}$				4		8	mA
Clock frequency, $f_{clock}$	0		30	0		30	MHz
Width of clock or clear pulse, $t_w(clock)$	16			16			ns
Width of clear input pulse, $t_w(clear)$	12			12			ns
Setup time, $t_{SU}$ (see Figure 1)	Shift/load	25		25			ns
	Serial and parallel data	15		15			
	Clear inactive-state	25		25			
Shift/load release time, $t_{release}$ (see Figure 1)		10			20		ns
Serial and parallel data hold time, $t_h$ (see Figure 1)	0			0			ns
Operating free-air temperature, $T_A$	-65		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS195A			SN74LS195A			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.7			0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL} \text{ max}$ , $I_{OH} = 400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 4 \text{ mA}$ $V_{IL} = V_{IL} \text{ max}$ , $I_{OL} = 8 \text{ mA}$		0.25	0.4	0.25	0.4		V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 2		14	21	14	21		mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 \text{ }^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs,  $I_{CC}$  is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25 \text{ }^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$ Maximum clock frequency	$C_L = 15 \text{ pF}$ , $R_L = 2 \text{ k}\Omega$ , See Figure 1	30	39		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear		19	30		ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock		14	22		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock		17	26		ns

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SN54S195, SN74S195  
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S195	-55°C to 125°C
SN74S195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S195			SN74S195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$		-1			-1		mA
Low-level output current, $I_{OL}$		20			20		mA
Clock frequency, $f_{clock}$	0	70	0	0	70	0	MHz
Width of clock input pulse, $t_w$ (clock)	7			7			ns
Width of clear input pulse, $t_w$ (clear)	12			12			ns
Setup time, $t_{SU}$ (see Figure 1)	Shift/load	11		11			ns
	Serial and parallel data	5		5			
	Clear inactive-state	9		9			
Shift/load release time, $t_{release}$ (see Figure 1)		2		6			ns
Serial and parallel data hold time, $t_h$ (see Figure 1)	3		3				ns
Operating free-air temperature, $T_A$	-55	125	0	0	70	0	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>		MIN	TYP <sup>‡</sup>	MAX	UNIT
	MIN	MAX				
$V_{IH}$ High-level input voltage				2		V
$V_{IL}$ Low-level input voltage				0.8		V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ ,	$I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ ,	$V_{IH} = 2 \text{ V}$ ,	<span style="border: 1px solid black; padding: 0 2px;">SN54S195</span>	2.5	3.4	V
	$V_{IL} = 0.8 \text{ V}$ ,	$I_{OH} = -1 \text{ mA}$	<span style="border: 1px solid black; padding: 0 2px;">SN74S195</span>	2.7	3.4	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ ,	$V_{IH} = 2 \text{ V}$ ,			0.5	V
	$V_{IL} = 0.8 \text{ V}$ ,	$I_{OL} = 20 \text{ mA}$				
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ ,	$V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ ,	$V_I = 2.7 \text{ V}$			50	μA
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ ,	$V_I = 0.5 \text{ V}$			-2	mA
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$			-40	-100	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ ,	See Note 2	<span style="border: 1px solid black; padding: 0 2px;">SN54S195</span>	70	99	mA
			<span style="border: 1px solid black; padding: 0 2px;">SN74S195</span>	70	109	

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs,  $I_{CC}$  is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

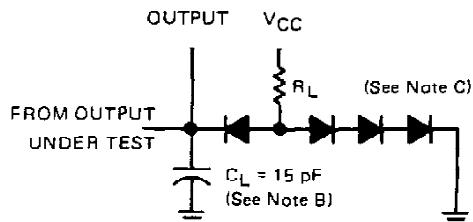
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		70	105		MHz
$f_{max}$ Maximum clock frequency	$C_L = 15 \text{ pF}$ ,				
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock			8	12	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock			11	16.5	ns

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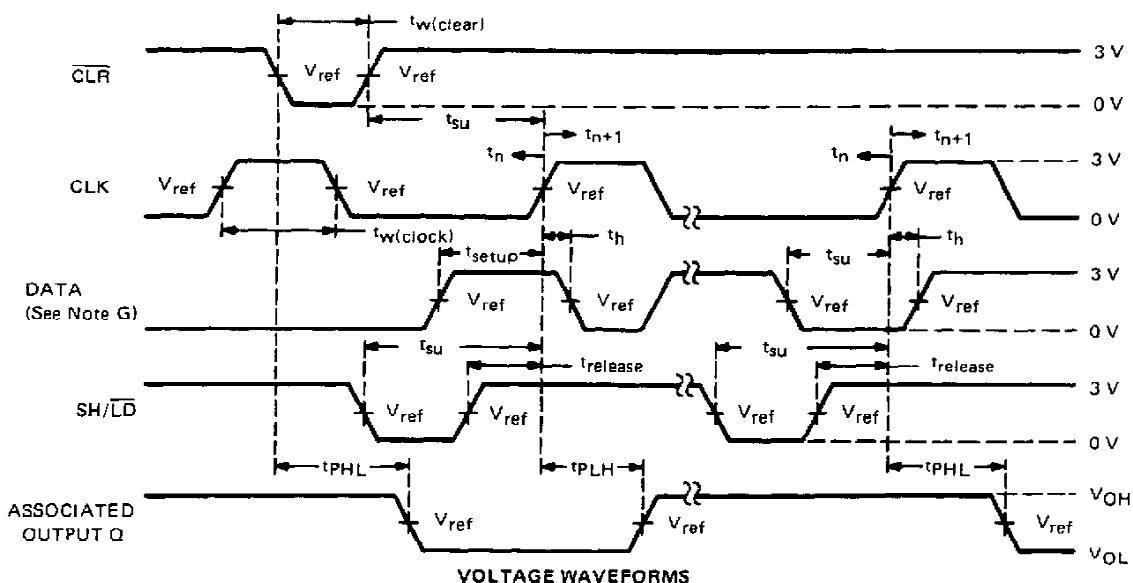
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**SN54195, SN54LS195A, SN54S195,  
SN74195, SN74LS195A, SN74S195  
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

## PARAMETER MEASUREMENT INFORMATION



**LOAD FOR OUTPUT UNDER TEST**



NOTES: A. The clock pulse generator has the following characteristics:  $Z_{out} \approx 50 \Omega$  and  $PRR \leq 1 \text{ MHz}$ . For '195,  $t_r \leq 7 \text{ ns}$  and  $t_f \leq 7 \text{ ns}$ . For 'LS195A,  $t_r \leq 15 \text{ ns}$  and  $t_f \leq 6 \text{ ns}$ . For 'S195,  $t_r = 2.5 \text{ ns}$  and  $t_f = 2.5 \text{ ns}$ . When testing  $f_{max}$ , vary the clock PRR.  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064 or equivalent.  
 D. A clear pulse is applied prior to each test.  
 E. For '195 and 'S195,  $V_{ref} = 1.5 \text{ V}$ ; for 'LS195A,  $V_{ref} = 1.3 \text{ V}$ .  
 F. Propagation delay times ( $t_{PLH}$  and  $t_{PHL}$ ) are measured at  $t_{n+1}$ . Proper shifting of data is verified at  $t_{n+4}$  with a functional test.  
 G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.  
 H.  $t_n$  = bit time before clocking transition.  
      $t_{n+1}$  = bit time after one clocking transition.  
      $t_{n+4}$  = bit time after four clocking transitions.

**FIGURE 1—SWITCHING TIMES**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/30602B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
JM38510/30602B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
JM38510/30602B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
JM38510/30602BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
JM38510/30602BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
JM38510/30602BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
JM38510/30602BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
M38510/30602B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
M38510/30602B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602B2A
M38510/30602BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
M38510/30602BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30602BEA
SN54LS195AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS195AJ
SN54LS195AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS195AJ
SN54LS195AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS195AJ
SN54LS195AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS195AJ
SNJ54LS195AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS195AJ
SNJ54LS195AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS195AJ
SNJ54LS195AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS195AJ
SNJ54LS195AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS195AJ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/30602B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30602B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30602B2A	FK	LCCC	20	55	506.98	12.06	2030	NA

# GENERIC PACKAGE VIEW

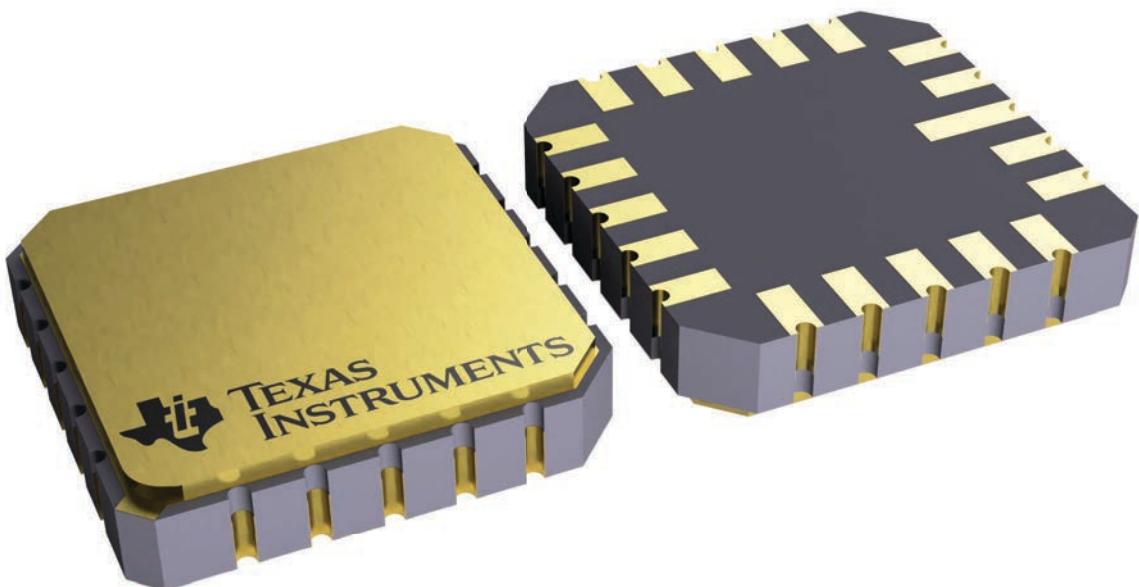
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

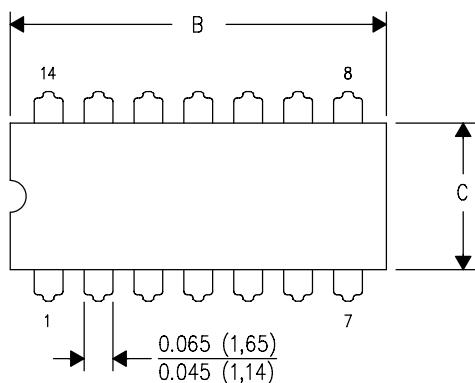


4229370VA\

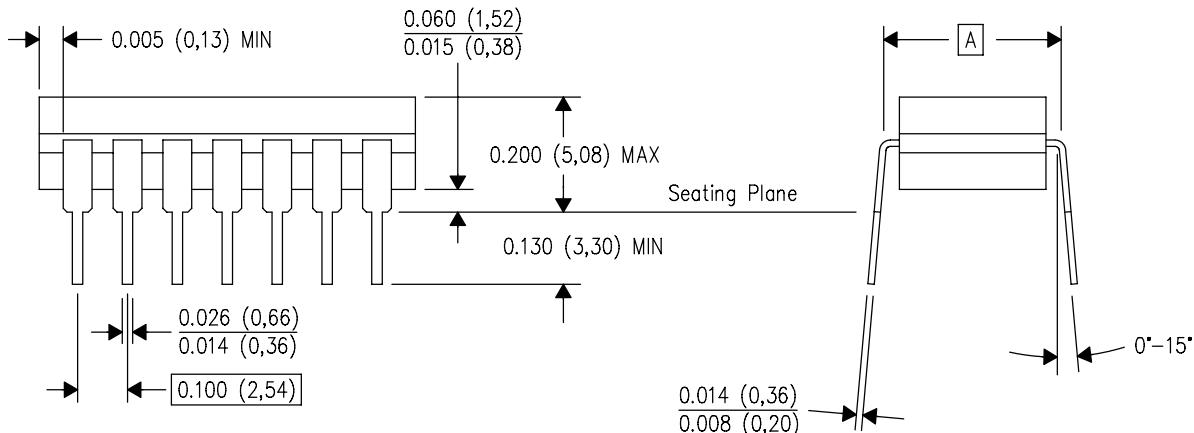
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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