

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

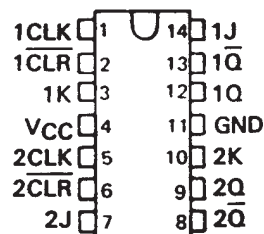
description

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the $\bar{Q}$ output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7473, and the SN74LS73A are characterized for operation from 0°C to 70°C .

SN5473, SN54LS73A . . . J OR W PACKAGE
SN7473 . . . N PACKAGE
SN74LS73A . . . D OR N PACKAGE
(TOP VIEW)



'73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H		L	L	Q_0	$\bar{Q}_0$
H		H	L	H	L
H		L	H	L	H
H		H	H	TOGGLE	TOGGLE

'LS73A
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H		L	L	Q_0	$\bar{Q}_0$
H		H	L	H	L
H		L	H	L	H
H		H	H	TOGGLE	TOGGLE
H	H	X	X	Q_0	$\bar{Q}_0$

FOR CHIP CARRIER INFORMATION,
CONTACT THE FACTORY

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

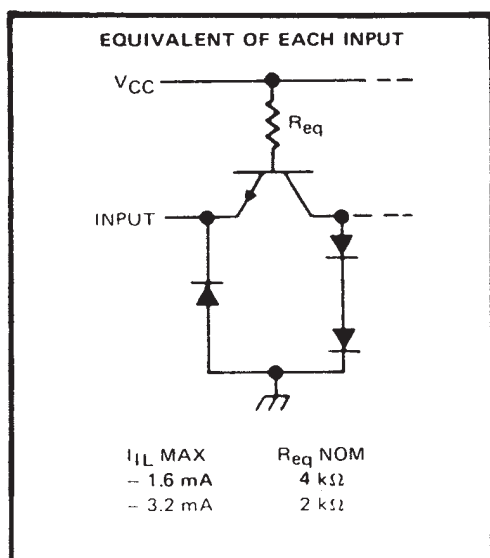
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logic symbols†

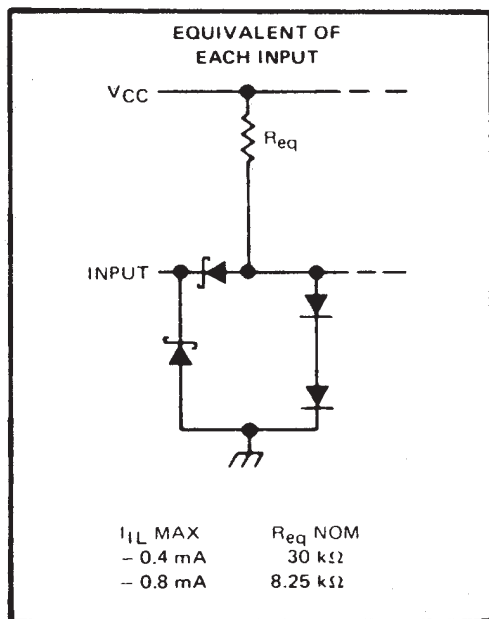
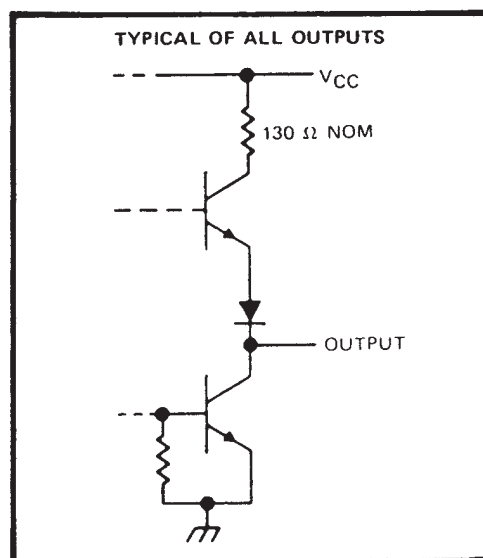


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

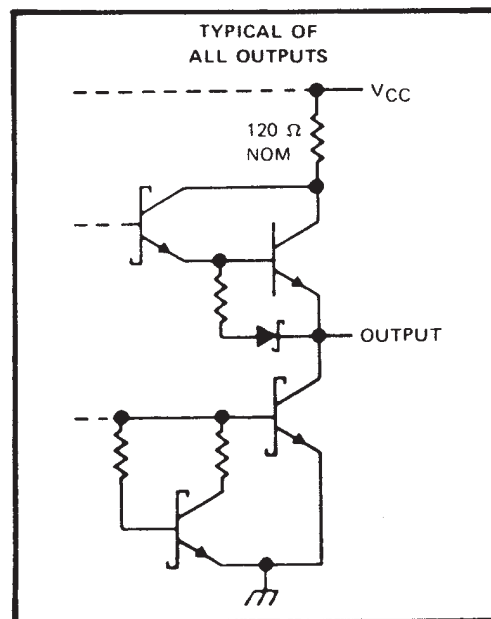
schematics of inputs and outputs



'73



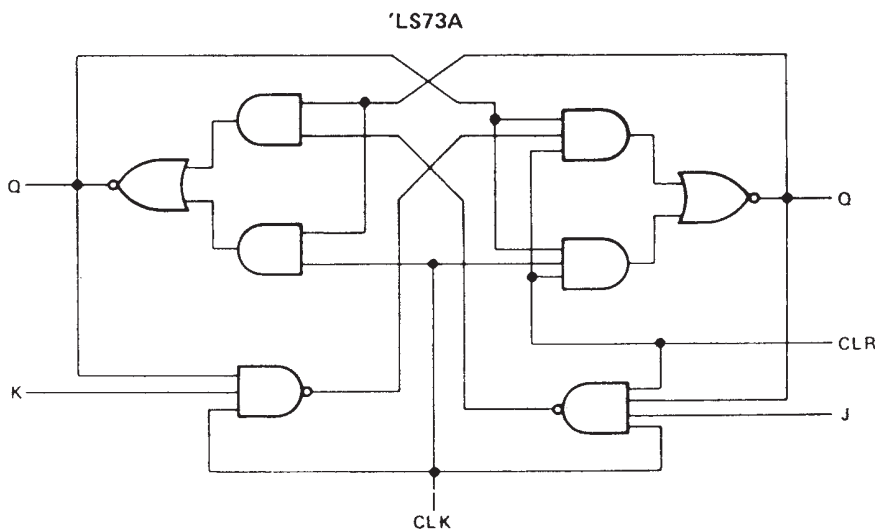
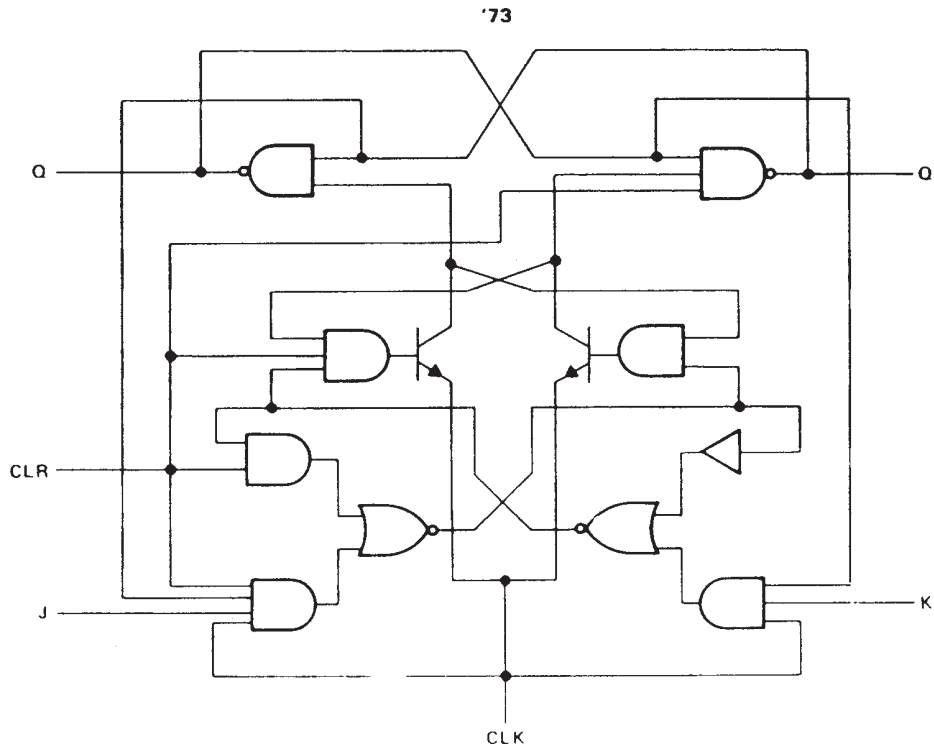
'LS73



SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage: '73	5.5 V
'LS73A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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recommended operating conditions

		SN5473			SN7473			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			– 0.4			– 0.4	mA
I_{OL}	Low-level output current			16			16	mA
t_w	Pulse duration	CLK high	20		20			ns
		CLK low	47		47			
		$\overline{CLR}$ low	25		25			
t_{su}	Input setup time before CLK $\uparrow$	0			0			ns
t_h	Input hold time data after CLK $\downarrow$	0			0			ns
T_A	Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5473			SN7473			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				– 1.5			– 1.5	V
V_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$		2.4	3.4		2.4	3.4		V
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.2	0.4		0.2	0.4	V
I_I		$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1	mA
I_{IH}	J or K	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40			40	μA
	$\overline{CLR}$ or CLK					80			80	
I_{IL}	J or K	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				– 1.6			– 1.6	mA
	$\overline{CLR}$					– 3.2			– 3.2	
	CLK					– 3.2			– 3.2	
$I_{OS}§$		$V_{CC} = \text{MAX}$		– 20		– 57	– 18		– 57	mA
$I_{CC}¶$		$V_{CC} = \text{MAX},$ See Note 2			10	20		10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

¶ Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				15	20		MHz
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		16	25	ns
t_{PHL}		Q			25	40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			16	25	ns
t_{PHL}					25	40	ns

f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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recommended operating conditions

			SN54LS73A			SN74LS73A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current		− 0.4			− 0.4			mA
I _{OL}	Low-level output current		4			8			mA
f _{clock}	Clock frequency		0 30			0 30			MHz
t _w	Pulse duration	CLK high	20			20			ns
		$\overline{\text{CLR}}$ low	25			20			
t _{su}	Set up time-before CLK ↓	data high or low	20			20			ns
		$\overline{\text{CLR}}$ inactive	20			20			
t _h	Hold time-data after CLK ↓		0			0			ns
T _A	Operating free-air temperature		− 55 125			0 70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS73A			SN74LS73A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = – 18 mA				– 1.5			– 1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = – 0.4 mA		2.5	3.4		2.7	3.4		V
V _{OL}		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA			0.25	0.4		0.25	0.4	V
		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA						0.35	0.5	
I _I	J or K	V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
	CLR					0.3			0.3	
	CLK					0.4			0.4	
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V				20			20	μA
	CLR					60			60	
	CLK					80			80	
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V				– 0.4			– 0.4	mA
	CLR or CLK					– 0.8			– 0.8	
I _{OS} §		V _{CC} = MAX, See Note 4		– 20		– 100	– 20		– 100	mA
I _{CC} (Total)		V _{CC} = MAX, See Note 2			4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 2 kΩ, C _L = 15 pF	30	45		MHz
t _{PLH}	CLR or CLK	Q or Q̄			15	20	ns
t _{PHL}					15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9675101QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QC A SNJ54LS73AJ
5962-9675101QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QD A SNJ54LS73AW
5962-9675101QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QD A SNJ54LS73AW
SN54LS73AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS73AJ
SN54LS73AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS73AJ
SN54LS73AJ.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS73AJ
SN54LS73AJ.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS73AJ
SN74LS73AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LS73A
SN74LS73AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LS73A
SN74LS73ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS73A
SN74LS73ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS73A
SN74LS73ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS73A
SN74LS73ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS73A
SN74LS73AN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS73AN
SN74LS73AN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS73AN
SN74LS73AN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS73AN
SN74LS73AN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS73AN
SN74LS73ANE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS73AN
SN74LS73ANE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS73AN
SNJ54LS73AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QC A SNJ54LS73AJ
SNJ54LS73AJ	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QC A SNJ54LS73AJ

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS73AJ.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QC A SNJ54LS73AJ
SNJ54LS73AJ.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QC A SNJ54LS73AJ
SNJ54LS73AW	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QD A SNJ54LS73AW
SNJ54LS73AW	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QD A SNJ54LS73AW
SNJ54LS73AW.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QD A SNJ54LS73AW
SNJ54LS73AW.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9675101QD A SNJ54LS73AW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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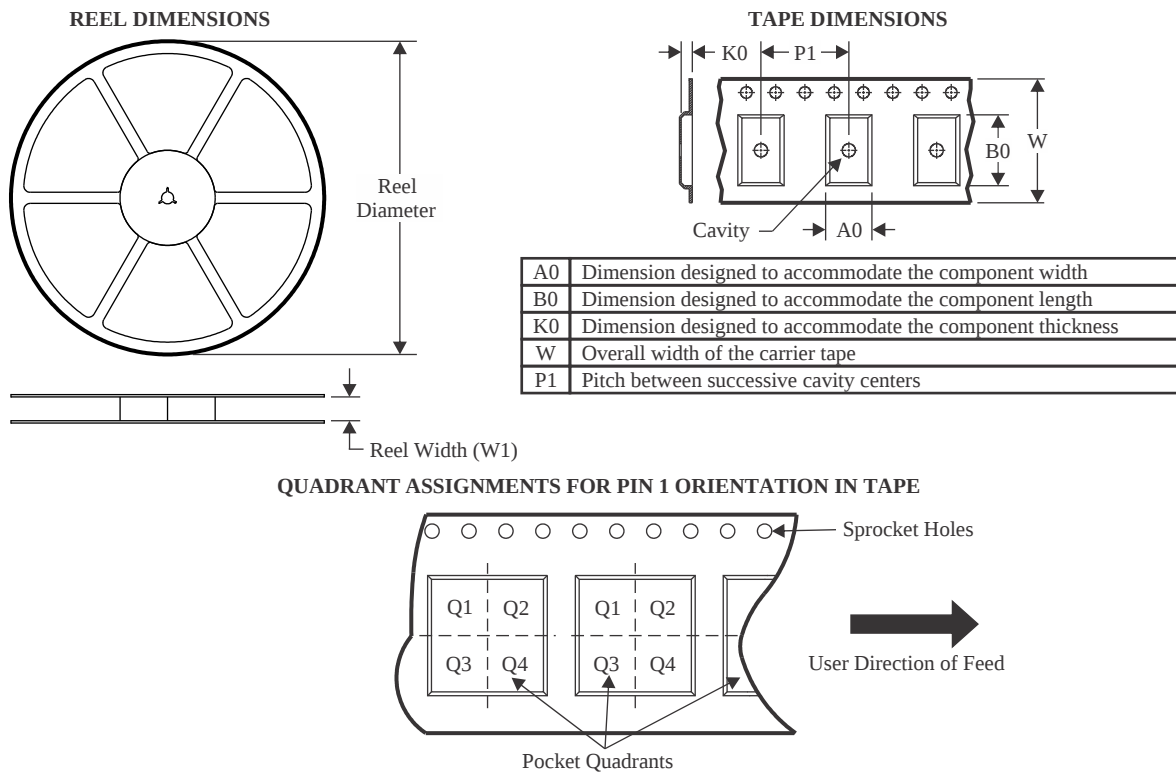
OTHER QUALIFIED VERSIONS OF SN54LS73A, SN74LS73A :

- Catalog : [SN74LS73A](#)
- Military : [SN54LS73A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS73ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

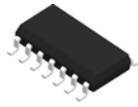
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS73ADR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE

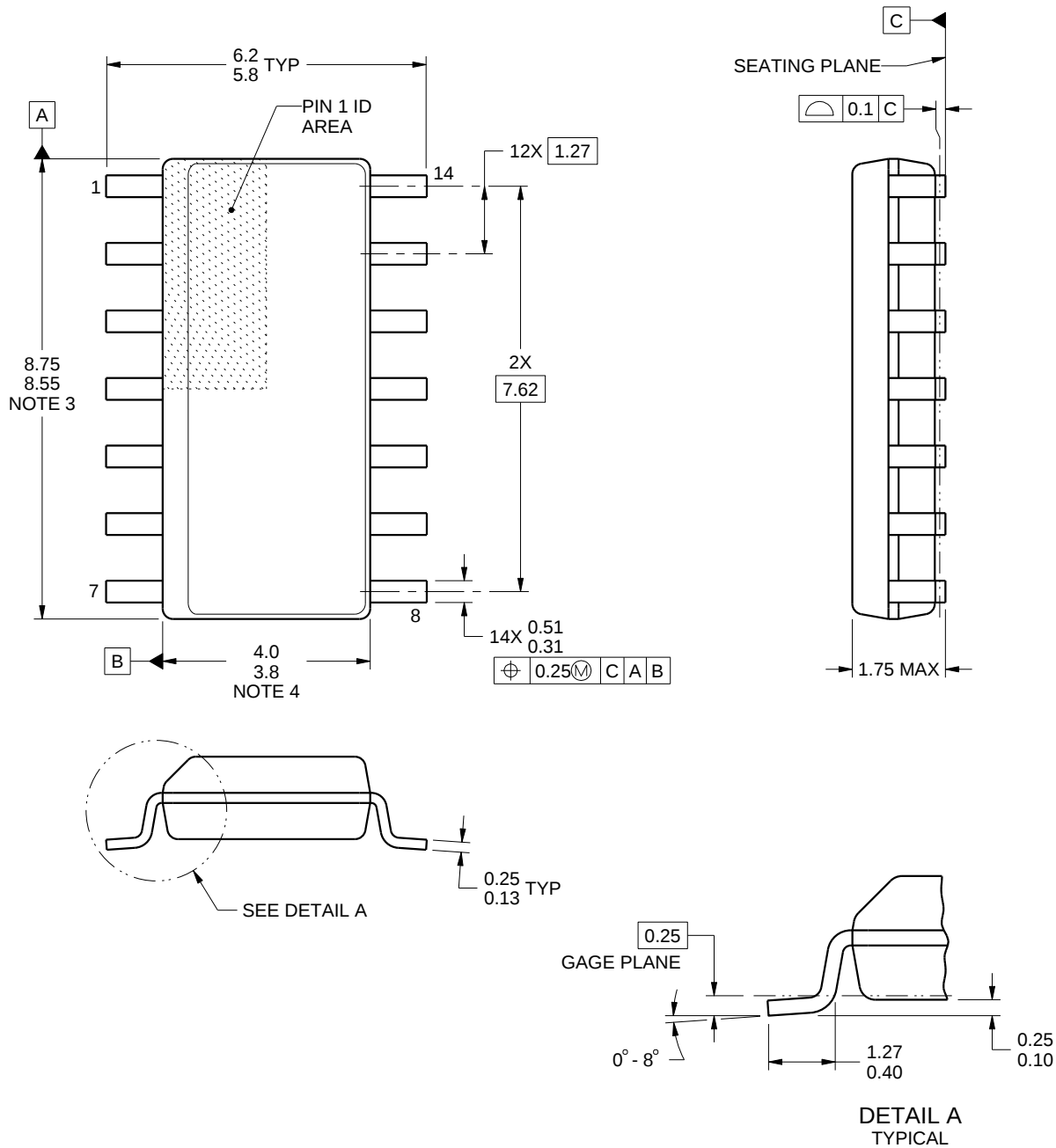


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9675101QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS73AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS73AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS73AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS73AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS73ANE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS73ANE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS73AW	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS73AW.A	W	CFP	14	25	506.98	26.16	6220	NA

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

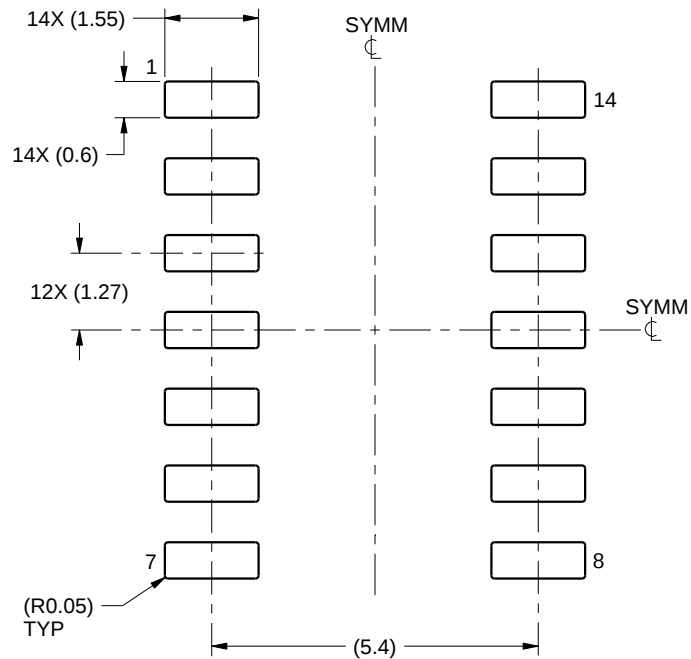
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

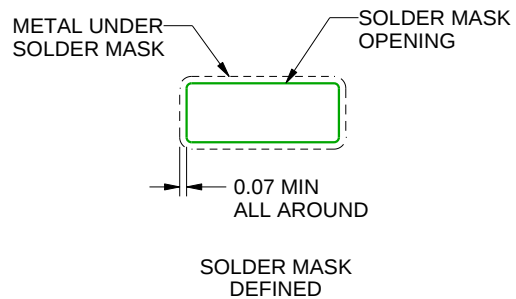
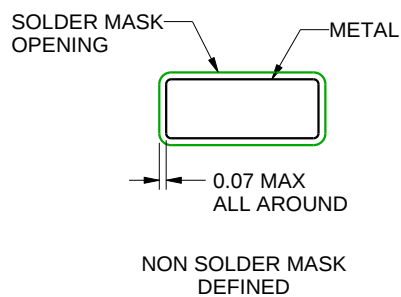
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

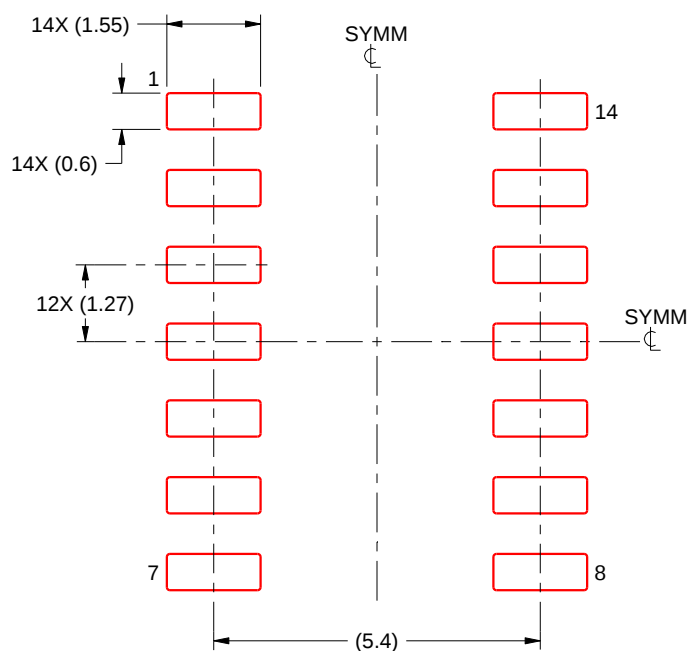
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

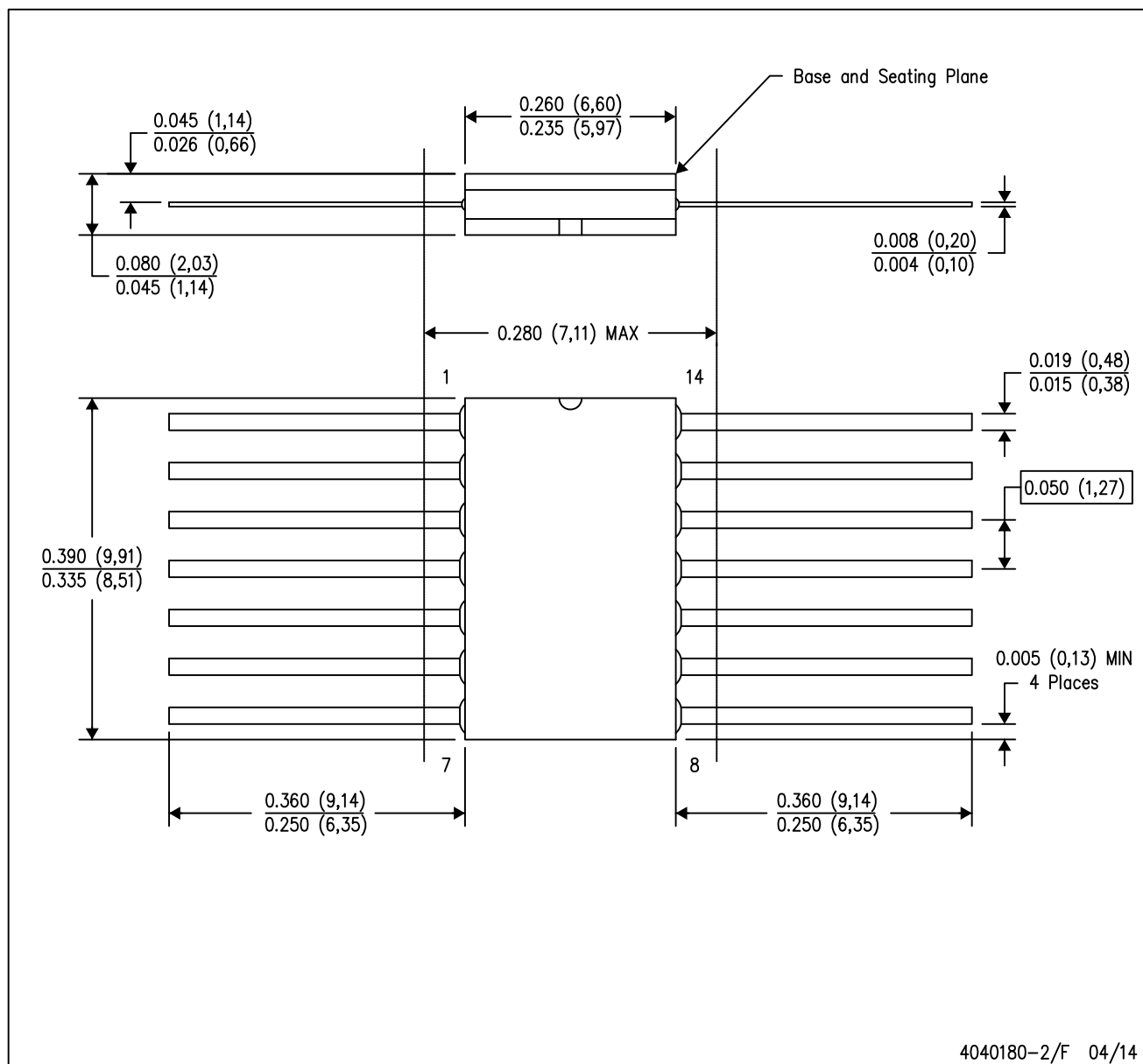
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



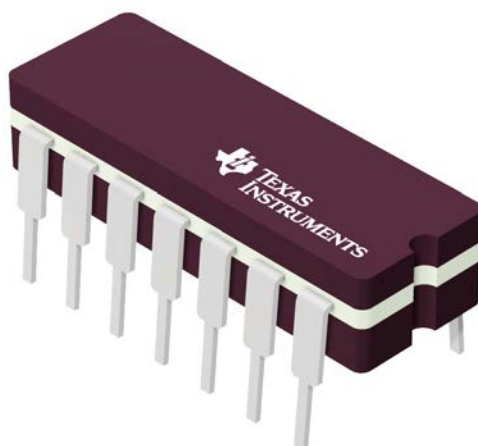
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14

J 14

GENERIC PACKAGE VIEW

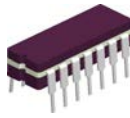
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

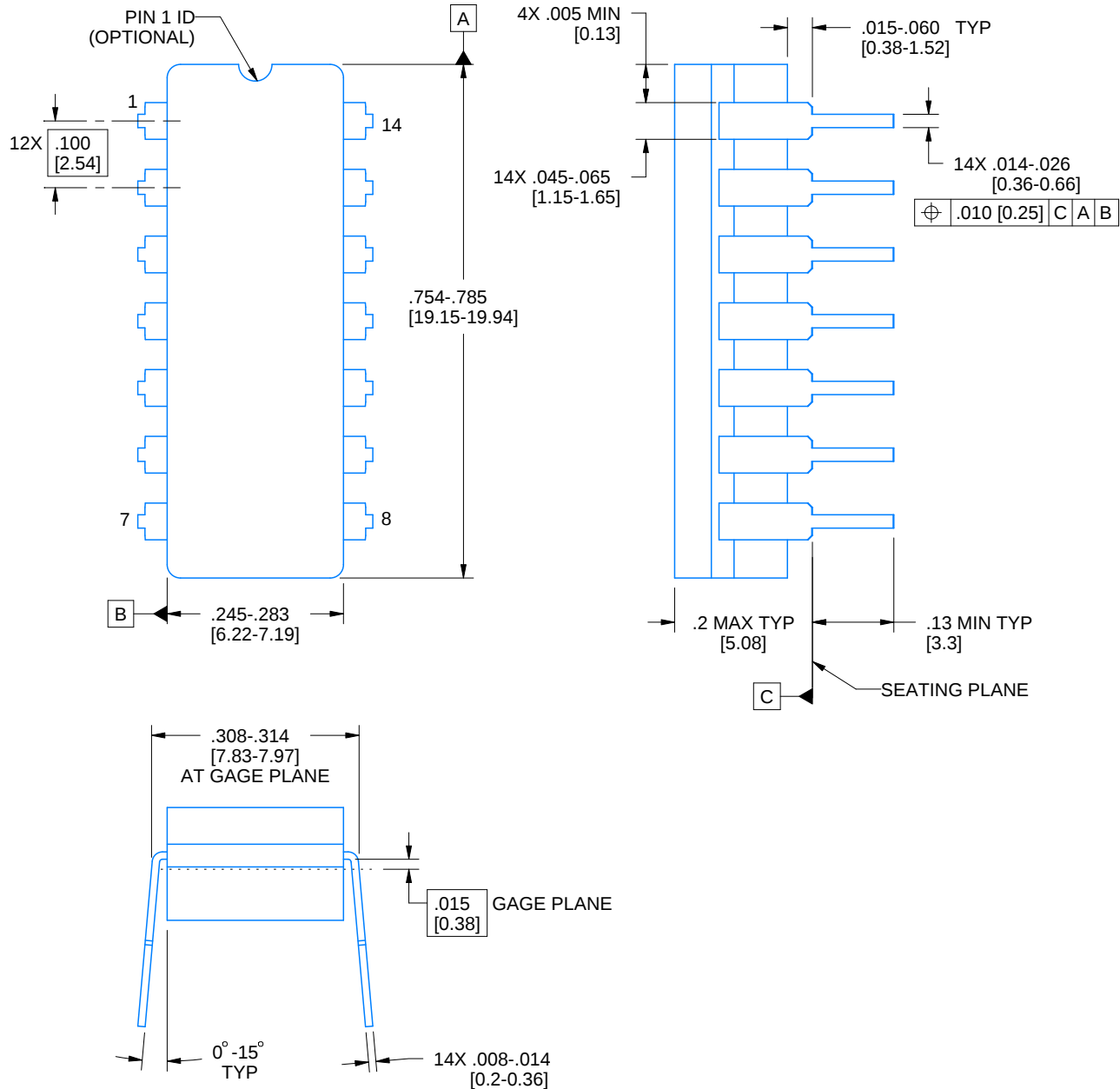


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

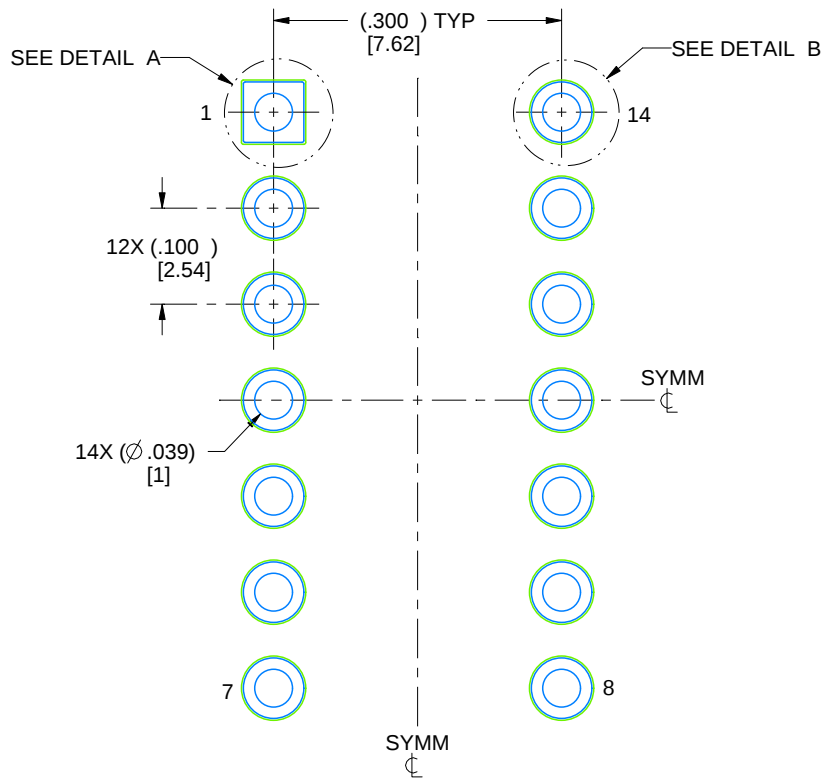
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

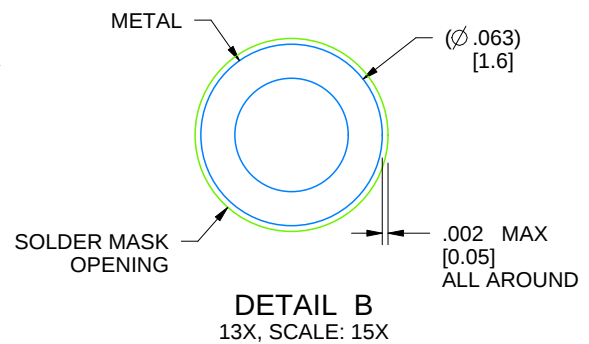
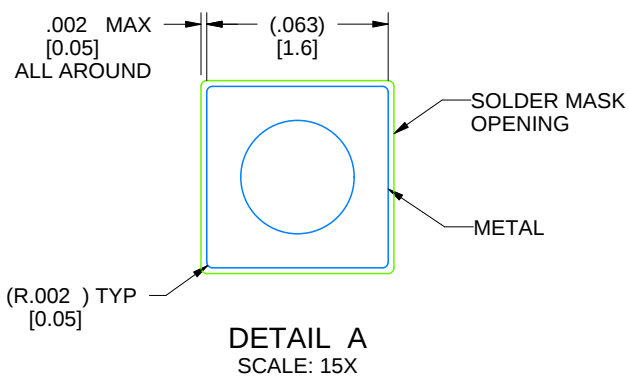
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

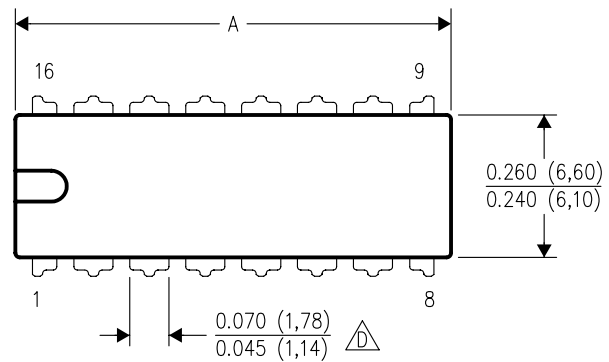


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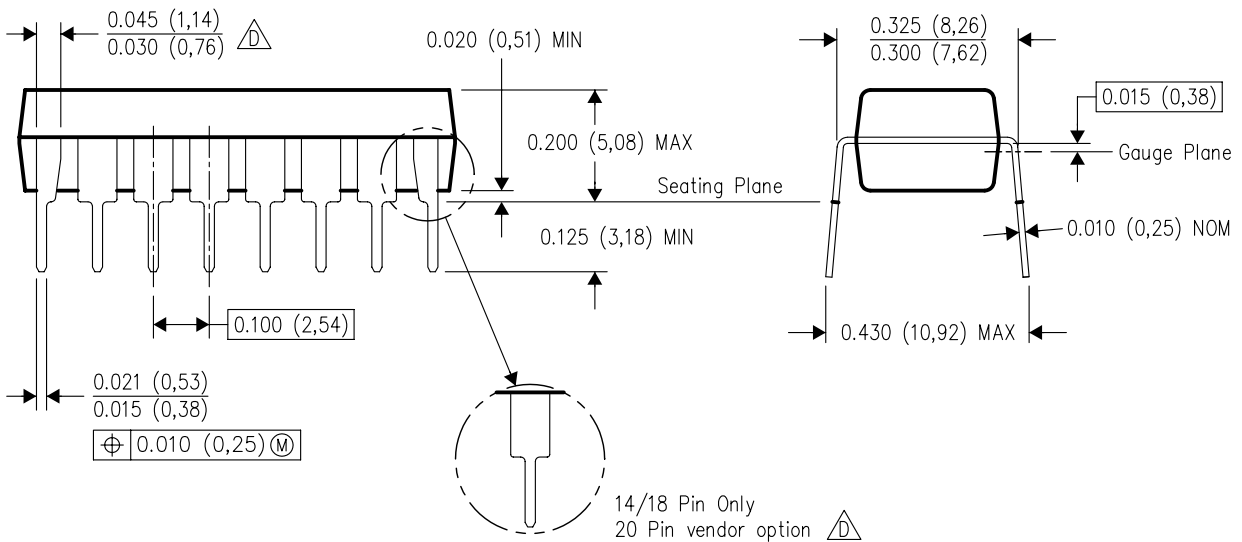
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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