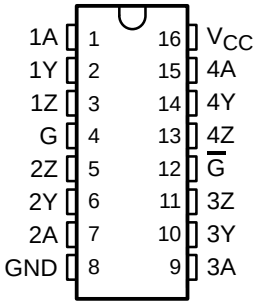
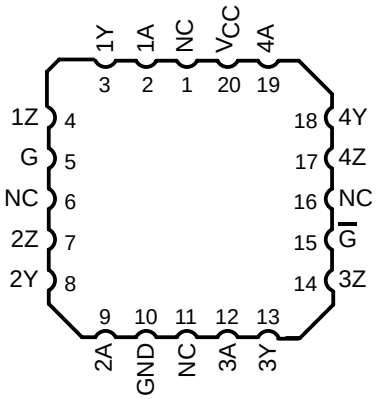
- **Meets Standard EIA-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Supports Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC172 is a monolithic quadruple differential line driver with 3-state outputs. This device is designed to meet the requirements of the Electronics Industry Association (EIA) standard RS-485. The SN55LBC172 is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry, making it suitable for party-line applications in noisy environments. The device is designed using the LinBiCMOS™ process, facilitating ultralow power consumption and inherent robustness.

The SN55LBC172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. This device offers optimum performance when used with the SN55LBC173M quadruple line receiver.

ORDERING INFORMATION‡

T_A	PACKAGE§		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	LCCC – FK	Tube	SNJ55LBC172FK	SNJ55LBC172FK
	CDIP – J	Tube	SNJ55LBC172J	SNJ55LBC172J
	CFP – W	Tube	SNJ55LBC172W	SNJ55LBC172W

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

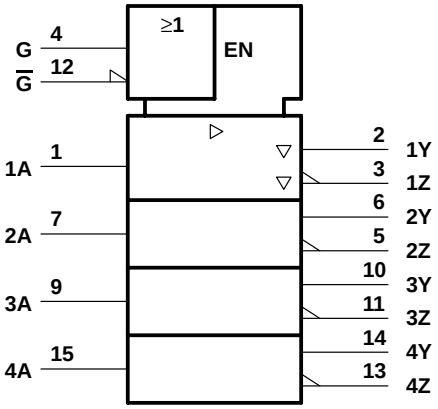
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FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

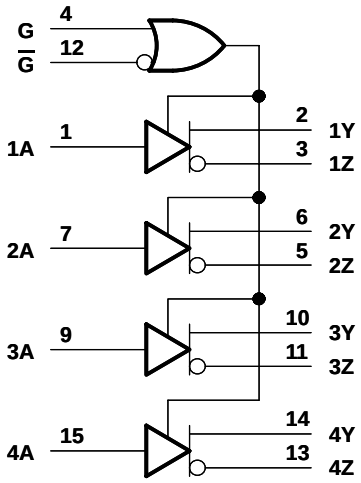
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†

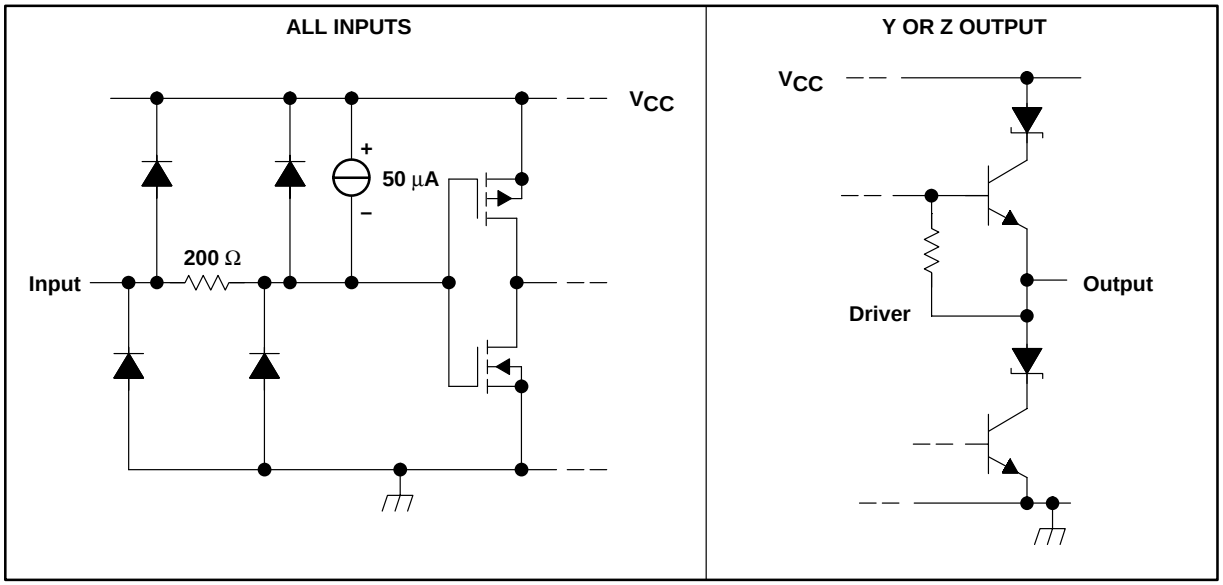


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J or W package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, V_O . . . . . –10 V to 15 V
Input voltage range, V_I . . . . . –0.3 V to 7 V
Continuous power dissipation . . . . . Internally limited‡
Operating free-air temperature range, T_A . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A=125°C	T_A = 125°C POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Output voltage at any bus terminal (separately or common mode), V_O	Y or Z			12	V
				–7	
High-level output current, I_{OH}	Y or Z			–60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A		–55		125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
$\|V_{OD}\|$	Differential output voltage‡	R_L = 54 Ω, See Figure 1		1.1	1.8	5	V
		R_L = 60 Ω, See Figure 2		1.1	1.7	5	
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3 – 1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = – 7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = – 7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				–100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, See Figure 3	25°C	2	11	20	ns
			–55°C to 125°C	2		40	
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω, See Figure 3	25°C	10	15	25	ns
			–55°C to 125°C	4		60	
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4	25°C			30	ns
			–55°C to 125°C			40	
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5	25°C			30	ns
			–55°C to 125°C			40	
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4	25°C			60	ns
			–55°C to 125°C			115	
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5	25°C			30	ns
			–55°C to 125°C			55	

PARAMETER MEASUREMENT INFORMATION

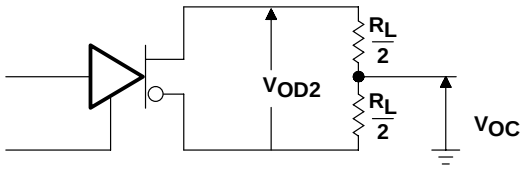


Figure 1. Differential and Common-Mode Output Voltages

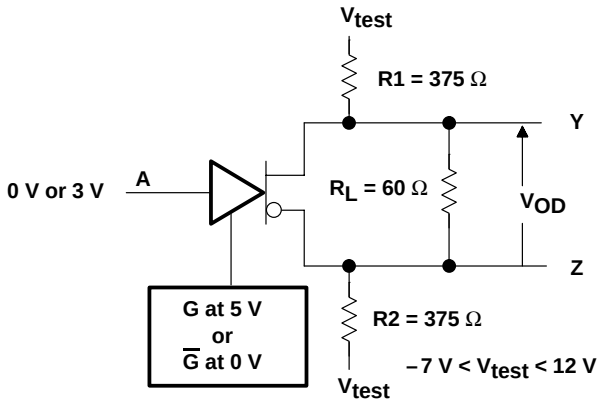
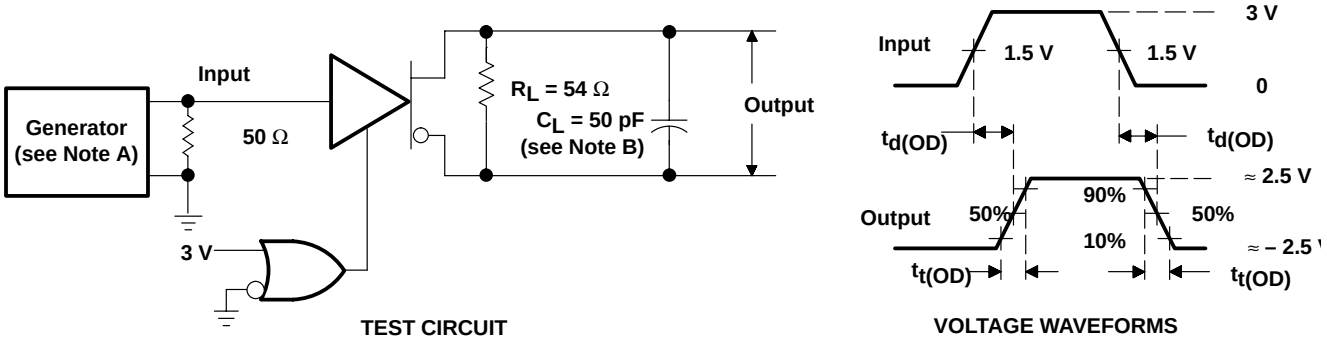


Figure 2. Driver V_{OD} Test Circuit

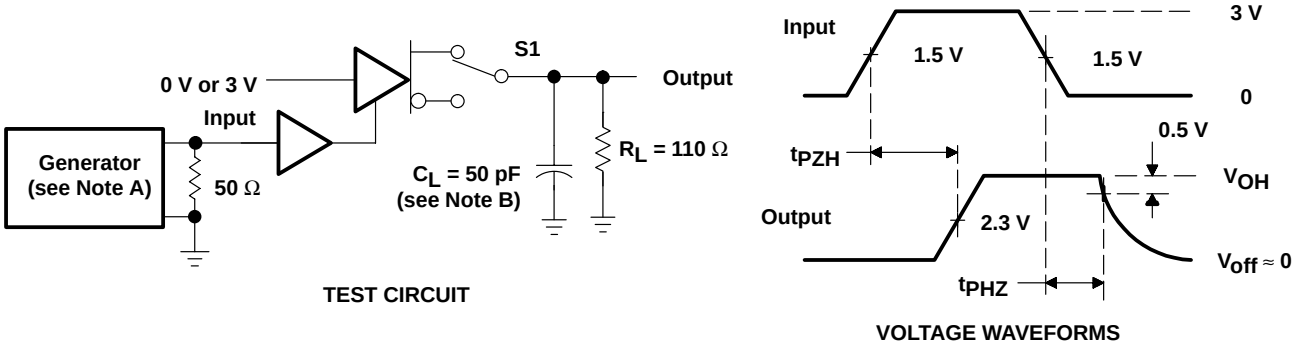


NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

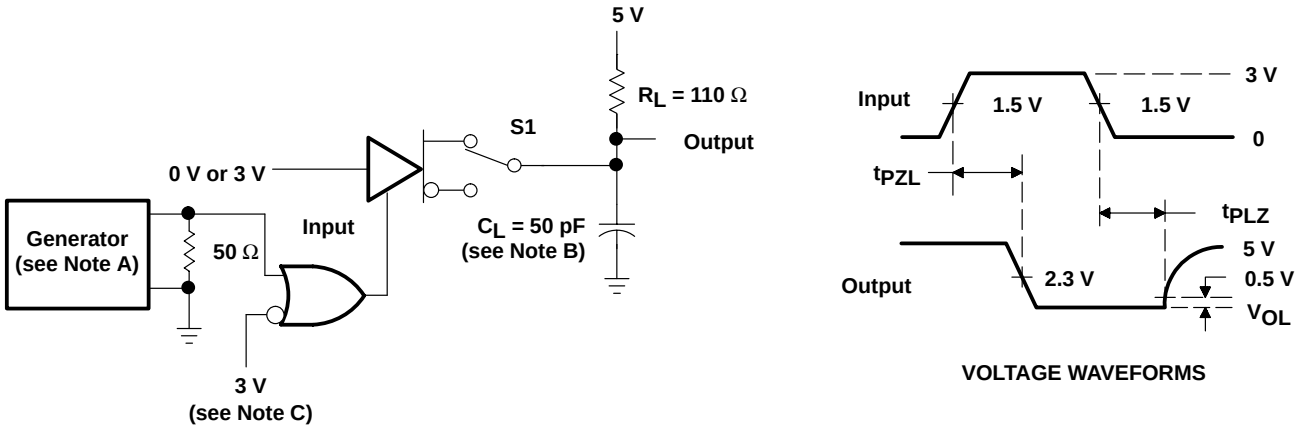
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

Figure 4. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE

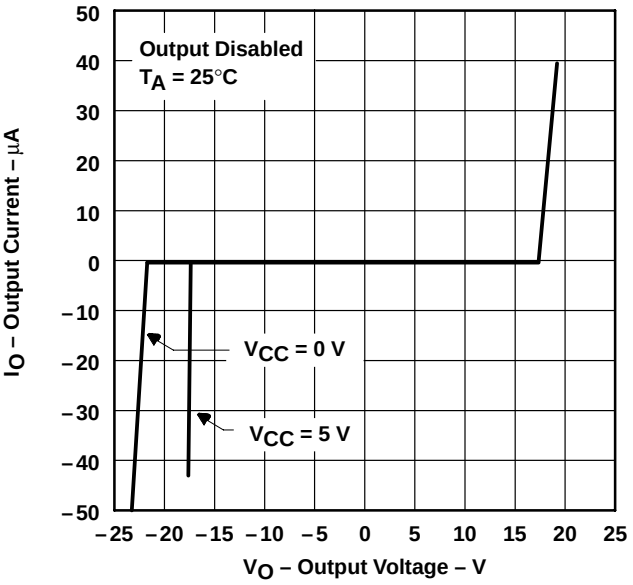


Figure 6

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

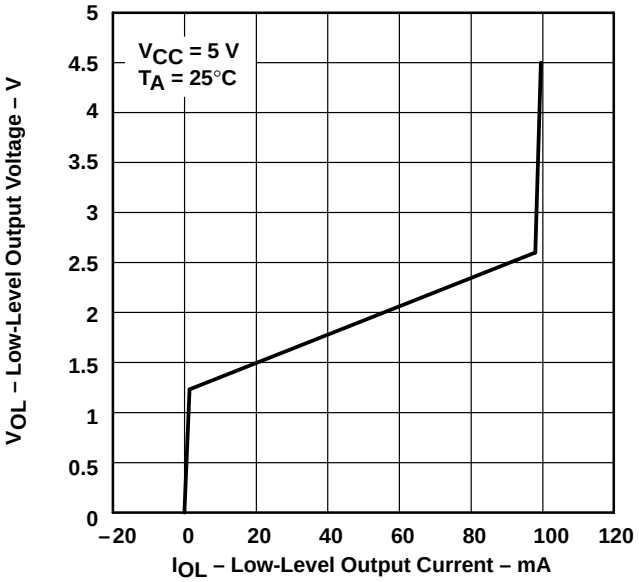


Figure 7

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

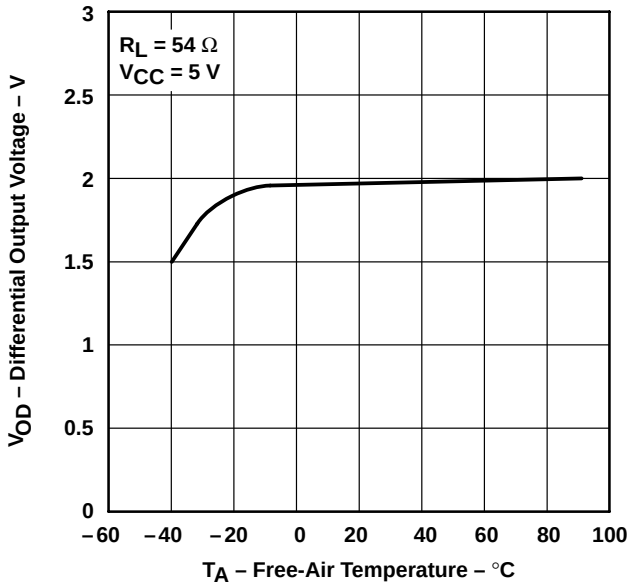


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

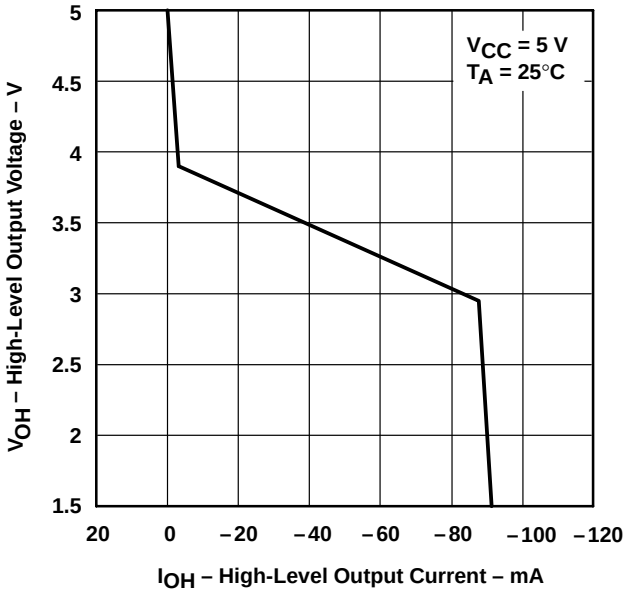


Figure 9

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

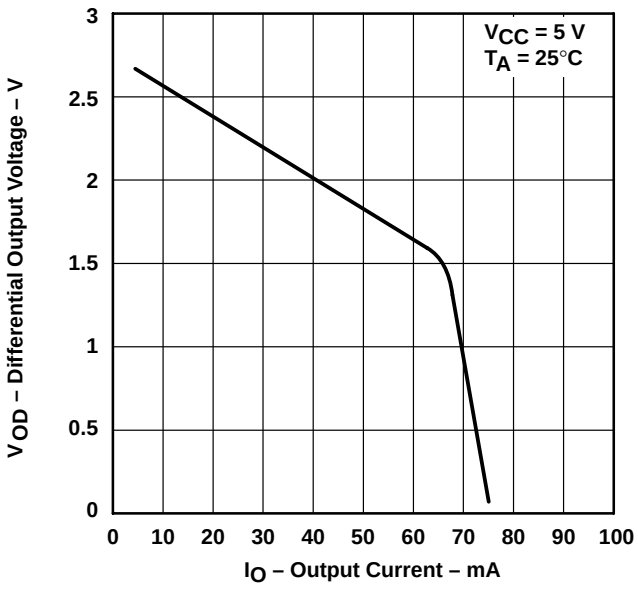


Figure 10

PROPAGATION DELAY TIME, DIFFERENTIAL OUTPUT vs FREE-AIR TEMPERATURE

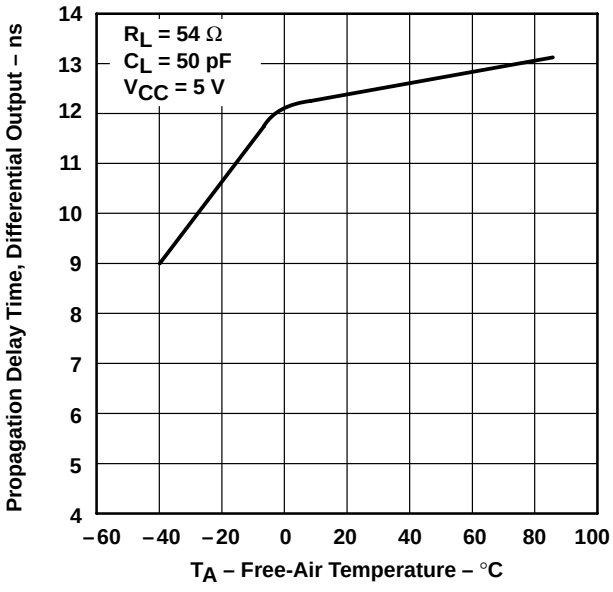


Figure 11

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9076503Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503Q2A SNJ55LBC172FK
5962-9076503QEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503QEA SNJ55LBC172J
5962-9076503QFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503QFA SNJ55LBC172W
SNJ55LBC172FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503Q2A SNJ55LBC172FK
SNJ55LBC172FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503Q2A SNJ55LBC172FK
SNJ55LBC172J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503QEA SNJ55LBC172J
SNJ55LBC172J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503QEA SNJ55LBC172J
SNJ55LBC172W	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503QFA SNJ55LBC172W
SNJ55LBC172W.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076503QFA SNJ55LBC172W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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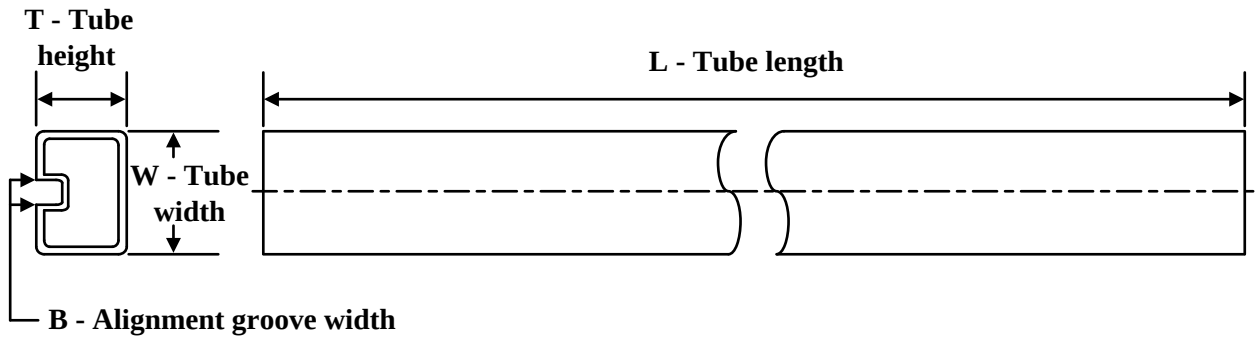
OTHER QUALIFIED VERSIONS OF SN55LBC172 :

- Catalog : SN75LBC172

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

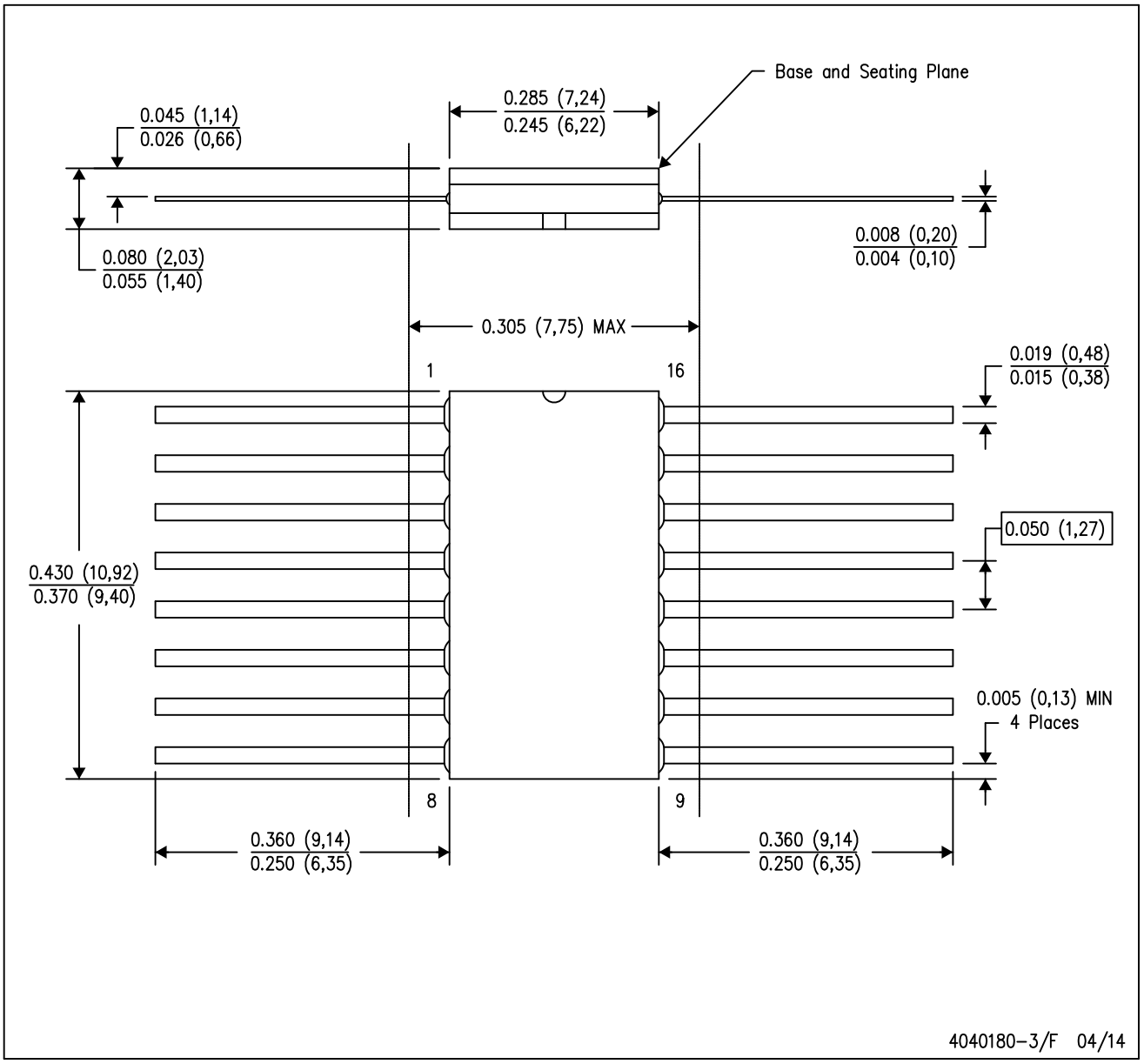
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9076503Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9076503QFA	W	CFP	16	25	506.98	26.16	6220	NA
SNJ55LBC172FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LBC172FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LBC172W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ55LBC172W.A	W	CFP	16	25	506.98	26.16	6220	NA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

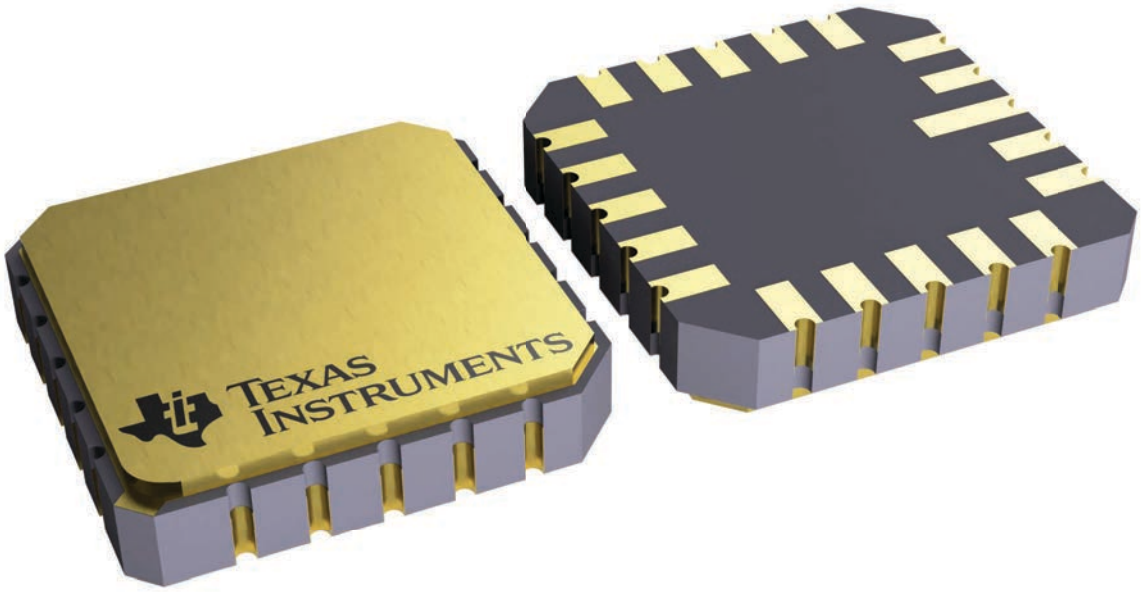
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

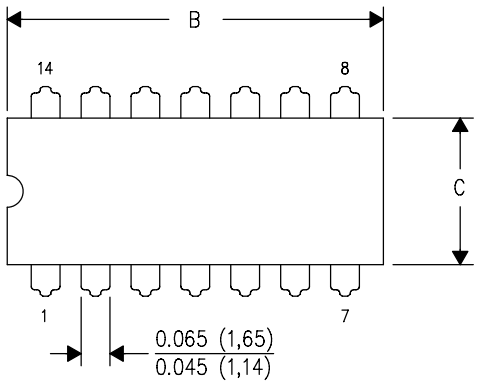


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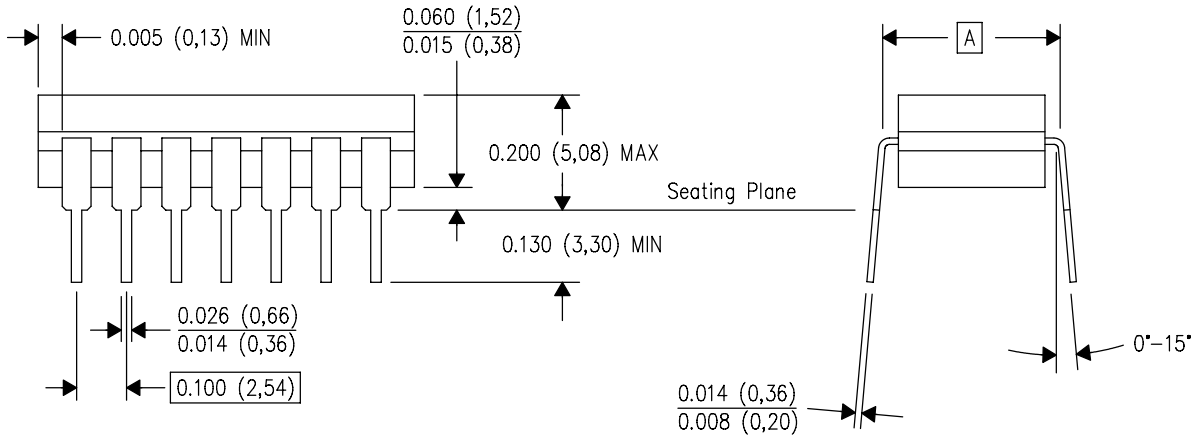
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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