

SN65C116xE 具有 $\pm 15\text{kV}$ ESD 保护的双路差分驱动器和接收器

1 特性

- 达到或超出 TIA/EIA-422-B 和 ITU Recommendation V.11 标准的要求
- 使用 5V 单电源供电
- 为 RS-422 总线引脚提供 ESD 保护
 - $\pm 15\text{kV}$ 人体放电模型 (HBM)
 - $\pm 8\text{kV}$ IEC 61000-4-2, 接触放电
 - $\pm 8\text{kV}$ IEC 61000-4-2, 空气间隙放电
- 低电源电流要求: 9mA (最大值)
- 低脉冲偏斜
- 接收器输入阻抗: $17\text{k}\Omega$ (典型值)
- 接收器输入灵敏度: $\pm 200\text{mV}$
- 接收器共模输入电压范围为 -7V 至 +7V
- 无干扰上电和断电保护
- 接收器三态输出低电平有效使能 (仅限 SN65C1167E)

2 应用

- 交流和伺服电机驱动器
- 工厂自动化和控制
- 无线基础设施

3 说明

SN65C1167E 和 SN65C1168E 由双驱动器和双接收器组成, 具有 $\pm 15\text{kV}$ ESD (人体放电模型 [HBM]) 和 $\pm 8\text{kV}$ ESD (IEC61000-4-2 空气间隙放电和接触放电) 保护, 适用于 RS-422 总线引脚。这些器件符合 TIA/EIA-422-B 和 ITU 建议 V.11 的要求。

SN65C1167E 整合了双三态差分线路驱动器和三态差分线路接收器, 两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端, 它们可以在外部连接在一起, 用作方向控制。

SN65C1168E 驱动器具有单独的高电平有效使能端。

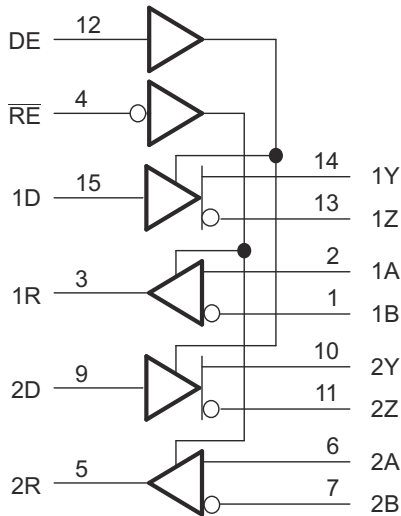
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN65C116xE	SO (16)	10.3mm × 5.3mm
	TSSOP (16)	5mm × 4.4mm
	VQFN (16)	4mm × 3.5mm

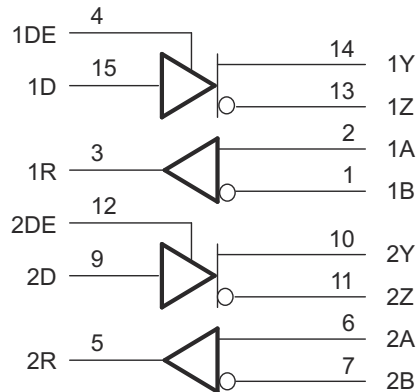
(1) 有关更多信息, 请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。

SN65C1167E



SN65C1168E



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方框图



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4 Pin Configuration and Functions

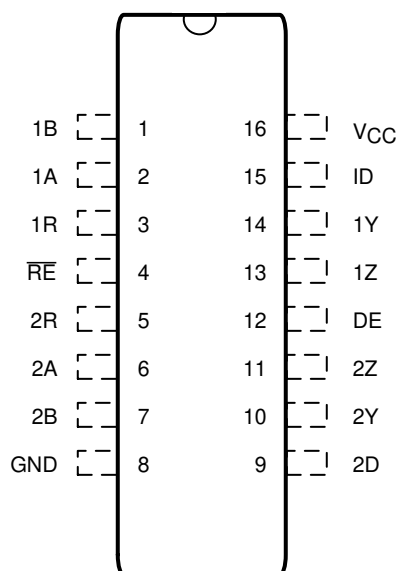


图 4-1. NS or PW Package 16 Pin (NS or TSSOP)
Top View

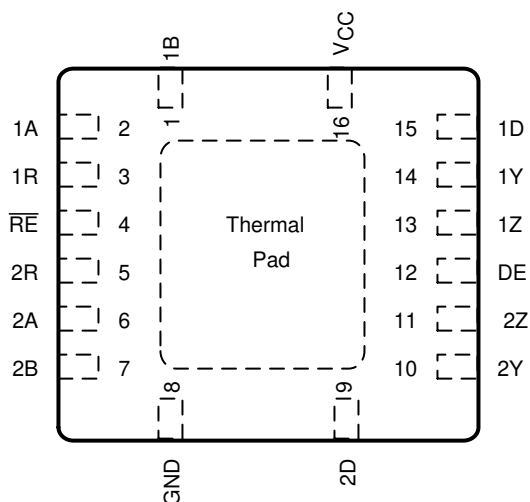


图 4-2. RGY Package 16 Pin (VQFN) Top View

表 4-1. Pin Functions, SN65C1167E

NAME	PIN			I/O	DESCRIPTION
	SO	TSSOP	VQFN		
1A	2	2	2	I	RS422 differential input (noninverting) to receiver 1
2A	6	6	6	I	RS422 differential input (noninverting) to receiver 2
1B	1	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	15	I	Logic data input to RS422 driver 1
2D	9	9	9	I	Logic data input to RS422 driver 2
DE	12	12	12	I	Driver enable (active high)
GND	8	8	8	—	Device ground pin
1R	3	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	5	O	Logic data output of RS422 receiver 2
RE	4	4	4	I	Receiver enable pin (active low)
V _{CC}	16	16	16	—	Power supply
1Y	14	14	14	O	RS-422 differential (noninverting) driver output 1
2Y	10	10	10	O	RS-422 differential (noninverting) driver output 2
1Z	13	13	13	O	RS-422 differential (inverting) driver output 1
2Z	11	11	11	O	RS-422 differential (inverting) driver output 2

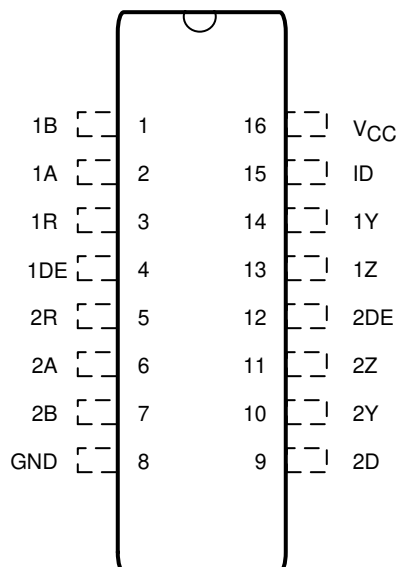


图 4-3. NS or PW Package 16 Pin (NS or TSSOP)
Top View

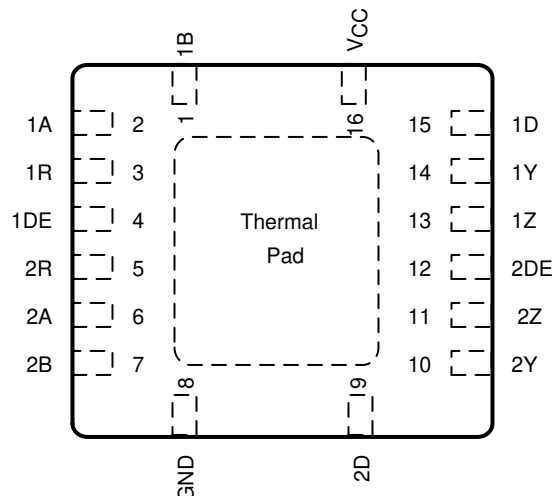


图 4-4. RGY Package 16 Pin (VQFN) Top View

表 4-2. Pin Functions, SN65C1168E

NAME	PIN			I/O	DESCRIPTION
	SO	TSSOP	VQFN		
1A	2	2	2	I	RS422 differential input (noninverting) to receiver 1
2A	6	6	6	I	RS422 differential input (noninverting) to receiver 2
1B	1	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	15	I	Logic data input to RS422 driver 1
2D	9	9	9	I	Logic data input to RS422 driver 2
1DE	4	4	4	I	Driver 1 enable (active high)
2DE	12	12	12	I	Driver 2 enable (active high)
GND	8	8	8	—	Device ground
1R	3	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	5	O	Logic data output of RS422 receiver 2
V _{CC}	16	16	16	—	Power supply
1Y	14	14	14	O	RS-422 differential (noninverting) driver output 1
2Y	10	10	10	O	RS-422 differential (noninverting) driver output 2
1Z	13	13	13	O	RS-422 differential (noninverting) driver output 1
2Z	11	11	11	O	RS-422 differential (noninverting) driver output 2

5 Specifications

5.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		- 0.5	7	V
V _I	Input voltage	Driver, DE, RE	- 0.5	7	V
		A or B, Receiver	- 14	14	
V _{ID}	Differential input voltage ⁽³⁾	Receiver	- 14	14	V
V _O	Output voltage	Driver	- 0.5	7	V
		Receiver	- 0.5	V _{CC} + 0.5	
I _{IK}	Input clamp current	Driver, V _I < 0		- 20	mA
I _{OK}	Output clamp current	Driver, V _O < 0		- 20	mA
		Receiver		±20	
I _O	Output current	Driver		±150	mA
		Receiver		±25	
I _{CC}	Supply current			200	mA
	GND current			- 200	mA
T _J	Operating virtual junction temperature			150	°C
T _A	Operating free-air temperature		- 40	85	°C
T _{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential input voltage are with respect to the network GND.
- (3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

5.2 Driver Output and Receiver Input ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±15000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		IEC 61000-4-2, air-gap discharge	±8000
		IEC 61000-4-2, contact discharge	±8000

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IC}	Common-mode input voltage ⁽¹⁾	Receiver			±7	V
V _{ID}	Differential input voltage	Receiver			±7	V
V _I	Input voltage	Except A, B	0		5.5	V
V _O	Output voltage	Receiver	0		V _{CC}	V
V _{IH}	High-level input voltage	Except A, B	2			V
V _{IL}	Low-level input voltage	Except A, B			0.8	V
I _{OH}	High-level output current	Receiver			- 6	mA
		Driver			- 20	
I _{OL}	Low-level output current	Receiver			6	mA
		Driver			20	
T _A	Operating free-air temperature		- 40		85	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65C116xE			UNIT
		SO (NS)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	88.5	107.5	48.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	46.2	38.4	46.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	50.7	53.7	24.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	13.5	3.2	2.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	50.3	53.1	24.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	8.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Driver Section Electrical Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK} Input clamp voltage	I _I = -18mA			-1.5	V
V _{OH} High-level output voltage	V _{IH} = 2V, V _{IL} = 0.8V, I _{OH} = -20mA	2.4	3.5		V
V _{OL} Low-level output voltage	V _{IH} = 2V, V _{IL} = 0.8V, I _{OL} = 20mA		0.2	0.4	V
V _{OD1} Differential output voltage 1	I _O = 0mA	2		6	V
V _{OD2} Differential output voltage 2	R _L = 100Ω, See 图 6-1 ⁽²⁾	2	3.7		V
Δ V _{OD} Change in magnitude of differential output voltage	R _L = 100Ω, See 图 6-1 ⁽²⁾			±0.4	V
V _{OC} Common-mode output voltage	R _L = 100Ω, See 图 6-1 ⁽²⁾			±3	V
Δ V _{OC} Change in magnitude of common-mode output voltage	R _L = 100Ω, See 图 6-1 ⁽²⁾			±0.4	V
I _{O(OFF)} Output current with power off	V _{CC} = 0V			100	μA
				100	
I _{OZ} High-impedance-state output current	V _O = 2.5V			20	μA
				-20	
I _{IH} High-level input current	V _I = V _{CC} or V _{IH}			1	μA
I _{IL} Low-level input current	V _I = GND or V _{IL}			-1	μA
I _{OS} Short-circuit output current	V _O = V _{CC} or GND ⁽³⁾	-30		-150	mA
I _{CC} Supply current (total package)	No load, Enabled			4	mA
				5	
C _i Input capacitance			6		pF

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) Refer to TIA/EIA-422-B for exact conditions.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

5.6 Receiver Section Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+} Positive-going input threshold voltage, differential input				0.2	V
V _{IT-} Negative-going input threshold voltage, differential input		-0.2 ⁽²⁾			V
V _{hys} Input hysteresis (V _{IT+} - V _{IT-})			60		mV
V _{IK} Input clamp voltage, RE	SN65C1167E, I _I = -18mA			-1.5	V
V _{OH} High-level output voltage	V _{ID} = 200mV, I _{OH} = -6mA	3.8	4.2		V
V _{OL} Low-level output voltage	V _{ID} = -200mV, I _{OL} = 6mA		0.1	0.3	V
I _{OZ} High-impedance state output current	SN65C1167E, V _O = V _{CC} or GND		±0.5	±5	μA
I _I Line input current	Other input at 0V			1.5	mA
				-2.5	
I _I Enable input current, RE	SN65C1167E, V _I = V _{CC} or GND			±1	μA
r _i Input resistance	V _{IC} = -7V to 7V, Other input at 0V	4	17		kΩ
I _{CC} Supply current (total package)	No load, Enabled			4	mA
				5	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) Refer to TIA/EIA-422-B for exact conditions.

5.7 Driver Section Switching Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50Ω, R3 = 500Ω, C1 = C2 = C3 = 40pF, S1 is open, See 图 6-2		8	16	ns
t_{PLH}	Propagation delay time, low- to high-level output			8	16	ns
$t_{sk(p)}$	Pulse skew			1.5	4	ns
t_r	Rise time	R1 = R2 = 50Ω, R3 = 500Ω, C1 = C2 = C3 = 40pF, S1 is open, See 图 6-3		5	8	ns
t_f	Fall time			5	8	ns
t_{PZH}	Output-enable time to high level	R1 = R2 = 50Ω, R3 = 500Ω, C1 = C2 = C3 = 40pF, S1 is closed, See 图 6-4		10	19	ns
t_{PZL}	Output-enable time to low level			10	19	ns
t_{PHZ}	Output-disable time from high level	R1 = R2 = 50Ω, R3 = 500Ω, C1 = C2 = C3 = 40pF, S1 is closed, See 图 6-4		7	16	ns
t_{PLZ}	Output-disable time from low level			7	16	ns
f_{SW}	Maximum switching frequency	R1 = R2 = 50Ω, R3 = 500Ω, C1 = C2 = C3 = 40pF, S1 is open, See 图 6-3	20			MHz

(1) All typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

5.8 Receiver Section Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 图 6-5	9	15	27	ns
t_{PHL}	Propagation delay time, high- to low-level output	See 图 6-5	9	15	27	ns
t_{TLH}	Transition time, low- to high-level output	$V_{IC} = V$, See 图 6-5		4	9	ns
t_{THL}	Transition time, high- to low-level output			4	9	ns
t_{PZH}	Output-enable time to high level	SN65C1167E $R_L = 1k\Omega$, $C_L = 50pF$ See 图 6-6		7	22	ns
t_{PZL}	Output-enable time to low level			7	22	ns
t_{PHZ}	Output-disable time from high level			12	22	ns
t_{PLZ}	Output-disable time from low level			12	22	ns

(1) All typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

(2) Measured per input while the other inputs are at V_{CC} or GND

6 Parameter Measurement Information

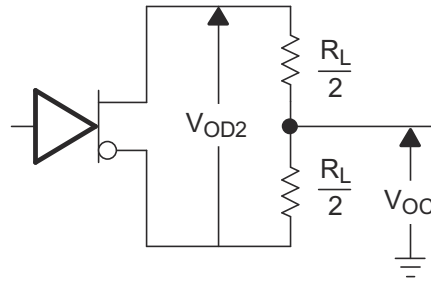
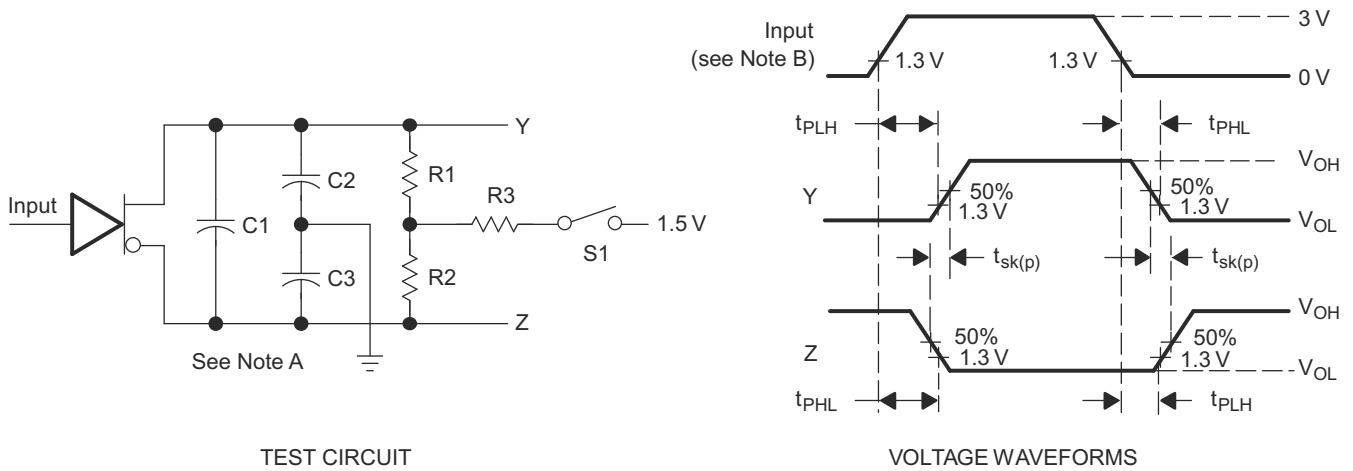
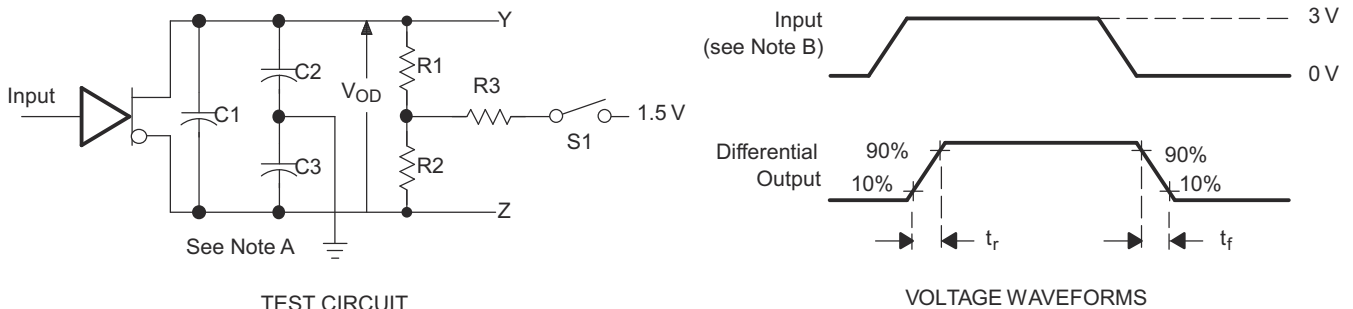


图 6-1. Driver Test Circuit, V_{OD2} and V_{OC}



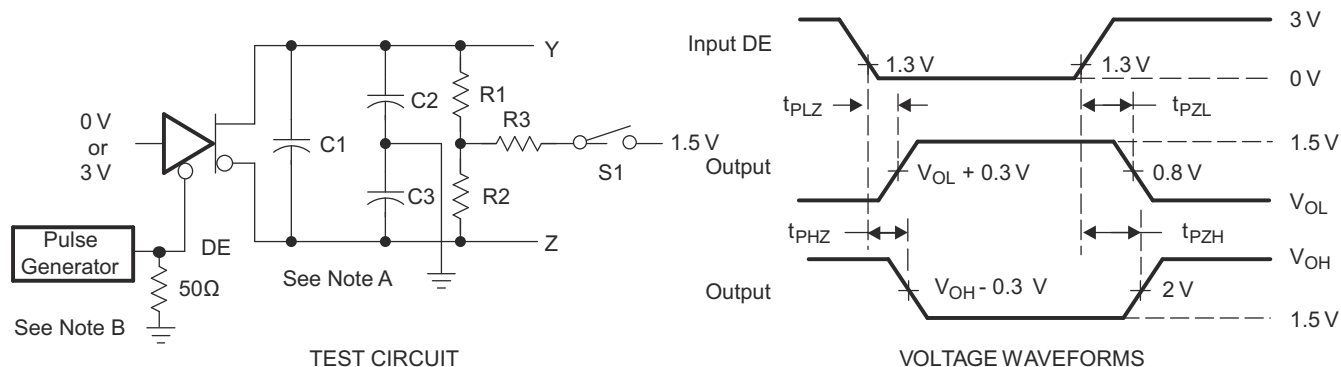
- A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

图 6-2. Driver Test Circuit and Voltage Waveforms



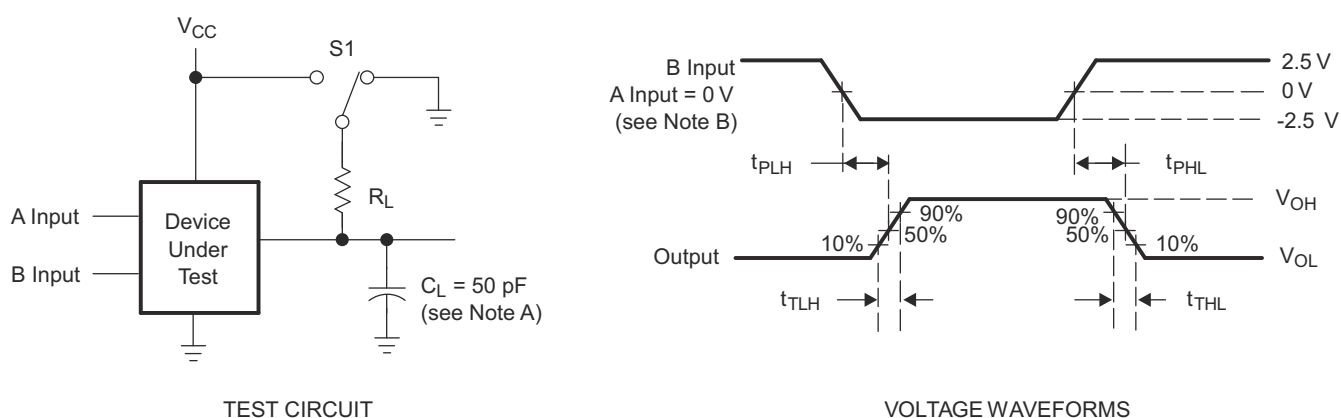
- A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

图 6-3. Driver Test Circuit and Voltage Waveforms



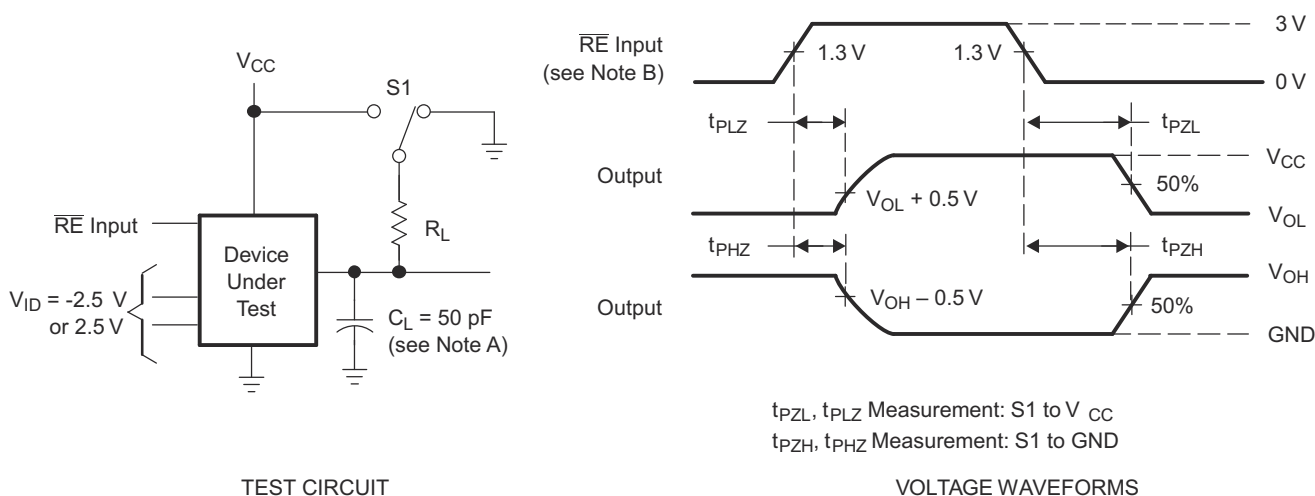
- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

图 6-4. Driver Test Circuit and Voltage Waveforms



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

图 6-5. Receiver Test Circuit and Voltage Waveforms



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

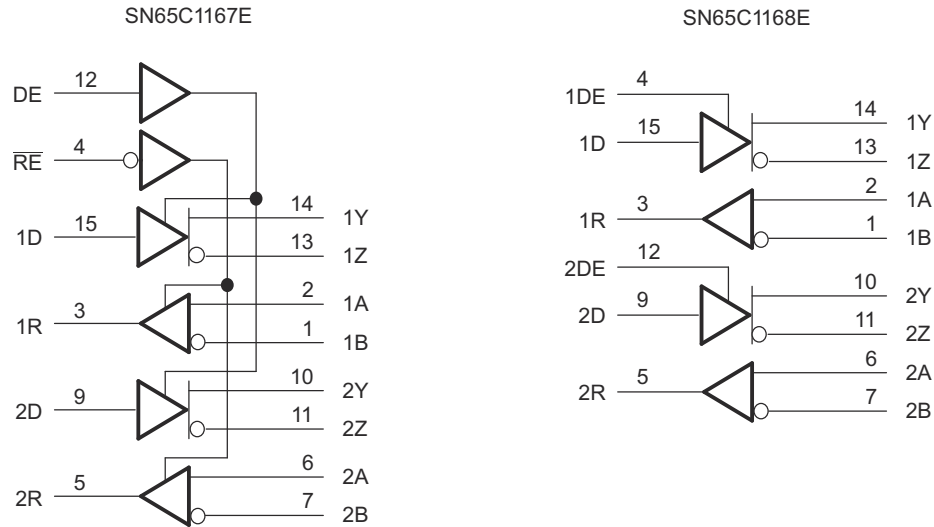
图 6-6. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN65C1167E and SN65C1168E consist of dual drivers and dual receivers powered from a single 5V supply. These devices meet the requirements of TIA/EIA-422-B and ITU recommendation V.11.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Active High Driver Output Enables

Both drivers of SN65C1167E can be configured with the single DE logic input. Both drivers are set at high-impedance when disabled.

SN65C1168E drivers can be configured individually by 1DE and 2DE logic inputs. Both drivers are set at high-impedance when disabled.

7.3.2 Active Low Receiver Enables

Both SN65C1167E receivers can be configured with the single $\overline{RE}$ logic input. Receiver logic outputs are set at high-impedance when disabled.

7.4 Device Functional Modes

表 7-1 和 表 7-2 list the functional modes of SN65C1167E and SN65C1168E.

表 7-1. Each Driver

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

表 7-2. SN65C1167E, Each Receiver⁽¹⁾

DIFFERENTIAL INPUTS A - B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Open	L	H

(1) H = High level, L = Low level, ? = Indeterminate, X = Irrelevant, Z = High impedance (off)

表 7-3. SN65C1168E, Each Receiver⁽¹⁾

DIFFERENTIAL INPUTS A - B	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	?
$V_{ID} \leq -0.2\text{ V}$	L
Open	H

(1) H = High level, L = Low level, ? = Indeterminate

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

图 8-1 shows a typical RS-422 application. One transmitter is able to broadcast to multiple receiving nodes connected together over a shared differential bus. Twisted-pair cabling with a controlled differential impedance is used, and a termination resistance is placed at the farthest receive end of the cable in order to match the transmission line impedance and minimize signal reflections.

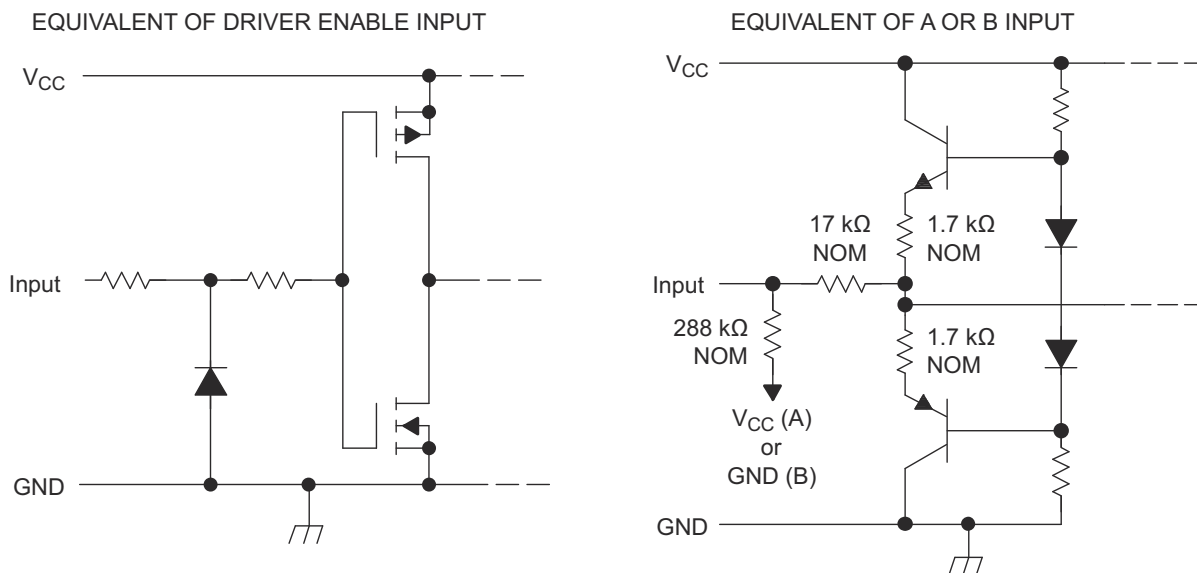


图 8-1. Schematic of Inputs

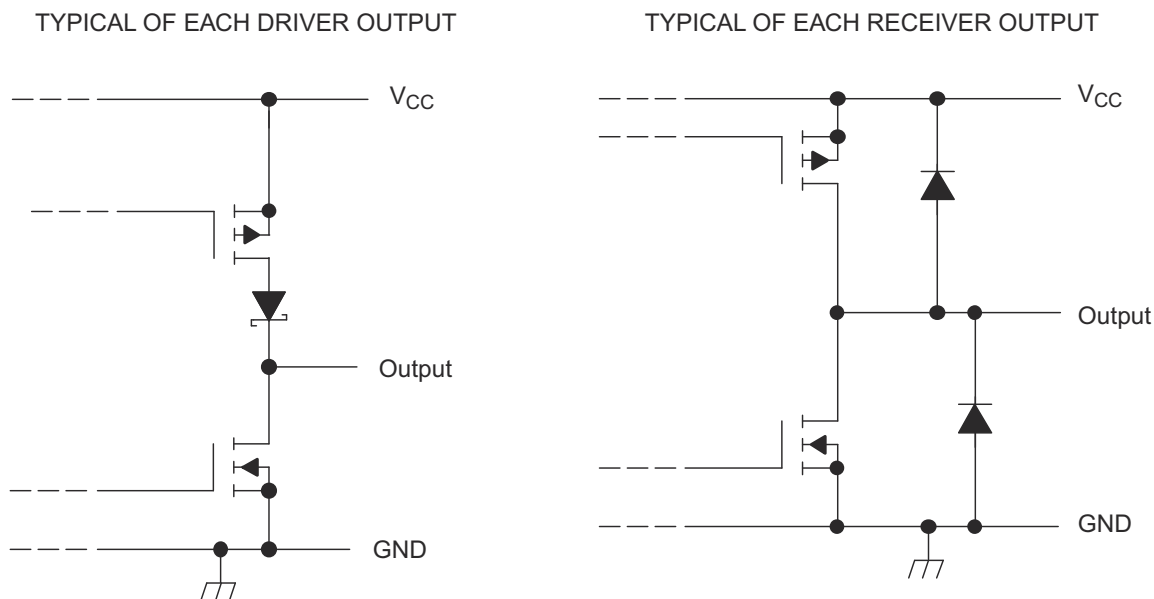


图 8-2. Schematic of Outputs

8.2 Typical Application

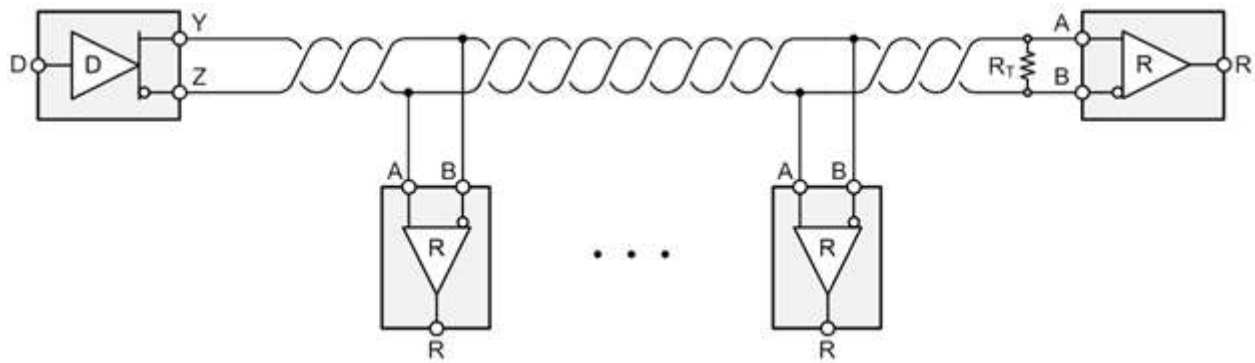


图 8-3. Typical RS-422 Application

8.2.1 Design Requirements

A typical RS-422 implementation using SN65C116xE requires the following:

- 5V power source.
- Connector that ensures the correct polarity for port pins.
- Cabling that supports the desired operating rate and transmission distance.

8.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure ± 200 mV on the A-B port when the driver circuit is disabled.

8.3 Power Supply Recommendations

Use a 5V power supply for V_{CC} place $0.1 \mu\text{F}$ bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high impedance power supplies.

9 Device and Documentation Support

9.1 Device Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 支持资源

[TI E2E™ 中文支持论坛](#)是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.4 Trademarks

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9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (May 2017) to Revision C (February 2024)	Page
• 将“器件信息”表更改为“封装信息”表.....	1
• Deleted the thermal packaging information from the <i>Absolute Maximum Ratings</i>	5
• Changed the <i>Thermal Information</i> table.....	6

Changes from Revision A (April 2007) to Revision B (May 2017)	Page
• 添加了 <i>ESD</i> 等级表、特性说明部分、器件功能模式、应用和实施方式部分、电源相关建议部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Changed the Rise Time Max value From: 10 ns To: 8 ns in the <i>Driver Section Switching Characteristics</i> table.....	8
• Changed the Fall Time Max value From: 10 ns To: 8 ns in the <i>Driver Section Switching Characteristics</i> table.....	8
• Added Maximum switching frequency to the <i>Driver Section Switching Characteristics</i> table.....	8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C1167ENS	Obsolete	Production	SOP (NS) 16	-	-	Call TI	Call TI	-40 to 85	65C1167E
SN65C1167ENSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167ENSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167ENSRG4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167ENSRG4.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167EPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	CB1167E
SN65C1167EPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167EPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167EPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167EPWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167ERGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1167ERGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1167ERGYRG4	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1167ERGYRG4.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1168ENSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168E
SN65C1168ENSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168E
SN65C1168EPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	CB1168E
SN65C1168EPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E
SN65C1168EPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E
SN65C1168EPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E
SN65C1168ERGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB1168
SN65C1168ERGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB1168
SN65C1168ERGYRG4	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168
SN65C1168ERGYRG4.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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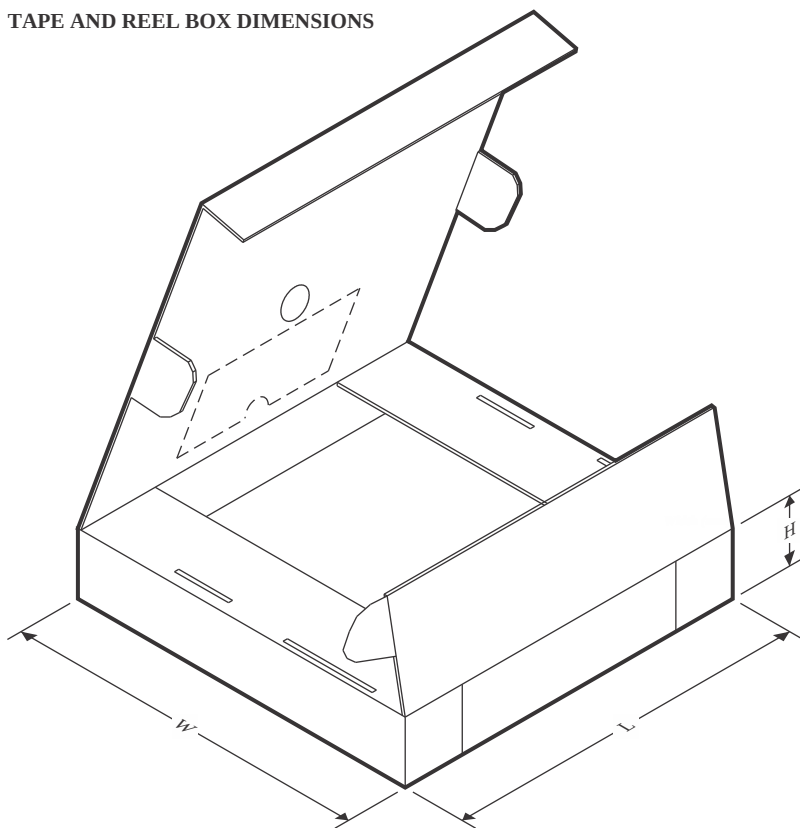
TAPE AND REEL INFORMATION



*All dimensions are nominal

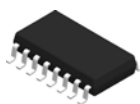
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1167ENSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65C1167ENSRG4	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65C1167EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1167EPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1167ERGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65C1167ERGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65C1168ENSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65C1168EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1168ERGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65C1168ERGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1167ENSR	SOP	NS	16	2000	353.0	353.0	32.0
SN65C1167ENSRG4	SOP	NS	16	2000	353.0	353.0	32.0
SN65C1167EPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C1167EPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C1167ERGYR	VQFN	RGY	16	3000	360.0	360.0	36.0
SN65C1167ERGYRG4	VQFN	RGY	16	3000	360.0	360.0	36.0
SN65C1168ENSR	SOP	NS	16	2000	353.0	353.0	32.0
SN65C1168EPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C1168ERGYR	VQFN	RGY	16	3000	360.0	360.0	36.0
SN65C1168ERGYRG4	VQFN	RGY	16	3000	360.0	360.0	36.0

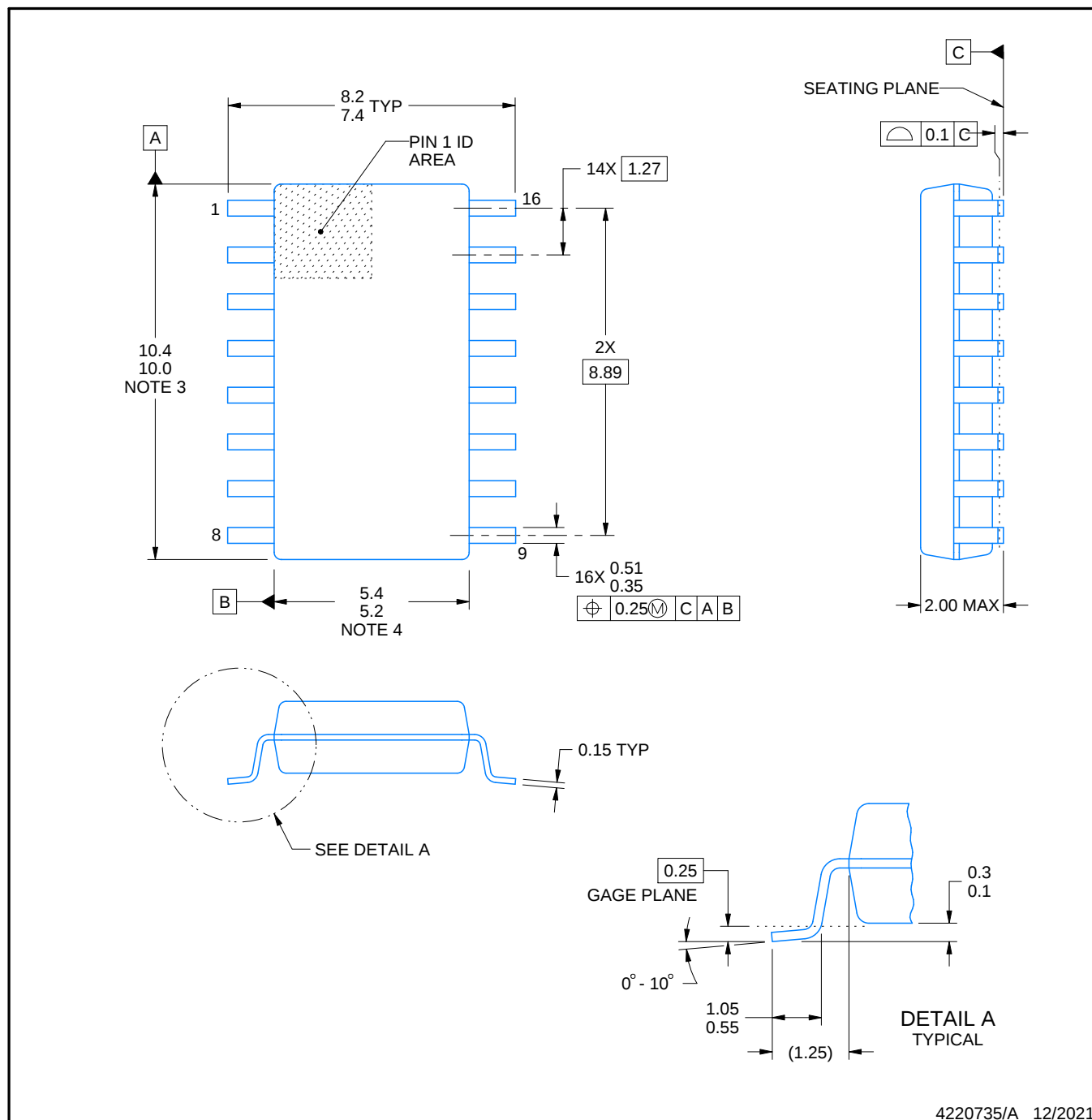


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

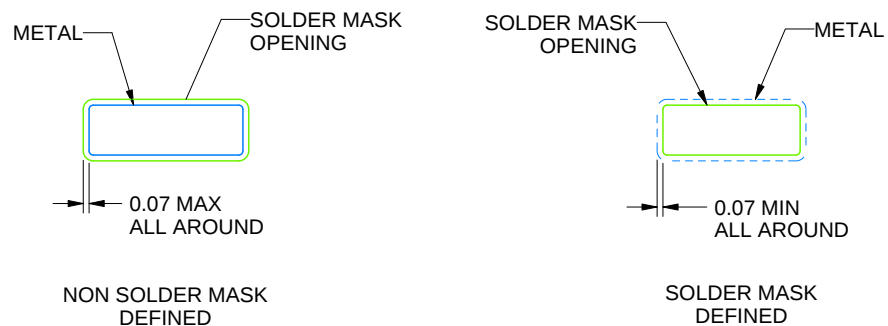
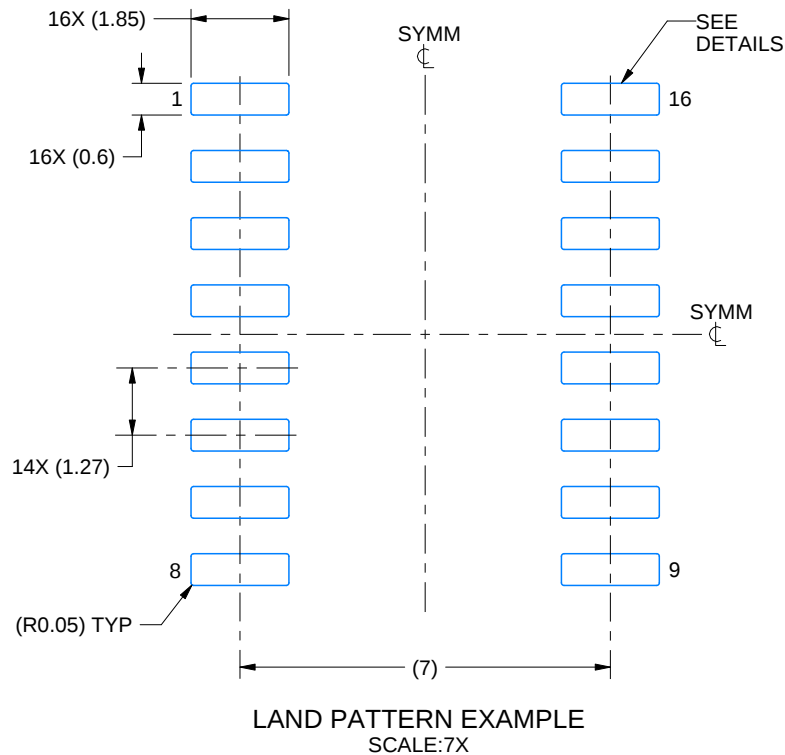
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



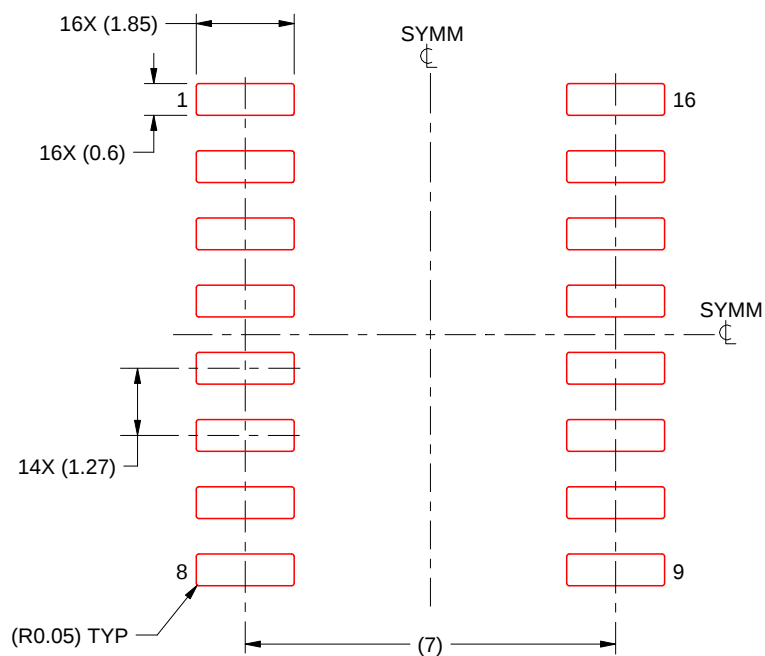
SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

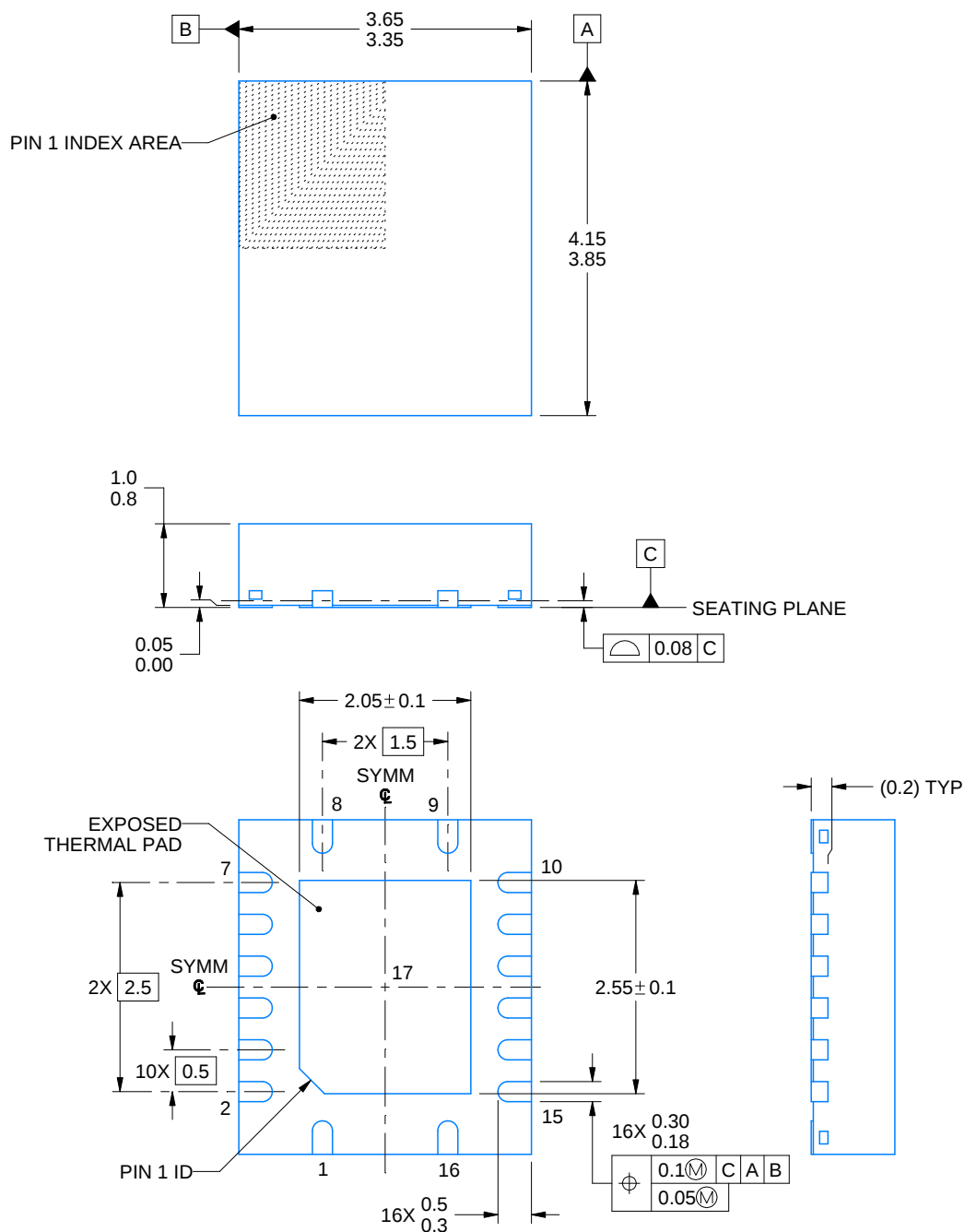
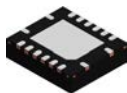


SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4225140/A 07/2019

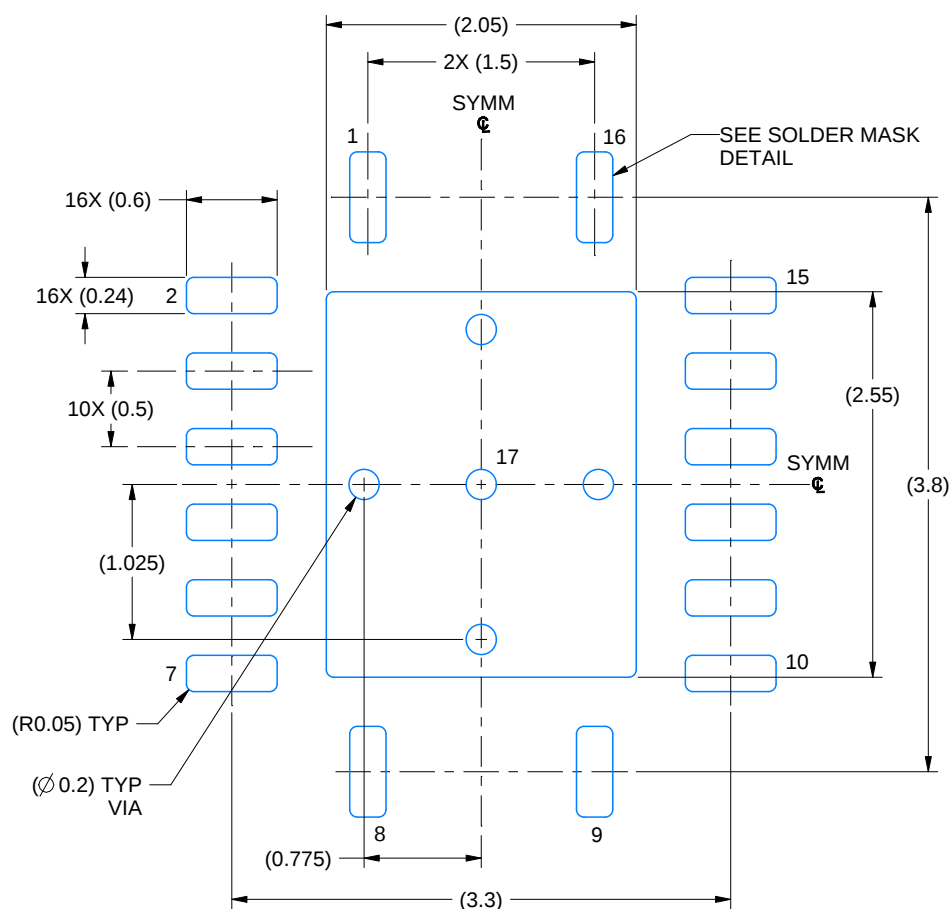
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

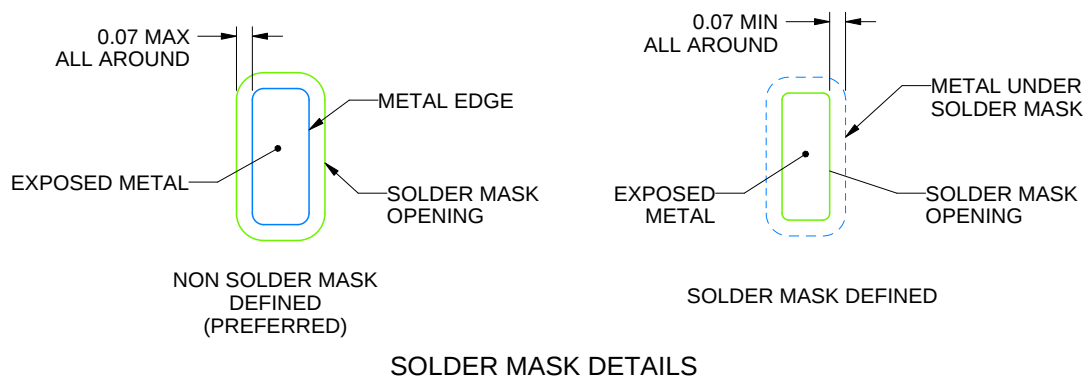
RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4225140/A 07/2019

NOTES: (continued)

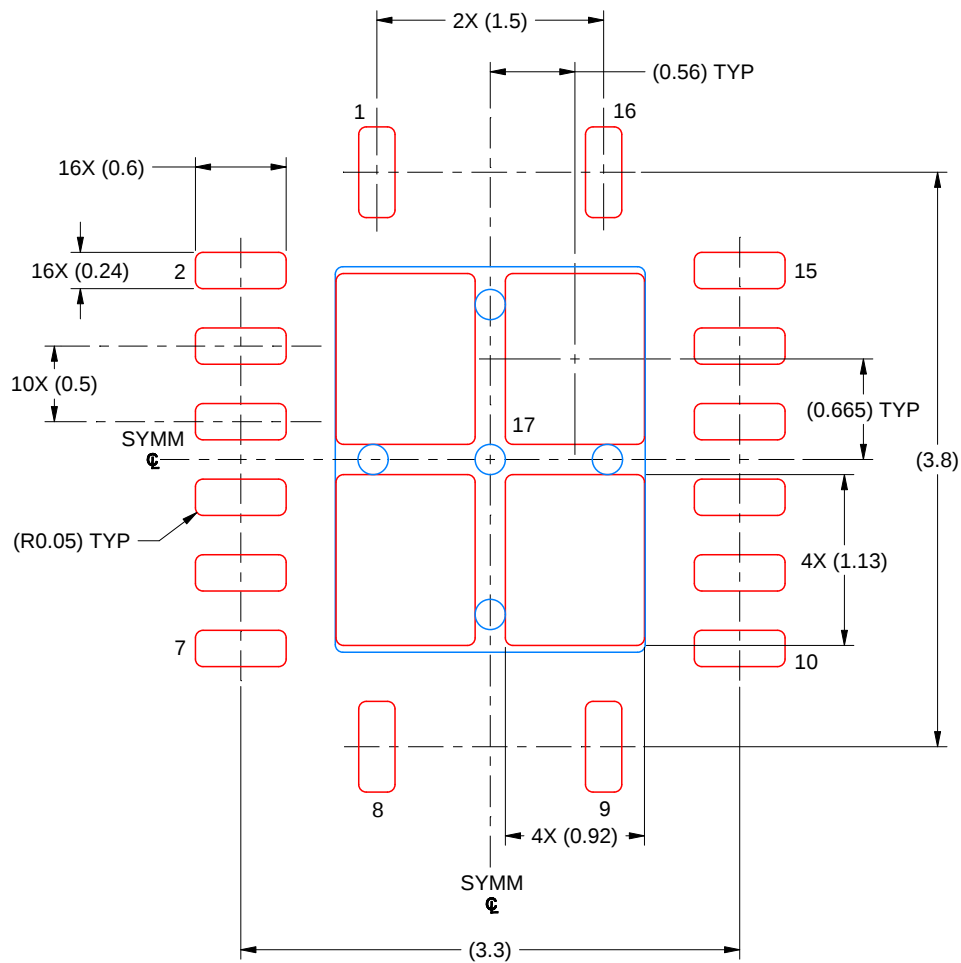
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225140/A 07/2019

NOTES: (continued)

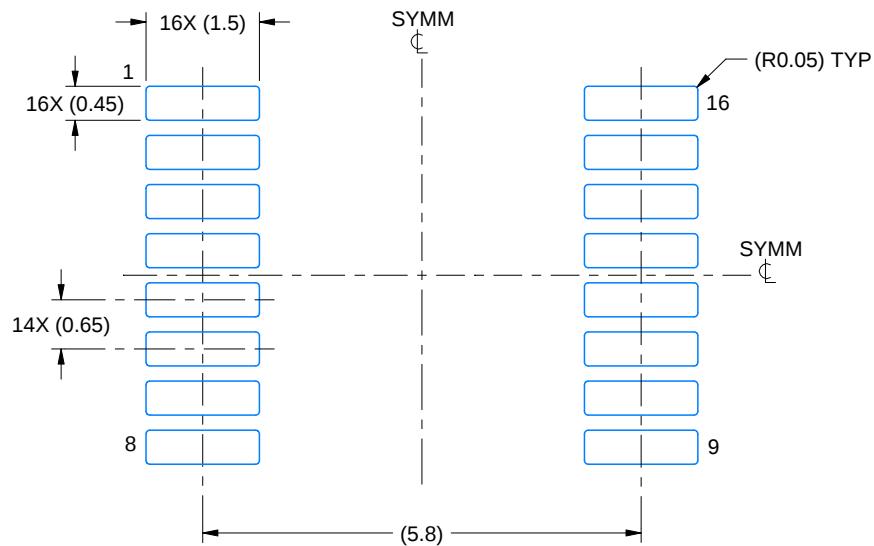
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

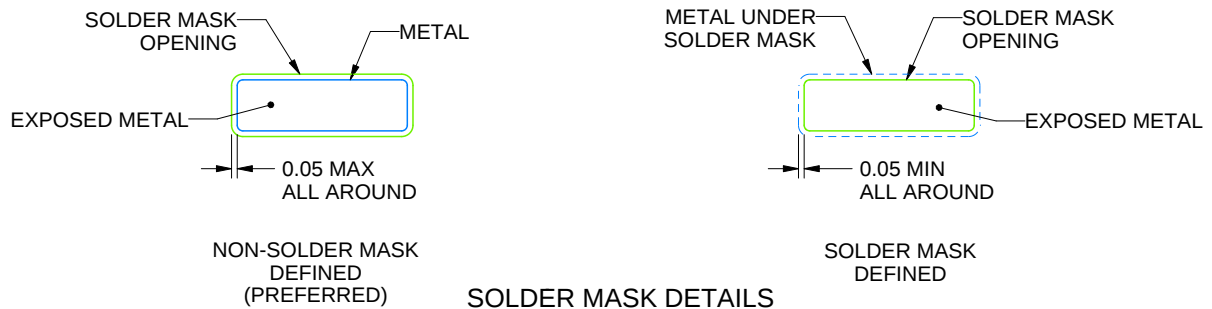
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

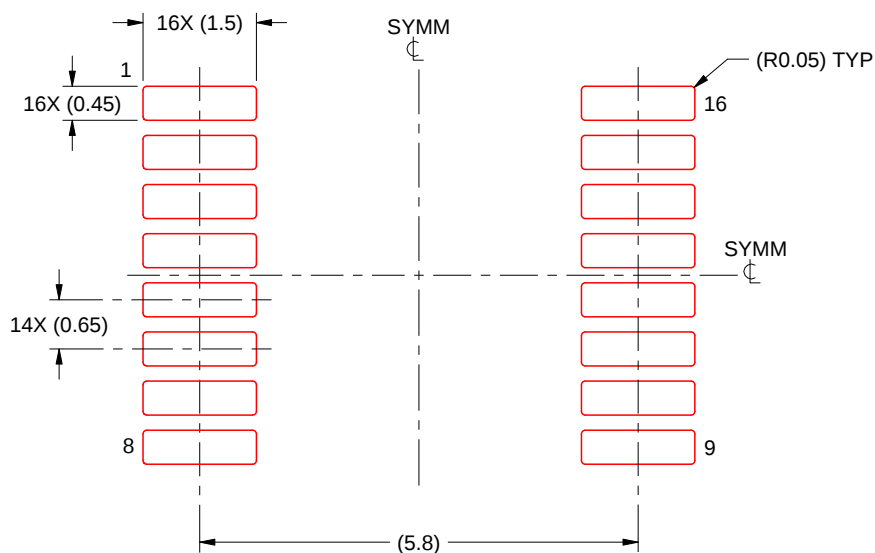
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月