



## 1.5-Gbps LVDS/LVPECL/CML-TO-CML TRANSLATOR/REPEATER

### FEATURES

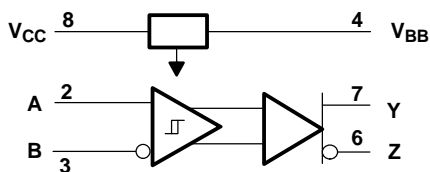
- Provides Level Translation From LVDS or LVPECL to CML, Repeating From CML to CML
- Signaling Rates<sup>(1)</sup> up to 1.5 Gbps
- CML Compatible Output Directly Drives Devices With 3.3-V, 2.5-V, or 1.8-V Supplies
- Total Jitter < 70 ps
- Low 100 ps (Max) Part-To-Part Skew
- Wide Common-Mode Receiver Capability Allows Direct Coupling of Input Signals
- 25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range
- Propagation Delay Times, 800 ps Maximum
- 3.3-V Supply Operation
- Available in SOIC and MSOP Packages

### APPLICATIONS

- Level Translation
- 622-MHz Central Office Clock Distribution
- High-Speed Network Routing
- Wireless Basestations
- Low Jitter Clock Repeater<sup>(1)</sup>

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

### FUNCTIONAL DIAGRAM



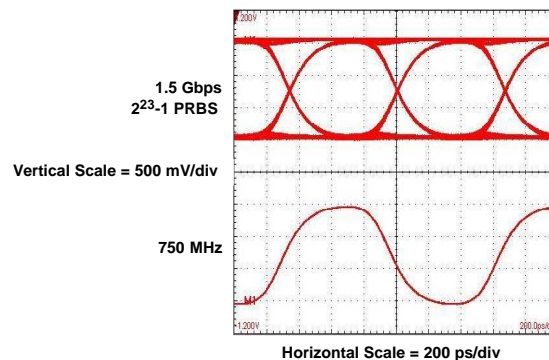
### DESCRIPTION

This high-speed translator/repeater is designed for signaling rates up to 1.5 Gbps to support various high-speed network routing applications. The driver output is compatible with current-mode logic (CML) levels, and directly drives 50-Ω or 25-Ω loads connected to 1.8-V, 2.5-V, or 3.3-V nominal supplies. The capability for direct connection to the loads may eliminate the need for coupling capacitors. The receiver input is compatible with LVDS (TIA/EIA-644), LVPECL, and CML signaling levels. The receiver tolerates a wide common-mode voltage range, and may also be directly coupled to the signal source. The internal data path from input to output is fully differential for low noise generation and low pulse-width distortion.

The  $V_{BB}$  pin is an internally generated voltage supply to allow operation with a single-ended LVPECL input. For single-ended LVPECL input operation, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage. When used, decouple  $V_{BB}$  with a 0.01-μF capacitor and limit the current sourcing or sinking to 400 μA. When not used,  $V_{BB}$  should be left open.

This device is characterized for operation from -40°C to 85°C.

### EYE PATTERN



$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $|V_{ID}| = 200\text{ mV}$ ,  $V_{IC} = 1.2\text{ V}$ ,  $V_{TT} = 3.3\text{ V}$ ,  $R_T = 50\ \Omega$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE	STATUS
SN65CML100D	CML100	SOIC	Production
SN65CML100DGK	NWB	MSOP	Production

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

		UNIT	
$V_{CC}$	Supply voltage range <sup>(2)</sup>	–0.5 V to 4 V	
$I_{BB}$	Sink/source	±0.5 mA	
	Voltage range, (A, B, Y, Z)	0 V to 4.3 V	
Electrostatic discharge	Human Body Model <sup>(3)</sup>	A, B, Y, Z, and GND	±5 kV
		All pins	±2 kV
	Charged-Device Model <sup>(4)</sup>	All pins	±1500 V
	Continuous power dissipation	See Dissipation Rating Table	
$T_{stg}$	Storage temperature range	–65°C to 150°C	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

### RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT		
$V_{CC}$	Supply voltage	3	3.3	3.6	V		
$V_{TT}$	Terminator supply voltage	3.3-V nominal supply at terminator		3	3.3	3.6	V
		2.5-V nominal supply at terminator		2.375	2.5	2.625	V
		1.8-V nominal supply at terminator		1.7		1.9	V
$ V_{ID} $	Magnitude of differential input voltage	0.1		1	V		
	Input voltage (any combination of common-mode or input signals)	0		4	V		
$V_{BB}$	Output current			400	μA		
$T_A$	Operating free-air temperature	–40		85	°C		

### PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DGK	425 mW	3.4 mW/°C	221 mW
D	725 mW	5.8 mW/°C	377 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## DEVICE CHARACTERISTICS

PARAMETER		MIN	NOM	MAX	UNIT
$I_{CC}$	Supply current, device only		9	12	mA
$V_{BB}$	Switching reference voltage <sup>(1)</sup>	1890	1950	2010	mV

(1)  $V_{BB}$  parameter varies 1:1 with  $V_{CC}$

## INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT+}$	Positive-going differential input voltage threshold	See Figure 1 and Table 1				100	mV
$V_{IT-}$	Negative-going differential input voltage threshold			-100			
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$				25		mV
$I_I$	Input current (A or B inputs)	$V_I = 0$ V or 2.4 V, Second input at 1.2 V		-20		20	$\mu$ A
		$V_I = 4$ V, Second input at 1.2 V				33	
$I_{I(OFF)}$	Power off input current (A or B inputs)	$V_{CC} = 1.5$ V, $V_I = 0$ V or 2.4 V, Second input at 1.2 V		-20		20	$\mu$ A
		$V_{CC} = 1.5$ V, $V_I = 4$ V, Second input at 1.2 V				33	
$I_{IO}$	Input offset current ( $ I_{IA} - I_{IB} $ )	$V_{IA} = V_{IB}$ , $0 \leq V_{IA} \leq 4$ V		-6		6	$\mu$ A
$C_i$	Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V			3		pF
		$V_{CC} = 0$ V			3		

(1) All typical values are at 25°C and with a 3.3-V supply.

## OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$	Output high voltage <sup>(2)</sup>	$R_T = 50$ $\Omega$ , $V_{TT} = 3$ V to 3.6 V or $V_{TT} = 2.5$ V $\pm 5\%$ , See Figure 2		$V_{TT}-60$	$V_{TT}-10$	$V_{TT}$	mV
$V_{OL}$	Output low voltage <sup>(2)</sup>			$V_{TT}-1100$	$V_{TT}-800$	$V_{TT}-640$	mV
$ V_{OD} $	Differential output voltage magnitude			640	780	1000	mV
$V_{OH}$	Output high voltage <sup>(3)</sup>	$R_T = 25$ $\Omega$ , $V_{TT} = 3$ V to 3.6 V or $V_{TT} = 2.5$ V $\pm 5\%$ , See Figure 2		$V_{TT}-60$	$V_{TT}-10$	$V_{TT}$	mV
$V_{OL}$	Output low voltage <sup>(3)</sup>			$V_{TT}-550$	$V_{TT}-400$	$V_{TT}-320$	mV
$ V_{OD} $	Differential output voltage magnitude			320	390	500	mV
$V_{OH}$	Output high voltage <sup>(2)</sup>	$R_T = 50$ $\Omega$ , $V_{TT} = 1.8$ V $\pm 5\%$ , See Figure 2		$V_{TT}-170$	$V_{TT}-10$	$V_{TT}$	mV
$V_{OL}$	Output low voltage <sup>(2)</sup>			$V_{TT}-1100$	$V_{TT}-800$	$V_{TT}-640$	mV
$ V_{OD} $	Differential output voltage magnitude			570	780	1000	mV
$V_{OH}$	Output high voltage <sup>(3)</sup>	$R_T = 25$ $\Omega$ , $V_{TT} = 1.8$ V $\pm 5\%$ , See Figure 2		$V_{TT}-85$	$V_{TT}-10$	$V_{TT}$	mV
$V_{OL}$	Output low voltage <sup>(3)</sup>			$V_{TT}-500$	$V_{TT}-400$	$V_{TT}-320$	mV
$ V_{OD} $	Differential output voltage magnitude			285	390	500	mV
$C_o$	Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V			3		pF
		$V_{CC} = 0$ V			3		

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) Outputs are terminated through 50- $\Omega$  resistors to  $V_{TT}$ ; CML level specifications are referenced to  $V_{TT}$  and tracks 1:1 with variation of  $V_{TT}$ .

(3) Outputs are terminated through 25- $\Omega$  resistors to  $V_{TT}$ ; CML level specifications are referenced to  $V_{TT}$  and tracks 1:1 with variation of  $V_{TT}$ .

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$R_T = 50 \Omega$ or $R_T = 25 \Omega$ , See <a href="#">Figure 4</a>	250		800	ps
$t_{PHL}$	Propagation delay time, high-to-low-level output		250		800	ps
$t_r$	Differential output signal rise time (20%–80%)				300	ps
$t_f$	Differential output signal fall time (20%–80%)				300	ps
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ ) <sup>(2)</sup>			0	50	ps
$t_{sk(pp)}$	Part-to-part skew <sup>(3)</sup>	$V_{ID} = 0.2 V$			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) <sup>(4)</sup>	750 MHz clock input <sup>(5)</sup>		1	5	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak) <sup>(4)</sup>	750 MHz clock input <sup>(6)</sup>		8	27	ps
$t_{jit(pp)}$	Peak-to-peak jitter <sup>(4)</sup>	1.5 Gbps 2 <sup>23</sup> -1 PRBS input <sup>(7)</sup>		30	70	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak <sup>(4)</sup>	1.5 Gbps 2 <sup>7</sup> -1 PRBS input <sup>(8)</sup>		25	65	ps

- (1) All typical values are at 25°C and with a 3.3-V supply.
- (2)  $t_{sk(p)}$  is the magnitude of the time difference between the  $t_{PLH}$  and  $t_{PHL}$ .
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (4) Jitter parameters are ensured by design and characterization. Measurements are made with a Tektronix TDS6604 oscilloscope running Tektronix TDSJIT3 software. Agilent E4862B stimulus system jitter 2 ps  $t_{jit(per)}$ , 16 ps  $t_{jit(cc)}$ , 25 ps  $t_{jit(pp)}$ , and 10 ps  $t_{jit(det)}$  has been subtracted from the values.
- (5)  $V_{ID} = 200$  mV, 50% duty cycle,  $V_{IC} = 1.2$  V,  $t_r = t_f \leq 25$  ns (20% to 80%), measured over 1000 samples.
- (6)  $V_{ID} = 200$  mV, 50% duty cycle,  $V_{IC} = 1.2$  V,  $t_r = t_f \leq 25$  ns (20% to 80%).
- (7)  $V_{ID} = 200$  mV,  $V_{IC} = 1.2$  V,  $t_r = t_f \leq 0.25$  ns (20% to 80%), measured over 100k samples.
- (8)  $V_{ID} = 200$  mV,  $V_{IC} = 1.2$  V,  $t_r = t_f \leq 0.25$  ns (20% to 80%). Deterministic jitter is sum of pattern dependent jitter and pulse width distortion.

PARAMETER MEASUREMENT INFORMATION

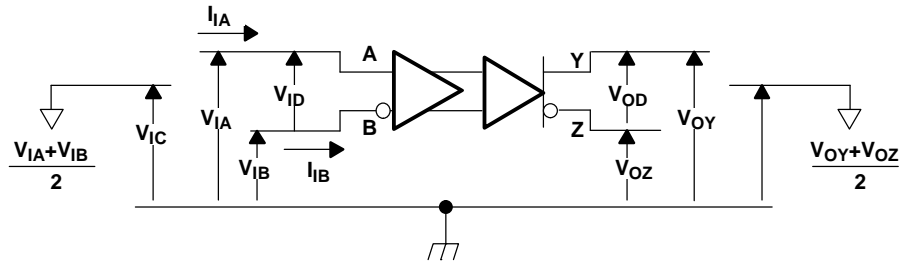


Figure 1. Voltage and Current Definitions

Table 1. Maximum Receiver Input Voltage Threshold

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT <sup>(1)</sup>
V <sub>IA</sub>	V <sub>IB</sub>	V <sub>ID</sub>	V <sub>IC</sub>	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	-100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4.0 V	-100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.5 V	H
0.0 V	0.1 V	-100 mV	0.5 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	-1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	-1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	-1000 mV	0.5 V	L

(1) H = high level, L = low level

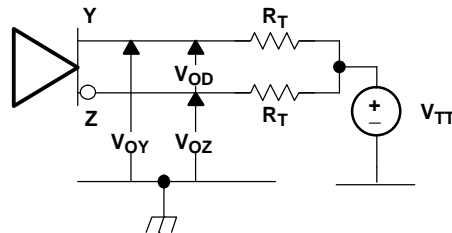


Figure 2. Output Voltage Test Circuit

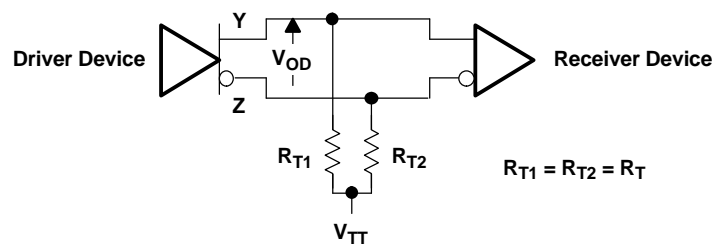
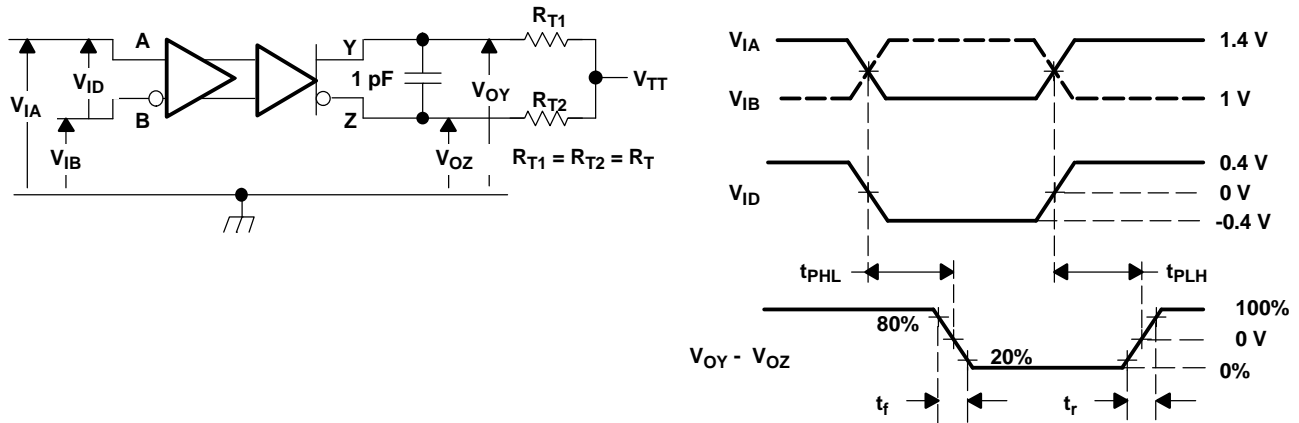


Figure 3. Typical Termination for Output Driver



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 0.25$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 4. Timing Test Circuit and Waveforms

**PIN ASSIGNMENTS**

D AND DGK PACKAGE  
(TOP VIEW)

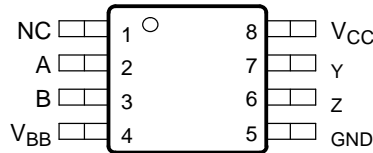


Table 2. PIN DESCRIPTIONS

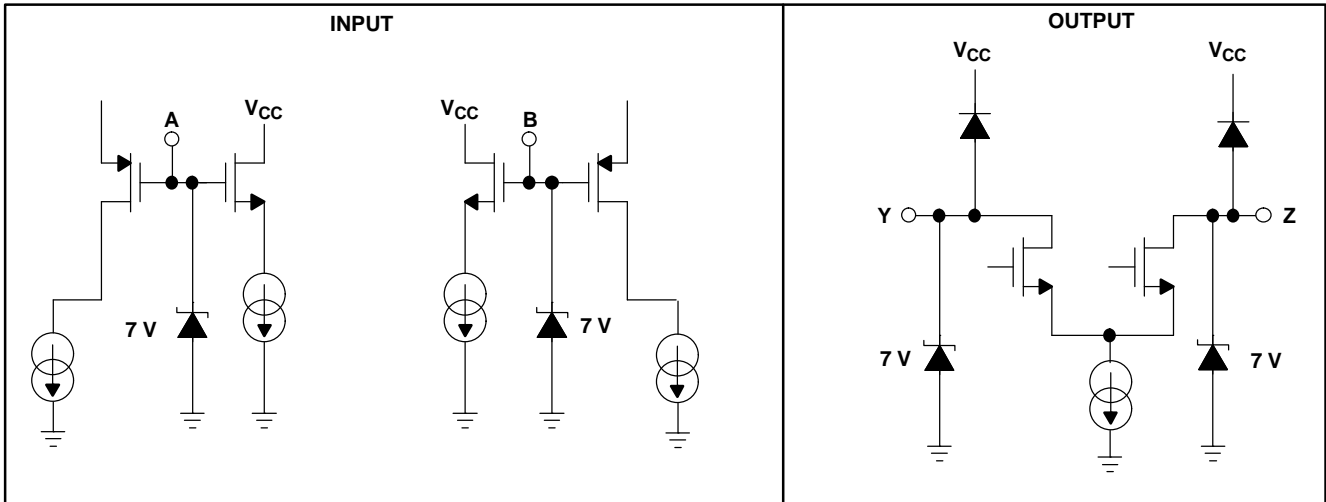
PIN	FUNCTION
A, B	Differential inputs
Y, Z	Differential outputs
$V_{BB}$	Reference voltage output
$V_{CC}$	Power supply
GND	Ground
NC	No connect

Table 3. FUNCTION TABLE

DIFFERENTIAL INPUT	OUTPUTS <sup>(1)</sup>	
$V_{ID} = V_A - V_B$	Y	Z
$V_{ID} \geq 100$ mV	H	L
$-100$ mV $< V_{ID} < 100$ mV	?	?
$V_{ID} \leq -100$ mV	L	H
Open	?	?

(1) H = high level, L = low level, ? = intermediate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

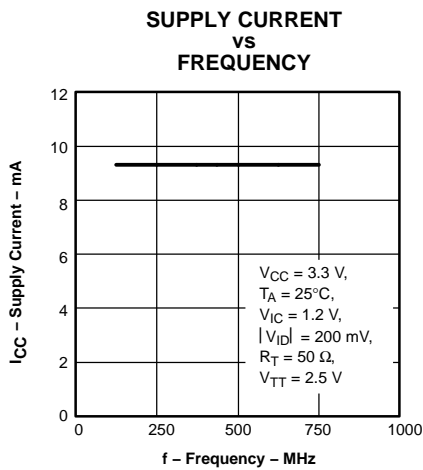


Figure 5.

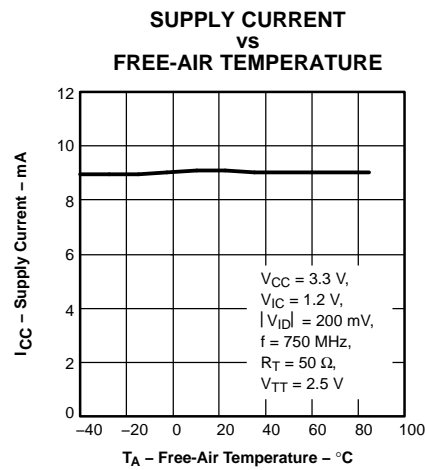


Figure 6.

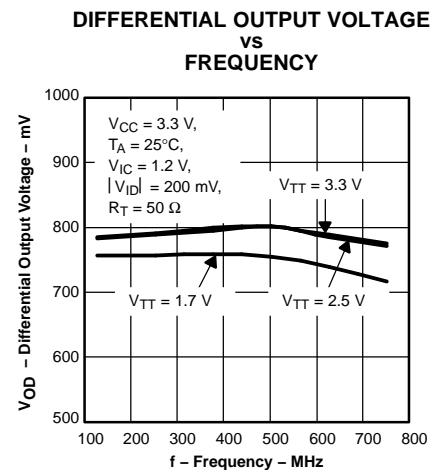


Figure 7.

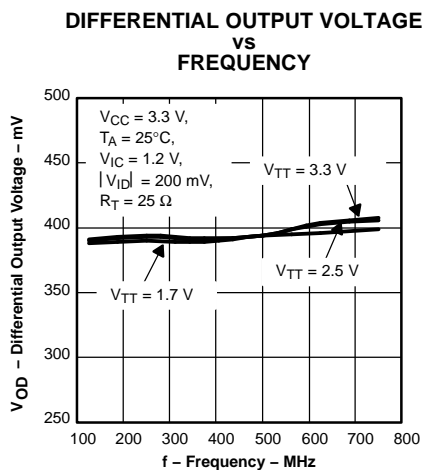


Figure 8.

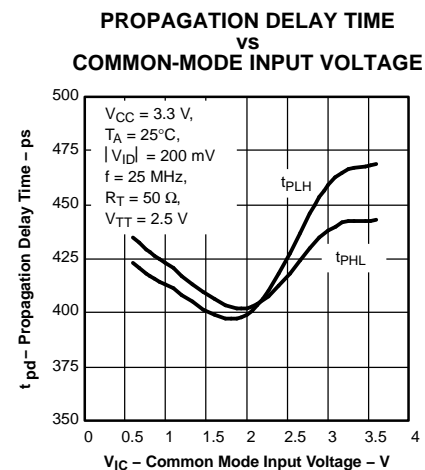


Figure 9.

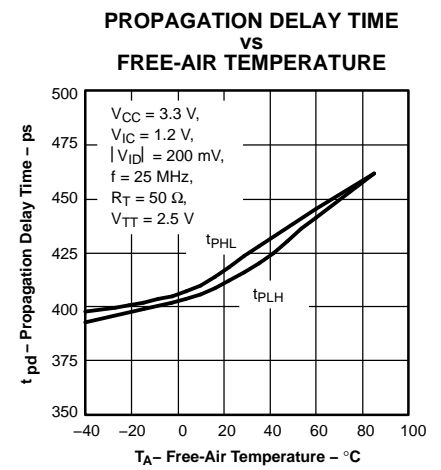


Figure 10.

TYPICAL CHARACTERISTICS (continued)

PROPAGATION DELAY TIME  
VS  
FREE-AIR TEMPERATURE

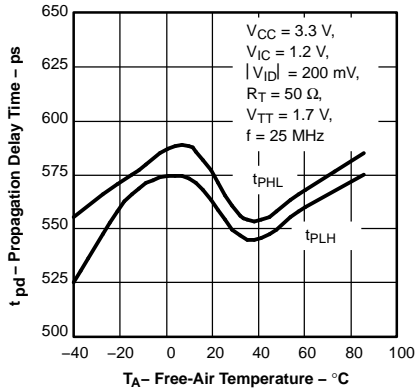


Figure 11.

PEAK-TO-PEAK JITTER  
VS  
FREQUENCY

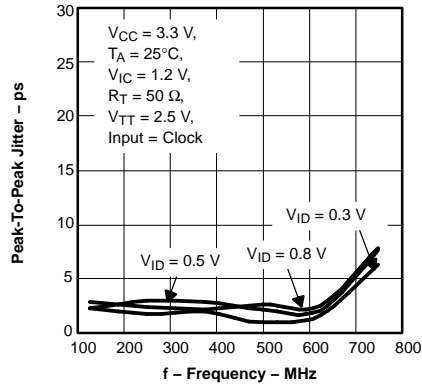


Figure 12.

PEAK-TO-PEAK JITTER  
VS  
DATA RATE

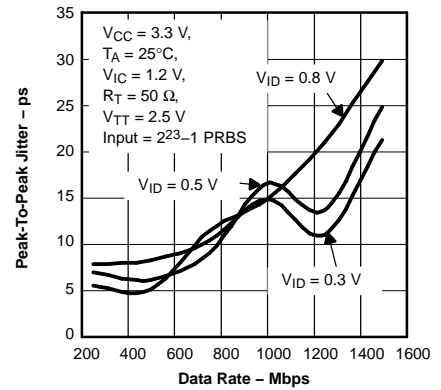


Figure 13.

PEAK-TO-PEAK JITTER  
VS  
COMMON MODE INPUT VOLTAGE

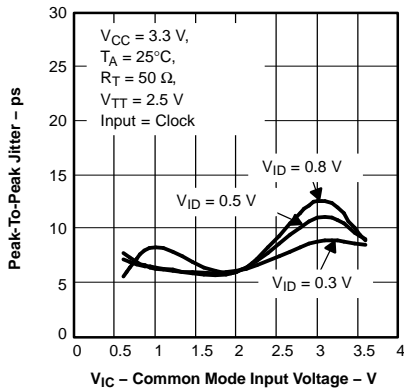


Figure 14.

PEAK-TO-PEAK JITTER  
VS  
COMMON MODE INPUT VOLTAGE

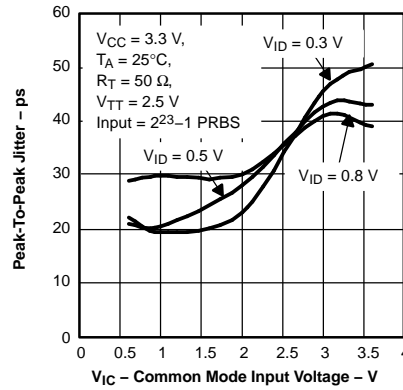


Figure 15.

PEAK-TO-PEAK JITTER  
VS  
DATA RATE

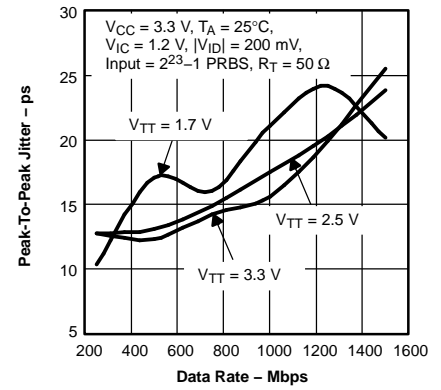


Figure 16.

PEAK-TO-PEAK JITTER  
VS  
DATA RATE

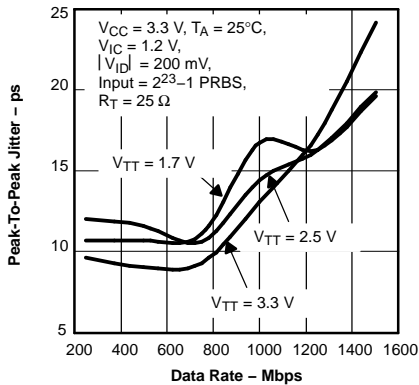
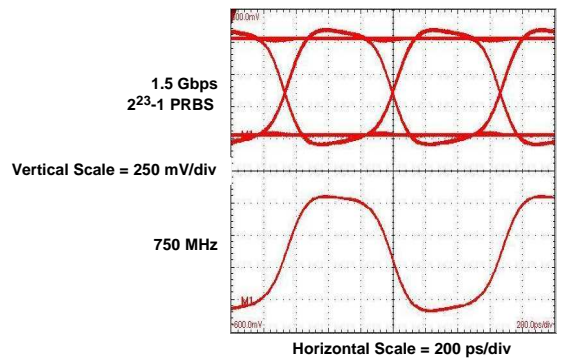


Figure 17.

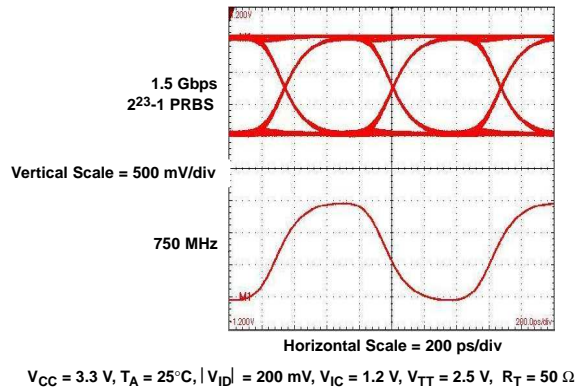


V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C, |V<sub>ID</sub>| = 200 mV, V<sub>IC</sub> = 1.2 V, V<sub>TT</sub> = 3.3 V, R<sub>T</sub> = 25 Ω

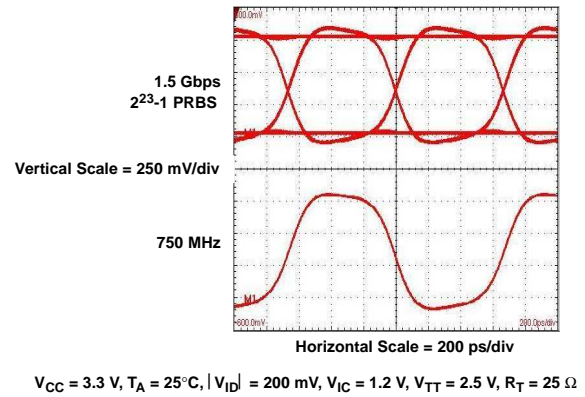
Figure 18.



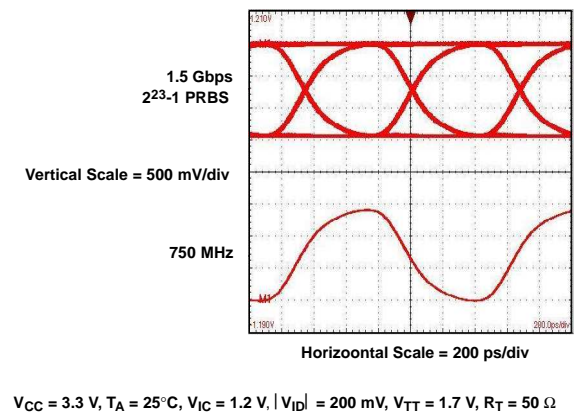
**TYPICAL CHARACTERISTICS (continued)**



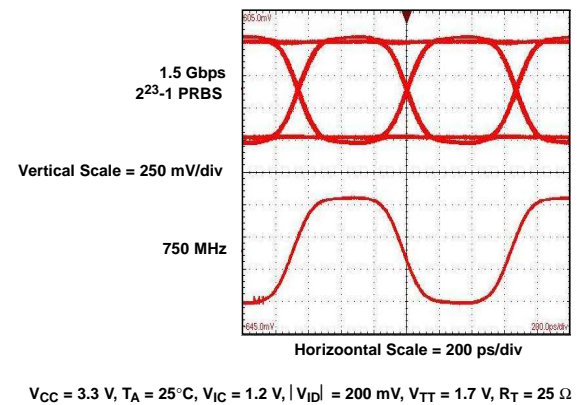
**Figure 19.**



**Figure 20.**



**Figure 21.**



**Figure 22.**

TYPICAL CHARACTERISTICS (continued)

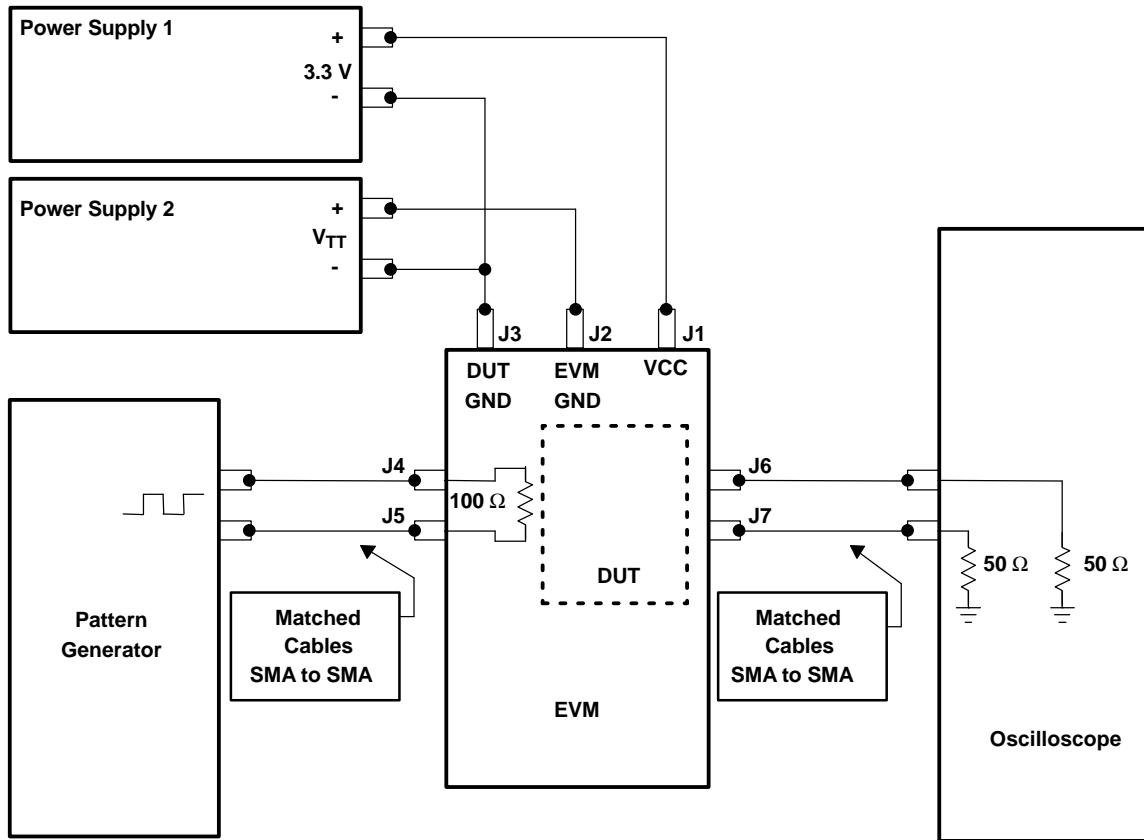


Figure 23. Jitter Setup Connections for SN65CML100

## APPLICATION INFORMATION

For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage. When  $V_{BB}$  is used, decouple  $V_{BB}$  via a 0.01- $\mu\text{F}$  capacitor and limit the current sourcing or sinking to 0.4 mA. When not used,  $V_{BB}$  should be left open.

### TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

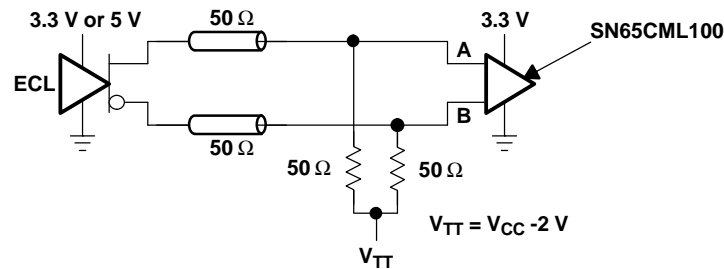


Figure 24. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

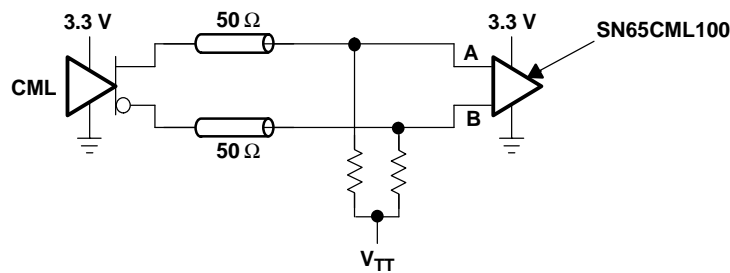


Figure 25. Current-Mode Logic (CML)

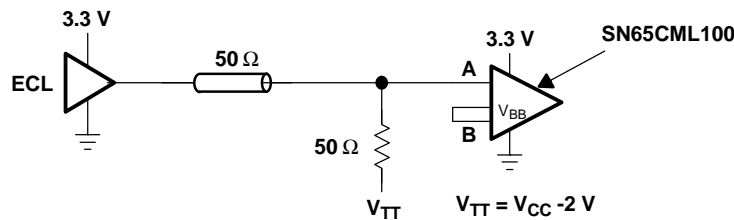


Figure 26. Single-Ended (LVPECL)

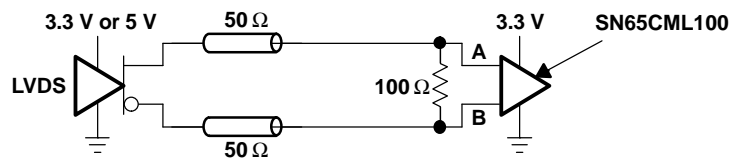


Figure 27. Low-Voltage Differential Signaling (LVDS)

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65CML100D</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100
SN65CML100D.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100
SN65CML100DG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100
SN65CML100DG4.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100
<a href="#">SN65CML100DGK</a>	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB
SN65CML100DGK.B	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB
SN65CML100DGKG4	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB
<a href="#">SN65CML100DGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB
SN65CML100DGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB
SN65CML100DGKR1G4	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB
SN65CML100DGKR1G4.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB
<a href="#">SN65CML100DR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100
SN65CML100DR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

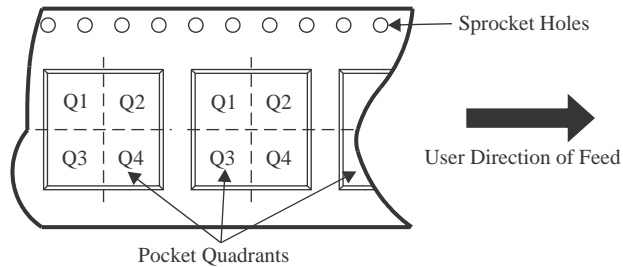
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


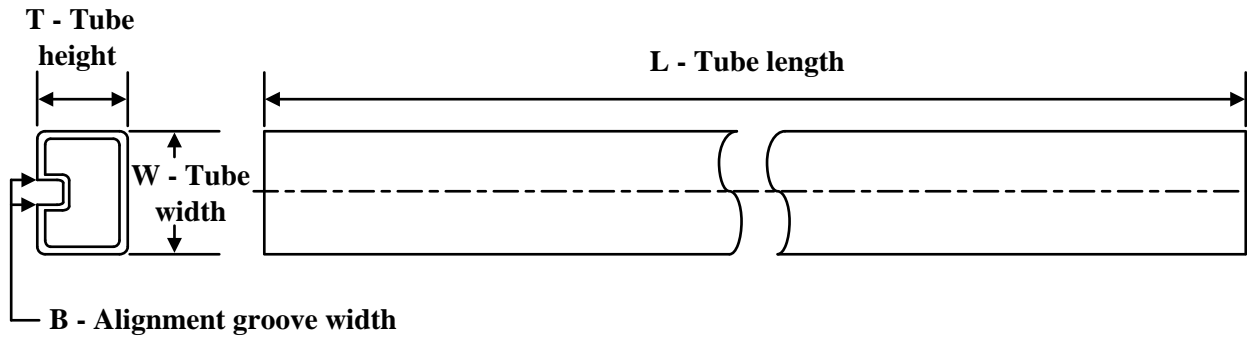
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65CML100DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65CML100DGKR1G4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65CML100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

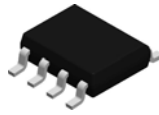
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65CML100DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65CML100DGKR1G4	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65CML100DR	SOIC	D	8	2500	340.5	336.1	25.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65CML100D	D	SOIC	8	75	505.46	6.76	3810	4
SN65CML100D	D	SOIC	8	75	507	8	3940	4.32
SN65CML100D.B	D	SOIC	8	75	507	8	3940	4.32
SN65CML100D.B	D	SOIC	8	75	505.46	6.76	3810	4
SN65CML100DG4	D	SOIC	8	75	507	8	3940	4.32
SN65CML100DG4.B	D	SOIC	8	75	507	8	3940	4.32



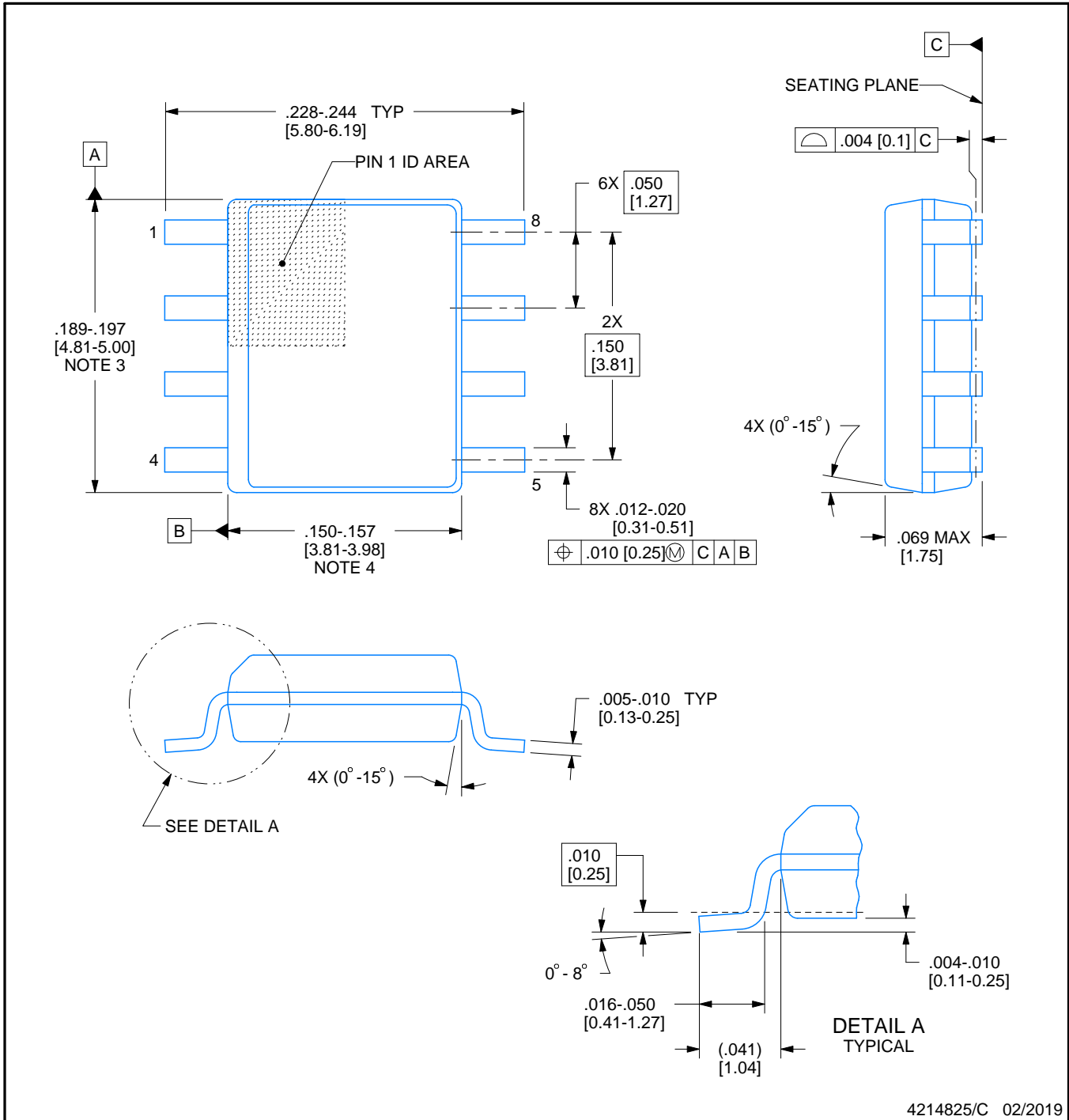


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

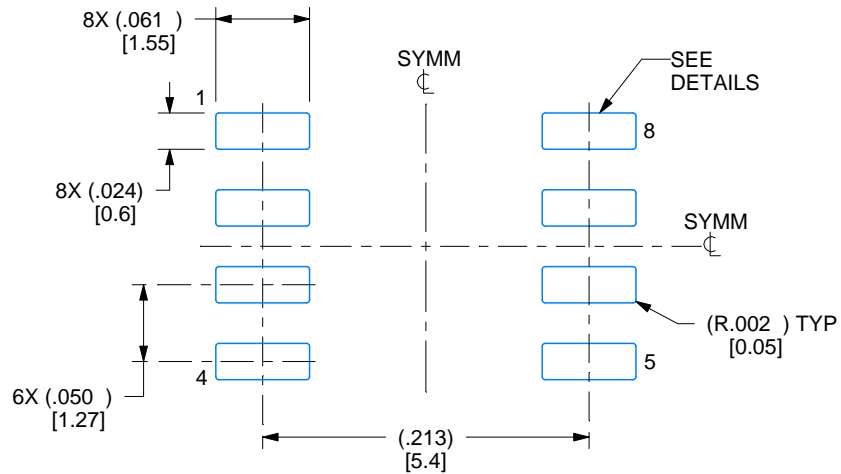
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

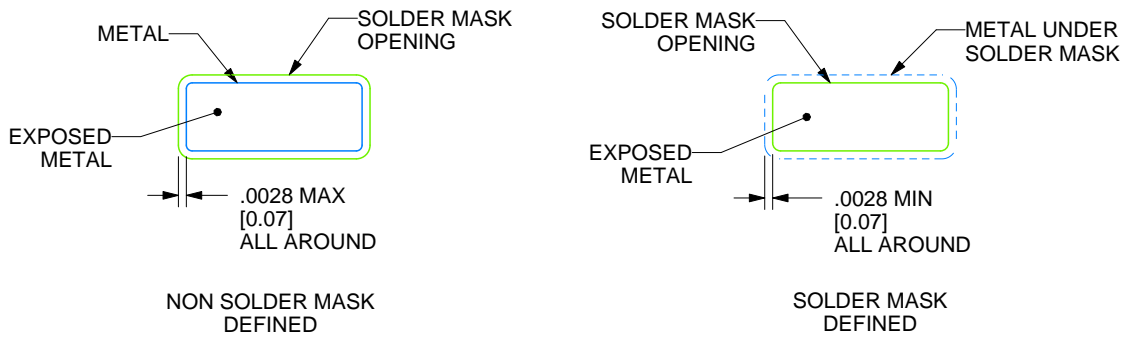
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

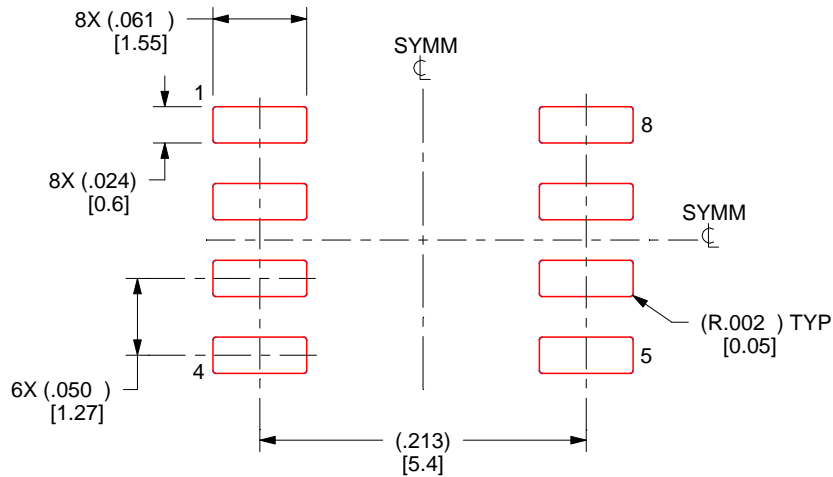
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



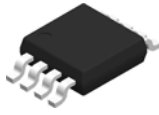
SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

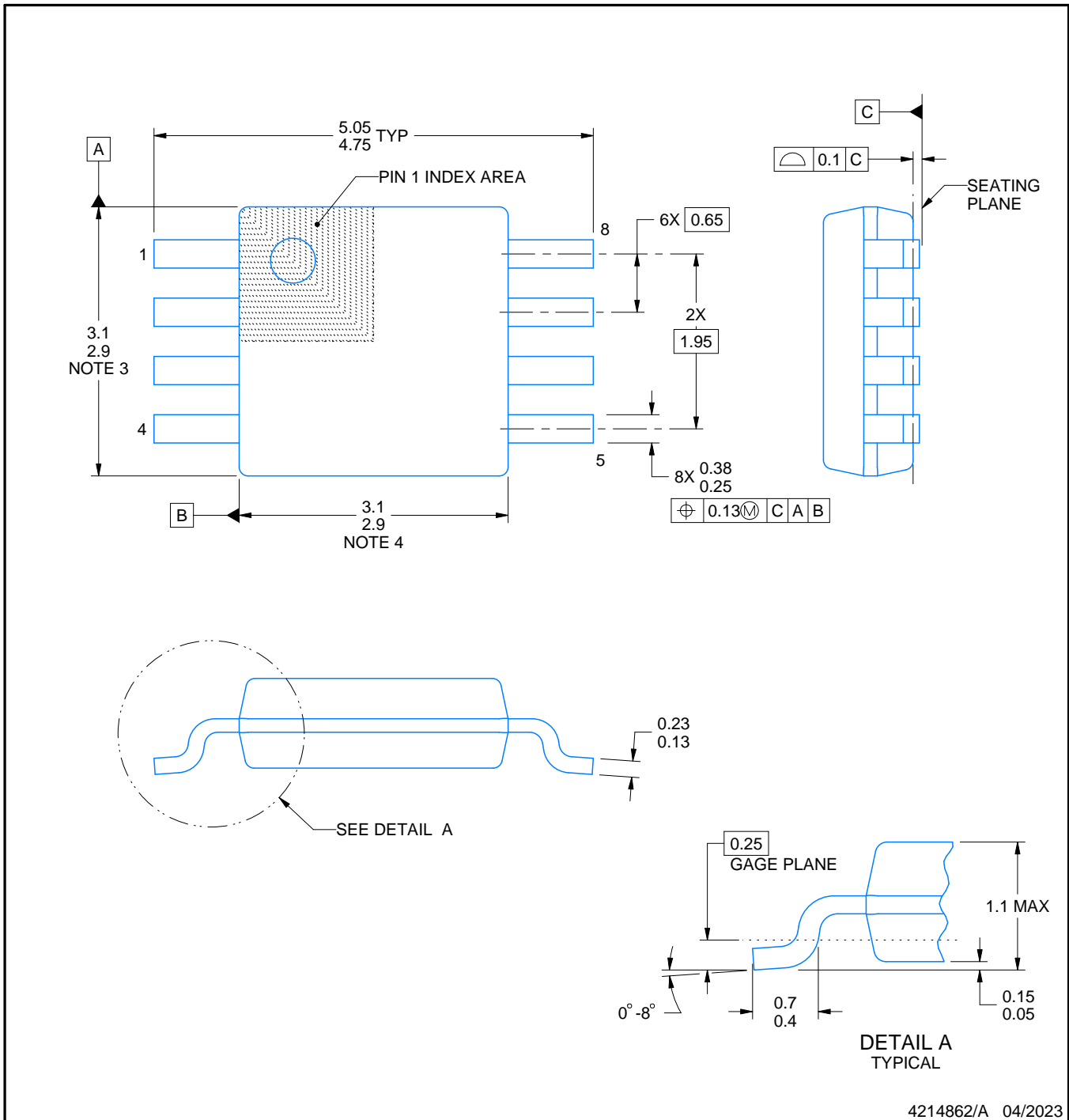
# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

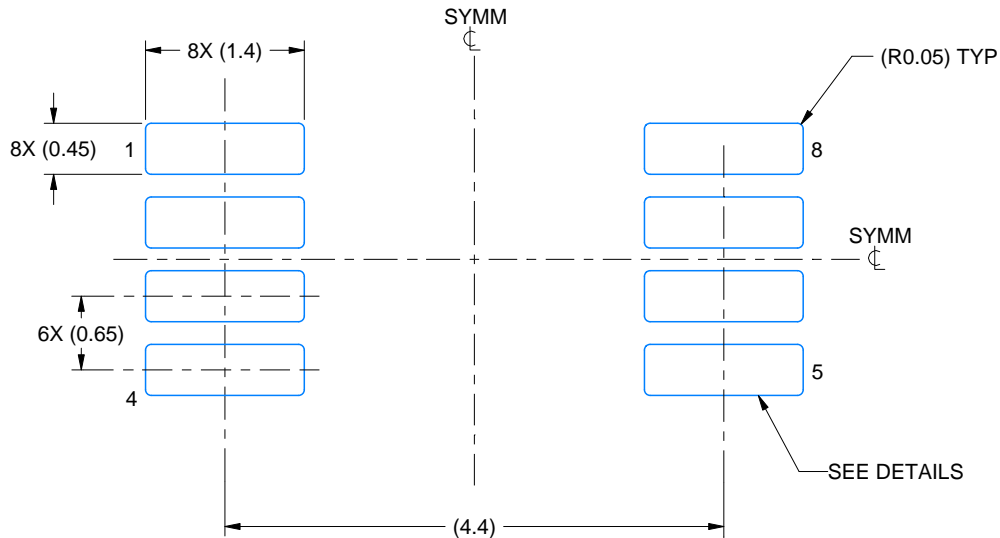
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

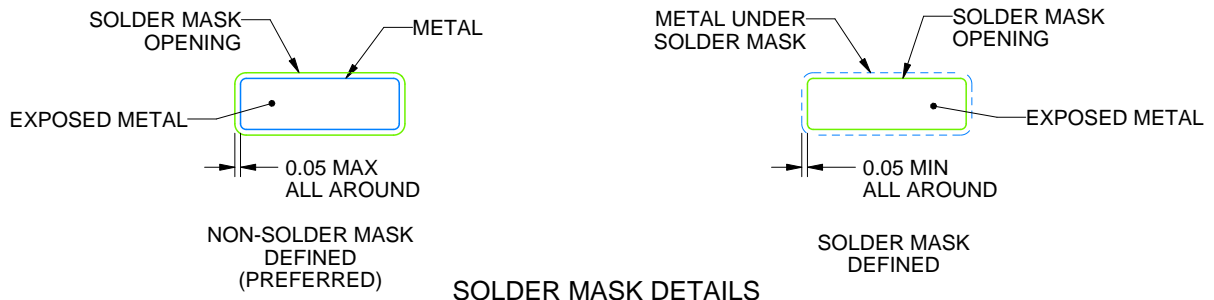
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

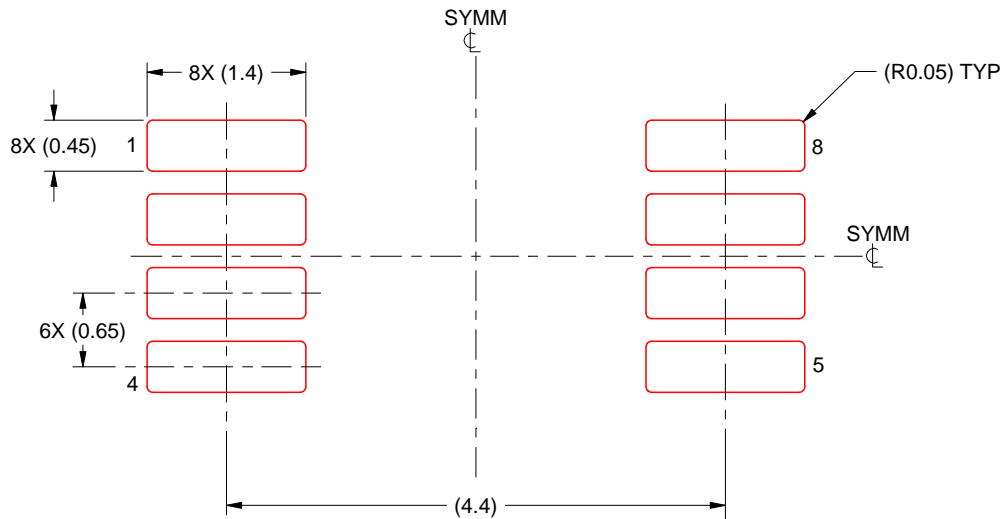
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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