

5-V TTL-to-Differential PECL Translator

Check for Samples: [SN65ELT20](#)

FEATURES

- 1.25-ns Maximum Propagation Delay
- Operating Range: $V_{CC} = 4.2\text{ V to }5.7\text{ V}$ With $GND = 0\text{ V}$
- Flow-Through Pinout Enables Easy Layout
- Built-In Temperature Compensation
- Drop-In Compatible With MC10ELT20, MC100ELT20

APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion for Clock or Data

DESCRIPTION

The SN65ELT20 is a TTL-to-differential PECL translator. It operates on a 5-V supply and ground only. The output is undetermined when the inputs are left floating. The low output skew makes the device an ideal solution for clock or data signal translation.

The SN65ELT20 is housed in an industry-standard SOIC-8 package and is also available in a TSSOP-8 package.

PINOUT ASSIGNMENT

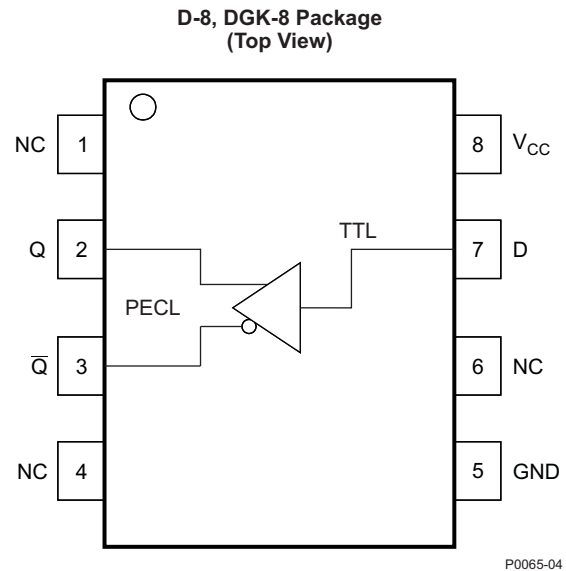


Table 1. Pin Description

PIN	FUNCTION
D	TTL input
$\overline{Q}, \overline{Q}$	PECL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT20D	SN65ELT20	SOIC	NiPdAu
SN65ELT20DGK	SN65ELT20	SOIC-TSSOP	NiPdAu

(1) Leaded device options not initially available; contact a sales representative for further details.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL-mode supply voltage	V_{CC} (GND = 0 V)	6	V
V_{IN} input voltage	GND = 0 V; $V_I \leq V_{CC}$	6	V
Output current	Continuous	50	mA
	Surge	100	mA
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT-BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT, NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
θ_{JC}	Junction-to-case thermal resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

KEY ATTRIBUTES

CHARACTERISTIC	VALUE
Moisture sensitivity level	SO-8: Level 1
	TSSOP-8: Level 3
Flammability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD—human body model	>4 kV
ESD—machine model	200 V
ESD—charged-device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

PECL DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 5\text{ V}$; $GND = 0\text{ V}$)⁽²⁾

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power-supply current		9.6	16		10.1	16		10.7	16	mA
V_{OH}	Output HIGH voltage ⁽³⁾	3915	3958	4120	3915	3963	4120	3915	3967	4120	mV
V_{OL}	Output LOW voltage ⁽³⁾	3170	3247	3380	3170	3244	3380	3170	3244	3380	mV

- (1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and are not valid simultaneously.
- (2) Output parameters vary 1:1 with V_{CC} .
- (3) Outputs are terminated through a 50- Ω resistor to $V_{CC} - 2\text{ V}$.

TTL INPUT DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 4.2\text{ V}$ to 5.7 V ; $T_A = -40^\circ\text{C}$ to 85°C)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IH}	Input HIGH current	$V_{IN} = 2.7\text{ V}$				20	μA
I_{IH}		$V_{IN} = V_{CC}$				20	
I_{IL}	Input LOW current	$V_{IN} = 0.5\text{ V}$				–0.6	mA
V_{IK}	Input clamp diode voltage	$I_{IN} = -18\text{ mA}$				–1.2	V
V_{IH}	Input HIGH voltage			2			V
V_{IL}	Input LOW voltage					0.8	V

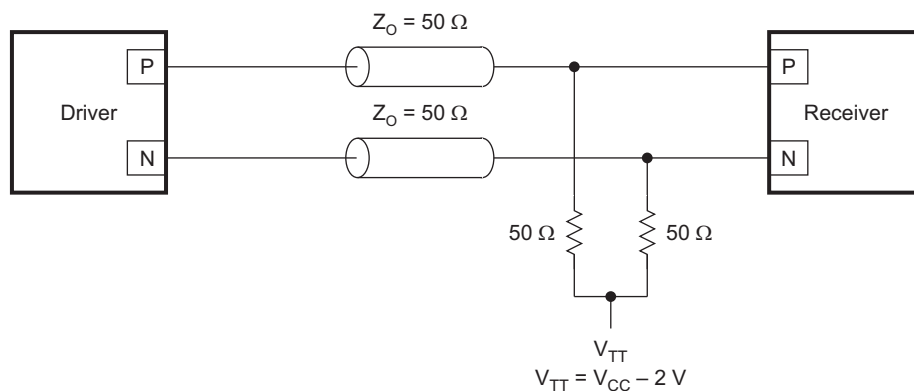
- (1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and are not valid simultaneously.

AC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 4.2\text{ V}$ to 5.7 V ; $GND = 0\text{ V}$)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum switching frequency ⁽²⁾ (See Figure 4.)		400			430			430		MHz
t_{PLH}	Propagation delay, 1.5 V to 50% (see Figure 2)	0.9		1.25	0.9		1.25	0.9		1.25	ns
t_{PHL}	Propagation delay, 1.5 V to 50% (see Figure 2)	0.7		1.2	0.7		1.2	0.7		1.2	ns
t_{JITTER}	Random clock jitter (RMS)		0.5			0.5			0.5		ps
t_r/t_f	Q-output rise/fall times (20%–80%) (see Figure 3)	1		1.5	1		1.5	1		1.5	ns

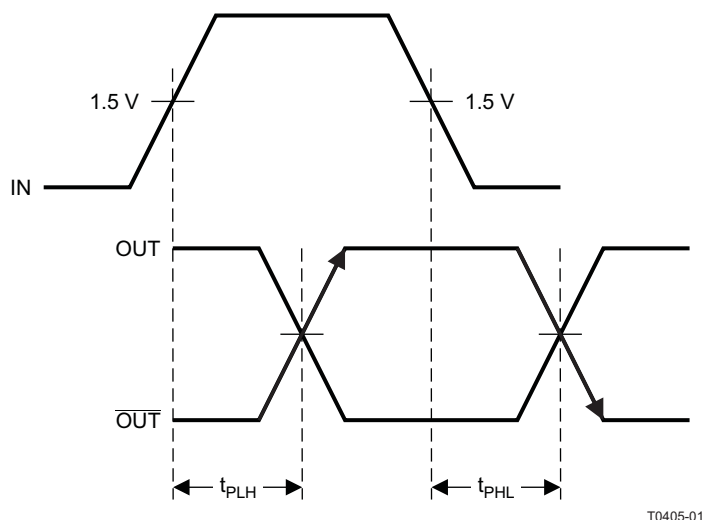
- (1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and are not valid simultaneously.
- (2) Maximum switching frequency is measured at an output amplitude of 300 mV_{PP}.

Typical Termination for Output Driver



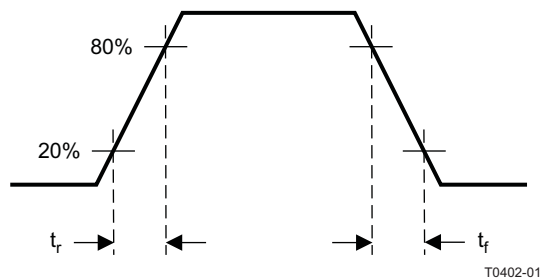
S0078-02

Figure 1. Typical Termination for Output Driver



T0405-01

Figure 2. Output Propagation Delay



T0402-01

Figure 3. Output Rise and Fall Times

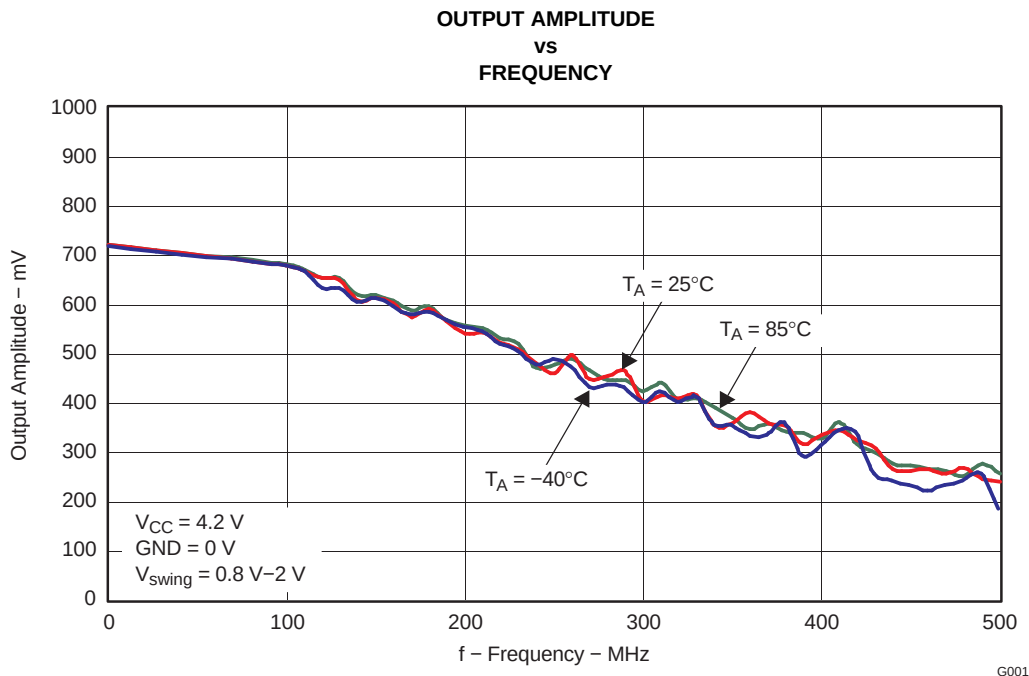


Figure 4.

REVISION HISTORY

Changes from Original (December 2008) to Revision A

Page

- Changed the ORDERING INFORMATION Table Part Number From: SN65ELT206D To: SN65ELT20D [1](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65ELT20D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT20
SN65ELT20D.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT20
SN65ELT20DGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SISI
SN65ELT20DGK.B	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SISI
SN65ELT20DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT20
SN65ELT20DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT20

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

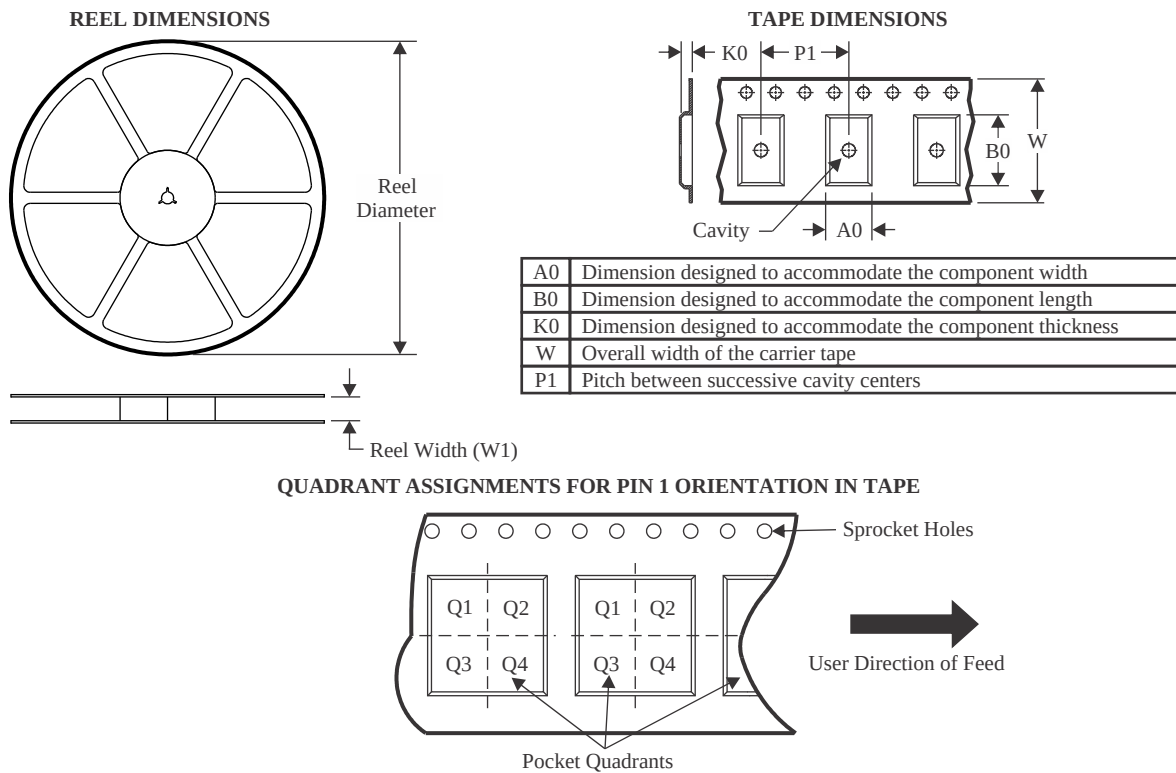
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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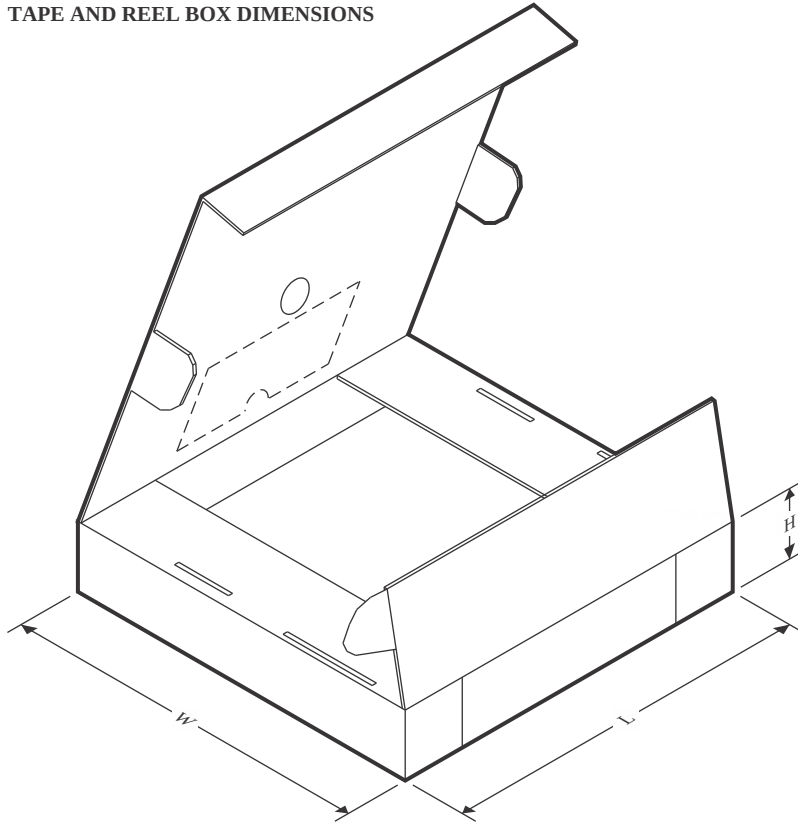
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT20DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

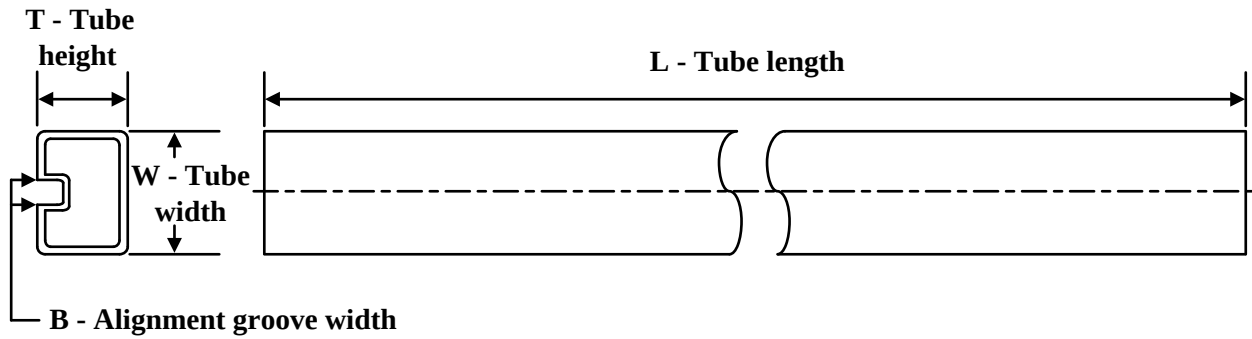
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

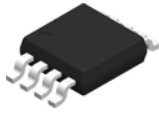
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT20DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE

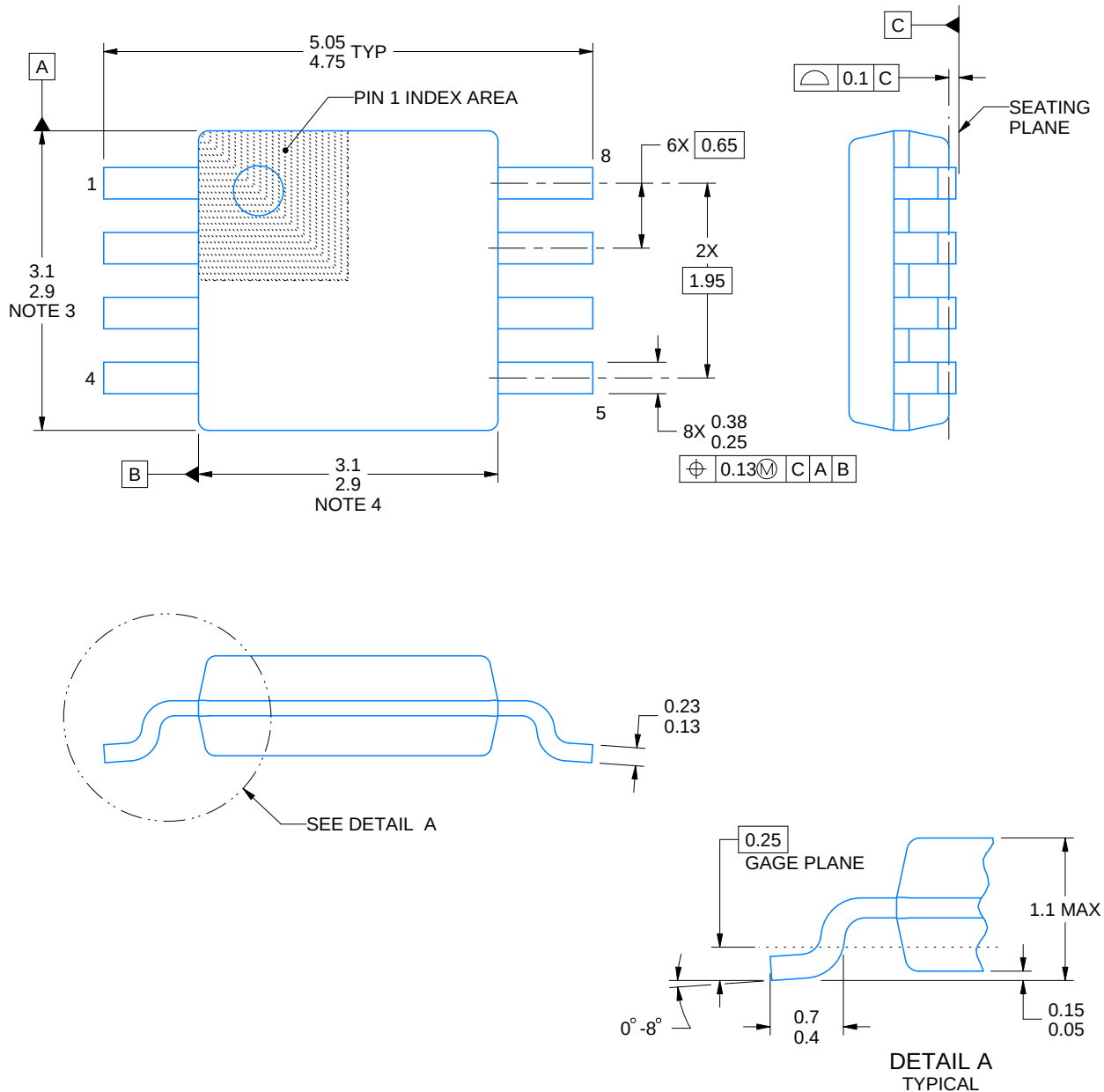


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65ELT20D	D	SOIC	8	75	506.6	8	3940	4.32
SN65ELT20D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65ELT20DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65ELT20DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

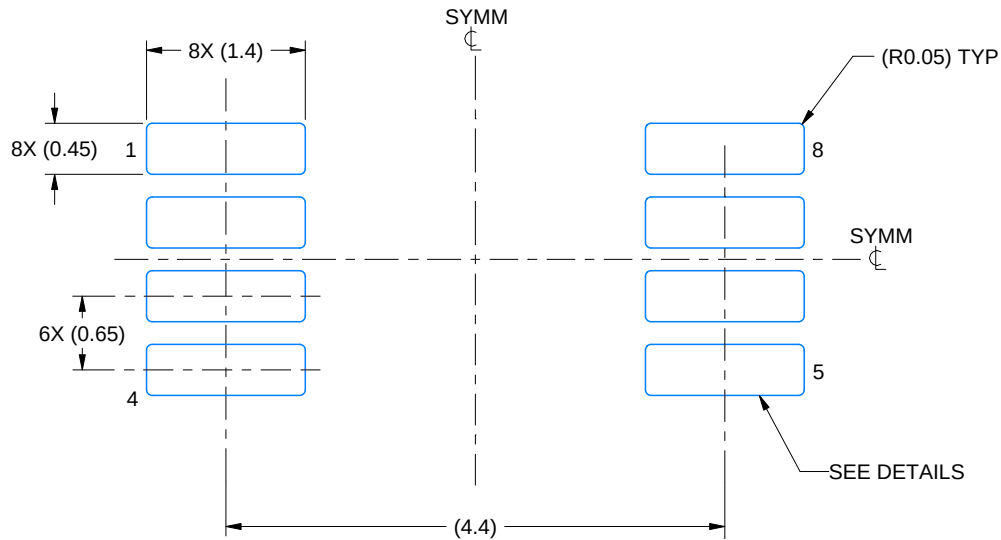
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

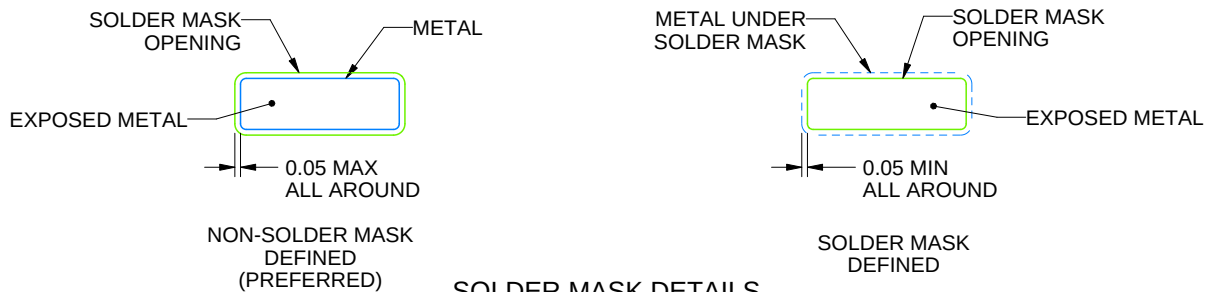
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

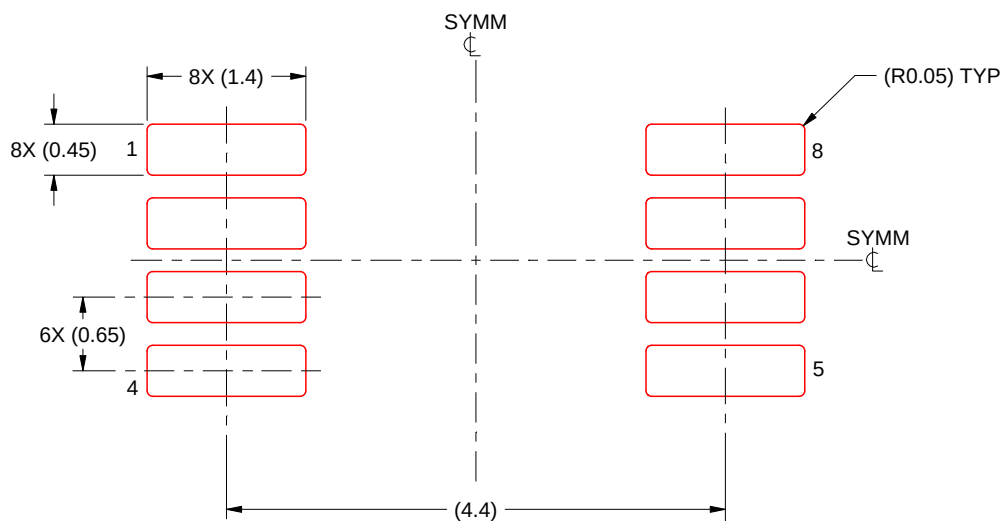
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

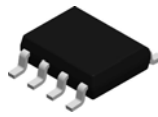


SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

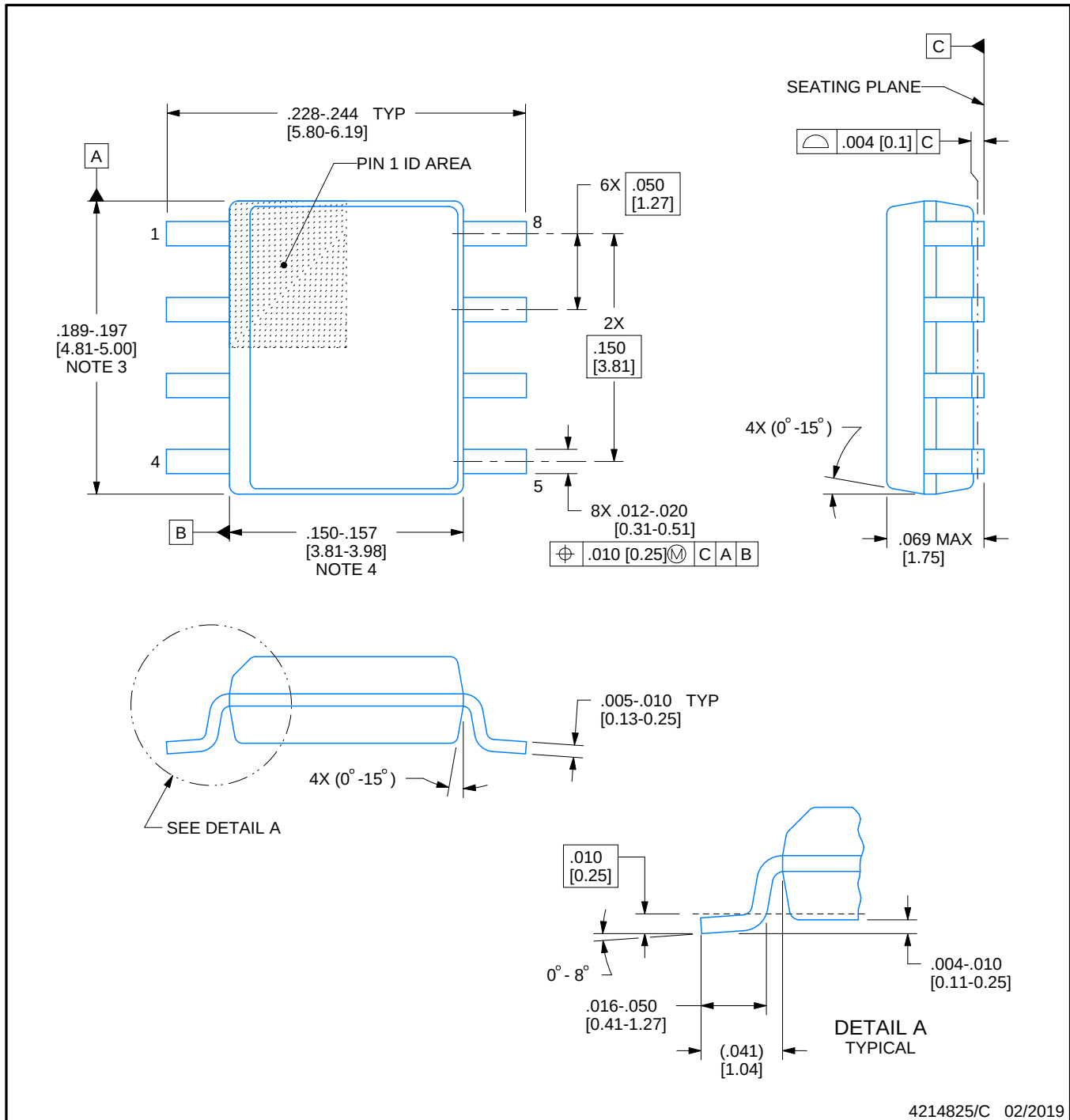


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

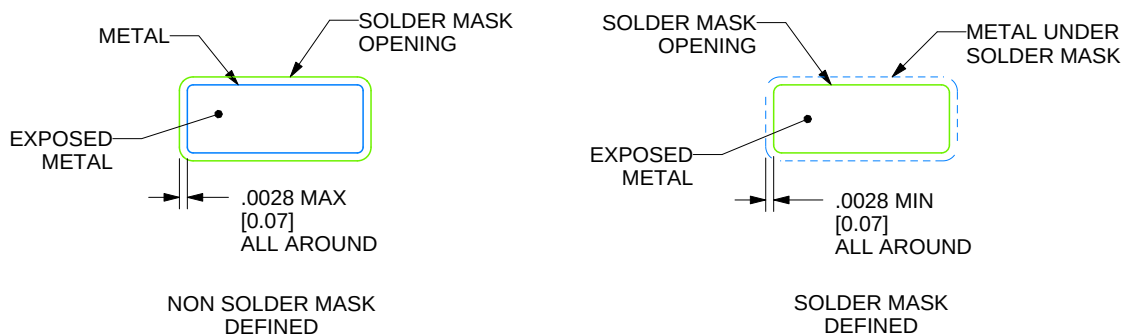
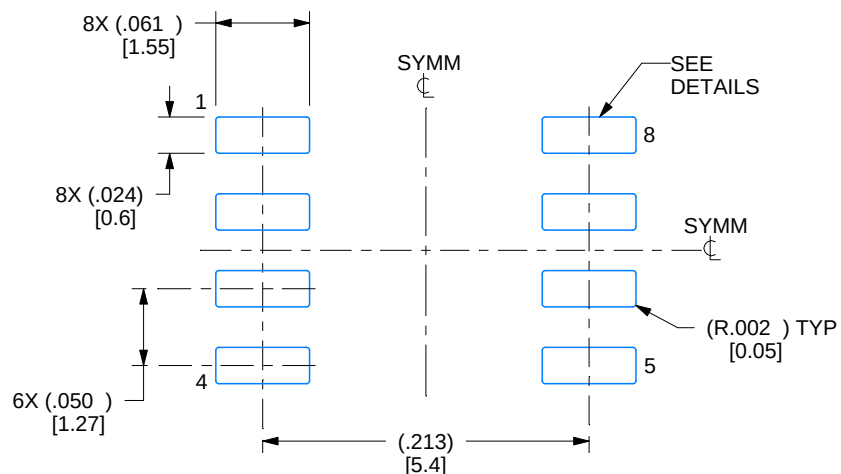
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

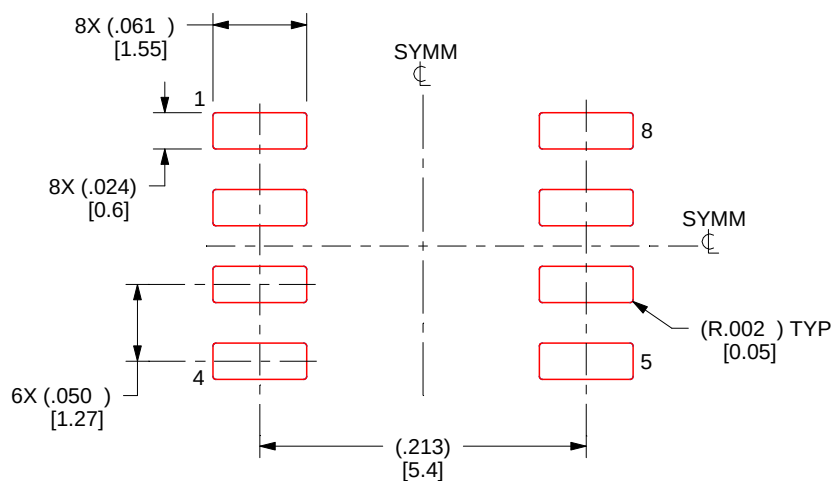
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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