SN65HVDA1040B-Q1 EMC 优化型高速 CAN 总线收发器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 0：–40°C 至 +125°C，T_A
  - HBM ESD 分类等级：
    - 除了引脚 5、引脚 6 和引脚 7 之外，所有引脚均为 3A 级
    - 引脚 5、引脚 6 和引脚 7 为 3B 级
  - CDM ESD 分类等级 C6
- 符合或超过 ISO 11898-2 和 ISO 11898-5 的要求
- 符合 GIFT/ICT 标准
- 具有总线唤醒功能的低电流待机模式，电流最大值小于 12µA
- 高电磁兼容性 (EMC)
- 适用于通过分离终端实现总线共模稳定的 SPLIT 电压源
- 数字输入与 3.3V 和 5V 微处理器兼容
- 封装选项：SOIC
- 保护 功能
  - –27V 至 40V 的总线故障保护
  - TXD 显性超时
  - 热关断保护
  - 上电和断电无干扰总线输入和输出
  - 具有低 V_{CC} 的高总线输入阻抗（未供电时总线上具有理想无源行为）

2 应用

- GMW3122 双线制 CAN 物理层
- SAE J2284 高速 CAN，适用于汽车 应用
- SAE J1939 标准数据总线接口
- ISO 11783 标准数据总线接口
- NMEA 2000 标准数据总线接口

3 说明

SN65HVDA1040B-Q1 器件符合或超过 ISO 11898 标准的要求，可用于使用控制器局域网 (CAN) 的 应用 。作为 CAN 收发器，此器件可为总线提供差分传输能力并为 CAN 控制器提供差分接收能力，其信号传输速率高达每秒 1 兆位 (Mbps)。线路的信号传输速率是每秒进行电压转换的次数，以单位 bps（每秒位数）来表示。

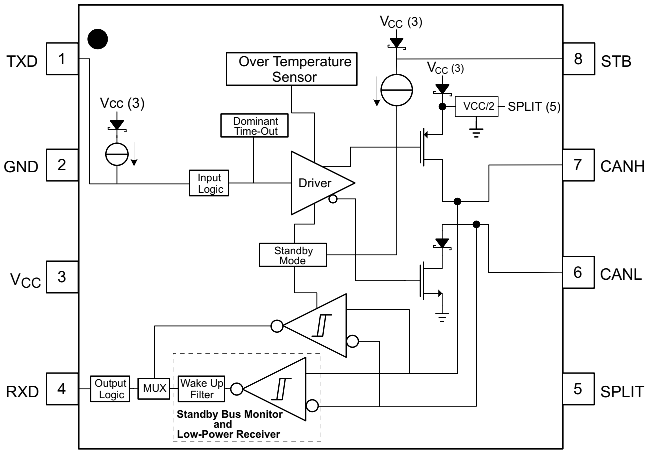
该器件设计用于在特别恶劣的环境下工作，并且具有众多器件保护 功能 ，如欠压锁定 (UVLO)、过热热关断、宽共模范围和接地失效保护。根据 ISO 7637，总线引脚还受到保护，可免受外部交叉线、–27V 至 40V 短路和电压瞬态的破坏。该器件符合汽车 应用标准。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
SN65HVDA1040B-Q1	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

方框图



English Data Sheet: SLLSFE2

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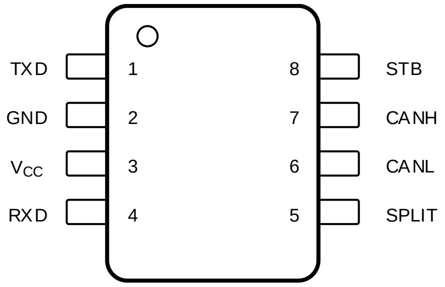
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 6 月	*	初始发行版。

5 Pin Configuration and Functions

**D Package
8-Pin SOIC
Top View**



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	SOIC		
TXD	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
GND	2	GND	Ground connection
V_{CC}	3	Supply	Transceiver 5-V supply voltage input
RXD	4	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
SPLIT	5	O	Common-mode stabilization output
CANL	6	I/O	Low-level CAN bus line
CANH	7	I/O	High-level CAN bus line
STB	8	I	Standby mode select pin (active high)
NC	—	NC	No connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
	Voltage range at bus terminals (CANH, CANL, SPLIT)	–27	40	V
I_O	Receiver output current		20	mA
V_I	Voltage input, ISO 7637 transient pulse (2) (CANH, CANL)	–150	100	V
V_I	Voltage input (TXD, STB)	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = –100 V, Pulse 2 = 100 V, Pulse 3a = –150 V, Pulse 3b = 100 V). If DC may be coupled with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with dc bus shorts to 40 V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to DC, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	Pins 7 and 6 (2)	±12000	V
			Pin 5 (3)	±10000	
			All pins	±4000	
		Charged-device model (CDM), per AEC Q100-011		±1500	
		IEC 61000-4-2 according to IBEE CAN EMC test specification	Pins 7 and 6 connected to pin 2	±7000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

(2) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.

(3) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, SPLIT pin stressed with respect to GND.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, STB	2	5.25	V
V_{IL}	Low-level input voltage	TXD, STB	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver (RXD)	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver (RXD)		2	
T_A	Operating free-air temperature range	See *Thermal Information*	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)			SN65HVDA1040B-Q1	UNIT
			D (SOIC)	
			8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance(2)	140	°C/W
		High-K thermal resistance(3)	112	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50	°C/W
ψ_{JT}	Junction-to-top characterization parameter		13	°C/W
ψ_{JB}	Junction-to-board characterization parameter		55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, Low-K board, as specified in JESD51-3, in an environment described in JESD51-2a.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

6.5 Electrical Characteristics

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
SUPPLY							
I_{CC}	5-V supply current	Standby mode	STB at V_{CC}, $V_I = V_{CC}$		6	12	µA
		Dominant	V_I = 0 V, 60-Ω load, STB at 0 V		50	70	mA
		Recessive	$V_I = V_{CC}$, No load, STB at 0 V		6	10	
UV_{VCC}	Undervoltage reset threshold			2.8		4	V
DRIVER							
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 16	2.9	3.4	4.5	V
		CANL		0.8		1.75	
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 16	2	2.5	3	V
V_O	Bus output voltage (standby mode)		STB at Vcc, R_L = 60 Ω, See Figure 3 and Figure 16	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 3, Figure 16, and Figure 4	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 3, Figure 16, and Figure 4	1.4		3	
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 16	–0.012		0.012	V
			V_I = 3 V, STB at 0 V, No load	–0.5		0.05	
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)} + V_{O(CANL)}$)		STB at 0 V, R_L = 60 Ω, See Figure 14	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
$V_{OC(ss)}$	Steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 9	2	2.5	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 9		30		mV
V_{IH}	High-level input voltage, TXD input			2			V
V_{IL}	Low-level input voltage, TXD input					0.8	V
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	µA
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	µA

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(1) All typical values are at 25°C with a 5-V supply.

Electrical Characteristics (continued)

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{OS(ss)}$	Short-circuit steady-state output current, Dominant	V_{CANH} = –12 V, CANL open, TXD = low, See Figure 12	–120	–85		mA
		V_{CANH} = 12 V, CANL open, TXD = low, See Figure 12		0.4	1	
		V_{CANL} = –12 V, CANH open, TXD = low, See Figure 12	–1	–0.6		
		V_{CANL} = 12 V, CANH open, TXD = low, See Figure 12		75	120	
		V_{CANH} = 0 V, CANL open, TXD = low, See Figure 12	–100	–75		
		V_{CANL} = 32 V, CANH open, , TXD = low, See Figure 12		75	125	
$I_{OS(ss)}$	Short-circuit steady-state output current, Recessive	–20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 12	–10		10	mA
		–20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 12	–10		10	
C_O	Output capacitance	See receiver input capacitance				
RECEIVER						
V_{IT+}	Positive-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1		800	900	mV
V_{IT-}	Negative-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		100	125		mV
V_{IT}	Input threshold voltage, standby mode	STB at V_{CC}	500		1150	mV
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 7	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 7		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current (unpowered bus leakage current)	CANH = CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			3	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		6		pF
R_{ID}	Differential input resistance	TXD at 3 V, STB at 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, STB at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] × 100%	$V_{(CANH)} = V_{(CANL)}$	–3%	0%	3%	
STB PIN						
V_{IH}	High-level input voltage, STB input		2			V
V_{IL}	Low-level input voltage, STB input				0.8	V
I_{IH}	High-level input current	STB at 2 V	–10		0	µA
I_{IL}	Low-level input current	STB at 0.8 V	–10		0	µA
SPLIT PIN						
V_O	Output voltage	–250 µA < I_O < 250 µA	0.3 V_{CC}	0.5 V_{CC}	0.7 V_{CC}	V
$I_{O(stb)}$	Leakage current, standby mode	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	µA

6.6 Power Dissipation Characteristics

over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		112		mW
		V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			170	
	Thermal shutdown temperature			185		°C

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	STB at 0 V, See Figure 10	90		230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	STB at 0 V, See Figure 10	90		230	ns
DRIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, See Figure 5	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low level output	STB at 0 V, See Figure 5	25	45	120	ns
t_r	Differential output signal rise time	STB at 0 V, See Figure 5		25		ns
t_f	Differential output signal fall time	STB at 0 V, See Figure 5		45		ns
t_{en}	Enable time from standby mode to normal mode and transmission of dominant	See Figure 8			10	µs
$t_{(dom)}$	Dominant time-out(1)	↓V_I, See Figure 11	300	450	700	µs
RECEIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V , See Figure 7	60	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output	STB at 0 V , See Figure 7	45	70	130	ns
t_r	Output signal rise time	STB at 0 V , See Figure 7		8		ns
t_f	Output signal fall time	STB at 0 V , See Figure 7		8		ns
t_{BUS}	Dominant time required on bus for wakeup from standby	STB at V_{CC}, See Figure 13	1		5	µs

(1) The TXD dominant time-out ($t_{(dom)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(dom)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where 5 successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:
Minimum Bit Rate = 11/ $t_{(dom)}$ = 11 bits / 300 µs = 37 kbps

6.8 Typical Characteristics

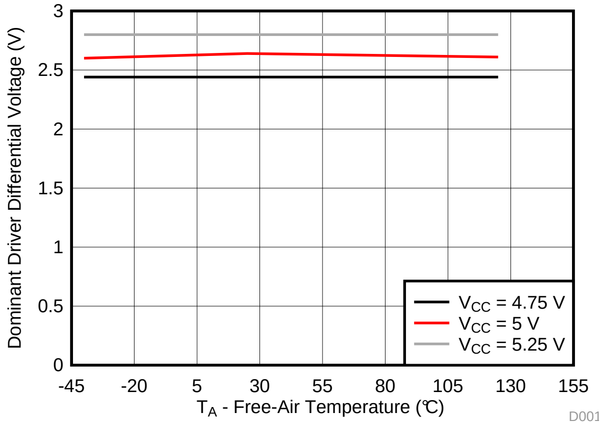


Figure 1. Dominant Driver Differential Voltage vs Free-Air Temperature

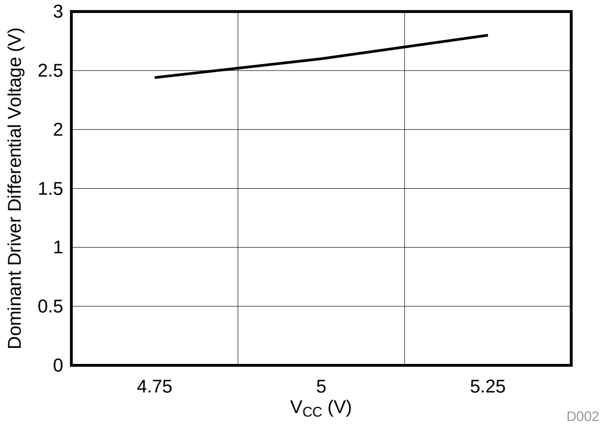


Figure 2. Driver Differential Voltage vs. Supply Voltage

7 Parameter Measurement Information

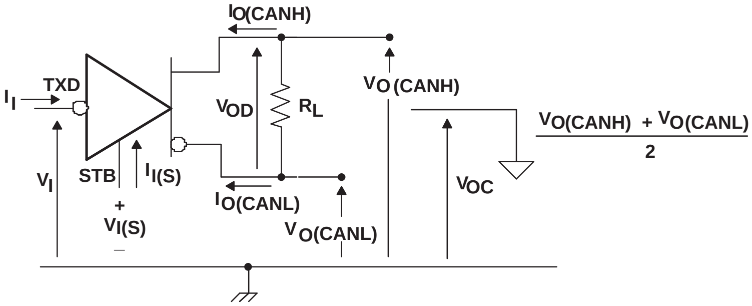


Figure 3. Driver Voltage, Current, and Test Definition

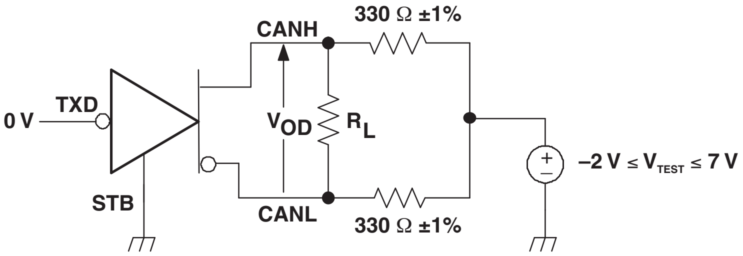


Figure 4. Driver V_{OD} Test Circuit

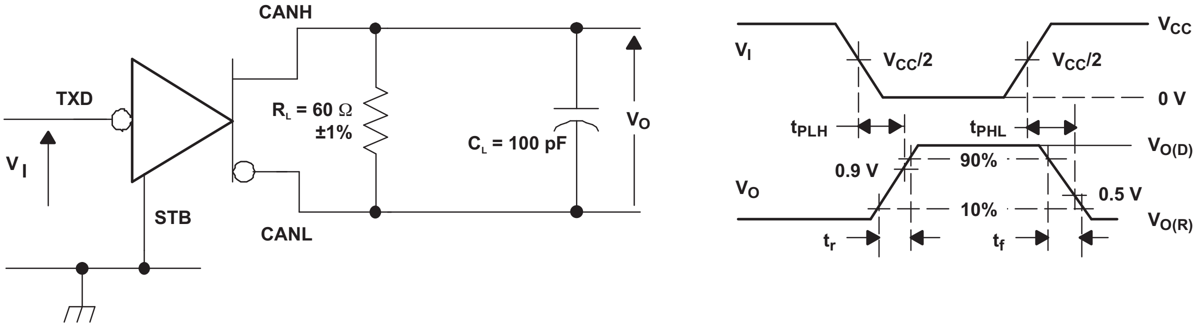


Figure 5. Driver Test Circuit and Voltage Waveforms

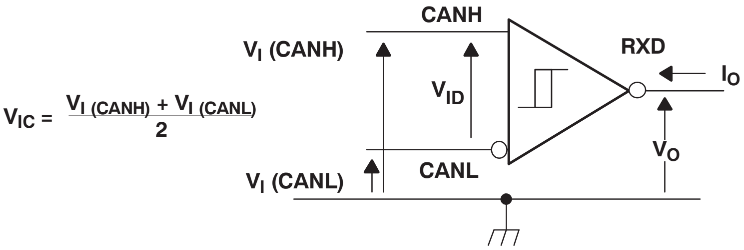
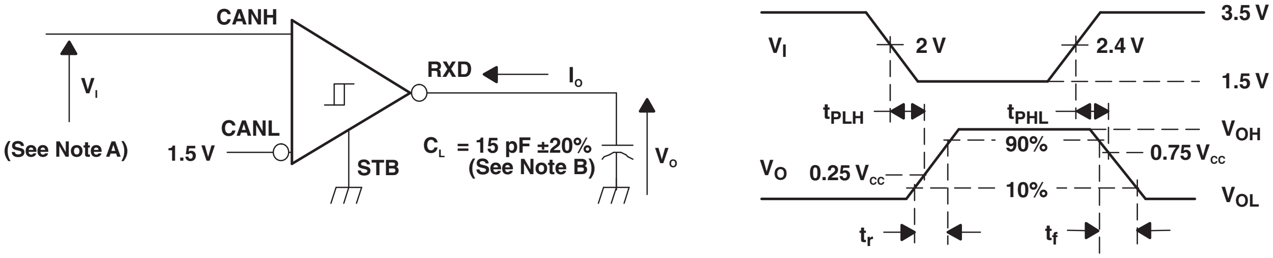


Figure 6. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)



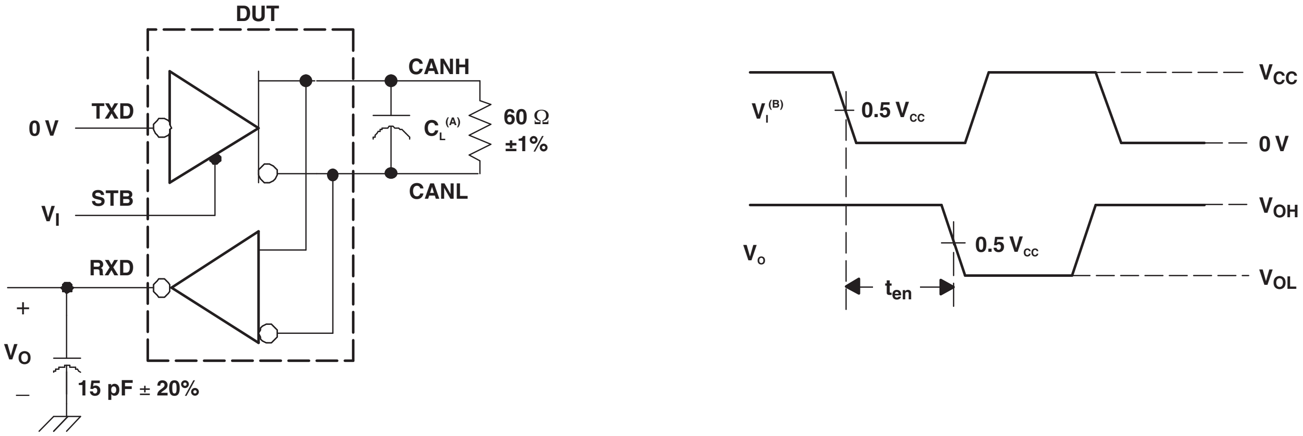
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

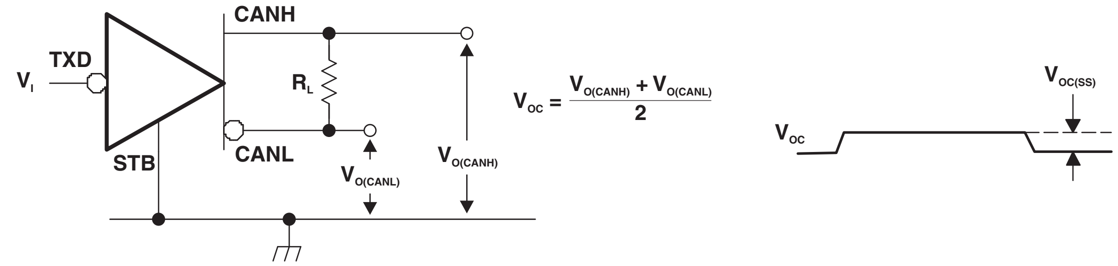
INPUT			OUTPUT R	
V_{CANH}	V_{CANL}	$\lvert V_{ID} \rvert$		
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

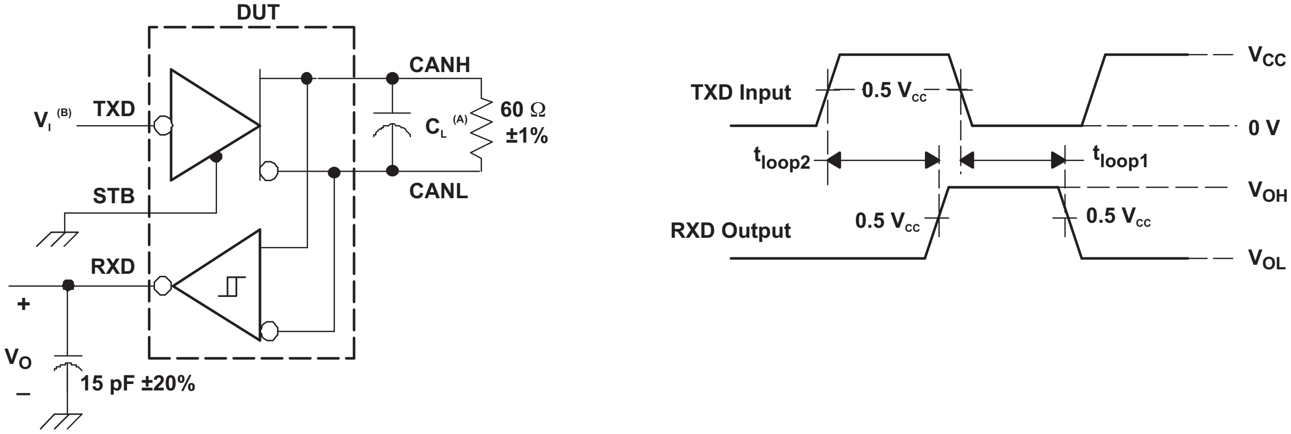
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

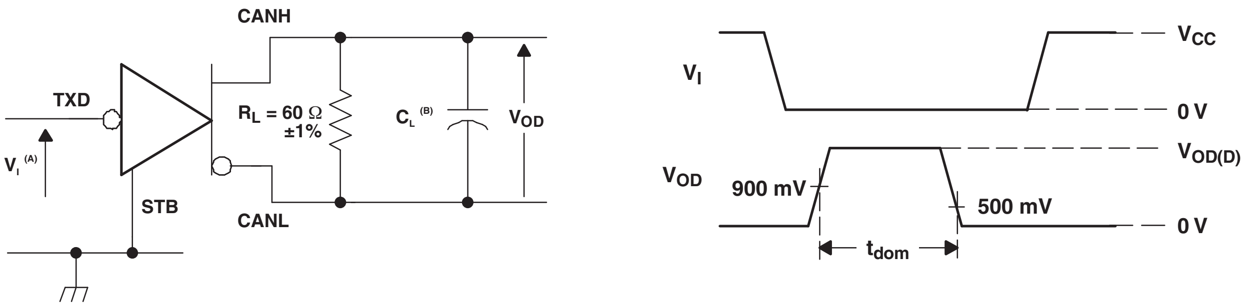
Figure 9. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 11. Dominant Time-Out Test Circuit and Waveforms

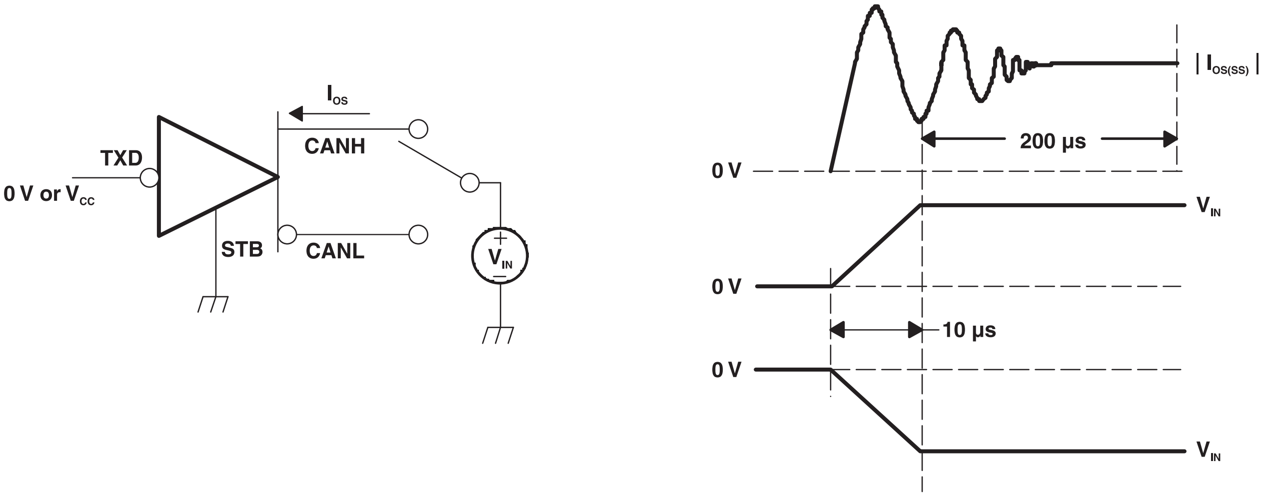
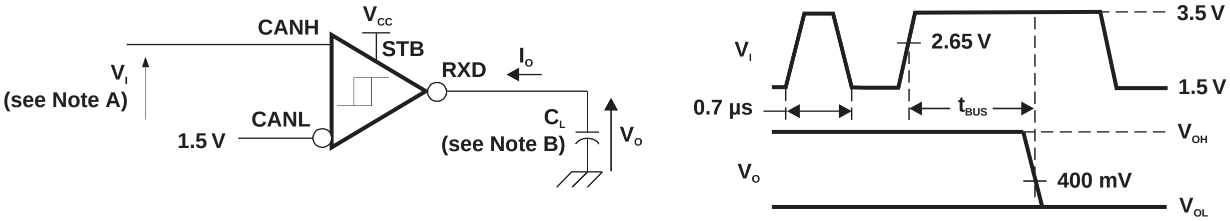


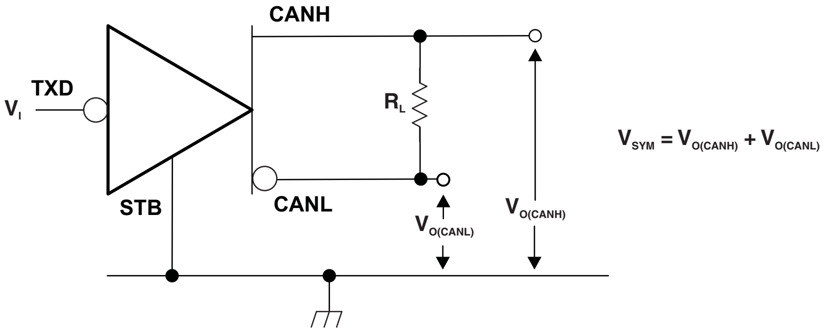
Figure 12. Driver Short-Circuit Current Test and Waveforms



A. For V_I bit width ≤ 0.7 µs, $V_O = V_{OH}$. For V_I bit width ≥ 5 µs, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics: $t_r/t_f < 6$ ns.

B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. t_{BUS} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: $t_r/t_f \le 6$ ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

Figure 14. Driver Output Symmetry Test Circuit

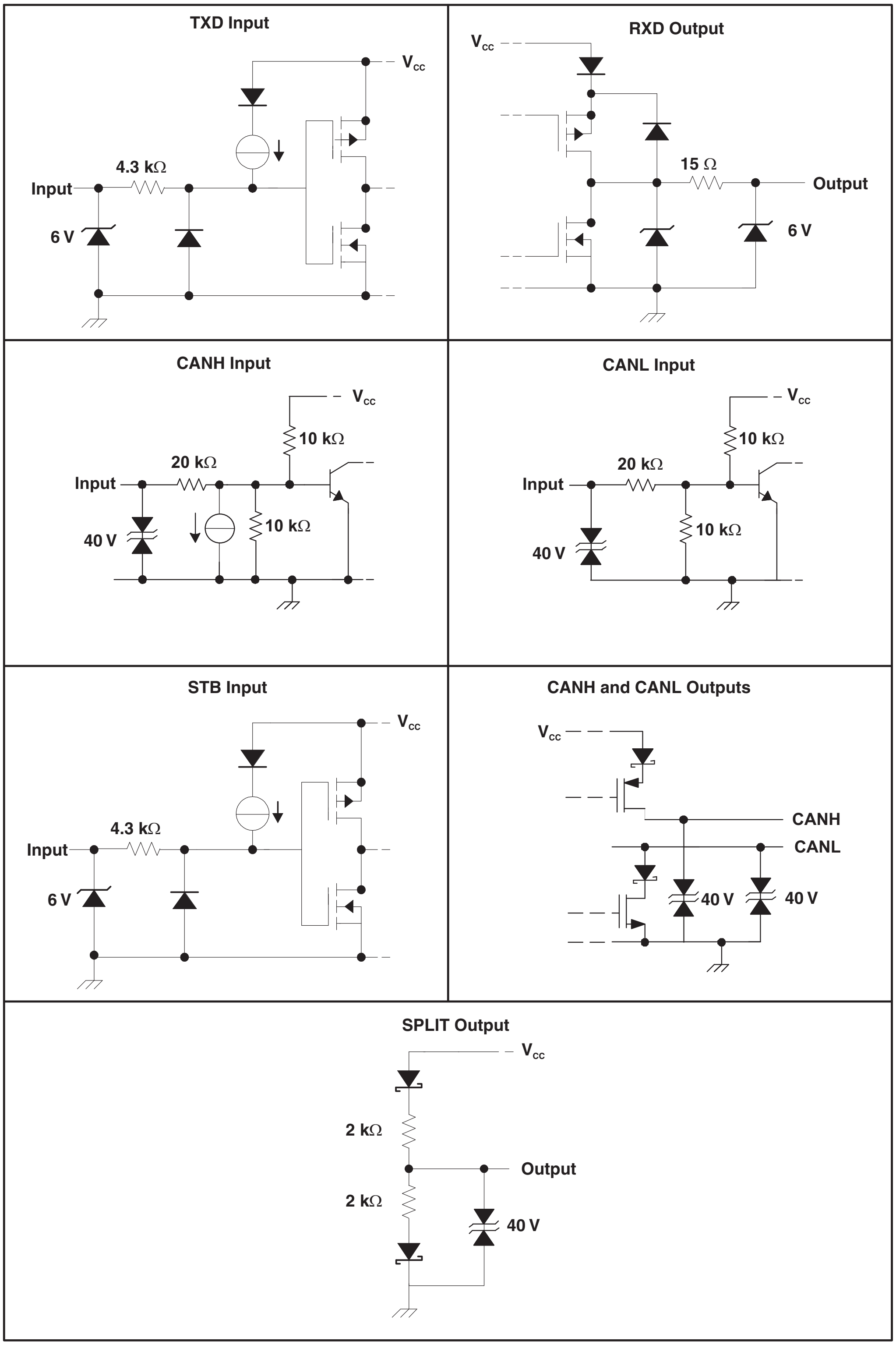


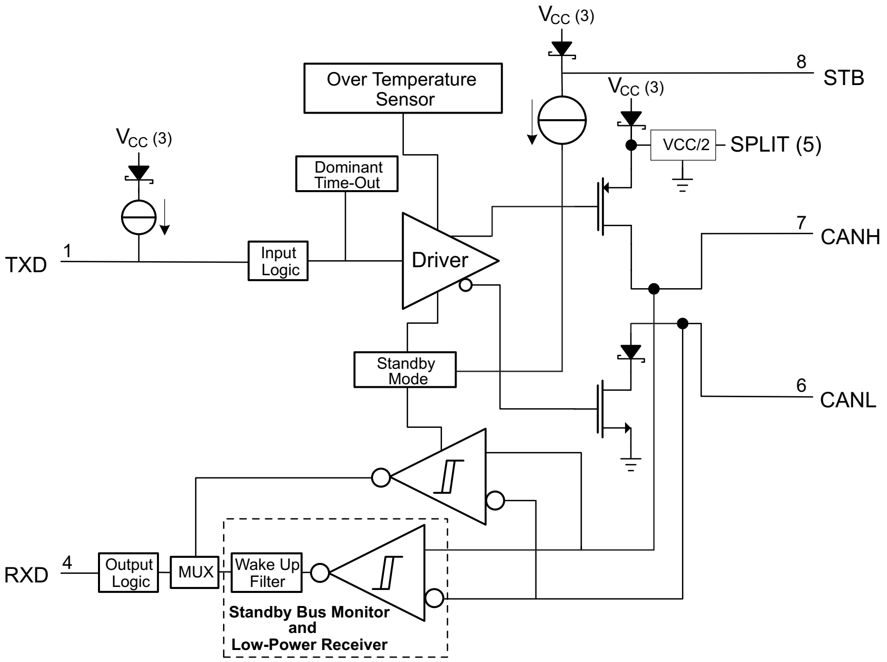
Figure 15. Equivalent Input and Output Schematic Diagrams

8 Detailed Description

8.1 Overview

The SN65HVDA1040B-Q1 CAN tranceiver is compatible with the ISO 11898-2 high-speed CAN (Controller Area Network) physical layer standard. The device is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Modes

The device has two main operating modes: normal mode and standby mode. Operating mode selection is made through the STB input pin.

Table 2. Operating Modes

STB PIN	MODE	DRIVER	RECEIVER	RXD PIN
LOW	NORMAL	Enabled (On)	Enabled (On)	Mirrors CAN bus
HIGH	STANDBY	Disabled (Off)	Low-power wake-up receiver and bus monitor enabled (On)	Low = wake-up request received High = no wake-up request received

8.3.1.1 Bus States by Mode

The CAN bus has three valid states during powered operation depending on the mode of the device. In normal mode the bus may be dominant (logic low) where the bus lines are driven differentially apart or recessive (logic high) where the bus lines are biased to $V_{CC}/2$ through the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low-power standby mode where the bus lines is biased to GND through the high-ohmic internal input resistors R_{IN} of the receiver.

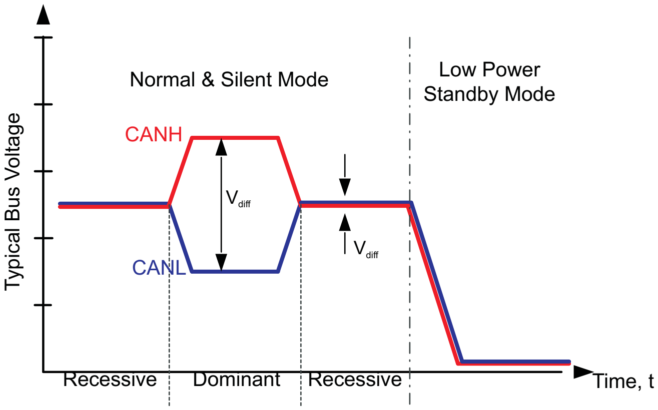


Figure 16. Bus States (Physical Bit Representation)

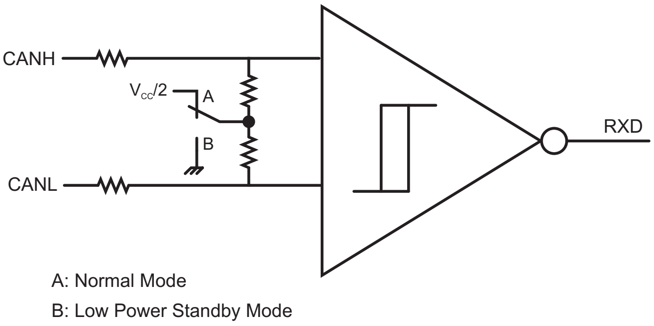


Figure 17. Simplified Common-Mode Bias and Receiver Implementation

8.3.1.2 Normal Mode

This is the normal operating mode of the device. It is selected by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the bus pins are biased to 0.5 × V_{CC}. In dominant state the bus pins (CANH and CANL) are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

The SPLIT pin is biased to 0.5 × V_{CC} for bus common-mode bus voltage bias stabilization in split termination network applications (see *Application and Implementation*).

8.3.1.3 Standby Mode and RXD Wake-Up Request

This is the low-power mode of the device. It is selected by setting STB high. The CAN driver and main receiver are turned off and bidirectional CAN communication is not possible. The low-power receiver and bus monitor are enabled to allow for wake-up requests through the bus. A wake-up request is output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake-up request. The CAN bus pins are weakly pulled to GND and the SPLIT pin is off (floating).

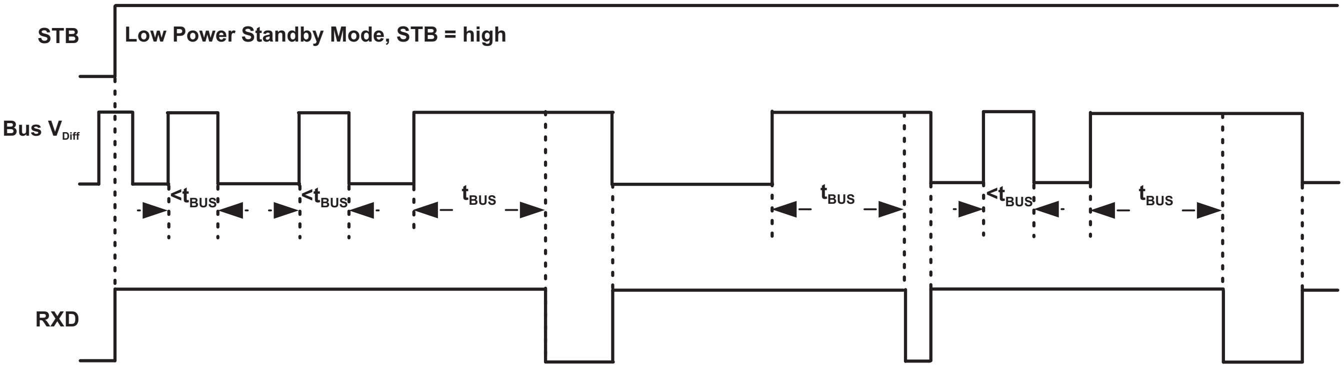


Figure 18. Standby Mode Low-Power Receiver and Bus Monitor Behavior

8.3.2 Protection Features

8.3.2.1 TXD Dominant State Time-Out

During normal mode (the only mode in which the CAN driver is active) the TXD dominant time-out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{DST}. The dominant time-out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires (t_{DST}), the CAN bus driver is disabled, thus freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the dominant state time-out. The CAN bus pins are biased to recessive level during a TXD dominant state time-out and SPLIT remains on.

NOTE

The maximum dominant TXD time allowed by the TXD Dominant state time-out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of 11 successive dominant bits (on TXD) for the worst case, where 5 successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = $11/t_{(dom)}$

8.3.2.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold the device turns off the CAN driver circuits, including the SPLIT pin. This condition is cleared when the temperature drops below the thermal shutdown temperature of the device.

8.3.2.3 Undervoltage Lockout and Unpowered Device

The device has undervoltage detection and lockout on the V_{CC} supply. If an undervoltage condition is detected on V_{CC}, the device protects the bus.

The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The STB is pulled up to V_{CC} to force the device in standby mode (low power) if the pin floats.

The bus pins (CANH, CANL, and SPLIT) all have extremely low leakage currents when the device is unpowered, so it does not load down the bus, but be an *ideal passive* load to the bus. This is critical, especially if some nodes of the network are unpowered while the rest of the network remains in operation.

8.4 Device Functional Modes

Table 3. Driver Function Table[1]

INPUTS		OUTPUTS		BUS STATE
TXD	**STB**	**CANH**	**CANL**	
L	L	H	L	Dominant
H	L	Z	Z	Recessive
Open	L	Z	Z	Recessive
X	H or Open	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = weak pulldown to GND, ? = indeterminate, Z = high impedance

Table 4. Receiver Function Table

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	STB	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	L	Dominant
$V_{ID} \geq 1.15$ V	H or Open	L	Dominant
0.5 V < V_{ID} < 0.9 V	X	?	?
$V_{ID} \leq 0.5$ V	X	H	Recessive
Open	X	H	Recessive

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Using With 3.3-V Microcontrollers

The input level threshold for the digital input pins of this device are 3.3-V compatible, however a few application considerations must be taken if using this device with 3.3-V microcontrollers. Both TXD and STB input pins have internal pullup sources to V_{CC}. Some microcontroller vendors recommend using an open-drain configuration on their I/O pins in this case even though the pullup limits the current. As such care must be taken at the application level that TXD and STB have sufficient pullup to meet system timing requirements for CAN. The internal pullup on TXD especially may not be sufficient to overcome the parasitic capacitances and allow for adequate CAN timing; thus, an additional external pullup may be required. Care should also be taken with the RXD pin of the microcontroller as the RXD output of this device drives the full V_{CC} range (5 V). If the microcontroller RXD input pin is not 5-V tolerant, this must be addressed at the application level. Other options include using a CAN transceiver from TI with I/O level adapting or a 3.3-V CAN transceiver.

9.1.2 Using SPLIT With Split Termination

The SPLIT pin voltage output provides 0.5 × V_{CC} in normal mode. The circuit may be used by the application to stabilized the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see Figure 19 and Figure 20). This pin provides a stabilizing recessive voltage drive to offset leakage currents of unpowered transceivers or other bias imbalances that might bring the network common-mode voltage away from 0.5 × V_{CC}. Using this feature in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltage levels at the start of message transmissions.

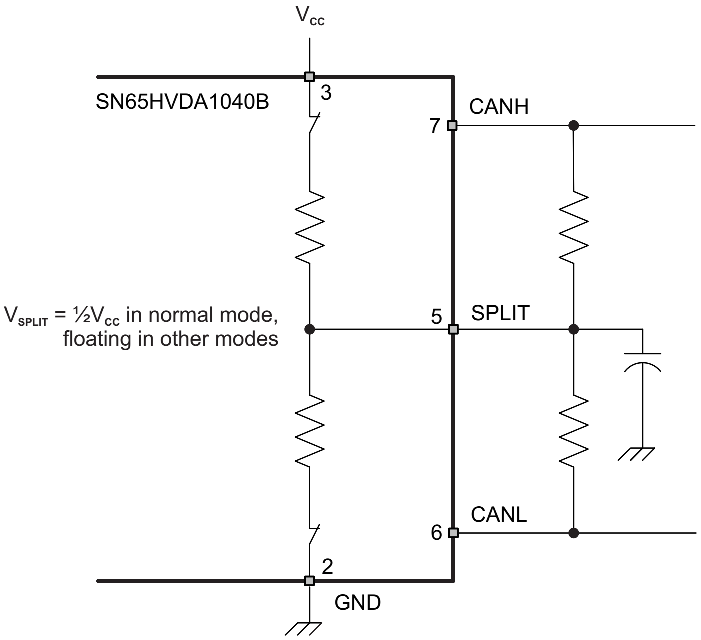


Figure 19. Split Pin Stabilization Circuitry and Application

9.2 Typical Application

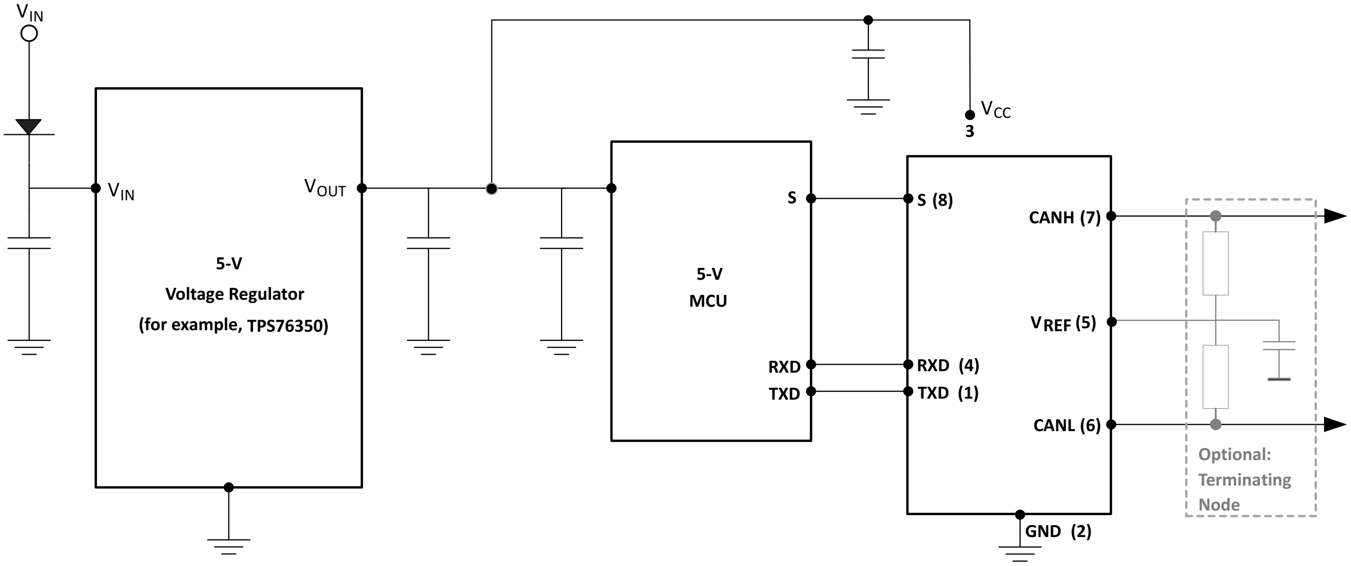


Figure 20. Typical Application Using Split Termination for Stabilization

9.2.1 Design Requirements

9.2.1.1 Bus Loading, Length, and Number of Nodes

The ISO 11898 Standard specifies up to 1 Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters, and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet, and NMEA200.

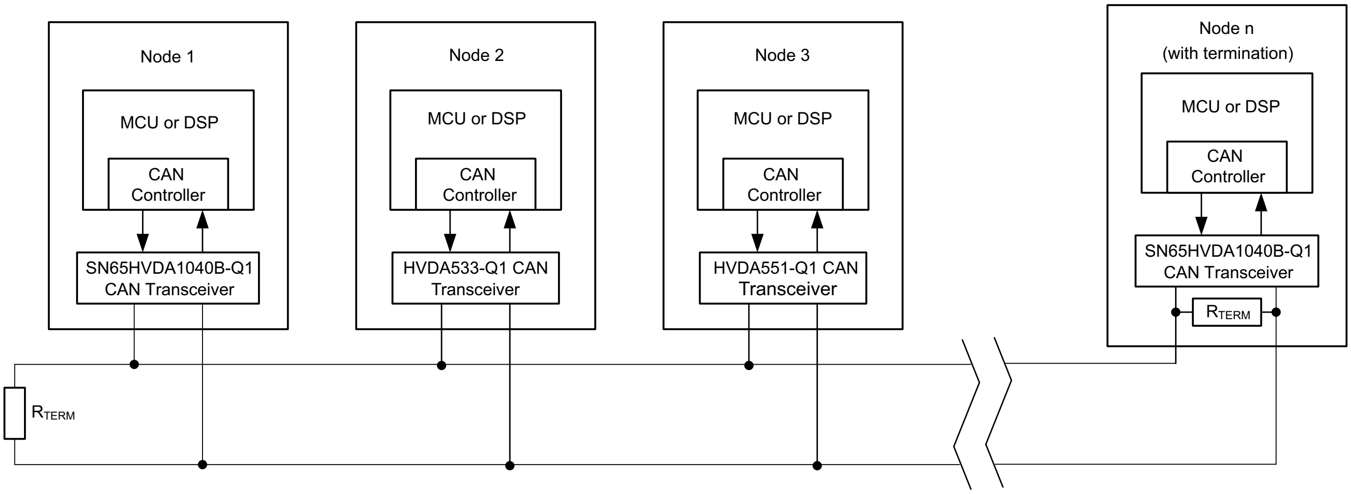


Figure 21. Typical CAN Bus Drawing

Typical Application (continued)

A high number of nodes requires a transceiver with high input impedance and wide common-mode range such as the SN65HVDA1040B-Q1 CAN transceiver. ISO 11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVDA1040B-Q1 device is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common-mode range of –2 V to 7 V through a 330-Ω coupling network. This network represents the bus loading of 90 SN65HVDA1040B-Q1 transceivers based on their minimum differential input resistance of 30 kΩ. Therefore, the SN65HVDA1040B-Q1 supports up to 90 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1-km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

9.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used (see Figure 22 and *Using SPLIT With Split Termination*).

Care should be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the CAN transceiver's current limit.

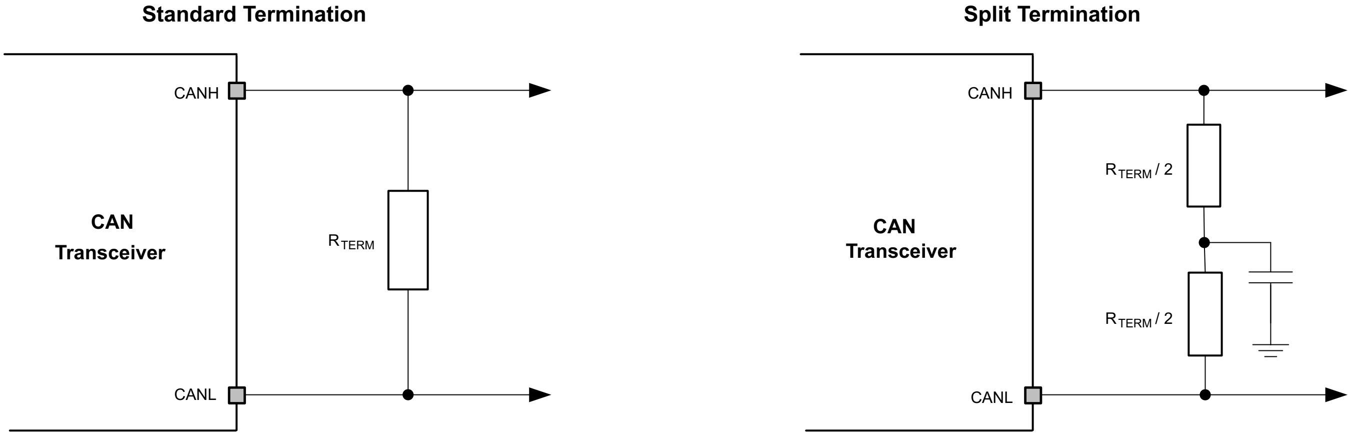


Figure 22. CAN Termination Schematic

9.2.1.3 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (the TXD pin) to the differential outputs (the CANH and CANL pins), plus the delay from the receiver inputs (the CANH and CANL) to its output (the RXD pin). A typical loop delay for the SN65HVDA1040B-Q1 transceiver is displayed in Figure 24 and Figure 25.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Voltage Suppresser (TVS) Diodes

Transient voltage suppressors are the preferred protection components for a CAN bus due to their low capacitance, which allows them to be designed into every node of a multinode network without requiring a reduction in data rate. With response times of a few picoseconds and power ratings of up to several kilowatts, TVS diodes present the most effective protection against ESD, burst, and surge transients.

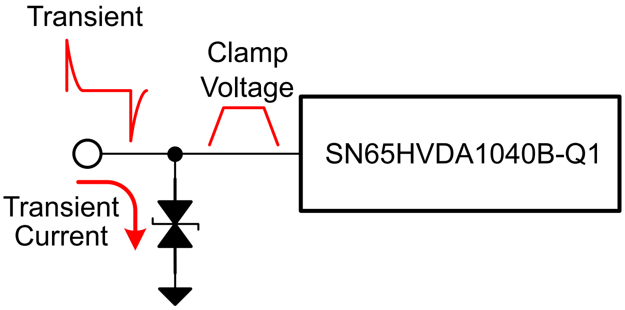


Figure 23. Transient Voltage Suppresser (TVS) Diodes Schematic

9.2.3 Application Curves

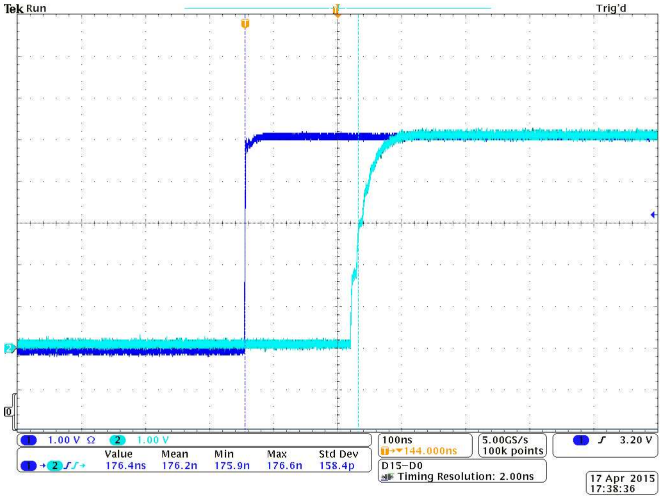


Figure 24. $t_{(LOOP)}$ Delay Waveform Dominant to Recessive

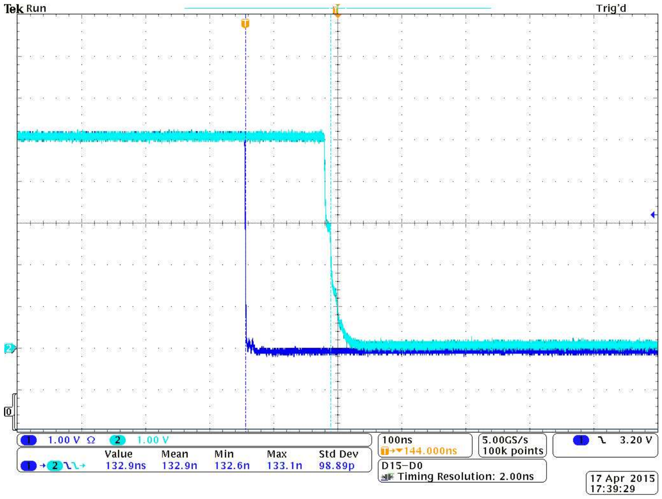


Figure 25. $t_{(LOOP)}$ Delay Waveform Recessive to Dominant

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close as possible to the V_{CC} supply pins as possible. The TPS76350 device is a linear voltage regulator suitable for the 5-V supply rail.

11 Layout

11.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. On-chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

- Use V_{CC} and ground planes to provide low inductance.

> **NOTE**
>
> High-frequency current follows the path of least inductance and not the path of least resistance.

- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 26.
- The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.
- Bus termination: Figure 22 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground through capacitor C6. Split termination provides common-mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this causes signal integrity issues if the bus is not properly terminated on both ends.
- Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples include C2 and C3 (V_{CC}).
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3, and R4.
- To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.
- Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10- kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.
- Pin 1: If an open-drain host processor is used to drive the TXD pin of the device an external pullup resistor between 1 kΩ and 10 kΩ should be used to drive the recessive input state of the device.
- Pin 5: SPLIT should be connected to the center point of a split temrination scheme to help stabalize the common-mode voltage to V_{CC} /2. If SPLIT is unused it should be left floating.
- Pin 8: Is shown assuming the mode pin, STB, is used. If the device only used in normal mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

11.2 Layout Example

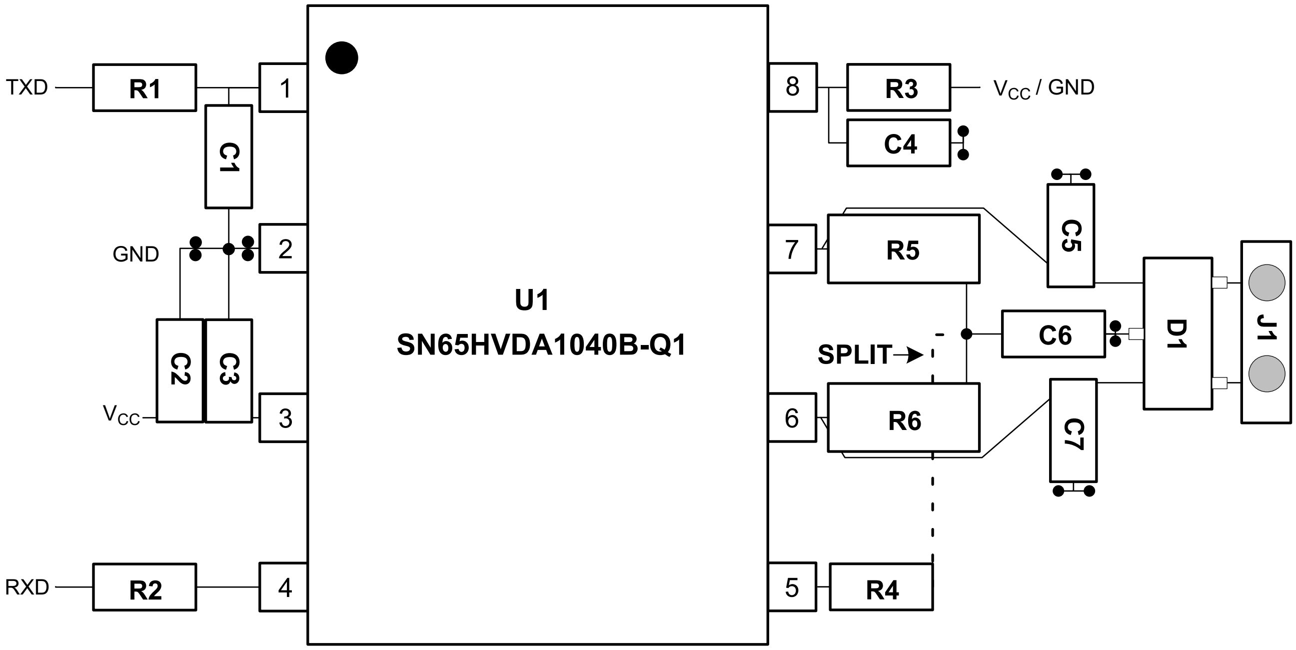


Figure 26. Typical CAN Bus Layout Example

11.3 ESD Protection

A typical application that employees a CAN bus network may require some form of ESD, burst, and surge protection to shield the CAN transceiver against unwanted transients that can potential damage the transceiver. To help shield the SN65HVDA1040B-Q1 transceiver against these high energy transients, transient voltage suppressors can be implemented on the CAN differential bus terminals. These devices help absorb the impact of a ESD, burst, and/or surge strike.

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：:

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVDA1040BQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1040B
SN65HVDA1040BQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1040B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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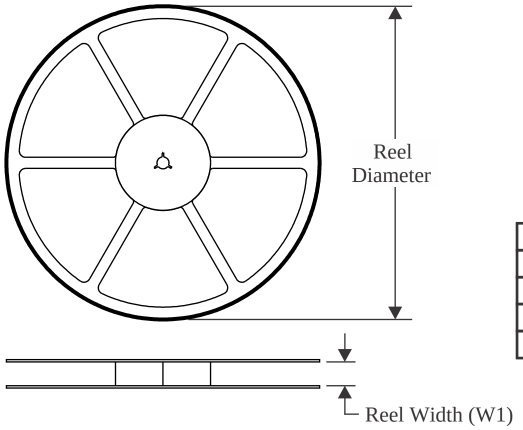
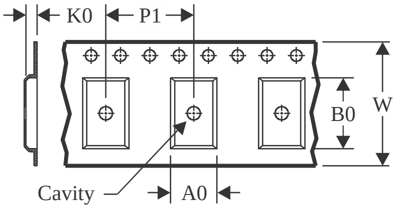
TAPE AND REEL INFORMATION

REEL DIMENSIONS

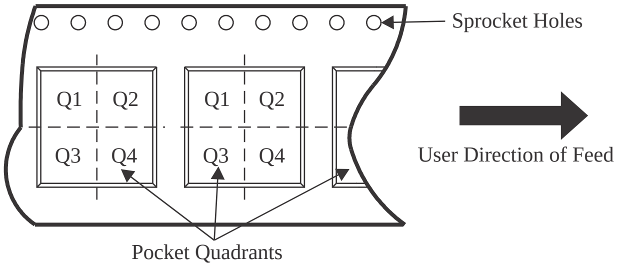


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

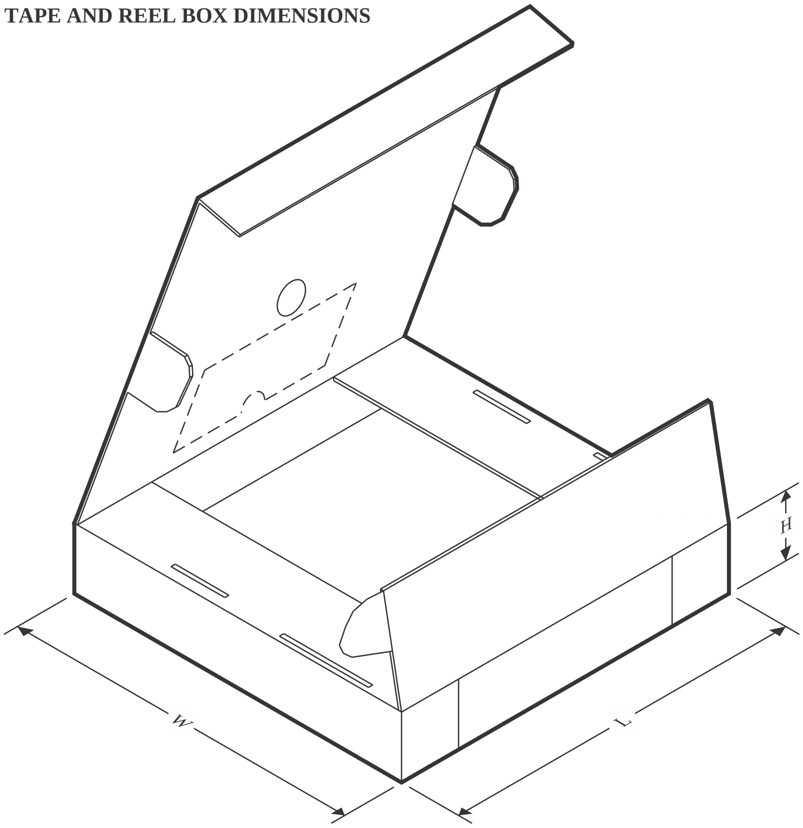
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

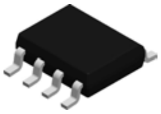
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVDA1040BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVDA1040BQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

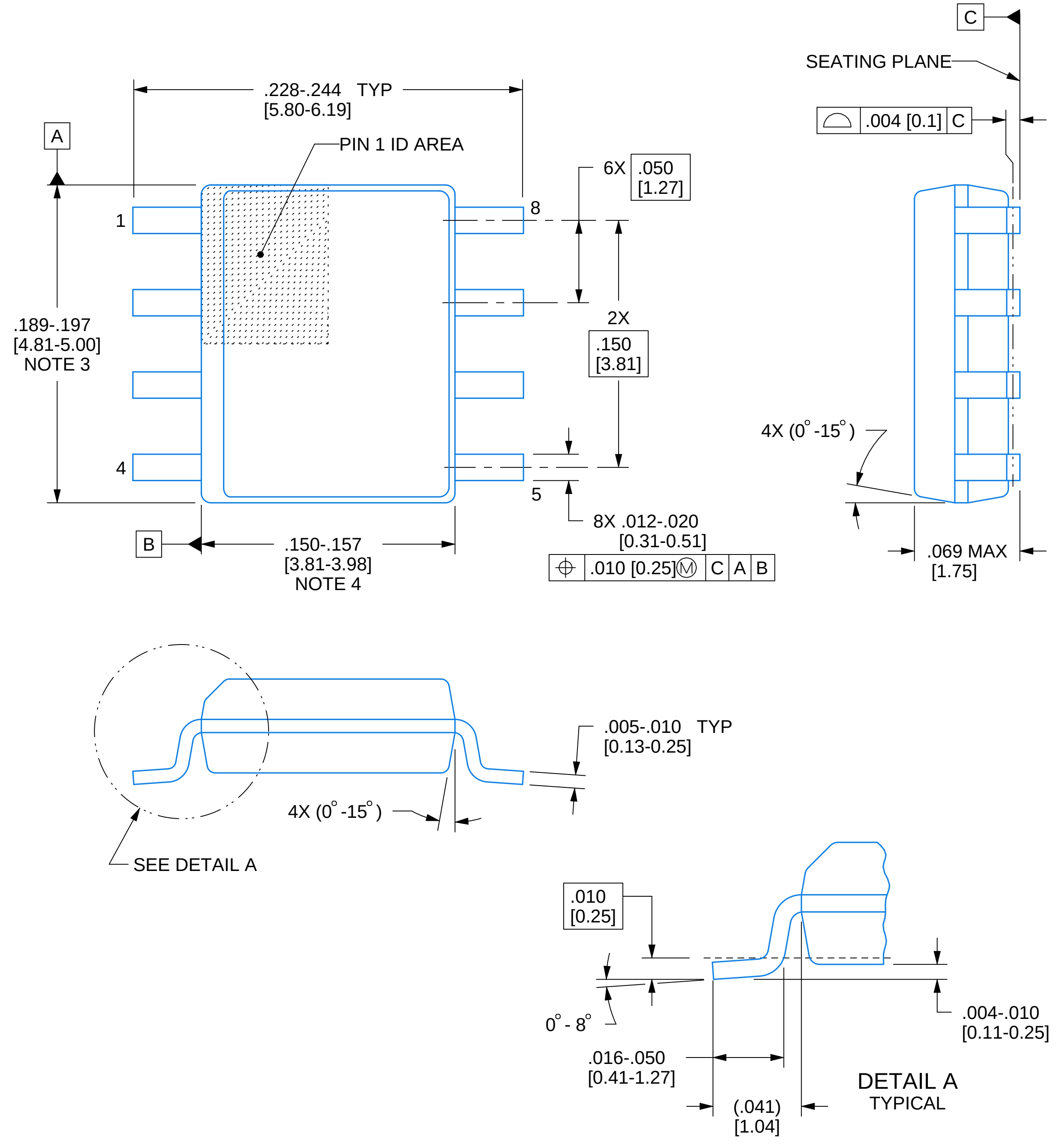


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

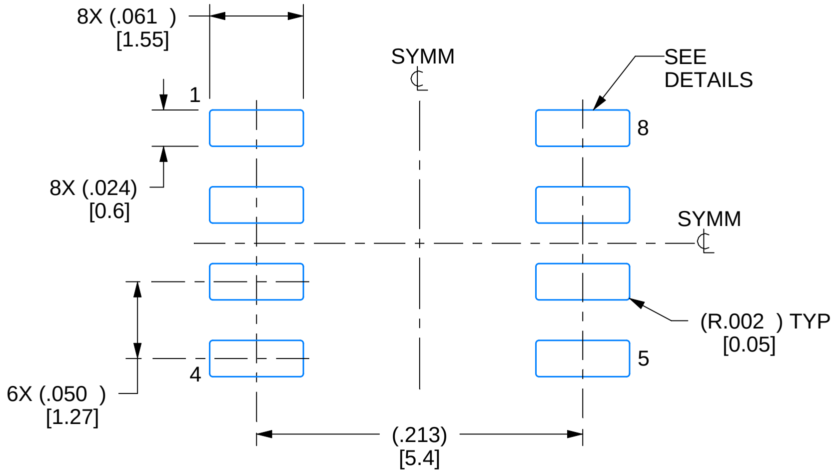
SMALL OUTLINE INTEGRATED CIRCUIT



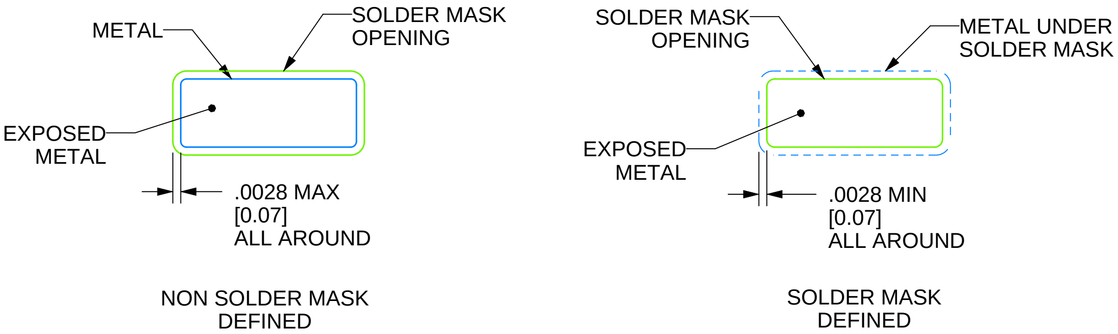
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



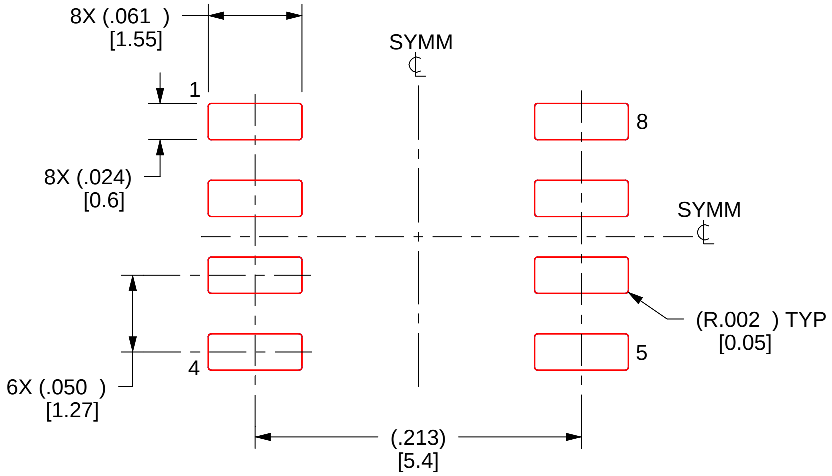
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

最后更新日期：2025 年 10 月