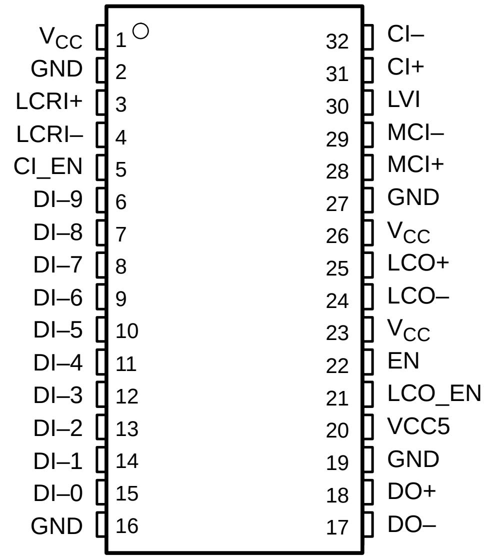
MuxIt™ SERIALIZER-TRANSMITTER

FEATURES

- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Supports Serialization of up to 10 Bits of Parallel Data Input at Rates up to 200 Mbps**
- **PLL Lock/Valid Input Provided to Enable Link Data Transfers**
- **Cascadable With Additional SN65LVDS151 MuxIt Serializer-Transmitters for Wider Parallel Input Data Channel Widths**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI TIA/EIA-644-A**
- **LVDS Inputs and Outputs ESD Protection Exceeds 12 kV HBM**
- **LVTTL Compatible Inputs for Lock/Valid, Enables, and Parallel Data Inputs Are 5-V Tolerant**
- **Operates With 3.3 V Supply**
- **Packaged in 32-Pin DA Thin Shrink Small-Outline Package With 26 Mil Terminal Pitch**

SN65LVDS151DA
(Marked as 65LVDS151)



DESCRIPTION

MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user-selectable and allows for higher transmission efficiencies than with existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644-A) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications: the SN65LVDS150 phase locked loop frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

The SN65LVDS151 consists of a 10-bit parallel-in/serial-out shift register, three LVDS differential transmission line receivers, a pair of LVDS differential transmission line drivers, plus associated input buffers. It accepts up to 10 bits of user data on parallel data inputs (DI-0 → DI-9) and serializes (multiplexes) the data for transmission over an LVDS transmission line link. Two or more SN65LVDS151 units may be connected in series (cascaded) to accommodate wider parallel data paths for higher serialization values. Data is transmitted over the LVDS serial link at M times the input parallel data clock frequency. The multiplexing ratio M, or number of bits per data clock cycle, is programmed on the companion SN65LVDS150 MuxIt programmable PLL frequency multiplier with configuration pins (M1 → M5). The range of multiplexing ratio M supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier is between 4 and 40. Table 1 shows some of the combinations of LCRI and MCI supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Data is parallel loaded into the SN65LVDS151 input latches on the first rising edge of the M-clock input (MCI) signal following a rising edge of the link clock reference input (LCRI). The data is read out serially from the SN65LVDS151 shift registers on the rising edges of the M-clock input (MCI). The lowest order bit of parallel input data, DI-0, is output from DO on the third rising edge of MCI following the rising edge of LCRI. The remaining bits of parallel input data, DI-1 → DI-(M-1) are clocked out sequentially, in ascending order, by subsequent MCI rising edges. The link clock output (LCO) signal rising edge is synchronized to the data output (DO) by an internal circuit clocked by MCI. The LCO signal rising edge follows the first rising edge of MCI after the rising edge of LCRI. Examples of operating waveforms for values of M = 4 and M = 10 are provided in Table 1.

Both the LCRI and MCI signals are intended to be sourced from the SN65LVDS150 MuxIt programmable frequency multiplier. They are carried over LVDS differential connections to minimize skew and jitter. The SN65LVDS151 includes LVDS differential line drivers for both the serialized data output (DO) stream and the link clock output (LCO). The cascade input (CI) is also an LVDS connection, and when it is used it is tied to the DO output of the preceding SN65LVDS151.

An internal power-on reset (POR) and an enable input (EN) control the operation of the SN65LVDS151. When V_{CC} is below 1.5 V, or when EN is low, the device is in a low-power disabled state, and the DO and LCO differential outputs are in a high-impedance state. When V_{CC} is above 3 V and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link clock output enable input (LCO_EN) is used to turn off the LCO output when it is not being used. Cascade input enable (CI_EN) is used to turn off the CI input when it is not being used.

Serialized data bits are output from the DO output, starting in ascending order, from parallel input bit DI-0. The number of serialized data bits output per data clock cycle is determined by the multiplexing ratio M. For values of M less than or equal to 10, the cascade input (CI±) is not used, and only the first M parallel input bits (DI-0 thought DI-[M-1]) are used. For values of M greater than 10, all ten parallel input bits (DI-0 though DI-9) are used, and the cascade input is used to shift in the remaining data bits from additional SN65LVDS151 serializers. Table 2 shows which input data bits are used as a function of the multiplier M.

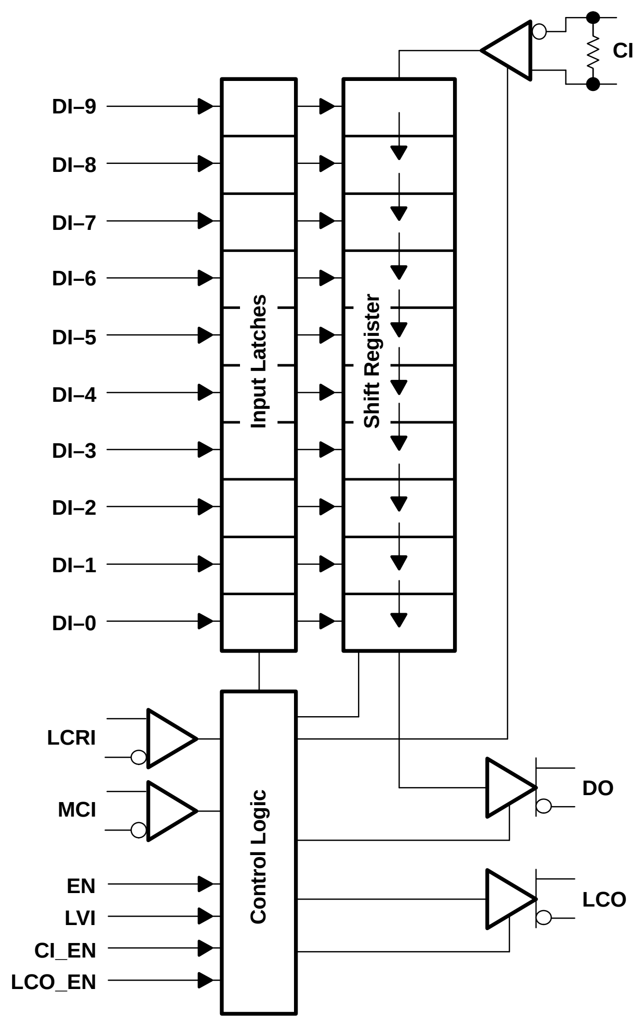
Table 1. Example Combinations of LCRI and MCI Supported by the SN65LVDS150 Muxit Programmable PLL Frequency Multiplier

	LCRI, MHz		MCI, MHz	
M	MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
4	5	50	20	200
10	5	20	50	200
20	5	10	100	200
40	5	5	200	200

Table 2. Input Data Bits Used as a Function of the Multiplier M

	M = 4	M = 5	M = 6	M = 7	M = 8	M = 9	M = 10	M >10
1st bit output	DI-0	DI-0	DI-0	DI-0	DI-0	DI-0	DI-0	DI-0
2nd bit output	DI-1	DI-1	DI-1	DI-1	DI-1	DI-1	DI-1	DI-1
3rd bit output	DI-2	DI-2	DI-2	DI-2	DI-2	DI-2	DI-2	DI-2
4th bit output	DI-3	DI-3	DI-3	DI-3	DI-3	DI-3	DI-3	DI-3
5th bit output	Invalid	DI-4	DI-4	DI-4	DI-4	DI-4	DI-4	DI-4
6th bit output	Invalid	Invalid	DI-5	DI-5	DI-5	DI-5	DI-5	DI-5
7th bit output	Invalid	Invalid	Invalid	DI-6	DI-6	DI-6	DI-6	DI-6
8th bit output	Invalid	Invalid	Invalid	Invalid	DI-7	DI-7	DI-7	DI-7
9th bit output	Invalid	Invalid	Invalid	Invalid	Invalid	DI-8	DI-8	DI-8
10th bit output	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI-9	DI-9
11th + bits output	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	CI bits

BLOCK DIAGRAM



NOTE: The CI input includes a 110 Ω termination resistor.

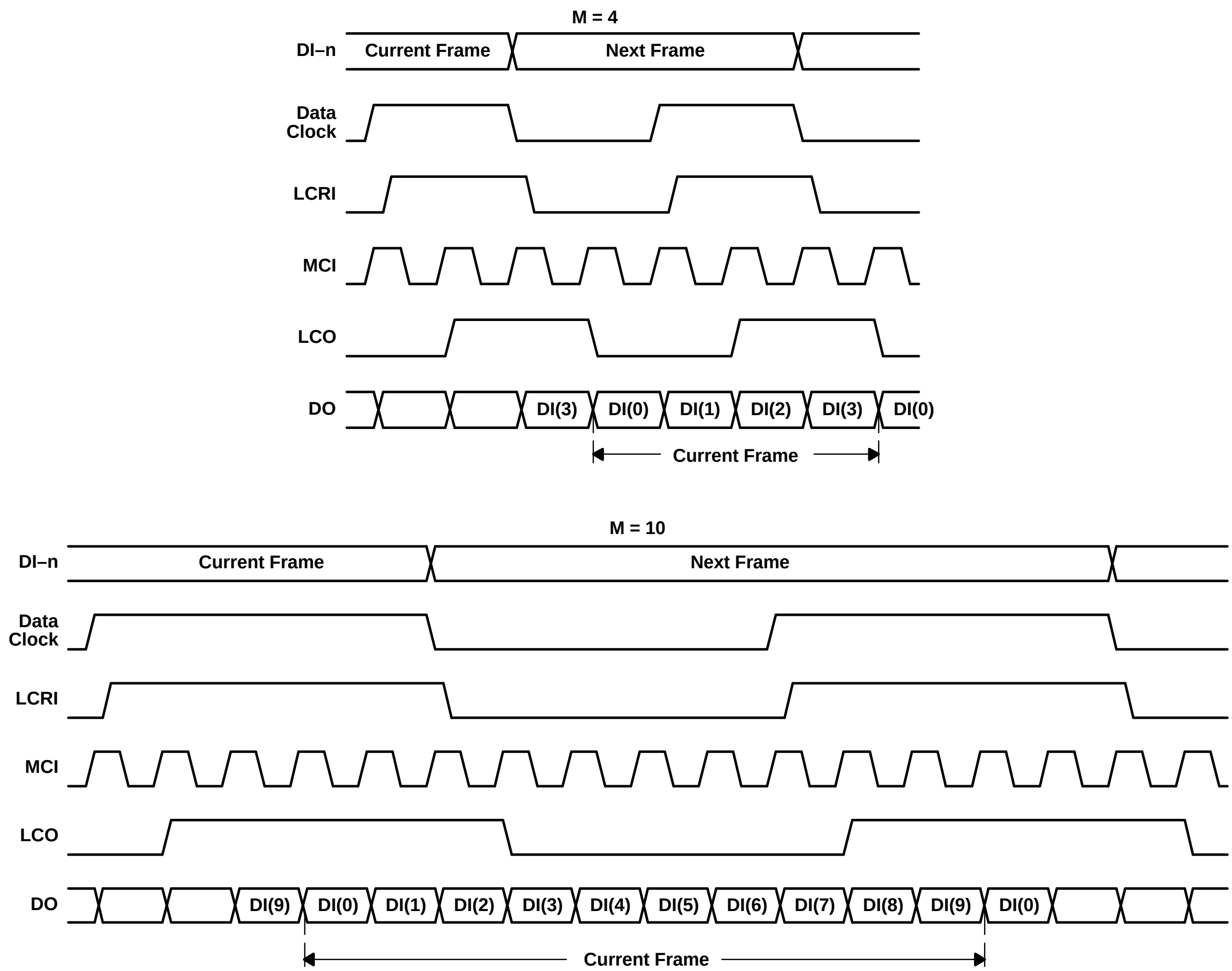
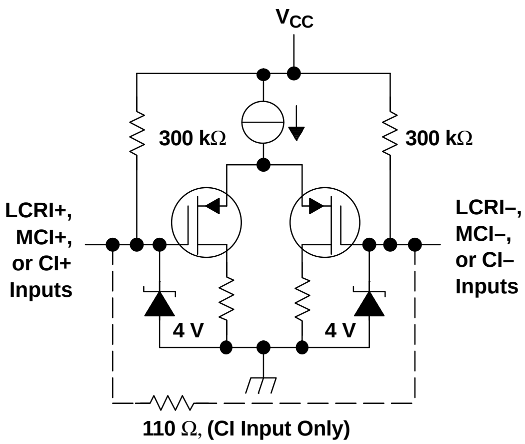
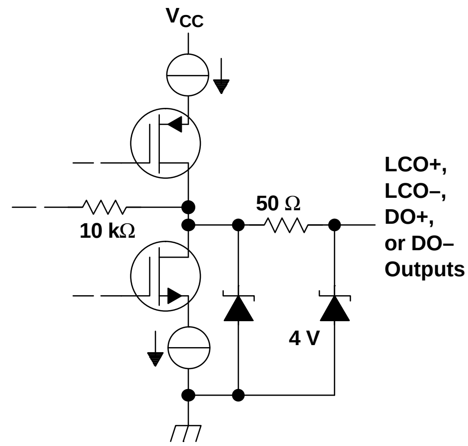
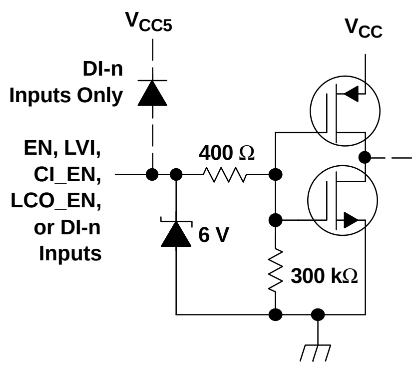


Figure 1. Operating Waveform Examples

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS







Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	TYPE	DESCRIPTION
CI+, CI–	31, 32	I	LVDS	Cascade input. This may be used to connect additional SN65LVDS151 units when the multiplexing ratio M value is greater than 10. This input has an internal 110-Ω nominal termination resistor.
CI_EN	5	I	LVTTL	Cascade input enable. Used to enable or disable the cascade input differential receiver. A high-level input enables the CI input, a low-level input disables the CI input.
DO–, DO+	17, 18	O	LVDS	Data output. This is the data being transmitted to the destination end of the serial link, or being supplied to another SN65LVDS151 unit in cascade.
EN	22	I	LVTTL	Enable. Controls device operation. A high-level input enables the device; a low-level input disables and resets the device. When initially enabled, all outputs are in a low-level condition.
GND	2, 16, 19, 27		NA	Circuit ground
LCO+, LCO–	25, 24	O	LVDS	Link clock output This is the data block synchronization clock being transmitted to the destination end of the serial link.
LCO_EN	21	I	LVTTL	Link clock output enable. Used to disable the link clock output when it is not being used. A high-level input enables the LCO output; a low-level input disables the LCO output.
LCRI+, LCR–	3, 4	I	LVDS	Link clock reference input. This is the clock for latching in the parallel data; it comes from the PLL frequency multiplier.
LVI	30	I	LVTTL	Lock/valid input. This is a signal required for proper Muxlt system operation. It is directly connected to the LVO output of a SN65LVDS150. It is used to inhibit the operation of this device until after the PLL has stabilized. A low level input forces a reset of the internal latches and shift registers, and forces the DO and LCO outputs to a low level. A high level input enables operation.
MCI+, MC–	28, 29	I	LVDS	M-clock input. This is the high frequency multiplied clock input from the local PLL frequency multiplier. It synchronizes the transmission of the link data
DI-9–DI-0	6-15	I	LVTTL	Parallel data inputs. Data is latched into the device on the first rising edge of MCI following a rising edge of LCRI.
V_{CC}	1, 23, 26		NA	Supply voltage
VCC5	20		NA	5-V V_{CC} tolerance bias. Tied to 5 V nominal when the LVTTL inputs are being driven by a device powered from a 5-V supply, otherwise tied to local V_{CC}

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage range, V_{CC} (2)		–0.5 V to 4 V
Voltage range	DI-0 through DI-9 inputs	–0.5 V to VCC5 +0.5 V
	EN, CI_EN, LCO_EN, LVI inputs, VCC5	–0.5 V to 5.5 V
	CI±, LCRI±, or MCI± Inputs, DO±, or LCO± outputs	–0.5 to 4 V
Electrostatic discharge, human body model(3)	MCI±, LCRI±, CI±, DO±, LCO±, and GND	±12 kV
	All pins	±2 kV
Charged-device model(4)	All pins	±500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
DA	1453 mW	11.6 mW/°C	756 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	DI-0 - DI-9, EN, LVI, LCO_EN, CI_EN	2			V
V_{IL}	Low-level input voltage	DI-0 - DI-9, EN, LVI, LCO_EN, CI_EN			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	LCRI, MCI, CI	0.1		0.6	V
V_{IC}	Common-mode input voltage	LCRI, MCI, CI	$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$	V
					V_{CC}-0.8	V
T_A	Operating free-air temperature		40		85	°C

TIMING REQUIREMENTS

PARAMETERS			TEST CONDITIONS	MIN	MAX	UNIT
$t_{su(1)}$	LCRI↑setup time before MCI↑		See Figure 2	0.5		ns
$t_{h(1)}$	LCRI hold time after MCI↑		See Figure 2	0.3		ns
$t_{su(2)}$	Data setup time, DI-0–DI-9 before MCI↑ after LCRI↑		See Figure 3	0		ns
$t_{h(2)}$	Data hold time, DI-0–DI-9 valid after MCI↑ after LCRI↑		See Figure 3	2		ns
$t_{su(3)}$	CI setup time before MCI↑	$T_A \leq 25°C$	See Figure 4	0.8		ns
		T_A = 85°C	See Figure 4	1.1		ns
$t_{h(3)}$	CI hold time after MCI↑		See Figure 4	2.5		ns
t_c	Clock cycle time	LCRI		20	200	ns
		MCI		5	50	ns
t_w	High-level clock pulse width duration	MCI, LCRI		0.4 t_c	0.6 t_c	ns

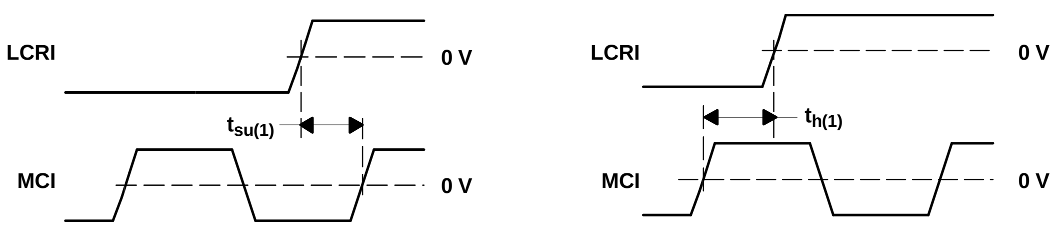


Figure 2. Clock Input Timing Requirements

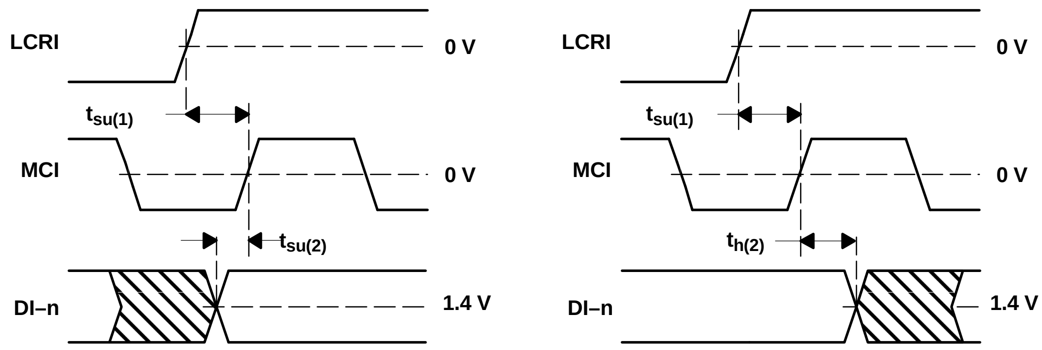


Figure 3. Data Input Timing Requirements

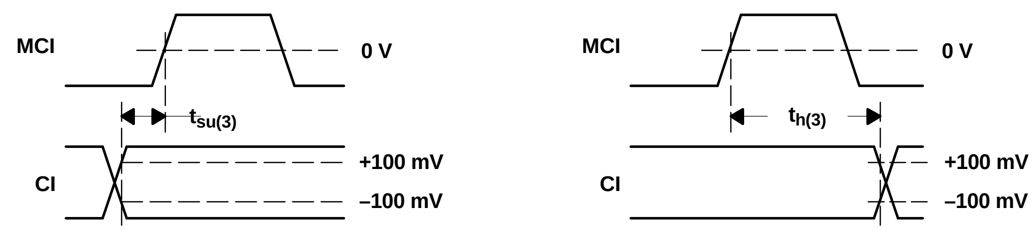


Figure 4. Cascade Input Timing Requirements

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold		See Figure 5			100	mV
V_{ITH-}	Negative-going differential input voltage threshold			–100			mV
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude		R_L = 100 Ω, V_{ID} = ±100 mV, See Figure 6 and Figure 7	247	340	454	mV
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage magnitude between logic states			–50		50	mV
$V_{OC(SS)}$	Steady-stade common-mode output voltage		See Figure 8	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak change common-mode output voltage				50	150	mV
I_{CC}	Supply current		Enabled, R_L = 100 Ω		22	30	mA
			Disabled		0.5	1	
			$f_{(MCI)}$ = 200 MHz, $f_{(LCRI)}$ = 20 MHz, R_L = 100 Ω, DI-n= 1010101010		35	65	
I_{ID}	Differential input current	(I_{I+} - I_{I-}) (CI input)	V_{ID} = 0.4 V, V_{IC} = 2.2 V or 0.2 V	3		4.4	mA
		(I_I+ - I_I-) (LCRI, MCI inputs)	V_{IC} = 0.05 V to 2.35 V, V_{ID} = ±0.1 V	–2		2	µA
I_I	Input current	LCRI, MCI inputs	V_I = 0 V	–2		–20	µA
			V_I = 2.4 V	–1.2			
		CI input	V_I = 0 V	–4		–40	µA
			V_I = 2.4 V	–2.4			
$I_{I(OFF)}$	Power-off output current	LCRI, MCI inputs	V_{CC} = 0 V , V_I = 3.6 V			20	µA
		CI input				40	
I_{IH}	High-level input current	EN, LVI, DI-n, LCO_EN	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current	EN, LVI, DI-n, LCO_EN	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	DO, LCO	V_{O+} or V_{O-} = 0 V	–10		10	mA
			V_{OD} = 0 V	–10		10	

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
I_{OZ}	High-impedance output current		V_O = 0 V or V_{CC}	–5		5	μA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 1.5 V , V_I = 3.6 V	–5		5	μA
C_I	Input capacitance	LCRI, MCI inputs	V_{ID} = (0.4sin(4E6πt) + 0.5) V		3		pF

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(1)}$	Propagation delay time, MCI↑ to DO↑	$T_A \leq 25°C$	R_L = 100 Ω, C_L = 10 pF, See Figure 9	3	5	5.8	ns
		T_A = 85°C		3	5	6.1	
$t_{d(2)}$	Propagation delay time, MCI↑ to DO↓	$T_A \leq 25°C$		3	5	5.8	ns
		T_A = 85°C		3	5	6.1	
$t_{d(3)}$	Propagation delay time, MCI↑ to LCO↑	$T_A \leq 25°C$		3	5	5.8	ns
		T_A = 85°C		3	5	6.1	
t_r	Differential output signal rise time		R_L = 100 Ω, C_L = 10 pF, See Figure 10	0.3	0.8	1.5	ns
t_f	Differential output signal fall time			0.3	0.8	1.5	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$), DO			–250	0	250	ps
$t_{sk(pp)}$	Part-to-part output skew, DO				0	2.3	ns
$t_{sk(\omega)}$	Multiple-frequency skew, LCO↑ to DO↑ or DO↓		See Figure 11	-250	0	250	ps
t_{PZL}	Propagation delay time, high-impedance to low-level		EN input to DO, LCO output, See Figure 12		3	20	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance				3	10	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance				4	10	ns

PARAMETER MEASUREMENT INFORMATION

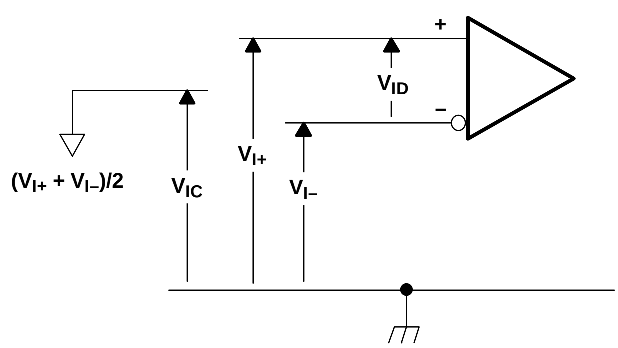


Figure 5. Receiver Voltage Definitions

Table 3. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{I+}	V_{I-}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

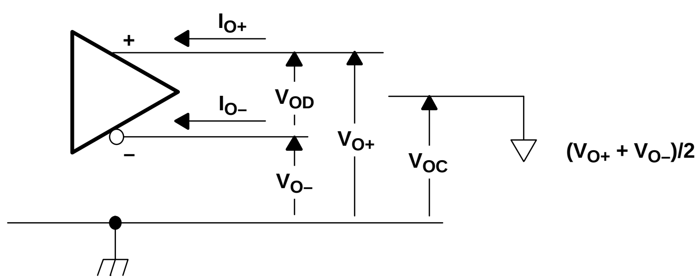


Figure 6. Driver Voltage and Current Definitions

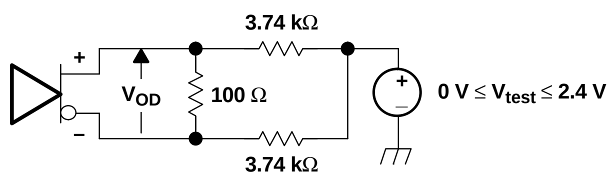
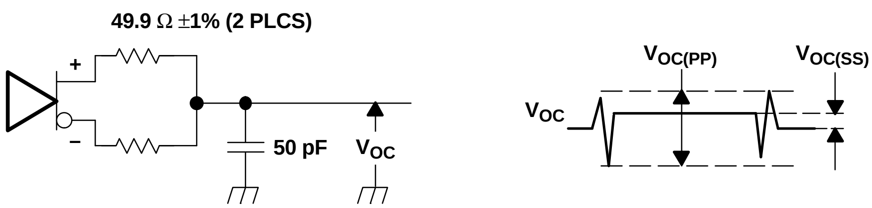


Figure 7. V_{OD} Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 5 GHz.

Figure 8. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

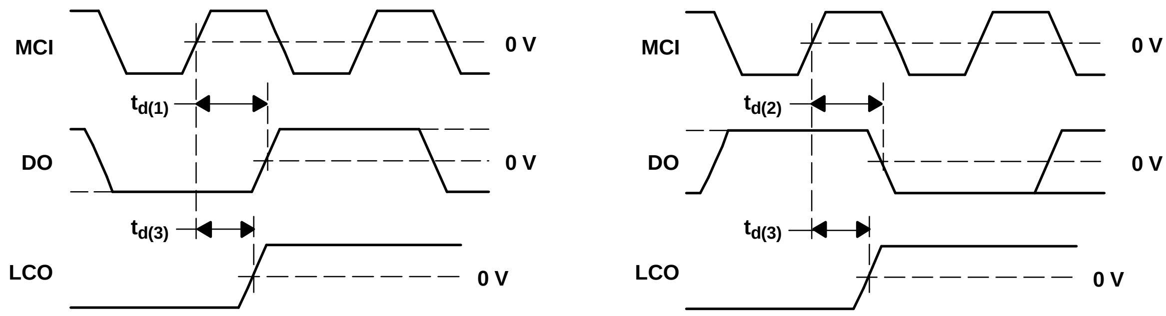
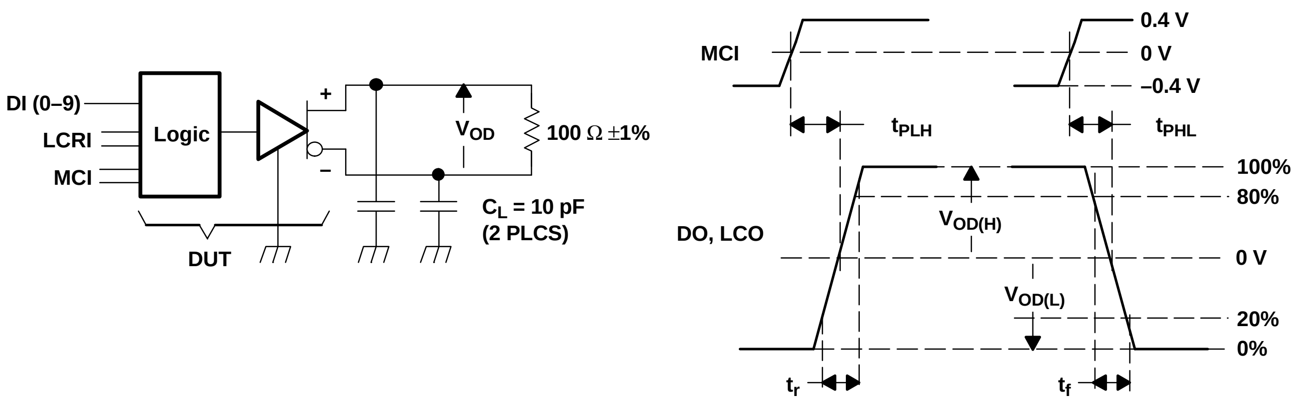


Figure 9. Output Timing Waveforms



A. All input pulses are supplied by generators having the following characteristics: t_r or $t_f \leq 1$ ns, MCI pulse repetition rate (PRR) = 50 Mpps, MCI Pulse width = 10 ± 0.2 ns, LCRI pulse repetition rate (PRR) = 5 Mpps, LCRI pulse width = 100 ±20 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 10. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

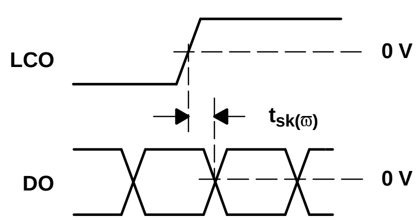


Figure 11. LCO to DO Multiple-Frequency Skew Waveforms

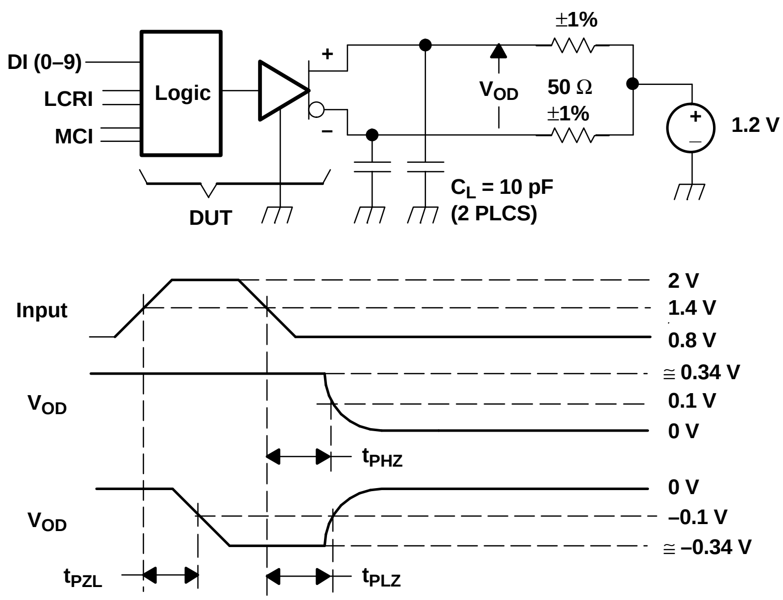


Figure 12. Enable/Disable Time Waveforms

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

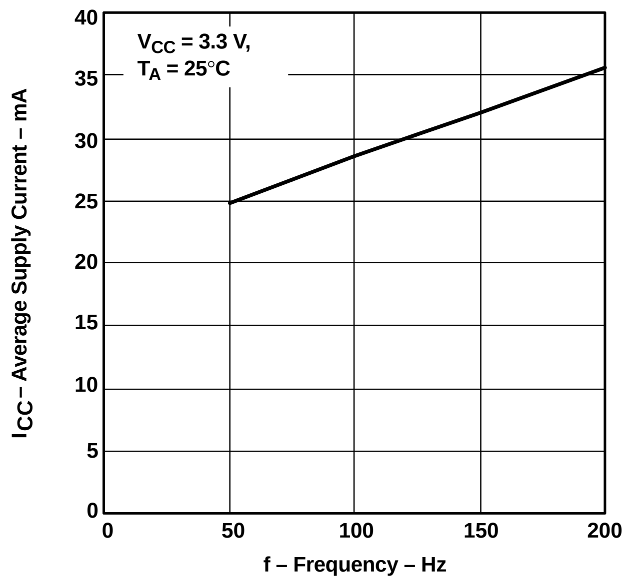


Figure 13.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS151DA	Last Time Buy	Production	TSSOP (DA) | 32	46 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65LVDS151
SN65LVDS151DA.B	Last Time Buy	Production	TSSOP (DA) | 32	46 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65LVDS151
SN65LVDS151DAR	Last Time Buy	Production	TSSOP (DA) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65LVDS151
SN65LVDS151DAR.B	Last Time Buy	Production	TSSOP (DA) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65LVDS151

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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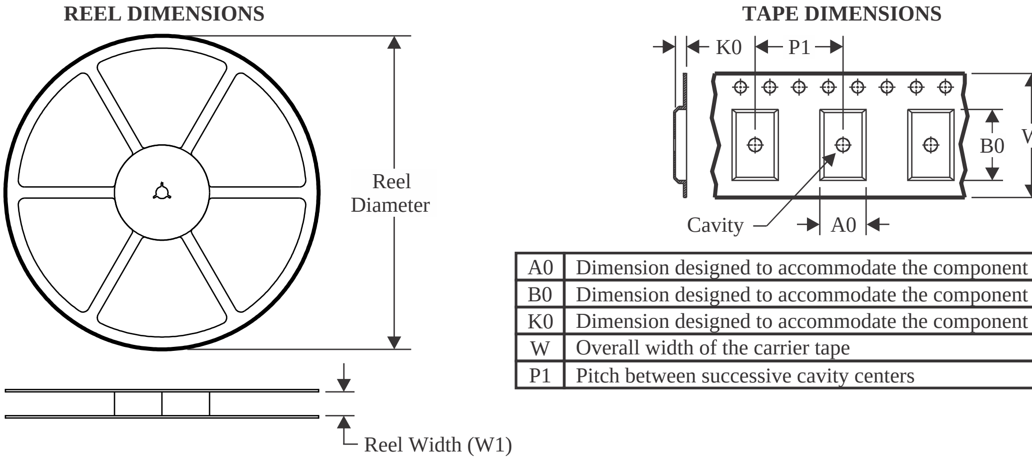
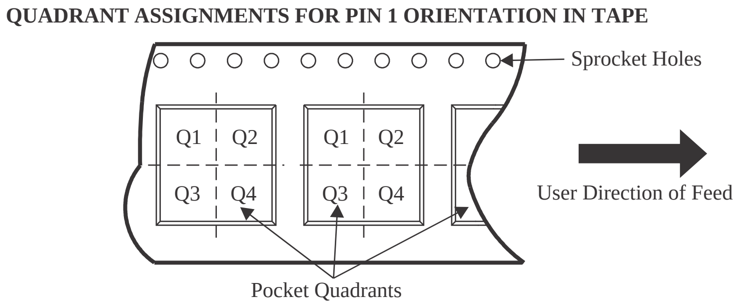
TAPE AND REEL INFORMATION



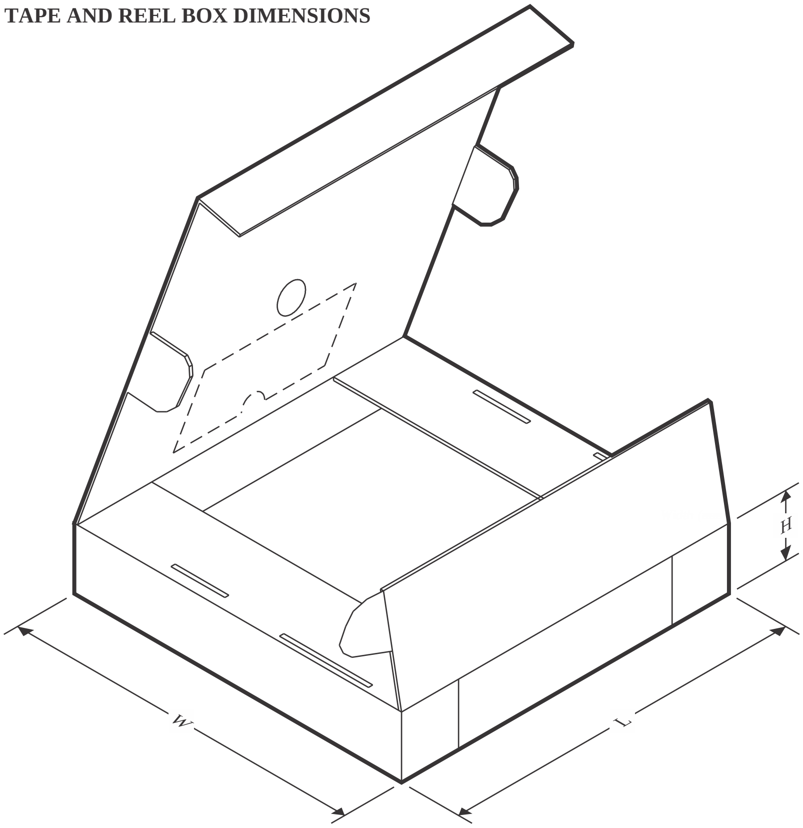
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS151DAR	TSSOP	DA	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

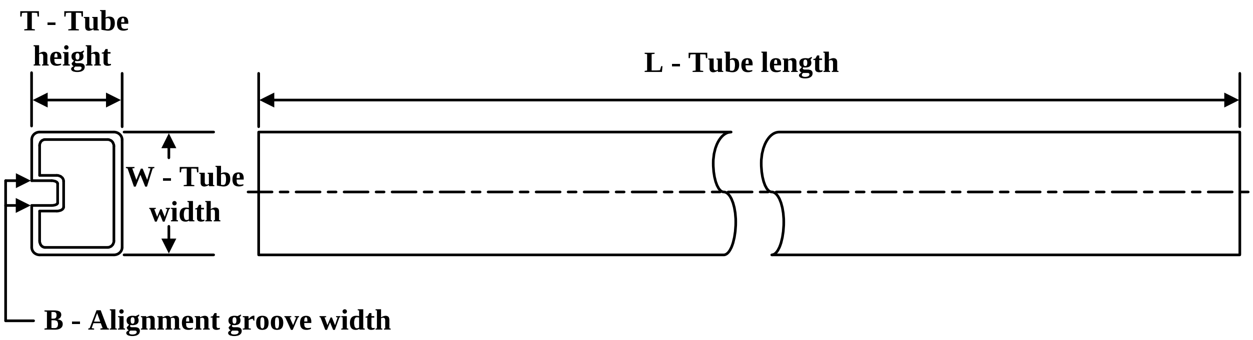
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS151DAR	TSSOP	DA	32	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS151DA	DA	TSSOP	32	46	530	11.89	3600	4.9
SN65LVDS151DA.B	DA	TSSOP	32	46	530	11.89	3600	4.9

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