双信道 USB3.0 转接驱动器，均衡器

查询样片: SN65LVPE512

特性

- 单线路 **USB 3.0** 均衡器，转接驱动器
- 可选均衡、去加重以及输出摆幅控制
- 集成型端接
- 支持热插拔
- 低有源功耗（**U0** 状态）
  - **315mW**（典型值）V_{CC} **= 3.3V**
- **USB 3.0** 低功耗支持
  - 未检测到连接时功耗为 **7mW** （典型值）
  - 在 **U2**，**U3** 模式下进行链接时功耗为 **70mW**（典型值)
- 优异的抖动与损耗补偿性能：
  - **FR4** 上大于 **40** 英寸的总共 **4mil** 带状线
- 小封装尺寸 **- 3mm x 3mm** 和 **4mm x 4mm 24** 引脚四方扁平无引线 **(QFN)** 封装
- 针对静电放电 **(ESD)** 瞬态的高度保护功能
  - 人体模型 **(HBM)**：**5000V**
  - 充电器件模型 **(CDM)**：**1500V**
  - 机器模型 **(MM)**：**200V**

应用范围

- 笔记本、台式机、扩展坞、有源线缆、背板与有源线缆

说明

SN65LVPE512 是一款支持 5Gbps 数据速率的双信道、单线路 USB 3.0 转接驱动器与信号调节器。 该器件符合 USB 3.0 技术规范修订版本 1.0，支持针对 USB 3.0 电源管理模式的电气空闲调节与低频率周期信号 (LFPS)。

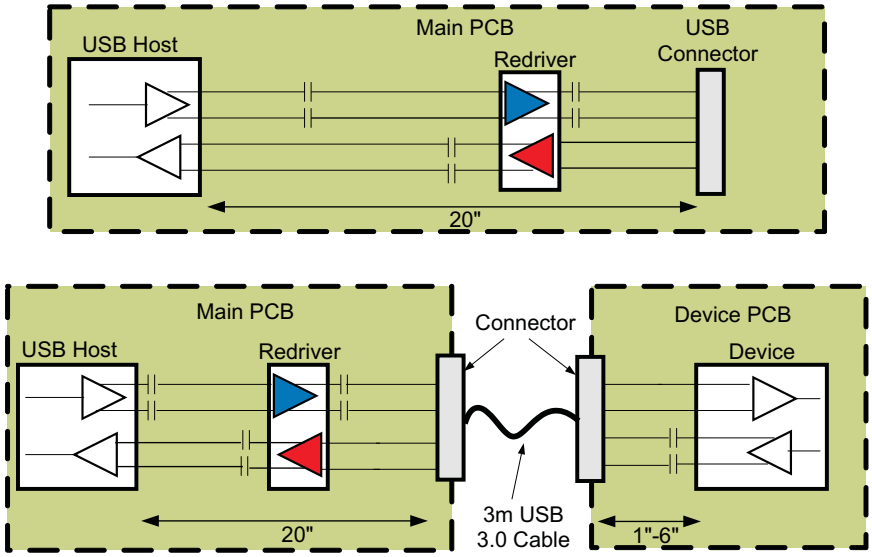


Figure 1. Typical Application

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

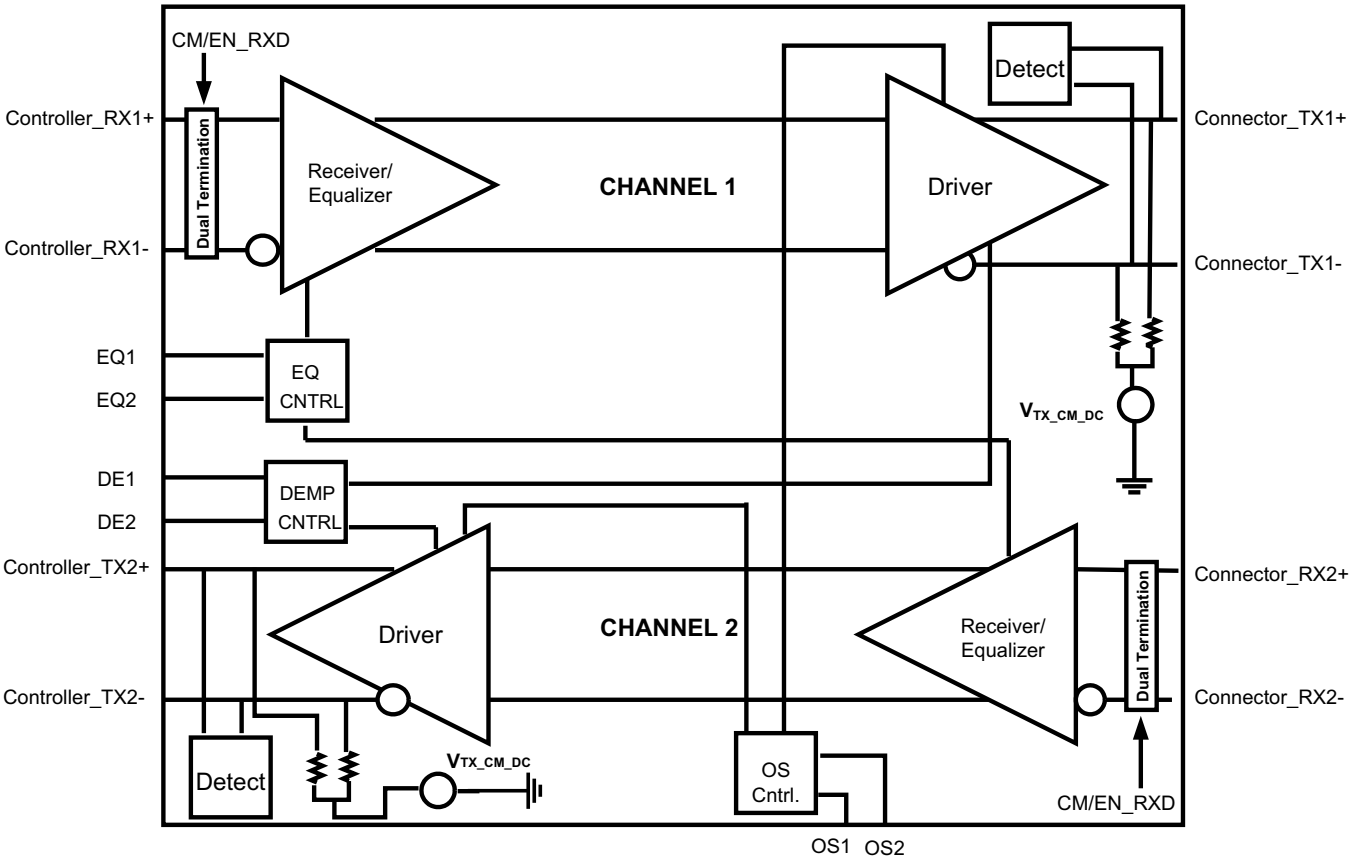


Figure 2. Data Flow Block Diagram

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range(2)	V_{CC}	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control I/O	–0.5	VCC + 0.5	V
Electrostatic discharge	Human body model(3)		±5000	V
	Charged-device model(4)		±1500	V
	Machine model(5)		±200	V
Continuous power dissipation		See the Thermal Table		

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

THERMAL INFORMATION

THERMAL METRIC		RGE PACKAGE	RMQ PACKAGE	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	47.5	41.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.6	37.0	
θ_{JB}	Junction-to-board thermal resistance	24.6	11.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.4	6.4	
Ψ_{JT}	Junction-to-top characterization parameter	1.4	0.5	
Ψ_{JB}	Junction-to-board characterization parameter	24.6	11.4	

THERMAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation	RSVD, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 mV_{p-p}		330	450	mW
P_{Slp}	Device power dissipation in sleep mode	EN_RXD = GND		0.03	0.4	mW

Device Power

The SN65LVPE512 is designed to operate from a single 3.3V supply.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	AC Coupling capacitor		75		200	nF
	Operating free-air temperature		-40		85	°C
DEVICE PARAMETERS						
I_{CC}	Supply current	EN_RXD, RSVD, EQ cntrl = NC, K28.5 pattern at 5 Gbps, VID = 1000mVp-p		100	120	mA
$ICC_{Rx.Detect}$		In Rx.Detect mode		2	5	
ICC_{sleep}		EN_RXD = GND		0.01	0.1	
ICC_{U2-U3}		Link in USB low power state		21		
	Maximum data rate				5	Gbps
t_{ENB}	Device enable time	Sleep mode exit time EN_RXD L → H With Rx termination present			100	µs
t_{DIS}	Device disable time	Sleep mode entry time EN_RXD H → L			2	µs
$T_{RX.DETECT}$	Rx.Detect start event	Power-up time			100	µs
CONTROL LOGIC						
V_{IH}	High level input voltage		2.8		V_{CC}	V
V_{IL}	Low level input voltage		–0.3		0.5	V
V_{HYS}	Input hysteresis			150		mV
I_{IH}	High level input current	OSx, EQx, DEx = V_{CC}			30	µA
		EN_RXD = V_{CC}			1	
		RSVD = V_{CC}			30	
I_{IL}	Low level input current	OSx, EQx, DEx = GND	–30			µA
		EN_RXD = GND	–30			
		RSVD = GND	–1			

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER AC/DC						
Vin_{diff_p-p}	RX1, RX2 input voltage swing	AC coupled differential RX peak to peak signal	100		1200	mVpp
VCM_RX	RX1, RX2 common mode voltage			3.3		V
Vin_{COM_P}	RX1, RX2 AC peak common mode voltage	Measured at Rx pins with termination enabled			150	mVP
Z_{CM_RX}	DC common mode impedance		18	26	30	Ω
Z_{diff_RX}	DC differential input impedance		72	80	120	Ω
$Z_{RX\_High\_IMP+}$	DC Input high impedance	Device in sleep mode Rx termination not powered measured with respect to GND over 500mV max	50	85		kΩ
$V_{RX-LFPS-DETpp}$	Low frequency periodic signaling (LFPS) detect threshold	Measured at receiver pin, below minimum output is squelched, above max input signal is passed to output	100		300	mVpp
$RL_{RX-DIFF}$	Differential return loss	50 MHz – 1.25 GHz	10	11		dB
		1.25 GH – 2.5 GHz	6	7		
RL_{RX-CM}	Common mode return loss	50 MHz– 2.5 GHz	11	13		dB
TRANSMITTER AC/DC						
$V_{TXDIFF\_TB\_P-P}$	Differential peak-to-peak output voltage (VID = 800, 1200 mVpp, 5 Gbps)	R_L = 100 Ω ±1%, DEx, OSx = NC, **Transition Bit**	900	1241	1500	mV
		R_L = 100 Ω ±1%, DEx = NC, OSx = GND **Transition Bit**		1105		
		R_L = 100 Ω ±1%, DEx = NC, OSx = VCC **Transition Bit**		1324		
$V_{TXDIFF\_NTB\_P-P}$		R_L = 100 Ω ±1%, DEx=NC, OSx = 0,1,NC **Non-Transition Bit**		1241		mV
		R_L = 100 Ω ±1%, DEx=0 OSx = 0,1,NC **Non-Transition Bit**		866		
		R_L = 100 Ω ±1%, DEx=1 OSx = 0,1,NC **Non-Transition Bit**		691		
DE	De-emphasis level OS1,2 = NC (for OS1, 2 = 1 and 0 see Table 2)	DE1/DE2 = NC		0		dB
		DE1/DE2 = 0		–3		
		DE1/DE2 = 1		–5		
T_{DE}	De-emphasis width			0.85		UI
Z_{diff_TX}	DC differential impedance		72	90	120	Ω
Z_{CM_TX}	DC common mode impedance	Measured w.r.t to AC ground over 0-500mV	18	23	30	Ω
RL_{diff_TX}	Differential return loss	f = 50 MHz – 1.25 GHz	9	10		dB
		f = 1.25 GHz – 2.5 GHz	6	7		
RL_{CM_TX}	Common mode return loss	f = 50 MHz – 2.5 GHz	11	12		dB
I_{TX_SC}	TX short circuit current	TX± shorted to GND			60	mA
$V_{TX\_CM\_DC}$	Transmitter DC common-mode voltage	OSx = NC	2.0	2.6	3.0	V
$V_{TX\_CM\_AC\_Active}$	TX AC common mode voltage active			30	100	mVpp
$VT_{X\_idle\_diff-AC-pp}$	Electrical idle differential peak to peak output voltage	HPF to remove DC	0		10	mVpp
$V_{TX\_CM\_DeltaU1-U0}$	Absolute delta of DC CM voltage during active and idle states			35	200	mV
$V_{TX\_idle\_diff-DC}$	DC Electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		10	mV
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise/fall time	20%–80% of differential voltage measured 1" from the output pin	30	65		ps
t_{RF_MM}	Output rise/fall time mismatch	20%–80% of differential voltage measured 1" from the output pin		1.5	20	ps
T_{diff_LH}, T_{diff_HL}	Differential propagation delay	De-Emphasis = –3.5 dB (CH 0 and CH 1). Propagation delay between 50% level at input and output		305	370	ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times	See Figure 4		4	6	ns
C_{TX}	Tx input capacitance to GND	At 2.5 GHz		1.25		pF

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
JITTER						
T_{TX-EYE} (1) (2)	**Total jitter (Tj) at point A**	Device setting: OS1 = L, DE1 = –6 dB, EQ1 = 7 dB		0.23	0.5	UI(3)pp
DJ_{TX} (2)	Deterministic jitter (Dj)			0.14	0.3	
RJ_{TX} (2) (4)	Random jitter (Rj)			0.08	0.2	
T_{TX-EYE} (1) (2)	**Total jitter (Tj) at point B**	Device setting: OS2 = H, DE2 = –6 dB, EQ2 = 7dB		0.15	0.5	UI(3)Pp
DJ_{TX} (2)	Deterministic jitter (Dj)			0.07	0.3	
RJ_{TX} (2) (4)	Random jitter (Rj)			0.08	0.2	

(1) Includes RJ at 10^{-12} BER
(2) Determininstic jitter measured with K28.5 pattern, Random jitter measured with K28.5 pattern at the ends of reference channel in , VID=1000mVpp, 5Gbps, –3.5dB DE from source
(3) UI = 200ps
(4) Rj calculated as 14.069 times the RMS random jitter for 10^{-12} BER

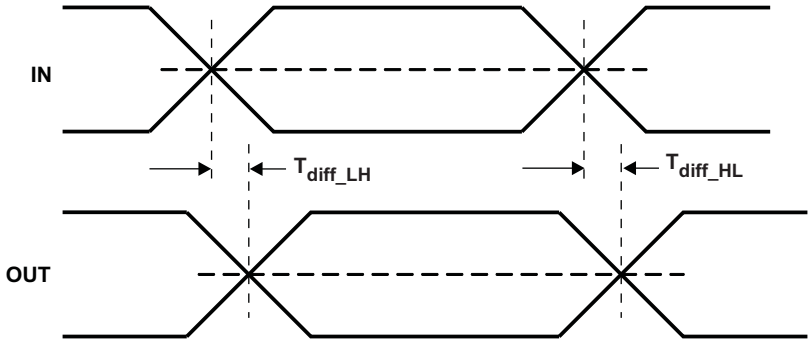


Figure 3. Propagation Delay

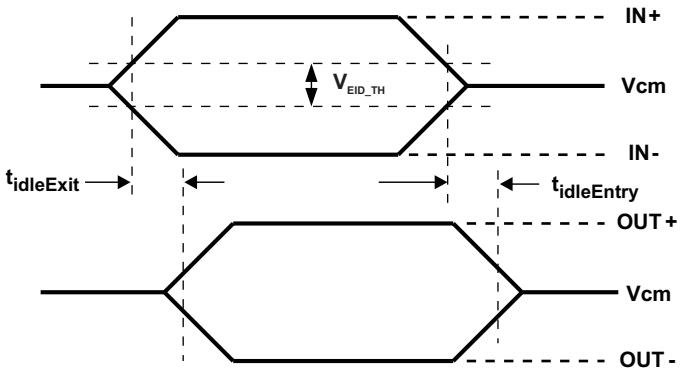


Figure 4. Electrical Idle Mode Exit and Entry Delay

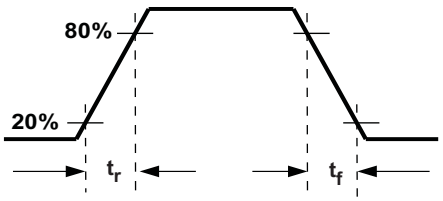


Figure 5. Output Rise and Fall Times

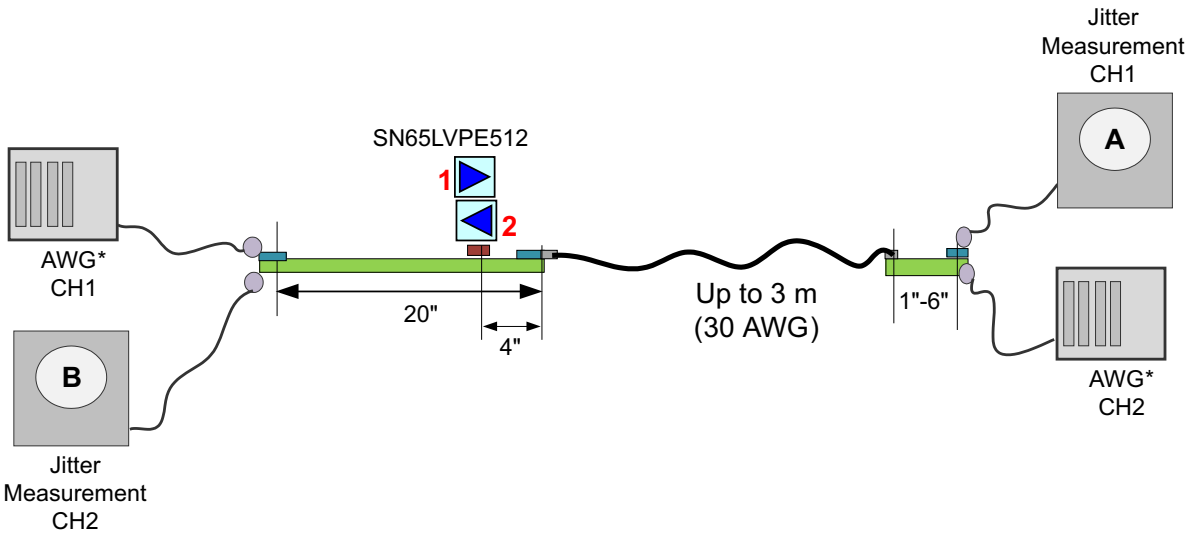


Figure 6. Jitter Measurement Setup

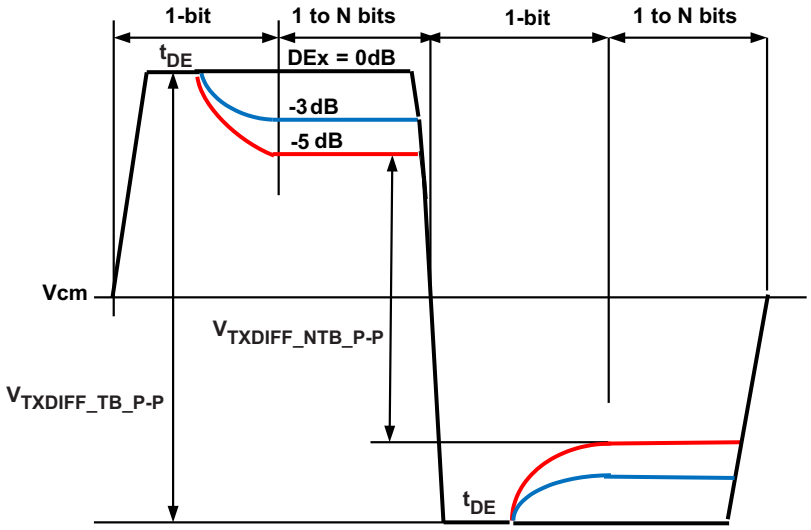
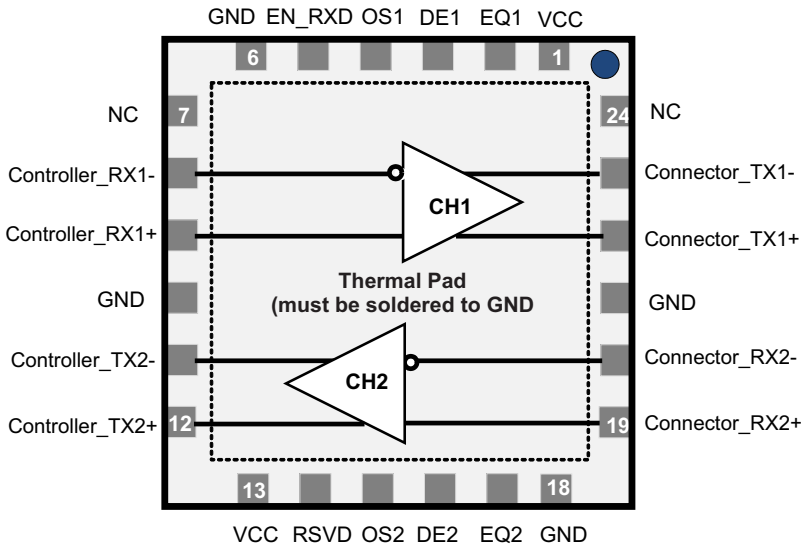


Figure 7. Output De-Emphasis Levels OSx = NC

DEVICE INFORMATION

RGE PACKAGE
(Top View)



RMQ PACKAGE
(Top View)

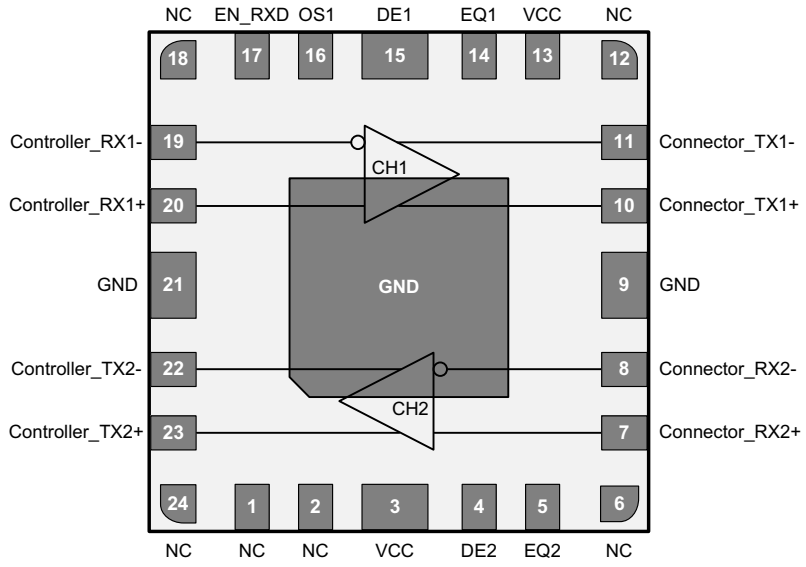


Table 1. Pin Functions

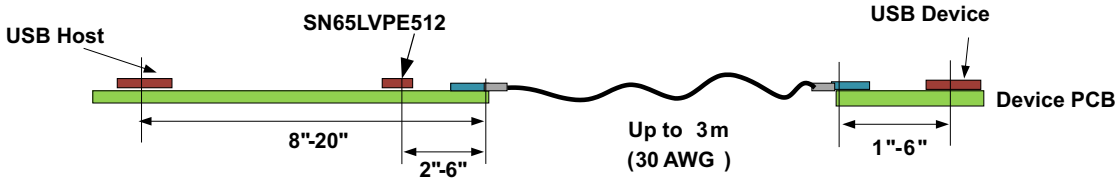
PIN			I/O Type	Description
'LVPE512 RGE	'LVPE512 RMQ	Name		
HIGH SPEED DIFFERENTIAL I/O PINS				
8	19	Controller_RX1–	I, CML	Non-inverting and inverting CML differential input for CH1 and CH2. These pins are tied to an internal voltage bias by dual termination resistor circuit. Pins labeled "Controller" must connect to the USB 3.0 host or device controller. Pins labeled "Connector" must connect to the USB 3.0 connector.
9	20	Controller_RX1+	I, CML	
20	8	Connector_RX2–	I, CML	
19	7	Connector_RX2+	I, CML	
23	11	Connector_TX1–	O, CML	Non-inverting and inverting CML differential output for CH1 and CH2. These pins are tied to an internal voltage bias by termination resistors. Pins labeled "Controller" must connect to the USB 3.0 host or device controller. Pins labeled "Connector" must connect to the USB 3.0 connector.
22	10	Connector_TX1+	O, CML	
11	22	Controller_TX2–	O, CML	
12	23	Controller_TX2+	O, CML	
DEVICE CONTROL PIN				
5	17	EN_RXD	I, LVCMOS	Sets device operation modes per Table 2. Internally pulled to V_{CC}.
14	—	RSVD	I, LVCMOS	RSVD. Can be left as No-Connect.
7, 24	1, 2, 6, 12, 18, 24	NC	No-Connect	Pads are not internally connected.
EQ CONTROL PINS(1)				
3, 16	15, 4	DE1, DE2	I, LVCMOS	Selects de-emphasis settings for CH1 and CH2 per Table 2. Internally tied to $V_{CC}/2$
2, 17	14, 5	EQ1, EQ2	I, LVCMOS	Selects equalization settings for CH1 and CH2 per Table 2. Internally tied to $V_{CC}/2$
4, 15	16, NC (2)	OS1, OS2	I, LVCMOS	Selects output amplitude for CH1 and CH2 per Table 2. Internally tied to $V_{CC}/2$
POWER PINS				
1,13	3	VCC	Power	Positive supply; should be 3.3V ±10%
6, 10, 18, 21, Thermal Pad	9, Thermal Pad	GND	Power	Supply Ground

(1) Internally biased to $V_{CC}/2$ with >200kΩ pull-up/pull-down. When pins are left as NC board leakage at this pin pad must be < 1 µA otherwise drive to Vcc/2 to assert mid-level state
(2) The RMQ has OS2 internally No-Connect, to select the 1042 mVpp level on TX2.

Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx	**TRANSISTION BIT AMPLITUDE (TYP mVpp)**	**EQx**	**EQUALIZATION (dB)**
NC (default)	1241	NC (default)	0
0	1105	0	7
1	1324	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DEx(1)	**OSx(1) = NC**	**OSx(1) = 0**	**OSx(1) = 1**
NC (default)	0 dB	0 dB	0 dB
0	–3 dB	–2 dB	–4 dB
1	–5 dB	–4 dB	–5.6 dB
CONTROL PINS SETTINGS			
EN_RXD	**DEVICE FUNCTION**		
1 (default)	Normal Operation		
0	Sleep Mode		

(1) Where x = Channel 1 or Channel 2



NOTE: For more detailed placement example of redriver see typical eye diagrams and jitter plots at end of data sheet.

Figure 8. Redriver Placement Example

DETAILED DESCRIPTION

Controller- and Connector-side Pins

The SN65LVPE512 features a link state machine that makes the device transparent on the USB 3.0 bus while minimizing power. The state machine relies on the system host or device controller to be connected to the pins named “Controller”. The pins labeled connector should be connected to the USB 3.0 receptacle or captive cable. Multiple SN65LVPE512 devices may be used in series.

Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE512 is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion USB 3.0 signal will experience. Level of de-emphasis will depend on the length of interconnect and its characteristics. The SN65LVPE512 provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All Rx and Tx equalization settings supported by the device are programmed by six 3-state pins as shown in Table 2.

Low Power Modes

Device supports three low power modes as described below

1. Sleep Mode

   Initiated anytime EN_RXD undergoes a high to low transition and stays low or when device powers up with EN_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode max power consumption is 1mW, entry time is 2µs, device exits sleep mode to Rx.Detect mode after EN_RXD is driven to Vcc, exit time is 100µs max.

2. RX Detect Mode--When no remote device is connected

   Anytime 'LVPE512 detects a break in link (that is, when upstream device is disconnected) or after power-up fails to find a remote device, 'LVPE512 goes to Rx Detect mode and conserves power by shutting down majority of its internal circuitry. In this mode, input termination for both channels are driven to Hi-Z. In Rx Detect mode device power is < 10mW (TYP) or less than 5% of its normal operating power. This feature is very useful in saving system power in mobile applications like notebook PC where battery life is critical.

   Anytime an upstream device gets reconnected the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.

3. U2/U3 Mode

   With the help of internal timers the device tracks when link enters USB 3.0 low power modes U2 and U3; in these modes link is in electrical idle state. 'LVPE512 will selectively turn-off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device will automatically revert to active mode when signal activity (LFPS) is detected.

Receiver Detection

At Power Up or Reset

After power-up or anytime EN_RXD is toggled, RX.Detect cycle is performed by first setting Rx termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If receiver is detected on both channel

- The TX and RX terminations are switched to Z_{DIFF_TX}, Z_{DIFF_RX} respectively.

If no receiver is detected on one or both channels

- The transmitter is pulled to Hi-Z
- The channel is put in low power mode
- Device attempts to detect Rx termination in 12 ms (TYP) interval until termination is found or device is put in sleep mode

During U2, U3 Link State

Rx detection is also performed periodically when link is in U2/U3 states. However in these states during Rx detection, input termination is not automatically disabled before performing Rx.Detect. If termination is found device goes back to its low power state if termination is not found then device disables its input termination and then jumps to power-up RX.Detect state.

Electrical Idle Support

Electrical idle support is needed for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. 'LVPE512 detects an electrical idle state when RX± voltage at the device pin falls below VRX_LFPS_DIFFp-p min. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds VRX_LFPS_DIFFp-p max normal operation is restored and output start passing input signal. Electrical idle exit and entry time is specified at < 6ns.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVPE512RGER	NRND	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVPE 512
SN65LVPE512RGER.B	NRND	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVPE 512
SN65LVPE512RMQR	NRND	Production	WQFN (RMQ) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN512
SN65LVPE512RMQR.B	NRND	Production	WQFN (RMQ) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN512

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

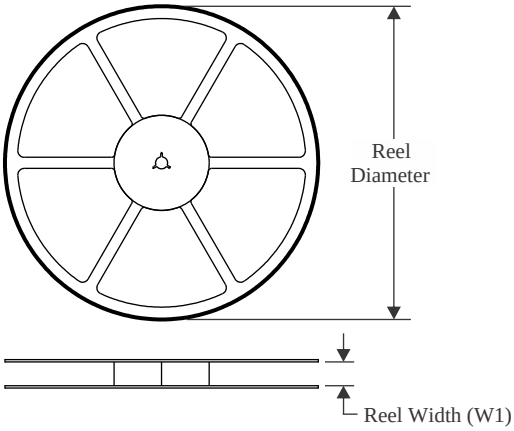
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

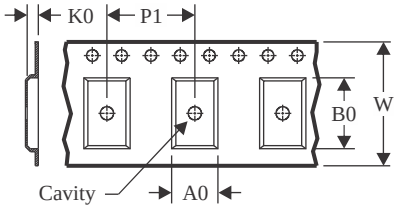
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

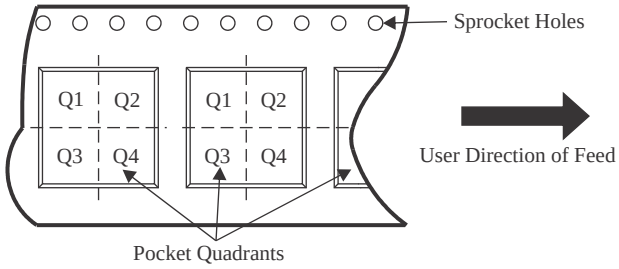


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

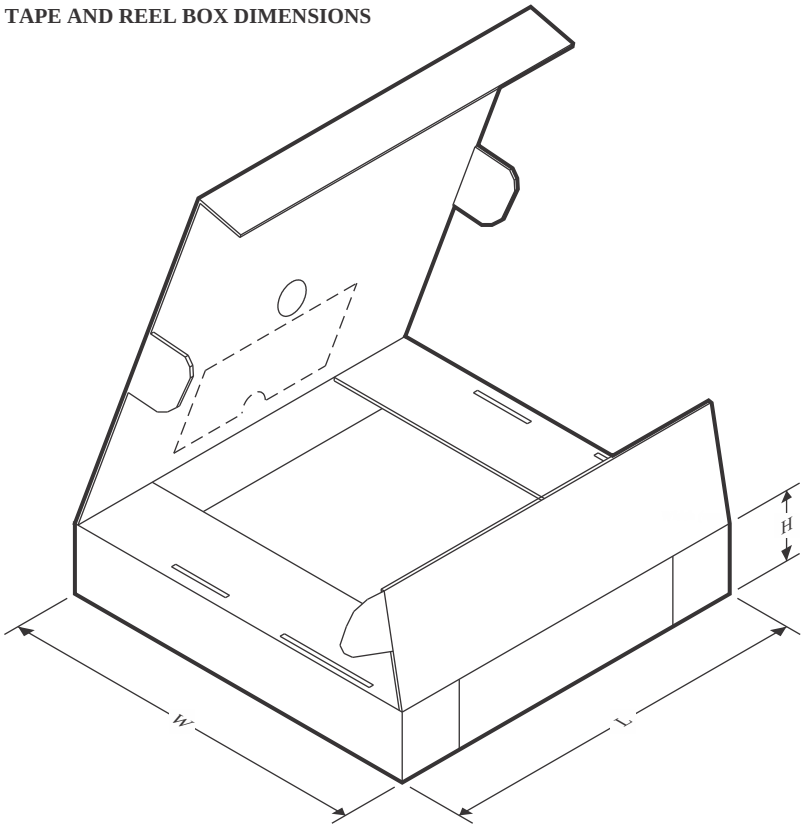
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE512RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVPE512RMQR	WQFN	RMQ	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



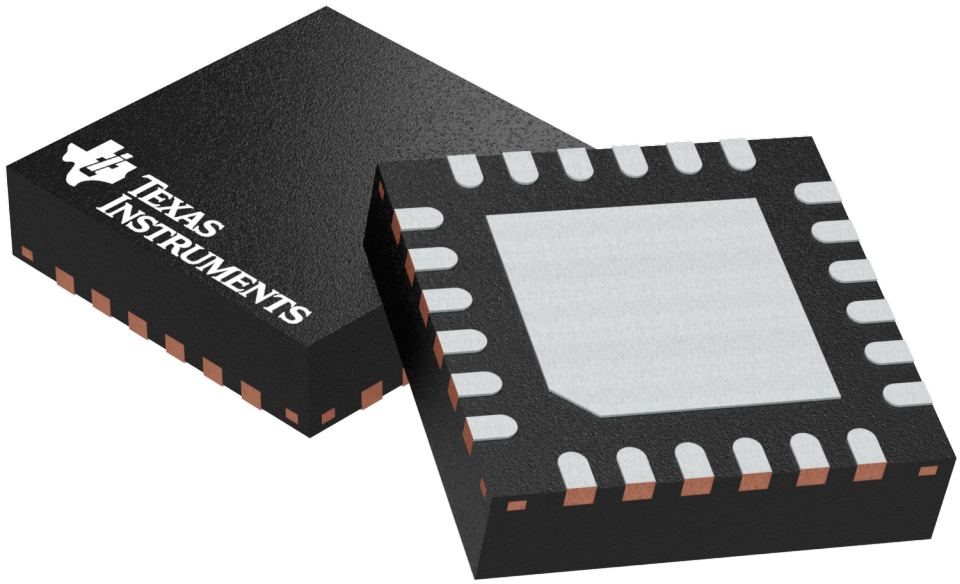
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE512RGER	VQFN	RGE	24	3000	353.0	353.0	32.0
SN65LVPE512RMQR	WQFN	RMQ	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

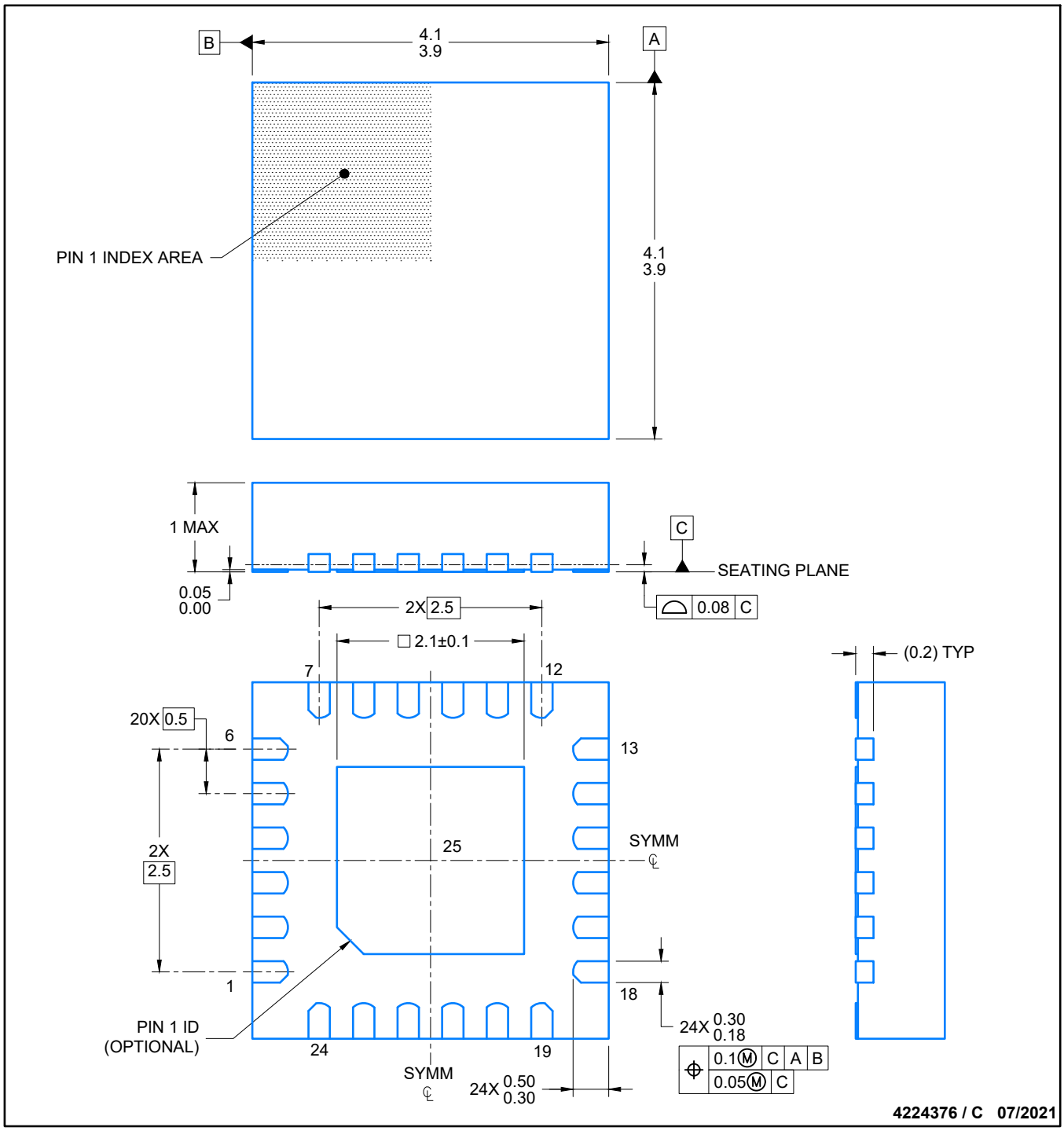
4204104/H

PACKAGE OUTLINE

RGE0024C

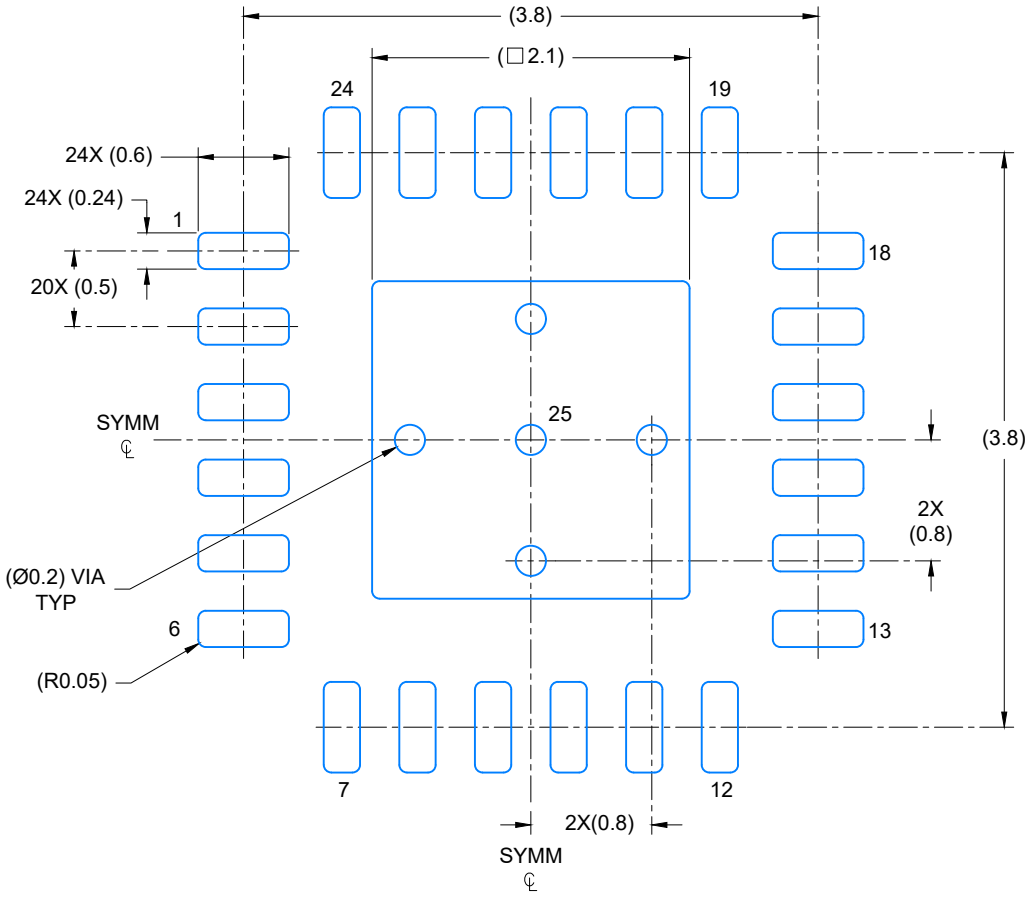
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



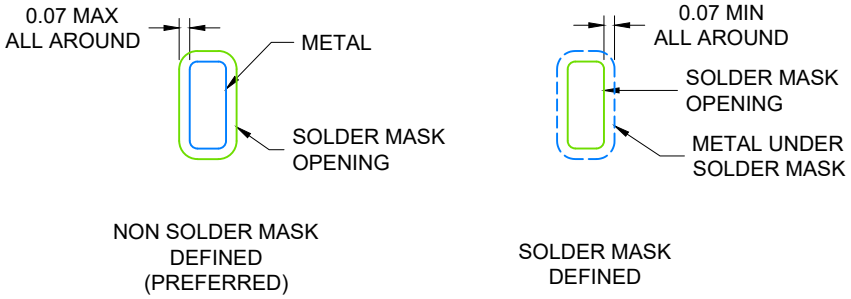
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

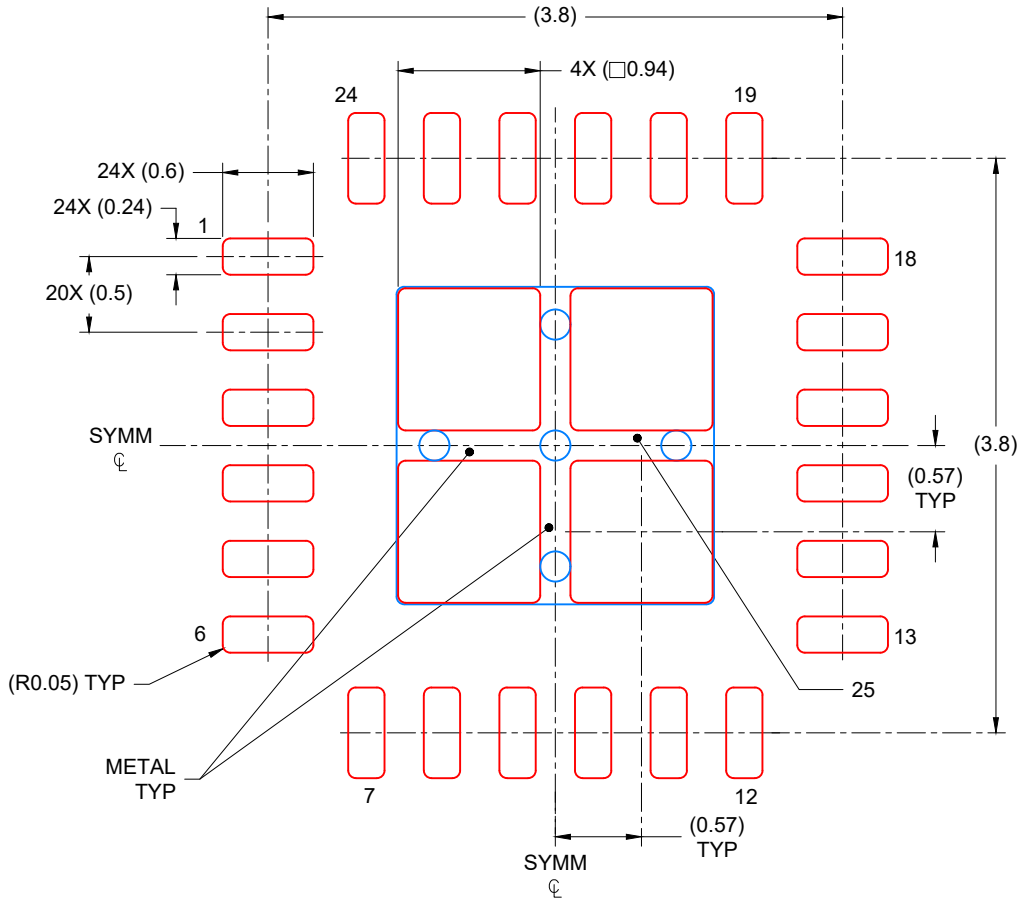


SOLDER MASK DETAILS

4224376 / C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

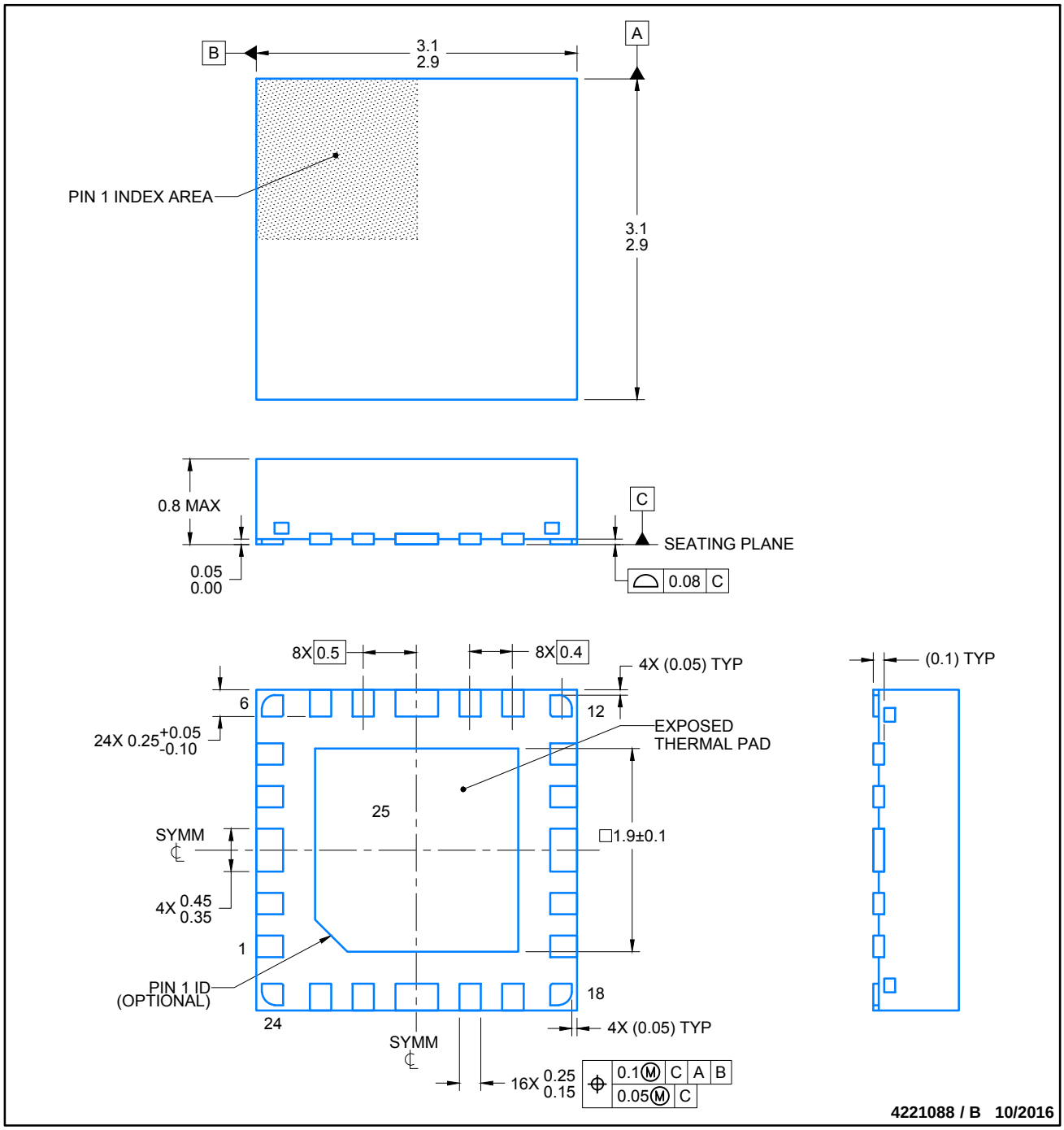
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGE OUTLINE

RMQ0024A

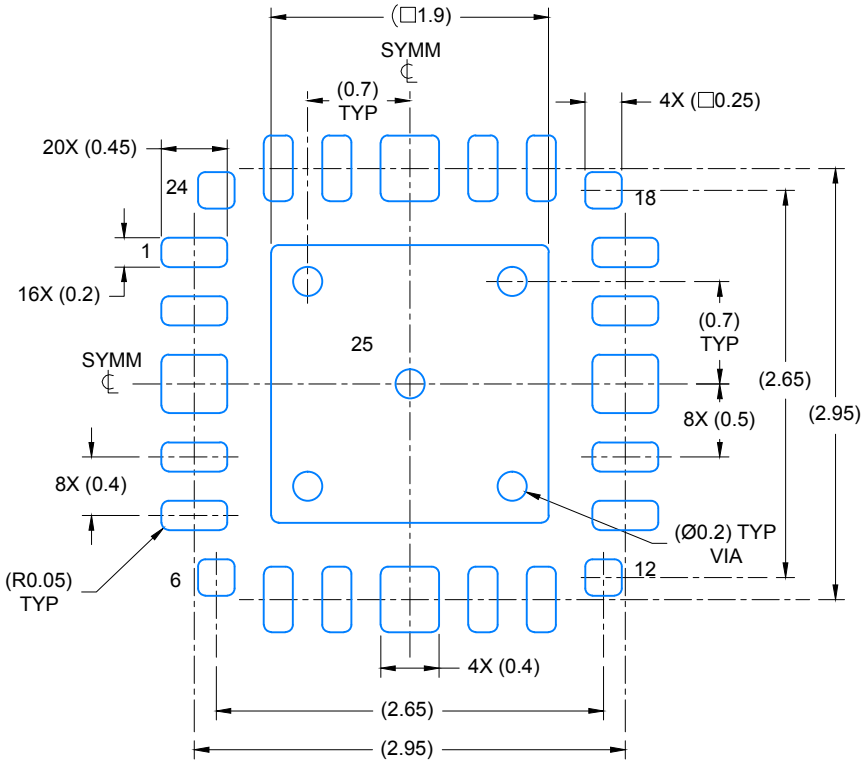
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



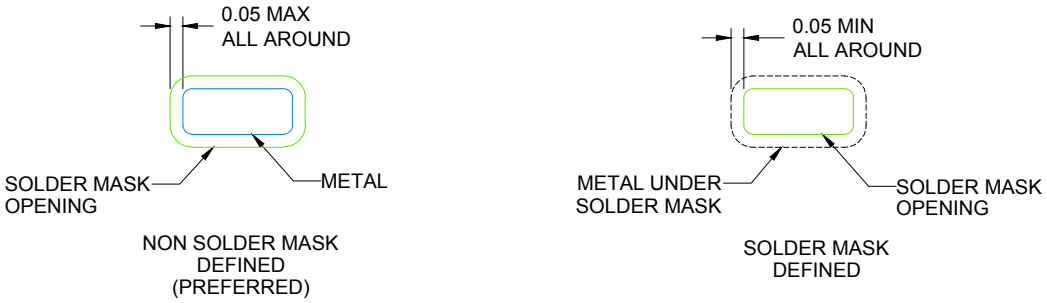
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

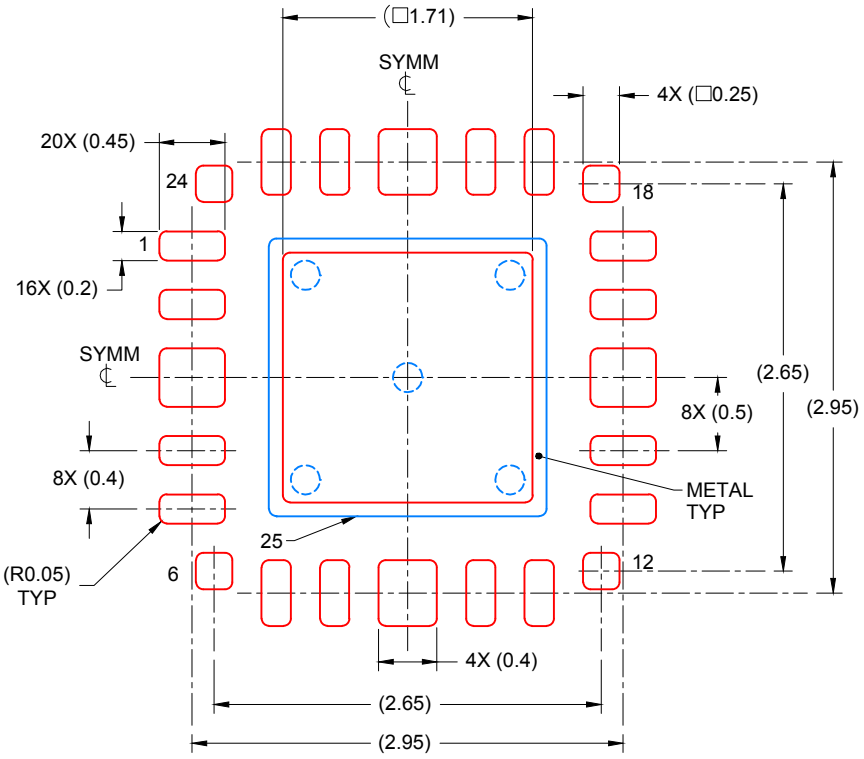


SOLDER MASK DETAILS

4221088 / B 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4221088 / B 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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最后更新日期：2025 年 10 月