SN74AC564 具有三态输出的八路边沿触发式 D 型触发器

1 特性

- 工作范围为 2V 至 6V V_{CC}
- 输入电压高达 6V
- 电压为 5V 时，t_{pd} 最大值为 9ns
- 三态反相输出直接驱动总线
- 针对负载的完全并行访问
- 采用直通架构来优化 PCB 布局

2 说明

’AC564 器件是八路边沿触发式 D 型触发器，具有专门设计用于驱动高容性或较低阻抗负载的反相三态输出。它们尤其适用于实现缓冲寄存器、I/O 端口、双向总线驱动器和工作寄存器。

封装信息

器件型号	封装(1)	封装尺寸(2)	封装尺寸(3)
SN74AC564	DB（SSOP，20）	7.2mm x 7.8mm	7.2mm x 5.30mm
	DW（SOIC，20）	12.80mm x 10.3mm	12.80mm x 7.50mm
	N（PDIP，20）	24.33mm x 9.4mm	24.33mm x 6.35mm
	PW（TSSOP，20）	6.50mm x 6.4mm	6.50mm x 4.40mm

(1) 有关更多信息，请参阅第 10 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。

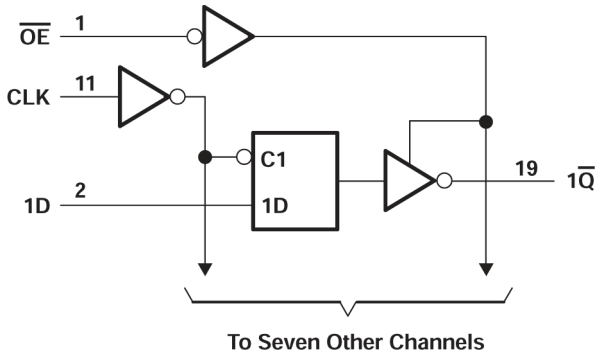


Table of Contents

3 Pin Configuration and Functions

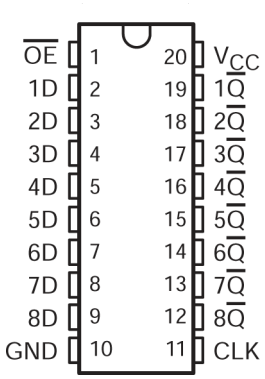


图 3-1. SN74AC564 DB, DW, N, NS, or PW Package (Top View)

表 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	Input	Output enable for all channels, active low
D1	2	Input	Input for channel 1
D2	3	Input	Input for channel 2
D3	4	Input	Input for channel 3
D4	5	Input	Input for channel 4
D5	6	Input	Input for channel 5
D6	7	Input	Input for channel 6
D7	8	Input	Input for channel 7
D8	9	Input	Input for channel 8
GND	10	—	Ground
CLK	11	Input	Clock input for all channels, rising edge triggered
Q8	12	Output	Output for channel 8
Q7	13	Output	Output for channel 7
Q6	14	Output	Output for channel 6
Q5	15	Output	Output for channel 5
Q4	16	Output	Output for channel 4
Q3	17	Output	Output for channel 3
Q2	18	Output	Output for channel 2
Q1	19	Output	Output for channel 1
V_{CC}	20	—	Positive supply

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I [2]	Input voltage range		−0.5	V_{CC} + 0.5	V
V_O [2]	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

(over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		−12	mA
		V_{CC} = 4.5 V		−24	
		V_{CC} = 5.5 V		−24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
Δt/Δv	Input transition rise or fall rate			8	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC(1)		SN74AC564					UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	58	69	60	126.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN74AC564		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −12 mA	3 V	2.56			2.46		
	I_{OH} = −24 mA	4.5 V	3.86			3.76		
		5.5 V	4.86			4.76		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	µA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF

4.5 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T_A = 25°C		SN74AC564		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		75		60	MHz
t_w	Pulse duration, CLK high or low	6		7		ns
t_{su}	Setup time, data before CLK ↑	2.5		3		ns
t_h	Hold time, data after CLK ↑	2		2		ns

4.6 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T_A = 25°C		SN74AC564		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		95		85	MHz
t_w	Pulse duration, CLK high or low	4		5		ns
t_{su}	Setup time, data before CLK ↑	2		2.5		ns

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T_A = 25°C		SN74AC564		UNIT
		MIN	MAX	MIN	MAX	
t_h	Hold time, data after CLK ↑	2		2		ns

4.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN74AC564		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			75			60		MHz
t_{PLH}	CLK	$\overline{Q}$	3.5	8.1	14	3.5	15.5	ns
t_{PHL}			3.5	8.2	12.5	3.5	14	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	2.5	7.2	11.5	2.5	12.5	ns
t_{PZL}			3	7.7	11	3.5	12	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	4	8.6	12.5	4.5	13.5	ns
t_{PLZ}			2	7.3	9.5	2.5	10.5	

4.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

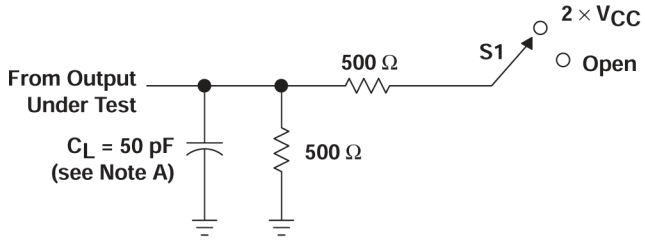
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN74AC564		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			95			85		MHz
t_{PLH}	CLK	$\overline{Q}$	2	4.9	10.5	2	11.5	ns
t_{PHL}			2	5	9.5	2	10.5	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	2	5.1	9	2	9.5	ns
t_{PZL}			1.5	5.2	8.5	2	9.5	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2	5.7	10.5	2	11.5	ns
t_{PLZ}			1.5	4.8	8	1.5	9	

4.9 Operating Characteristics

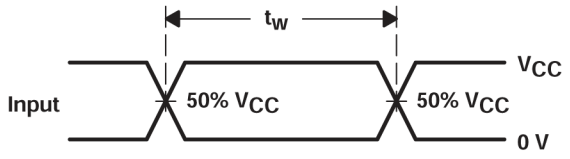
V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	50	pF

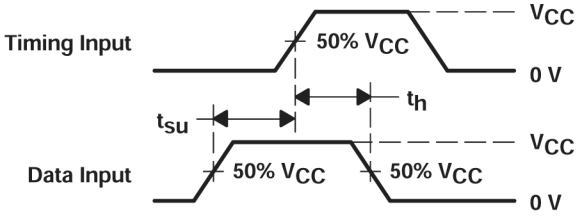
5 Parameter Measurement Information



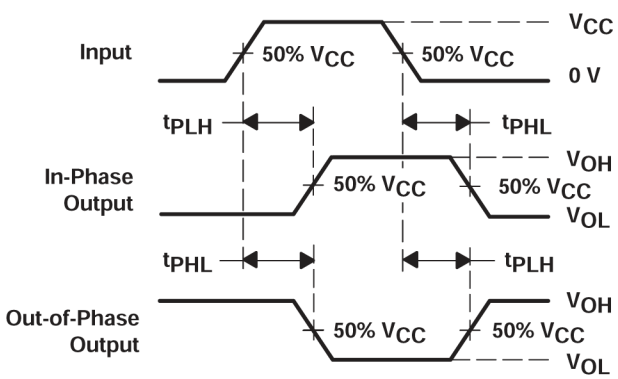
LOAD CIRCUIT



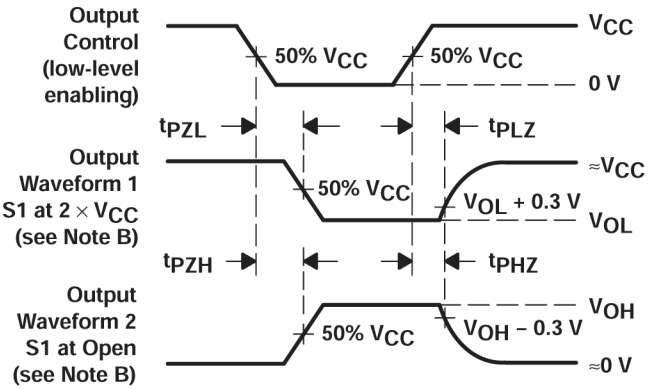
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_r ⩽ 2.5 ns, t_f ⩽ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

图 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

6 Detailed Description

6.1 Overview

On the positive transition of the clock (CLK) input, the $\overline{Q}$ outputs are set to the inverse logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For the specified high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram

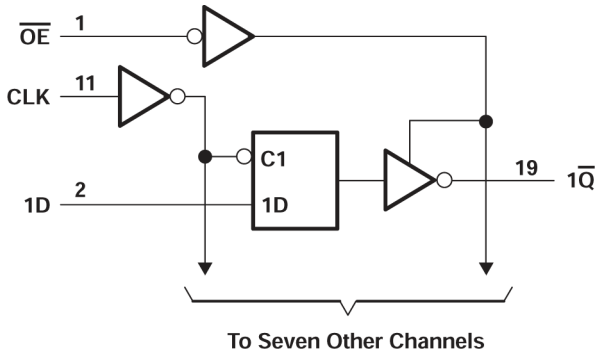


图 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

表 6-1. Function Table (Each Flip-flop)

INPUTS			OUTPUT $\overline{Q}$
$\overline{OE}$	CLK	D	
L	↑	H	L
L	↑	L	H
L	H or L	X	Q_0
H	X	X	Z

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01- μ F or 0.022- μ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

7.2 Layout

7.2.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. Layout example for the SN74AC564 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

7.2.2 Layout Example

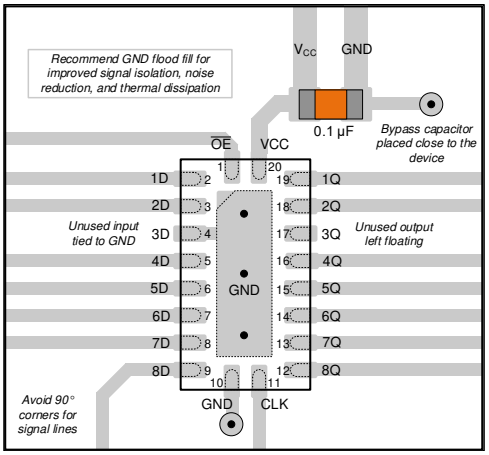


图 7-1. Layout example for the SN74AC564

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AC564	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (August 2023) to Revision F (February 2024)	Page
• Updated R θ JA value: PW = 83 to 126.2, all values in °C/W	5

Changes from Revision D (October 2003) to Revision E (August 2023)	Page
• 添加了*封装信息* 表、*引脚功能* 表、*热信息* 表、*器件功能模式*、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC564DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC564	Samples
SN74AC564DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC564	Samples
SN74AC564DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC564	Samples
SN74AC564N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC564N	Samples
SN74AC564PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC564	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

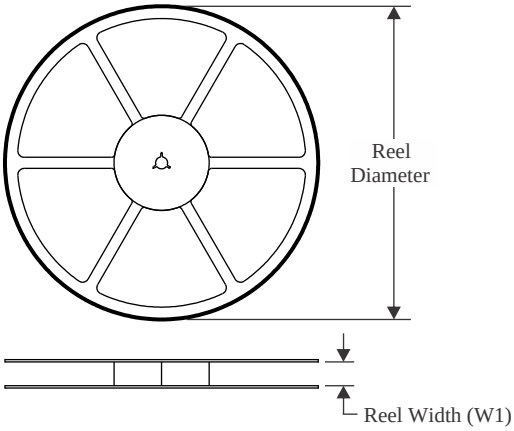
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

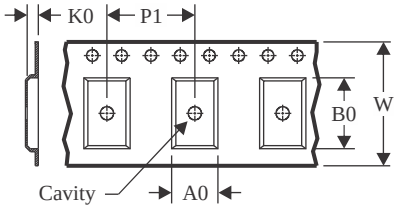
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

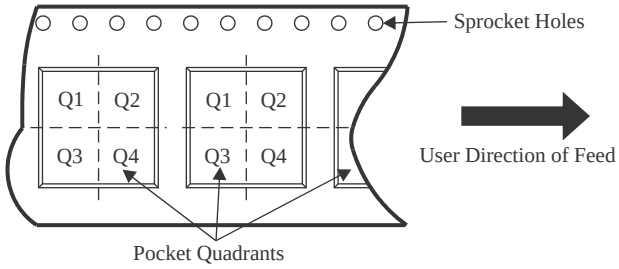


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

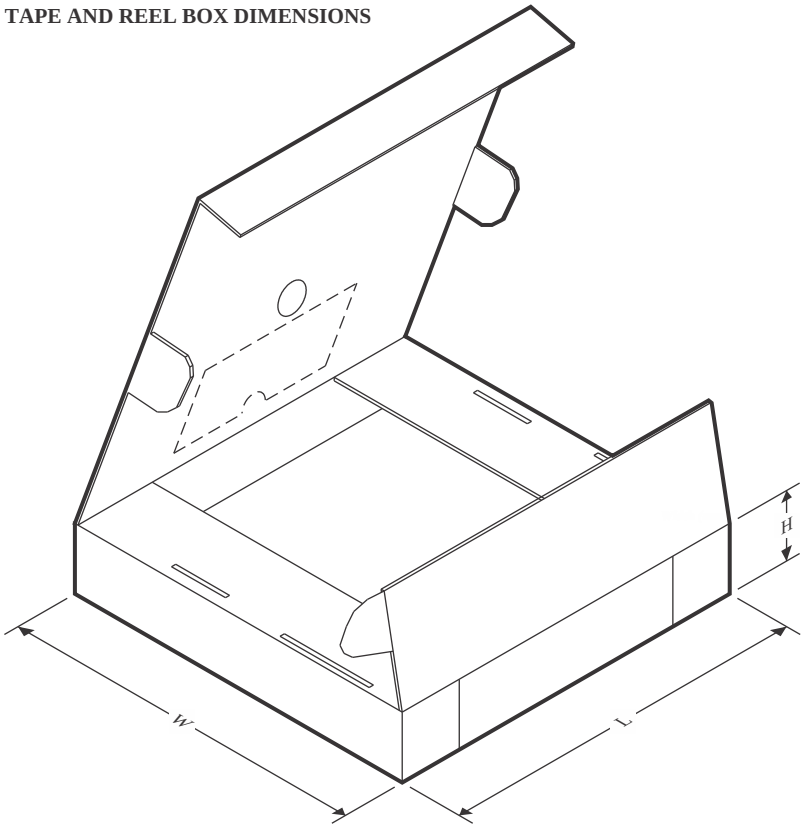
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC564DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC564PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

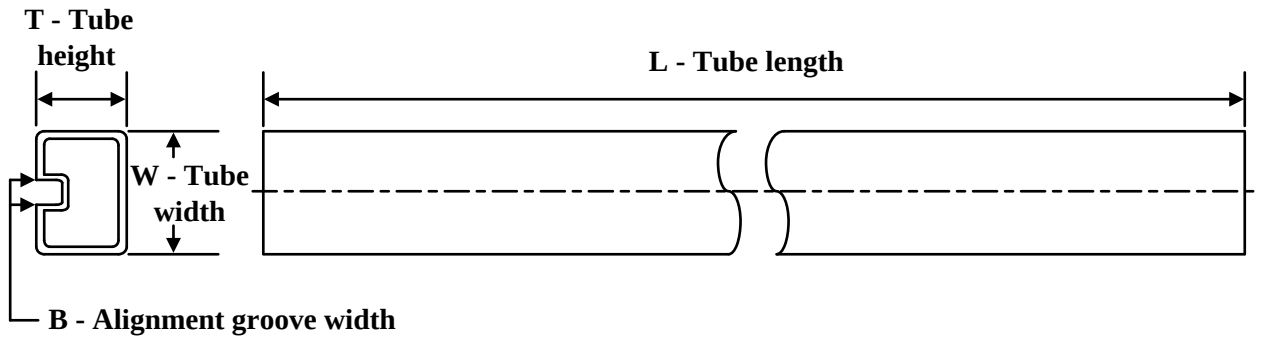
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC564DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AC564PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

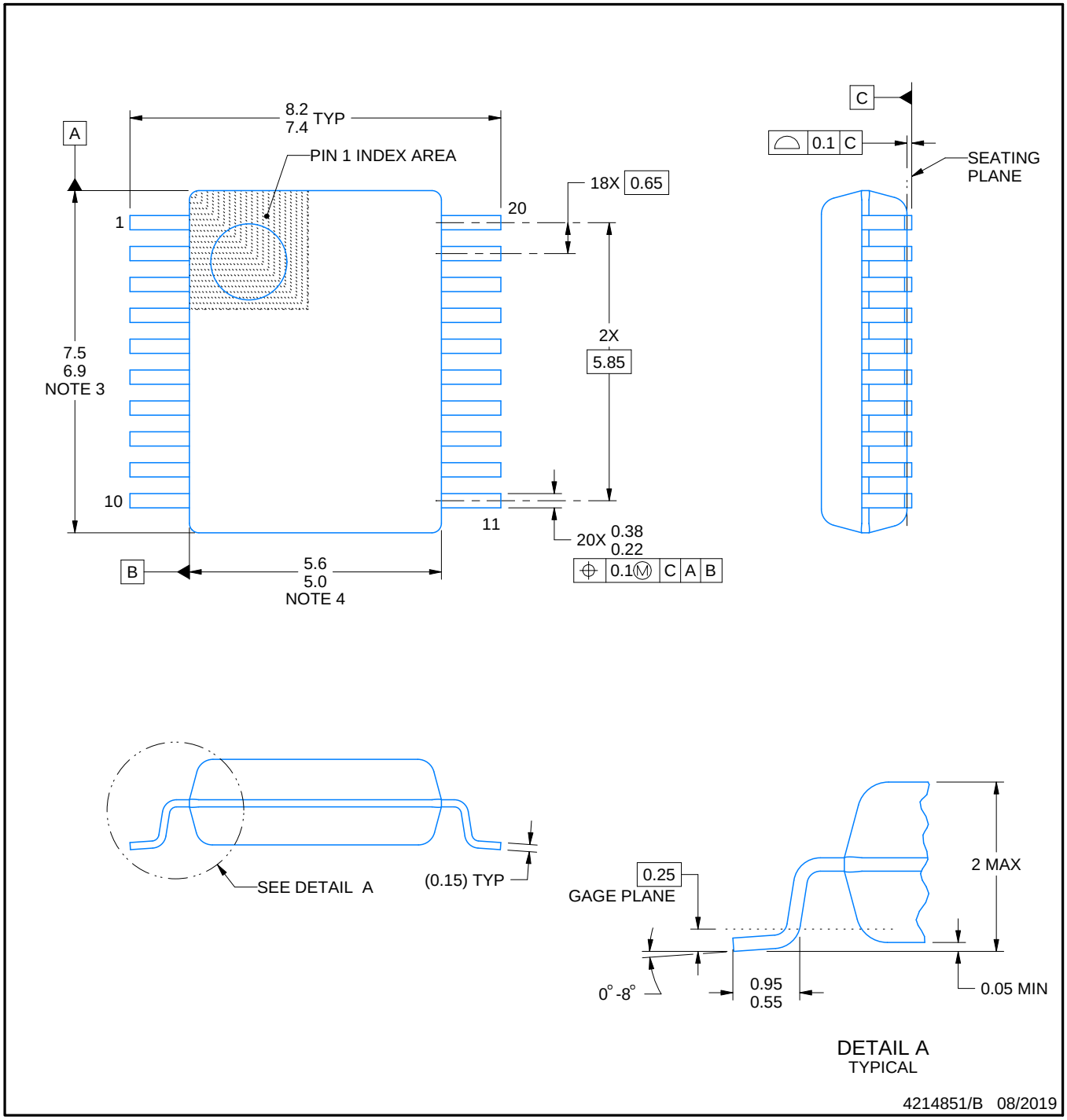
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AC564DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AC564DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AC564N	N	PDIP	20	20	506	13.97	11230	4.32

PACKAGE OUTLINE

DB0020A

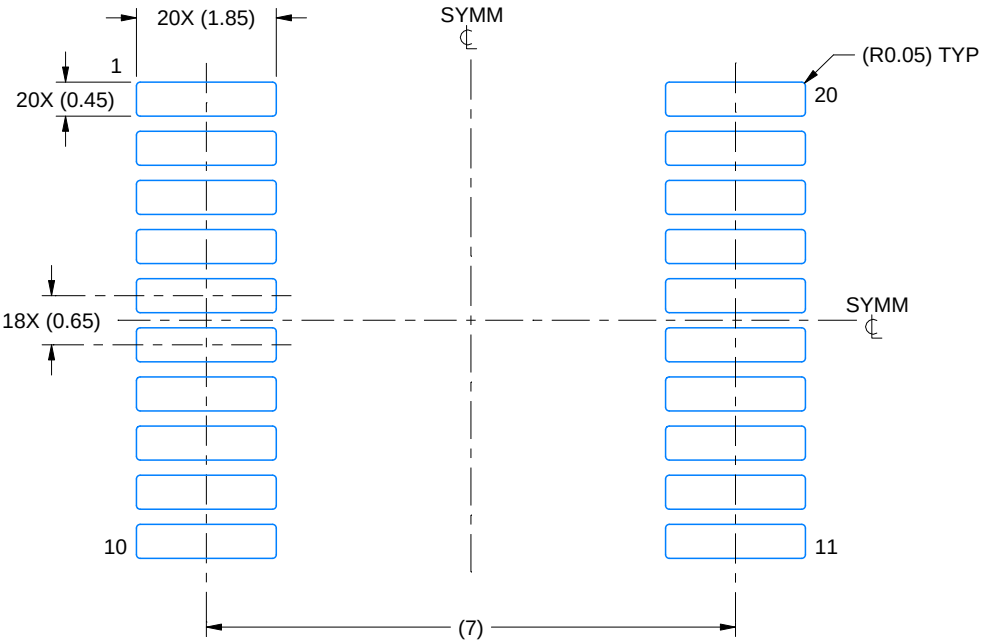
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

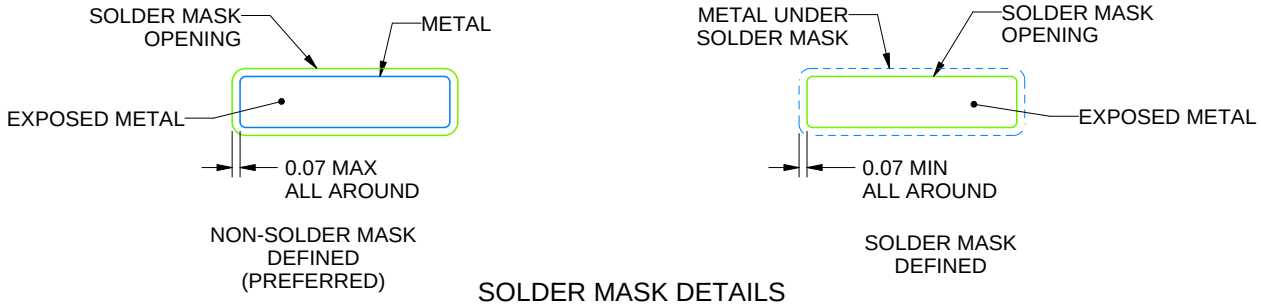


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

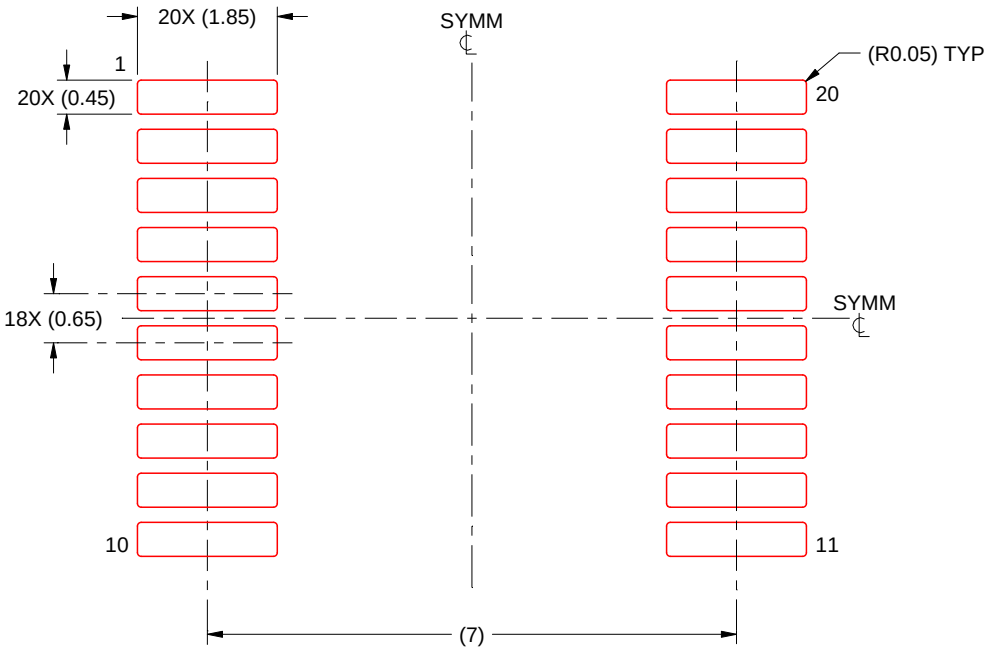
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

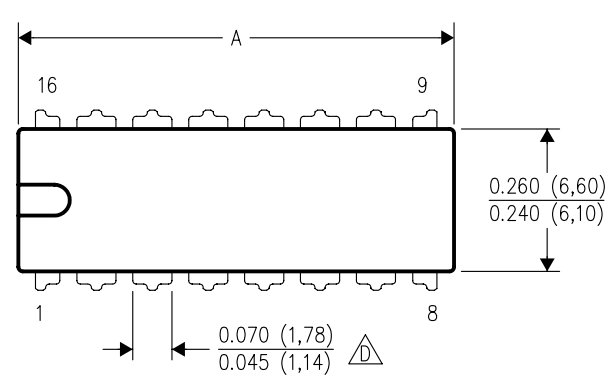
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

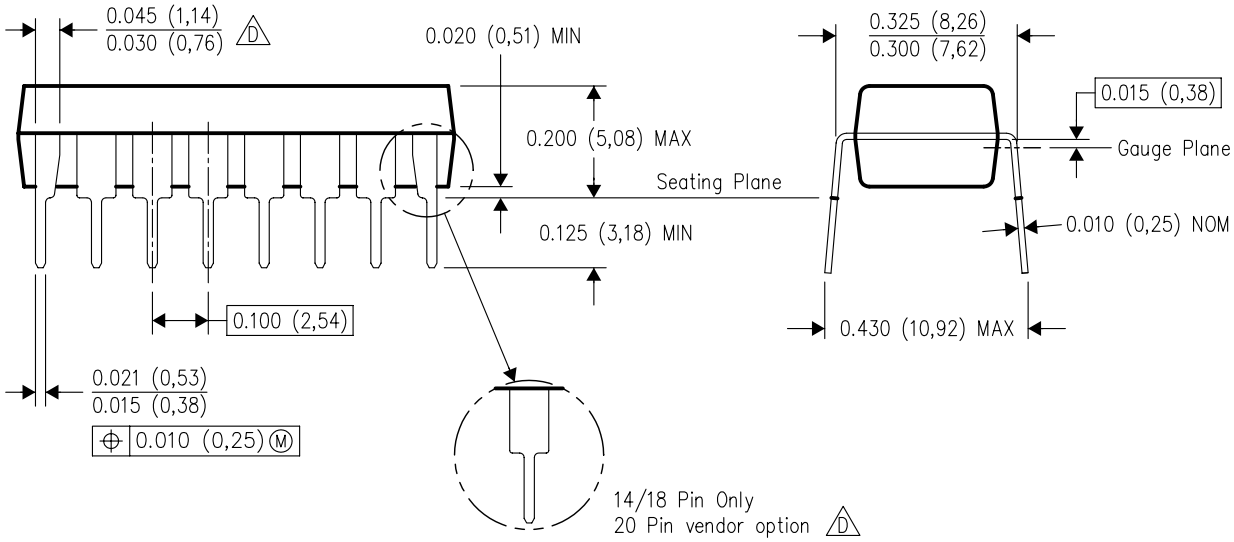
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

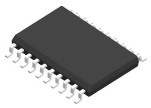


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

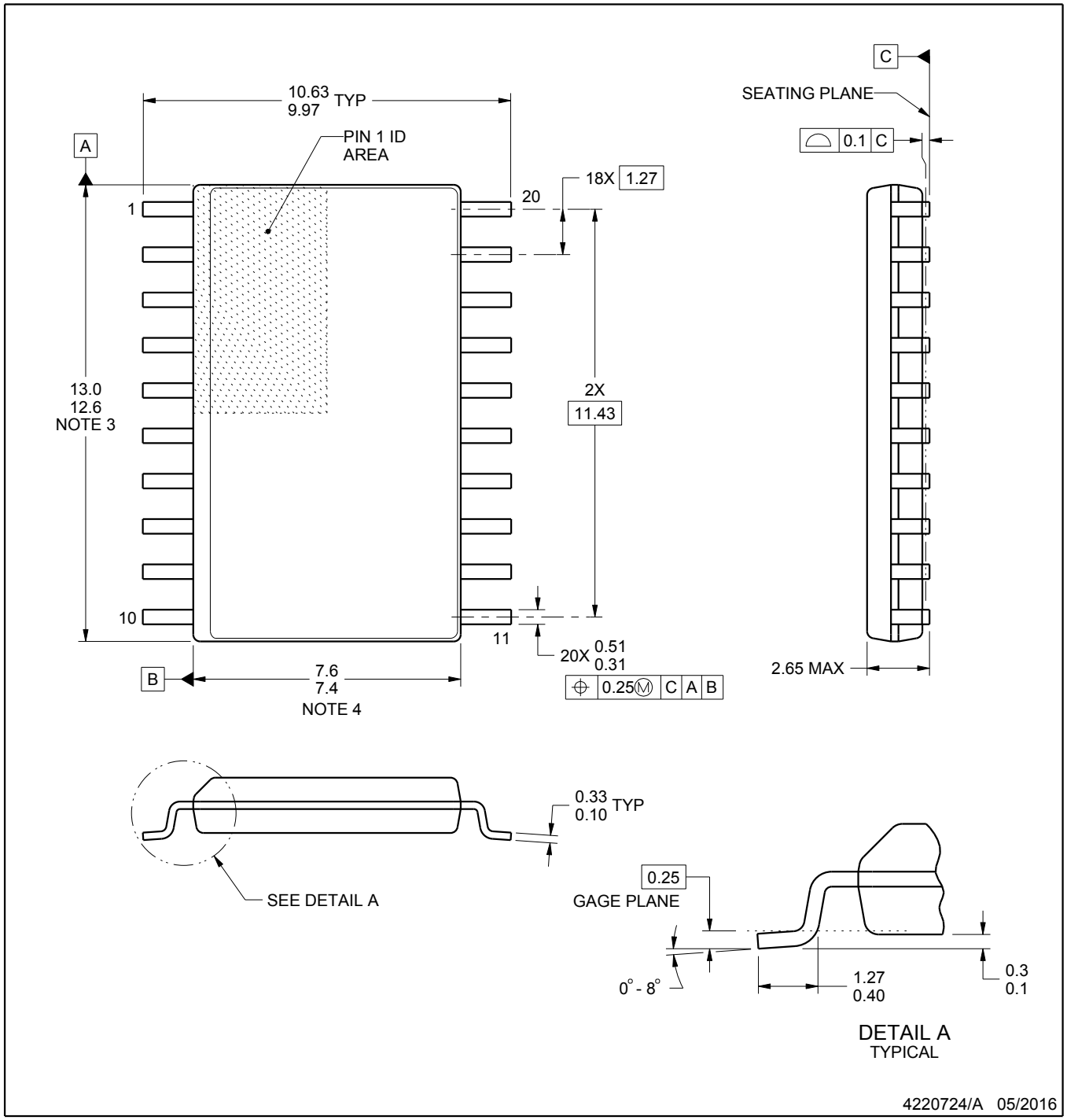


PACKAGE OUTLINE

DW0020A

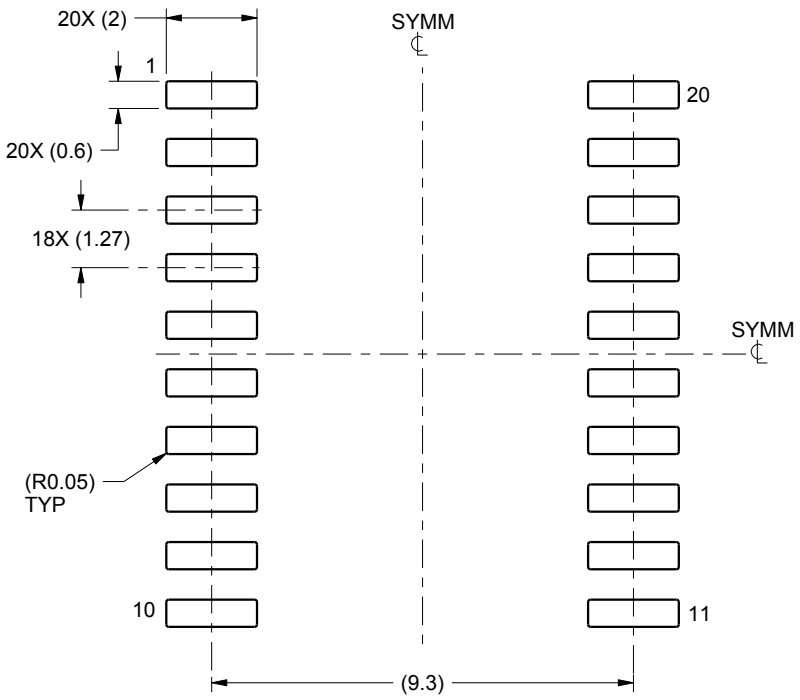
SOIC - 2.65 mm max height

SOIC

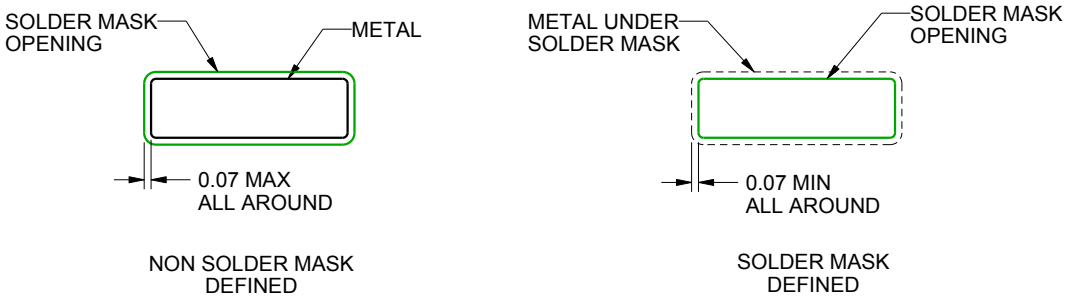


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

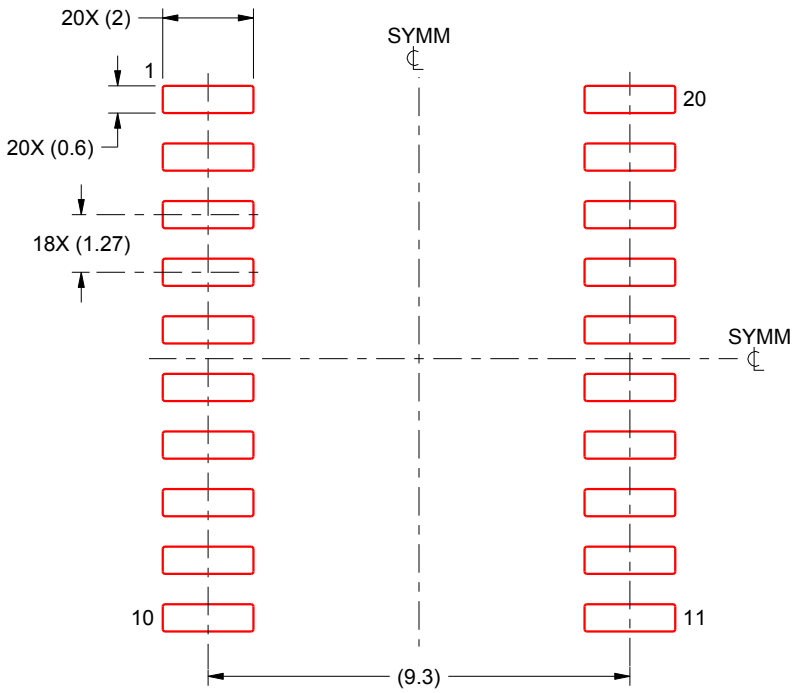


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

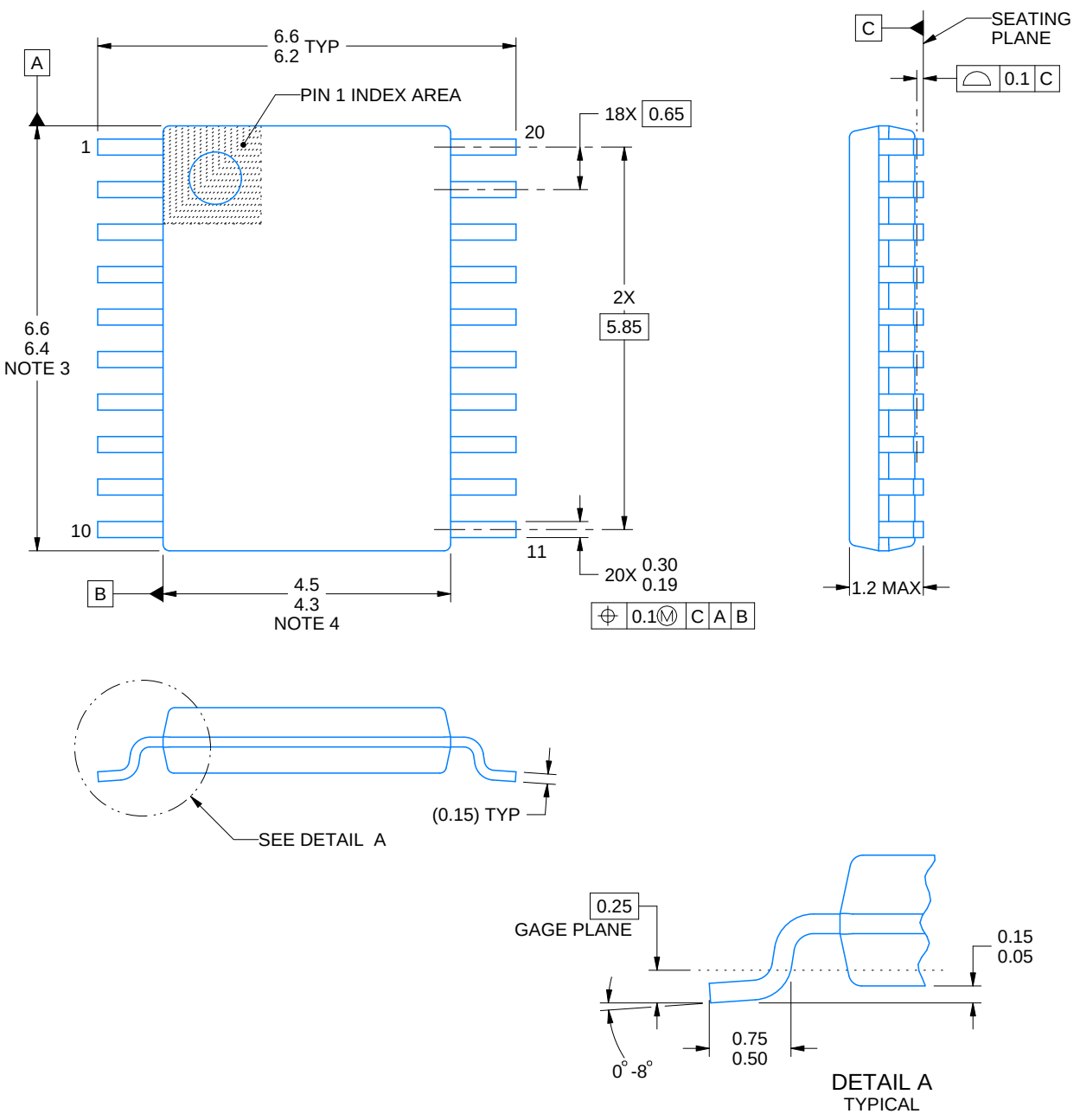
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

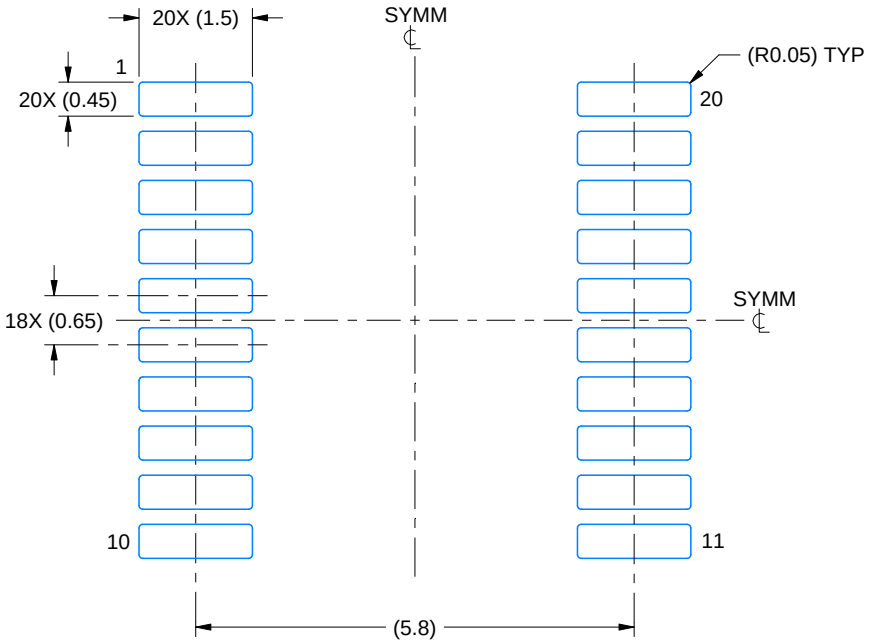
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



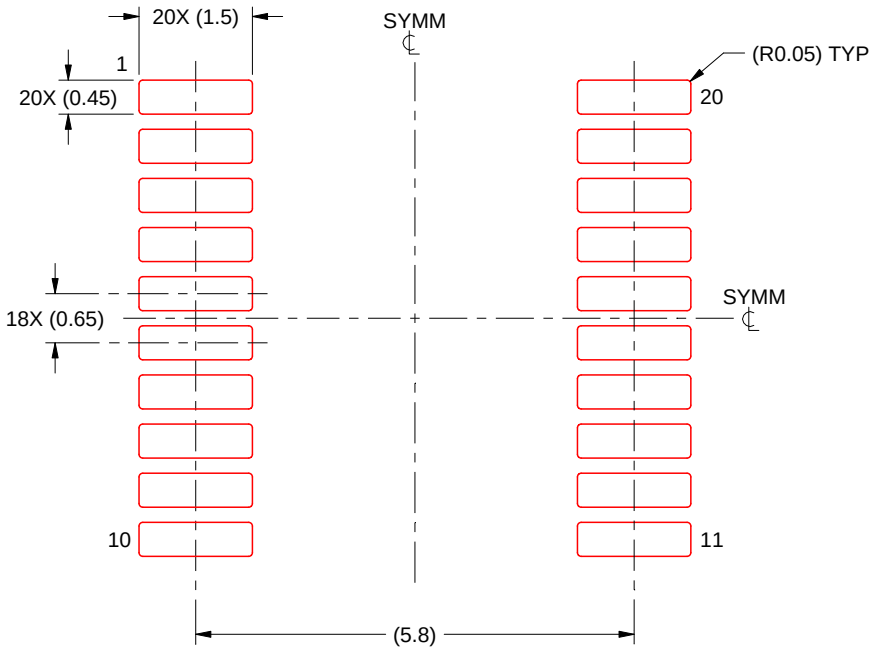
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



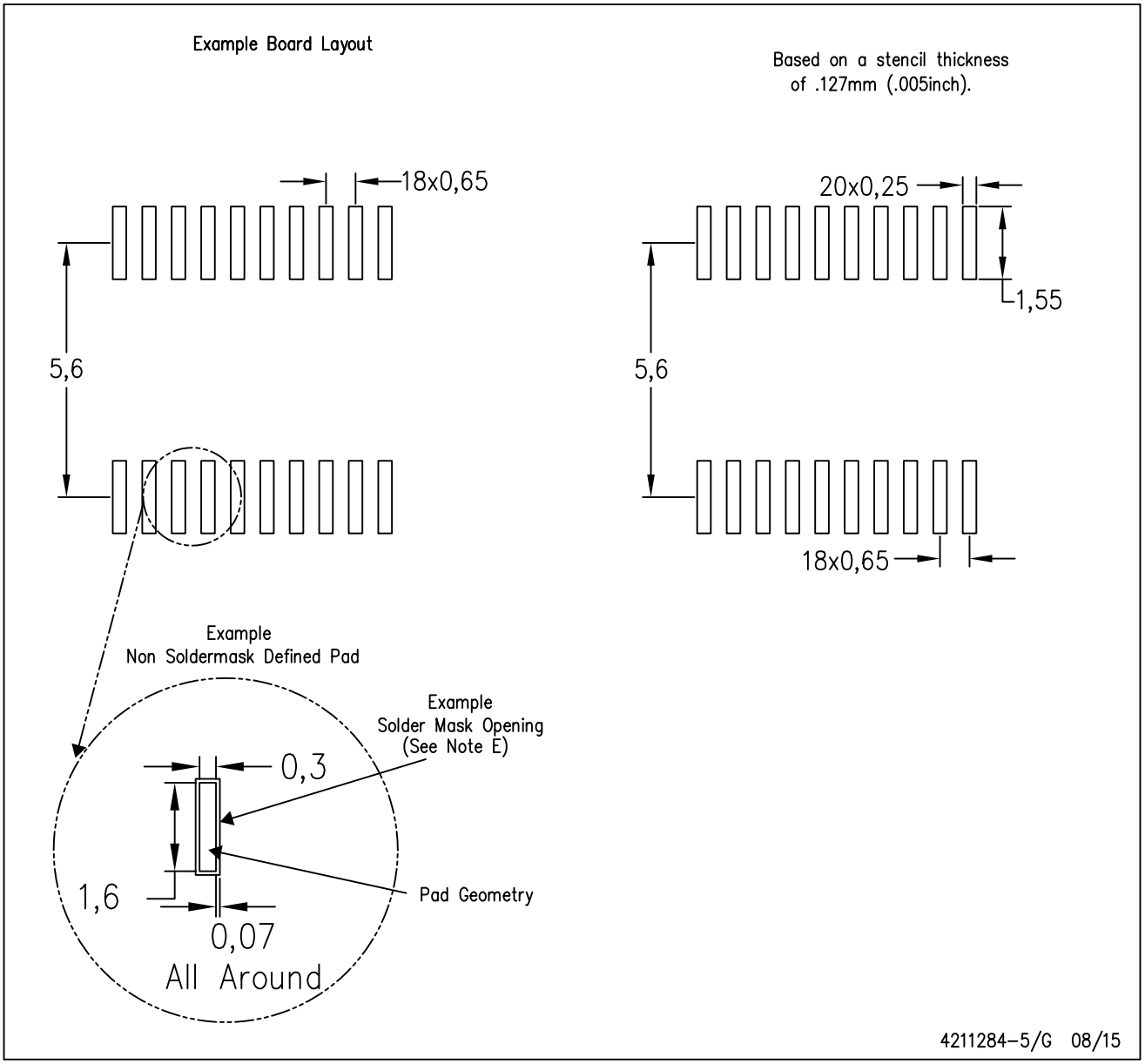
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265