SNx4AHC244 具有三态输出的八路缓冲器/驱动器

1 特性

- 在 2V 至 5.5V V_{CC} 范围内运行
- 闩锁性能超过 250mA，符合 JESD 17 规范
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 网络交换机
- 电力基础设施
- PC 和笔记本电脑
- 可穿戴保健和健身设备
- 测试和测量

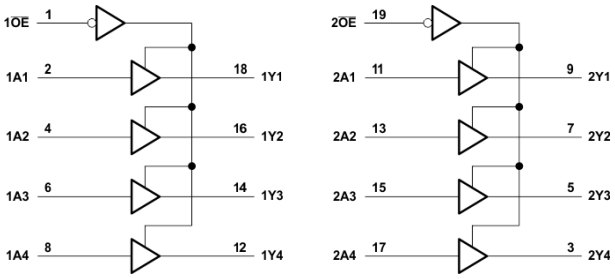
3 说明

这些八通道缓冲器和驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SN54AHC244	J（CDIP，20）	24.2mm x 7.62mm	24.2mm x 6.92mm
	W（CFP，20）	13.09mm x 8.13mm	13.09mm x 6.92mm
	FK（LCCC，20）	8.89mm x 8.89mm	8.89mm x 8.89mm
SN74AHC244	DB（SSOP，20）	7.2mm × 7.8mm	7.50mm x 5.30mm
	DW（SOIC，20）	12.80mm × 10.3mm	12.8mm x 7.5mm
	N（PDIP，20）	24.33mm x 9.4mm	25.40mm x 6.35mm
	NS（SOP，20）	12.60mm x 7.8mm	12.6mm x 5.30mm
	DGV（TVSOP，20）	5.00mm x 6.4mm	5.00mm x 4.40mm
	PW（TSSOP，20）	6.50mm × 6.4mm	6.50mm x 4.40mm
	DGS（VSSOP，20）	5.10mm × 4.90mm	5.10mm × 3.00mm
	RKS（VQFN，20）	4.50mm × 2.50mm	4.50mm × 2.50mm

(1) 有关更多信息，请参阅 节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。



内容

4 引脚配置和功能

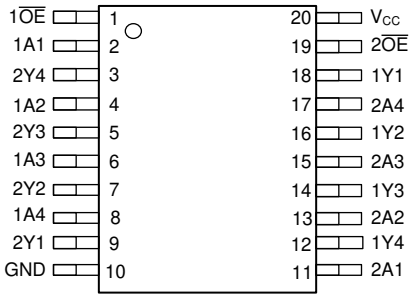


图 4-1. SN54AHC244 J 或 W 封装，20 引脚 CDIP 或 CFP（顶视图）

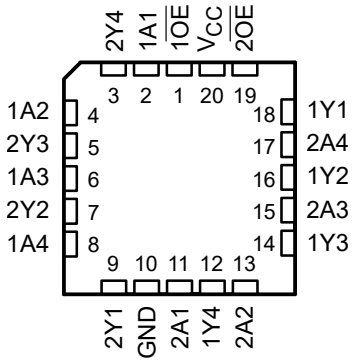


图 4-2. SN54AHC244 FK 封装，20 引脚 LCCC（顶视图）

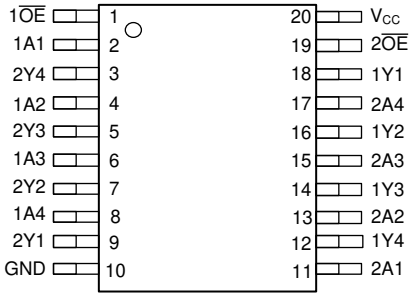


图 4-3. SN74AHC244 DB、DGV、DW、N、NS、PW 或 DGS 封装，20 引脚 SSOP、TVSOP、SOIC、PDIP、SOP、TSSOP 或 VSSOP（顶视图）

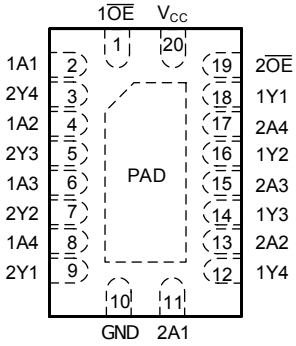


图 4-4. SN74AHC244 RKS 封装；20 引脚 VQFN（顶视图）

表 4-1. 引脚功能

引脚		类型[1]	说明
编号	名称		
1	1 $\overline{OE}$	I	输出使能 1
2	1A1	I	1A1 输入
3	2Y4	O	2Y4 输出
4	1A2	I	1A2 输入
5	2Y3	O	2Y3 输出
6	1A3	I	1A3 输入
7	2Y2	O	2Y2 输出
8	1A4	I	1A4 输入
9	2Y1	O	2Y1 输出
10	GND	—	接地引脚
11	2A1	I	2A1 输入
12	1Y4	O	1Y4 输出
13	2A2	I	2A2 输入
14	1Y3	O	1Y3 输出
15	2A3	I	2A3 输入
16	1Y2	O	1Y2 输出

表 4-1. 引脚功能（续）

引脚		类型[1]	说明
编号	名称		
17	2A4	I	2A4 输入
18	1Y1	O	1Y1 输出
19	2 $\overline{OE}$	I	输出使能 2
20	VCC	—	电源引脚
散热焊盘[2]			散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出
(2) 仅限 RKS 封装

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压		-0.5	7	V
V_I	输入电压 (2)		-0.5	7	V
V_O	输出电压范围(3)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-20	mA
I_{OK}	输出钳位电流	V_O < 0 或 V_O > V_{CC}		±20	mA
I_O	持续输出电流	V_O = 0 至 V_{CC}		±25	mA
	通过每个 V_{CC} 或 GND 的持续电流			±50	mA
T_{stg}	贮存温度		-65	150	°C

(1) 应力超出*绝对最大额定值*下面列出的值时可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。
(3) 封装热阻抗根据 JESD 51-7 计算。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准，所有引脚(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101，所有引脚(2)	±1500	

(1) JEDEC 文档 JEP155 指出：500V HBM 支持在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN54AHC244		SN74AHC244		单位
			最小值	最大值	最小值	最大值	
V_{CC}	电源电压		2	5.5	2	5.5	V
V_{IH}	高电平输入电压	V_{CC} = 2V	1.5		1.5		V
		V_{CC} = 3V	2.1		2.1		
		V_{CC} = 5.5V	3.85		3.85		
V_{IL}	低电平输入电压	V_{CC} = 2V		0.5		0.5	V
		V_{CC} = 3V		0.9		0.9	
		V_{CC} = 5.5V		1.65		1.65	
V_I	输入电压		0	5.5	0	5.5	V
V_O	输出电压		0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 2V		-50		-50	μA
		V_{CC} = 3.3V ± 0.3V		-4		-4	mA
		V_{CC} = 5V ± 0.5V		-8		-8	
I_{OL}	低电平输出电流	V_{CC} = 2V		50		50	μA
		V_{CC} = 3.3V ± 0.3V		4		4	mA
		V_{CC} = 5V ± 0.5V		8		8	
Δt/Δv	输入转换上升或下降速率	V_{CC} = 3.3V ± 0.3V		100		100	ns/V
		V_{CC} = 5V ± 0.5V		20		20	

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		SN54AHC244		SN74AHC244		单位
		最小值	最大值	最小值	最大值	
T_A	自然通风条件下的工作温度范围	-55	125	-40	125	°C

(1) 器件的所有未使用输入必须保持在 V_{CC} 或 GND，以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢或悬空的影响*，文献编号 SCBA004。

5.4 热性能信息

封装	引脚	热指标(1)						单位
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DB (SSOP)	20	99.9	61.7	55.2	22.6	54.8	不适用	°C/W
DGV (TVSOP)	20	119.2	34.5	60.7	1.2	60.0	不适用	
DW (SOIC)	20	81.1	48.9	53.8	19.5	53.1	不适用	
N (PDIP)	20	54.9	41.7	35.8	27.9	35.7	不适用	
NS (SOP)	20	77.6	42.7	45.7	10.2	45.2	不适用	
PW (TSSOP)	20	116.8	58.5	78.7	12.6	77.9	不适用	
DGS (VSSOP)	20	131.6	69.5	86.7	10.9	85.9	不适用	
RKS (VQFN)	20	90.4	92.2	63.4	29	63.5	41.3	

(1) 有关新旧热指标的更多信息，请参阅 *IC 封装热指标* 应用报告 SPRA953。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			SN54AHC244		SN74AHC244		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = -50μA	2V	1.9	2		1.9		1.9		V
		3V	2.9	3		2.9		2.9		
		4.5V	4.4	4.5		4.4		4.4		
	I_{OH} = -4mA	3V	2.58			2.48		2.48		
	I_{OH} = -8mA	4.5V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50μA	2V			0.1		0.1		0.1	V
		3V			0.1		0.1		0.1	
		4.5V			0.1		0.1		0.1	
	I_{OL} = 4mA	3V			0.36		0.5		0.44	
	I_{OL} = 8mA	4.5V			0.36		0.5		0.44	
I_I	V_I = 5.5V 或 GND	0V 至 5.5V			±0.1		±1(1)		±1	μA
I_{OZ}	$V_O = V_{CC}$ 或 GND，V_I ($\overline{OE}$) = V_{IL} 或 V_{IH}	5.5V			±0.25		±2.5		±2.5	μA
I_{CC}	$V_I = V_{CC}$ 或 GND，I_O = 0	5.5V			4		40		40	μA
C_i	$V_I = V_{CC}$ 或 GND	5V		2	10				10	pF
C_o	$V_O = V_{CC}$ 或 GND	5V		3.5						pF

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试（在 V_{CC} = 0V 时）。

5.6 开关特性，V_{CC} = 3.3V ± 0.3V

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 3.3V ± 0.3V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN54AHC244		SN74AHC244		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A	Y	C_L = 15pF		5.8(1)	8.4(1)	1(1)	10(1)	1	10	ns
t_{PHL}					5.8(1)	8.4(1)	1(1)	10(1)	1	10	
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF		6.6(1)	10.6(1)	1(1)	12.5(1)	1	12.5	ns
t_{PZL}					6.6(1)	10.6(1)	1(1)	12.5(1)	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF		5(1)	9.7(1)	1(1)	11(1)	1	11	ns
t_{PLZ}					5(1)	9.7(1)	1(1)	11(1)	1	11	
t_{PLH}	A	Y	C_L = 50pF		8.3	11.9	1	13.5	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	1	13.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF		9.1	14.1	1	16	1	16	ns
t_{PZL}					9.1	14.1	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF		10.3	14	1	16	1	16	ns
t_{PLZ}					10.3	14	1	16	1	16	
$t_{sk(o)}$			C_L = 50pF			1.5(2)				1.5	ns

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。
(2) 对于符合 MIL-PRF-38535 标准的产品，此参数不适用。

5.7 开关特性，V_{CC} = 5V ± 0.5V

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN54AHC244		SN74AHC244		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A	Y	C_L = 15pF		3.9(1)	5.5(1)	1(1)	6.5(1)	1	6.5	ns
t_{PHL}					3.9(1)	5.5(1)	1(1)	6.5(1)	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF		4.7(1)	7.3(1)	1(1)	8.5(1)	1	8.5	ns
t_{PZL}					4.7(1)	7.3(1)	1(1)	8.5(1)	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF		5(1)	7.2(1)	1(1)	8.5(1)	1	8.5	ns
t_{PLZ}					5(1)	7.2(1)	1(1)	8.5(1)	1	8.5	
t_{PLH}	A	Y	C_L = 50pF		5.4	7.5	1	8.5	1	8.5	ns
t_{PHL}					5.4	7.5	1	8.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF		6.2	9.3	1	10.5	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF		6.7	9.2	1	10.5	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	1	10.5	
$t_{sk(o)}$			C_L = 50pF			1(2)				1	ns

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。
(2) 对于符合 MIL-PRF-38535 标准的产品，此参数不适用。

5.8 噪声特性

V_{CC} = 5V，C_L = 50pF，T_A = 25°C (1)

参数		SN74AHC244			单位
		最小值	典型值	最大值	
$V_{OL(P)}$	安静输出，最大动态 V_{OL}		0.5		V
$V_{OL(V)}$	安静输出，最小动态 V_{OL}		-0.2		V
$V_{OH(V)}$	安静输出，最小动态 V_{OH}		4.8		V
$V_{IH(D)}$	高电平动态输入电压	3.5			V
$V_{IL(D)}$	低电平动态输入电压			1.5	V

(1) 特性仅适用于表面贴装封装。

5.9 工作特性

V_{CC} = 5V，T_A = 25°C

参数		测试条件		典型值	单位
C_{pd}	功率耗散电容	无负载，	f = 1MHz	8.6	pF

5.10 典型特性

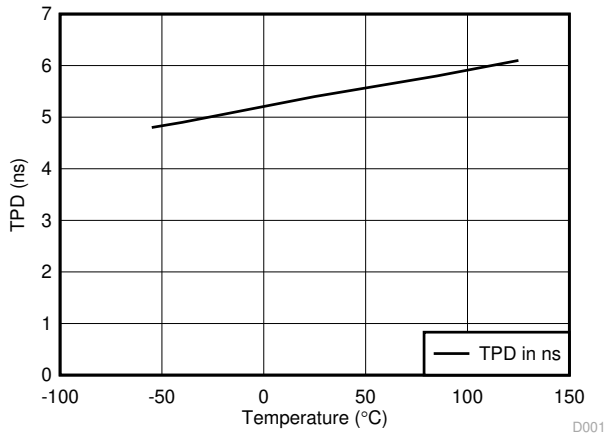


图 5-1. TPD 与温度间的关系

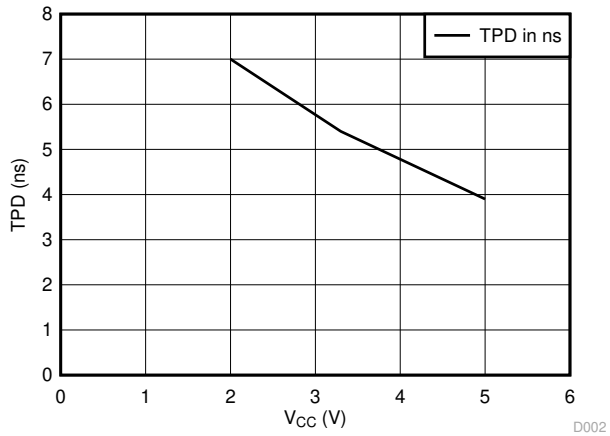
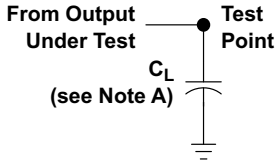
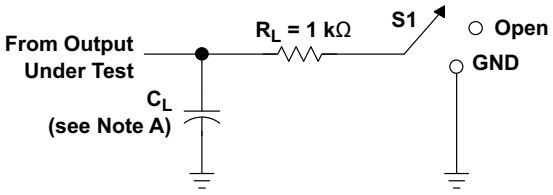


图 5-2. TPD 与 V_{CC} 间的关系

6 参数测量信息

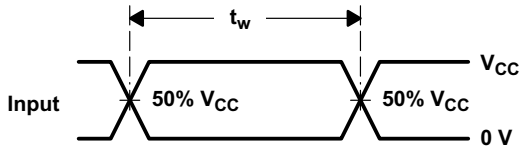


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

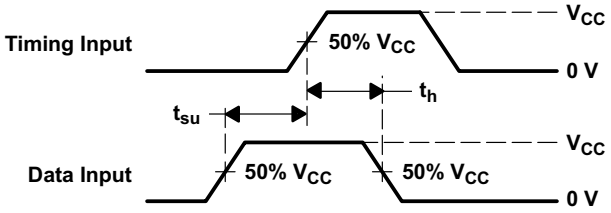


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

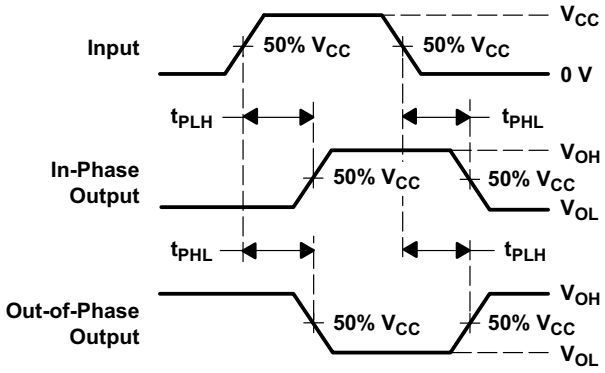
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



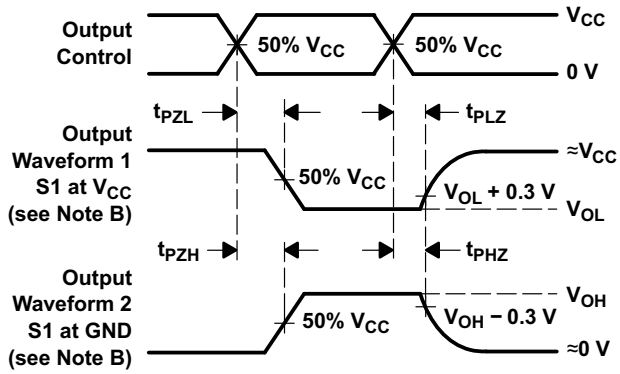
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. 负载电路和电压波形

7 详细说明

7.1 概述

SNx4AHC244 包含 8 个独立的高速 CMOS 缓冲器，配置为两个具有三态输出的 4 位缓冲器/线路驱动器。

每个缓冲器均可执行布尔逻辑函数 xYn = xAn，其中 *x* 为存储体编号，*n* 为通道编号。

每个输出使能 (x$\overline{OE}$) 控制四个缓冲器。当 x$\overline{OE}$ 引脚处于低电平状态时，存储体 x 中所有缓冲器的输出将被启用。当 x$\overline{OE}$ 引脚处于高电平状态时，存储体 x 中所有缓冲器的输出将被禁用。所有被禁用的输出将置于高阻抗状态。

为了在上电或断电期间将器件置于高阻抗状态，需将两个 $\overline{OE}$ 引脚通过一个上拉电阻连接至 V_{CC}；电阻的最小值由驱动器的灌电流能力和*电气特性* 表中定义的引脚漏电流决定。

7.2 功能方框图

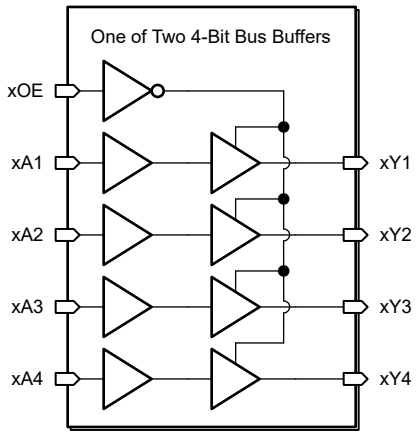


图 7-1. 逻辑图（正逻辑）

7.3 特性说明

7.3.1 平衡 CMOS 推挽式输出

该器件包括平衡 CMOS 推挽输出。术语*平衡* 表示器件可以灌入和拉出相似的电流。此器件的驱动能力可能在轻负载时产生快速边沿，因此应考虑布线和负载条件以防止振铃。此外，该器件的输出能够驱动的电流比此器件能够承受的电流更大，而不会损坏器件。务必限制器件的输出功率，以避免因过流而损坏器件。必须始终遵守*绝对最大额定值* 中规定的电气和热限值。

未使用的推挽 CMOS 输出必须保持断开状态。

7.3.2 平衡 CMOS 三态输出

此器件包含平衡 CMOS 三态输出。这些输出可以处于三种状态：高驱动、低驱动和高阻抗。术语*平衡* 表示器件可以灌入和拉出相似的电流。此器件的驱动能力可能在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。此外，该器件的输出能够驱动的电流比此器件能够承受、不会损坏的电流更大。务必限制器件的输出功率，以避免因过电流而损坏器件。必须始终遵守*绝对最大额定值* 中规定的电气和热限值。

当置于高阻态时，输出既不会拉出电流，也不会灌入电流，但*电气特性* 表中定义的小漏电流除外。在高阻抗状态下，输出电压不受器件控制，而取决于外部因素。如果没有其他驱动器连接到该节点，则这称为悬空节点且电压未知。上拉或下拉电阻可以连接到输出端，以便当输出端处于高阻抗状态时在输出端提供已知电压。电阻值将取决于多种因素，包括寄生电容和功耗限制。通常，可以使用 10kΩ 电阻器来满足这些要求。

未使用的三态 CMOS 输出应保持断开状态。

7.3.3 标准 CMOS 输入

此器件包括标准 CMOS 输入。标准 CMOS 输入为高阻抗，通常建模为与输入电容并联的电阻器，如*电气特性* 中所示。最坏情况下的电阻是根据*绝对最大额定值* 中给出的最大输入电压和*电气特性* 中给出的最大输入漏电流，使用欧姆定律 (R = V ÷ I) 计算得出的。

标准 CMOS 输入要求输入信号在有效逻辑状态之间快速转换，如*建议运行条件* 表中的输入转换时间或速率所定义。不符合此规范将导致功耗过大并可能导致振荡。更多详细信息，请参阅 *CMOS 输入缓慢或悬空的影响*。

在运行期间，任何时候都不要让标准 CMOS 输入悬空。未使用的输入必须在 V_{CC} 或 GND 端接。如果系统不会一直主动驱动输入，则可以添加上拉或下拉电阻器，以在这些时间段提供有效的输入电压。电阻值将取决于多种因素；但建议使用 10kΩ 电阻器，这通常可以满足所有要求。

7.3.4 钳位二极管结构

该器件的输出同时具有正负钳位二极管，而该器件的输入只有负钳位二极管，如图 7-2 所示。

小心

电压超出*绝对最大额定值*表中规定的值可能会损坏器件。如果遵守输入和输出钳制电流额定值，输入和输出电压可超过额定值。

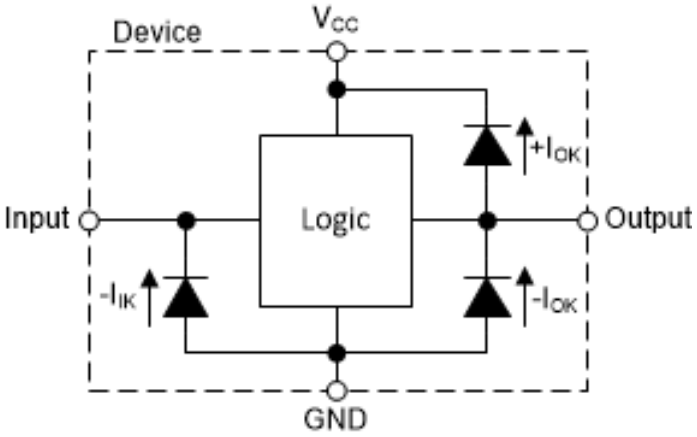


图 7-2. 每个输入和输出的钳位二极管的电气布置

7.4 器件功能模式

表 7-1 列出了 SNx4AHC244 的功能模式。

表 7-1. 功能表

输入(1)		输出
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(1) H = 高压电平，L = 低压电平，X = 无关，Z = 高阻抗状态

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

SNx4AHC244 是一款高驱动 CMOS 器件，可用于需要考虑输出驱动或 PCB 布线长度的多种总线接口类型应用。这些输入可在任何有效 V_{CC} 下接受高达 5.5V 的电压，使得该器件成为降压转换的理想选择。

8.2 典型应用

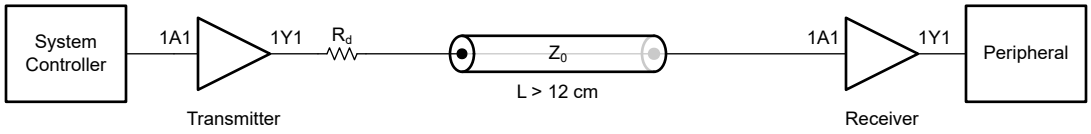


图 8-1. 应用原理图

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此请考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件：
   - 有关上升时间和下降时间规格，请参阅*建议运行条件*表中的 ($\Delta t/\Delta V$)。
   - 有关指定的高电平和低电平，请参阅*建议运行条件* 表中的 (V_{IH} 和 V_{IL})。
   - 输入可耐受过压，允许它们在任何有效 V_{CC} 下高达*建议运行条件* 表中的 (V_I 最大值) 。
2. 建议的输出条件上限：
   - 每路输出的负载电流不应超过 (I_O 最大值) ，且不能超过该器件的总电流 (通过 V_{CC} 或 GND 的持续电流) 。这些限值位于*绝对最大额定值* 表中。
   - 输出不应被拉至高于 V_{CC}。

8.2.3 应用曲线

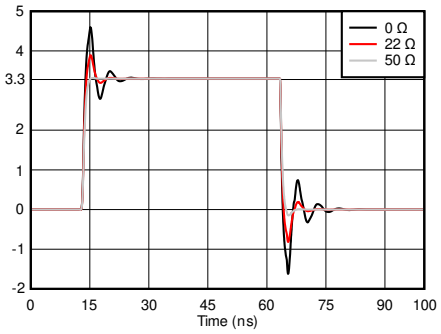


图 8-2. 使用不同阻尼电阻器 (R_d) 值的接收器模拟信号完整性

8.3 电源相关建议

电源可以是*建议运行条件* 中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。建议为该器件使用 0.1 µF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

8.4 布局

8.4.1 布局指南

- 旁路电容器的放置
  - 靠近器件的正电源端子放置
  - 提供电气短接地返回路径
  - 使用宽布线以最大限度减小阻抗
  - 尽可能将器件、电容器和布线保持在电路板的同一面
- 信号布线几何形状
  - 8mil 至 12mil 布线宽度
  - 布线长度小于 12cm 可最大限度减轻传输线路影响
  - 避免信号布线出现 90° 角
  - 在信号布线下方使用不间断的接地平面
  - 通过接地对信号布线周围的区域进行泛洪填充
  - 并行布线之间必须至少间隔 3 倍电介质厚度
  - 对于长度超过 12cm 的布线
    - 使用阻抗受控的布线
    - 在输出端附近使用串联阻尼电阻进行源端接
    - 避免分支；对必须单独分支的每条信号进行缓冲

8.4.2 布局示例

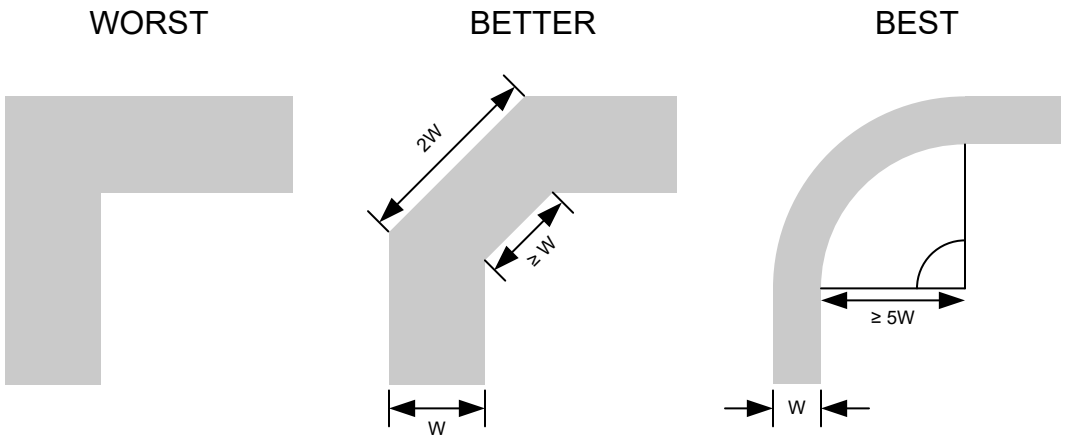


图 8-3. 可改善信号完整性的布线转角示例

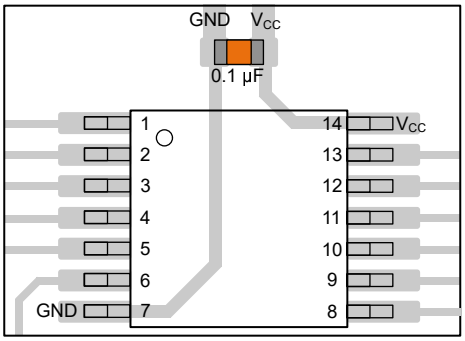


图 8-4. TSSOP 和类似封装的旁路电容器放置示例

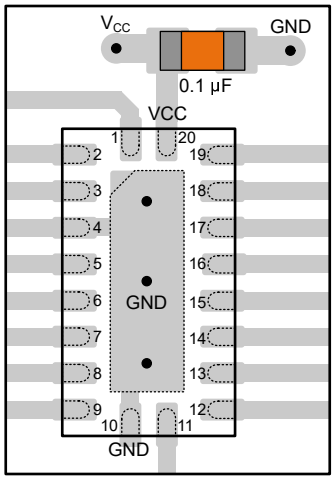


图 8-5. WQFN 和类似封装的旁路电容器放置示例

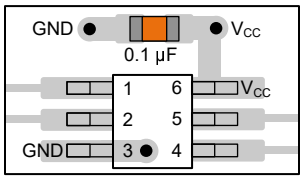


图 8-6. SOT、SC70 和类似封装的旁路电容器放置示例

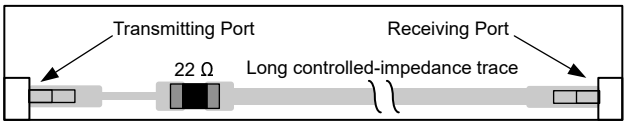


图 8-7. 可改善信号完整性的阻尼电阻放置示例

9 器件和文档支持

TI 提供大量的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

9.1 文档支持

9.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*CMOS 功耗与 C_{pd} 计算* 应用报告
- 德州仪器 (TI)，*使用逻辑器件进行设计* 应用报告
- 德州仪器 (TI)，*标准线性和逻辑 (SLL) 封装和器件的热特性* 应用报告

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (January 2025) to Revision N (June 2025)	Page
• 向*器件信息*表添加了 VSSOP 和 VQFN	1
• 添加了*概述* 部分、*特性说明* 部分、*应用信息* 部分和*典型应用* 部分	1
• 向*引脚配置和功能*中添加了 DGS 和 RKS 封装	3

Changes from Revision L (July 2024) to Revision M (January 2025)	Page
• 更新了 *ESD 等级*表中的 HBM 和 CDM 值	5

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9678201Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201Q2A SNJ54AHC244FK
5962-9678201QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201QRA SNJ54AHC244J
5962-9678201QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201QSA SNJ54AHC244W
5962-9678201VRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201VRA SNV54AHC244J
5962-9678201VRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201VRA SNV54AHC244J
5962-9678201VSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201VSA SNV54AHC244W
5962-9678201VSA.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201VSA SNV54AHC244W
SN74AHC244DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244DBRE4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244
SN74AHC244DGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244DGVR.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	AHC244
SN74AHC244DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244
SN74AHC244DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244
SN74AHC244DWRG4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244
SN74AHC244N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC244N

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC244N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC244N
SN74AHC244NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244
SN74AHC244NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244
SN74AHC244PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	HA244
SN74AHC244PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HA244
SN74AHC244PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA244
SN74AHC244PWRE4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244PWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA244
SN74AHC244RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244
SNJ54AHC244FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201Q2A SNJ54AHC 244FK
SNJ54AHC244FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201Q2A SNJ54AHC 244FK
SNJ54AHC244J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201QRA SNJ54AHC244J
SNJ54AHC244J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201QRA SNJ54AHC244J
SNJ54AHC244W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201QSA SNJ54AHC244W
SNJ54AHC244W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9678201QSA SNJ54AHC244W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54AHC244, SN54AHC244-SP, SN74AHC244 :

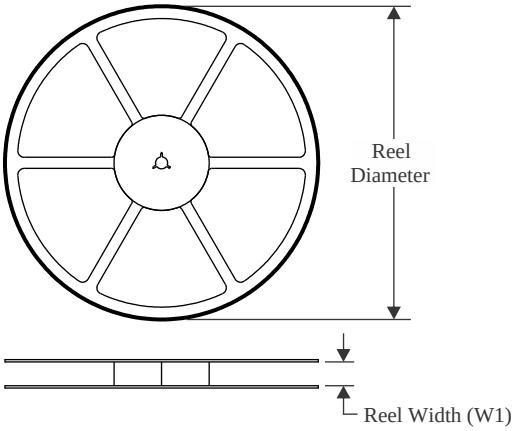
- Catalog : SN74AHC244, SN54AHC244
- Automotive : SN74AHC244-Q1, SN74AHC244-Q1
- Enhanced Product : SN74AHC244-EP, SN74AHC244-EP
- Military : SN54AHC244
- Space : SN54AHC244-SP

NOTE: Qualified Version Definitions:

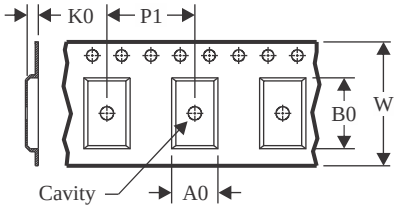
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

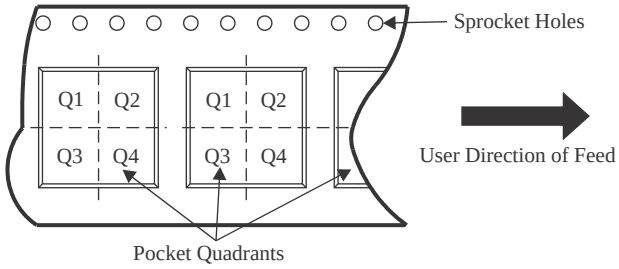


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

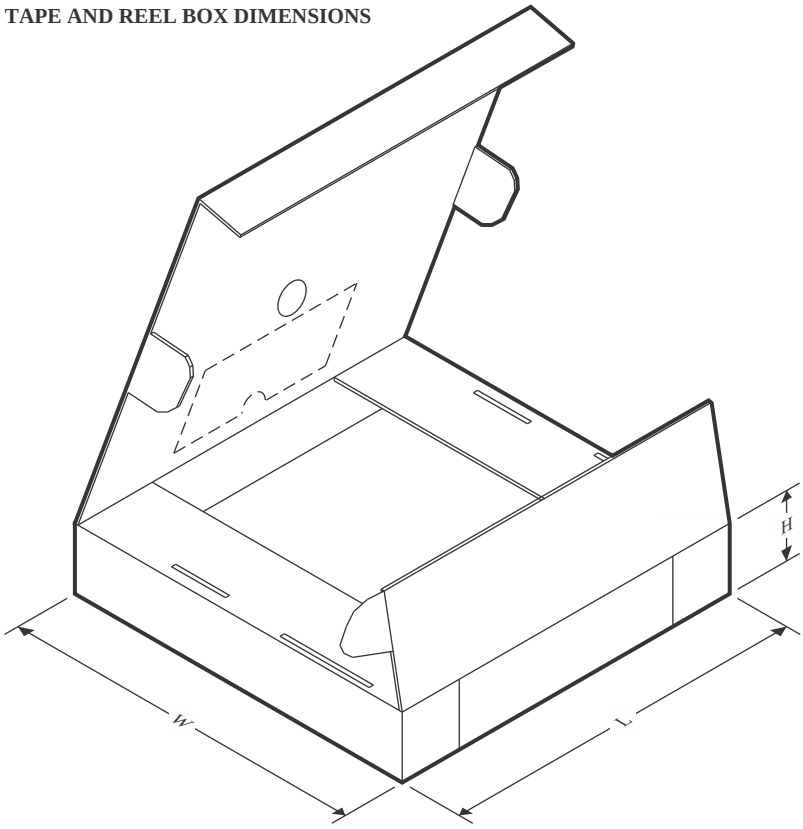
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC244DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHC244DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC244NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC244RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

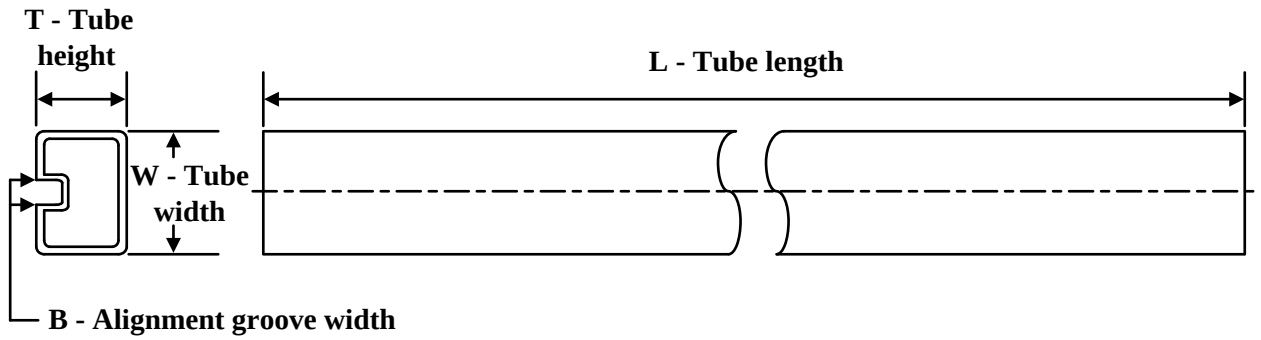
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC244DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHC244DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHC244DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74AHC244DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC244DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC244NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHC244PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC244PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC244PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC244RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



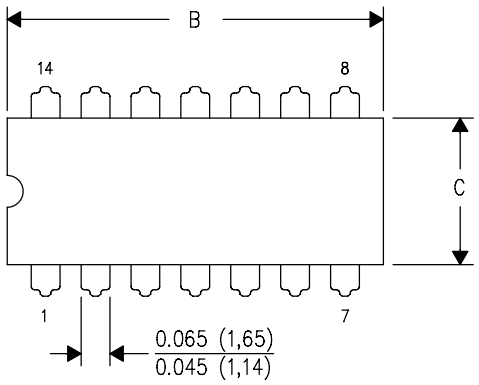
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9678201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9678201QSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9678201VSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9678201VSA.A	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC244N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC244FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC244FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC244W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHC244W.A	W	CFP	20	25	506.98	26.16	6220	NA

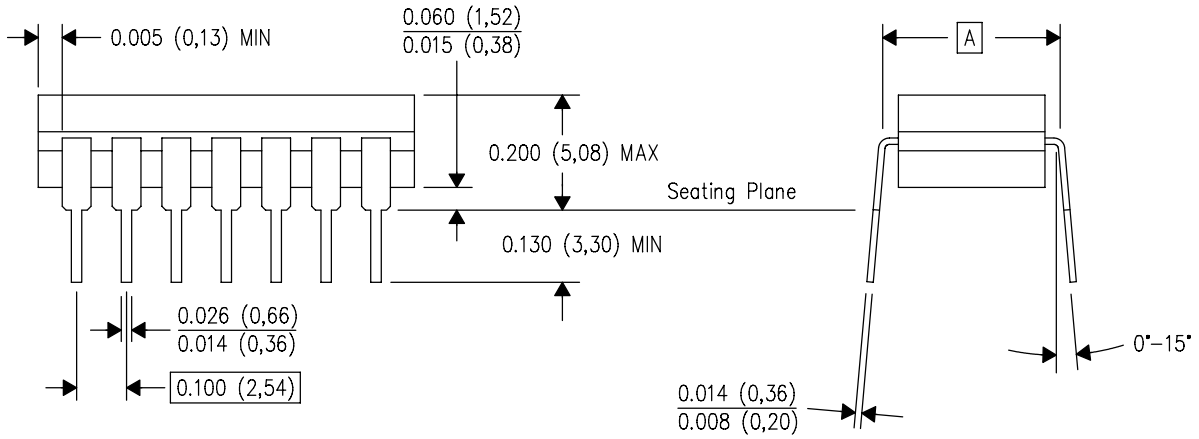
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

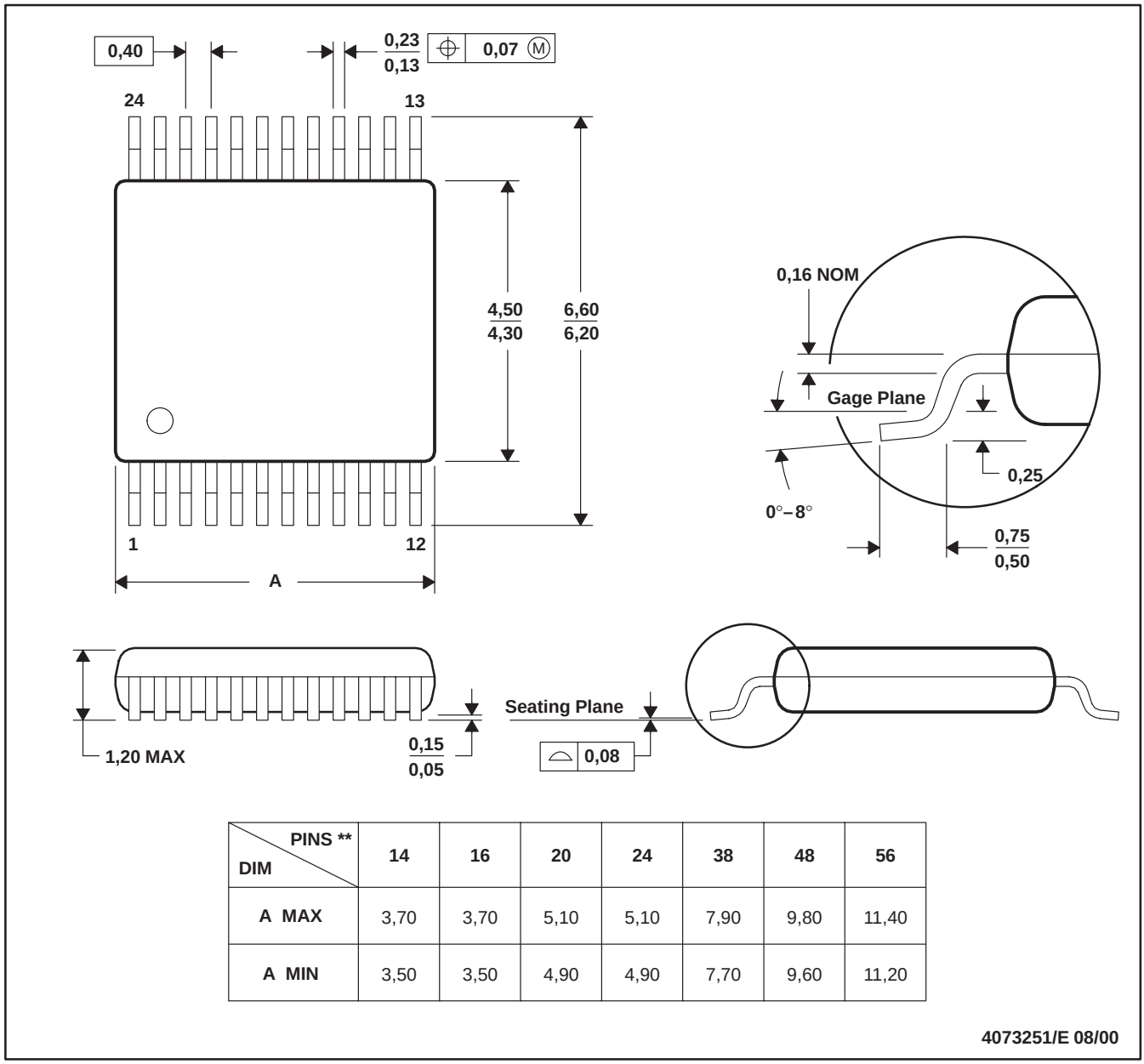


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

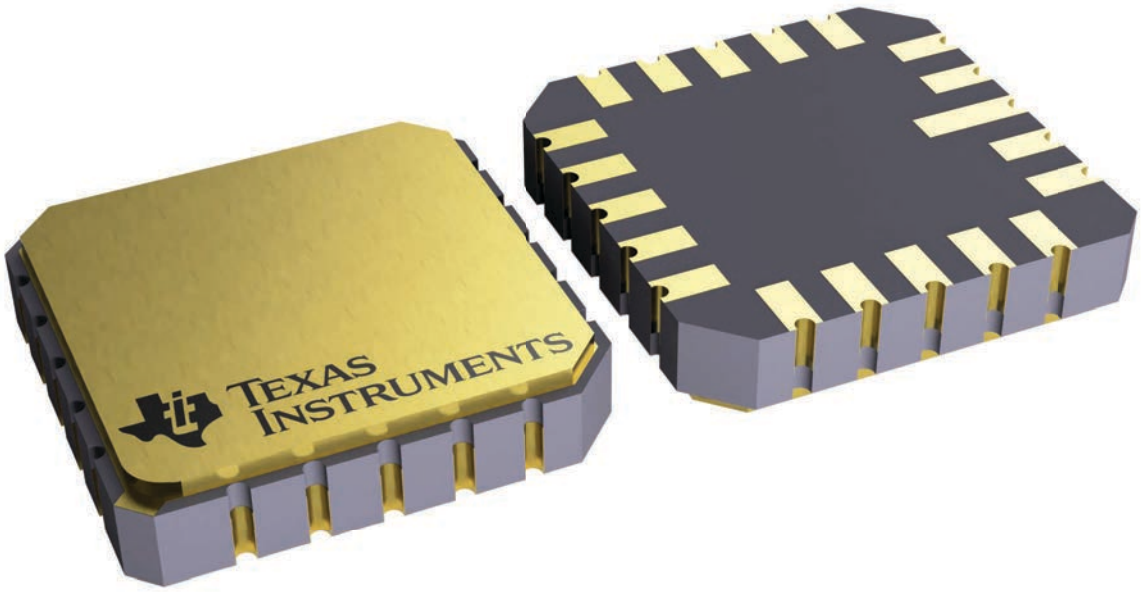
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

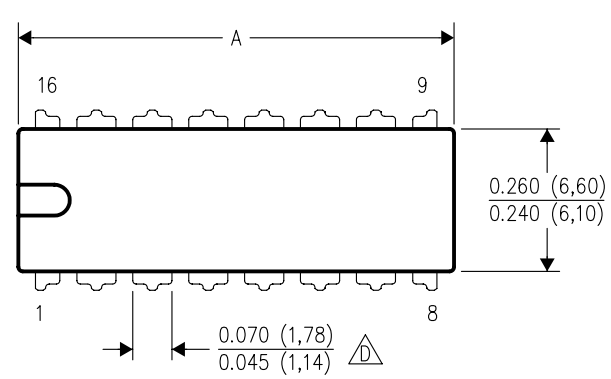


4229370VA\

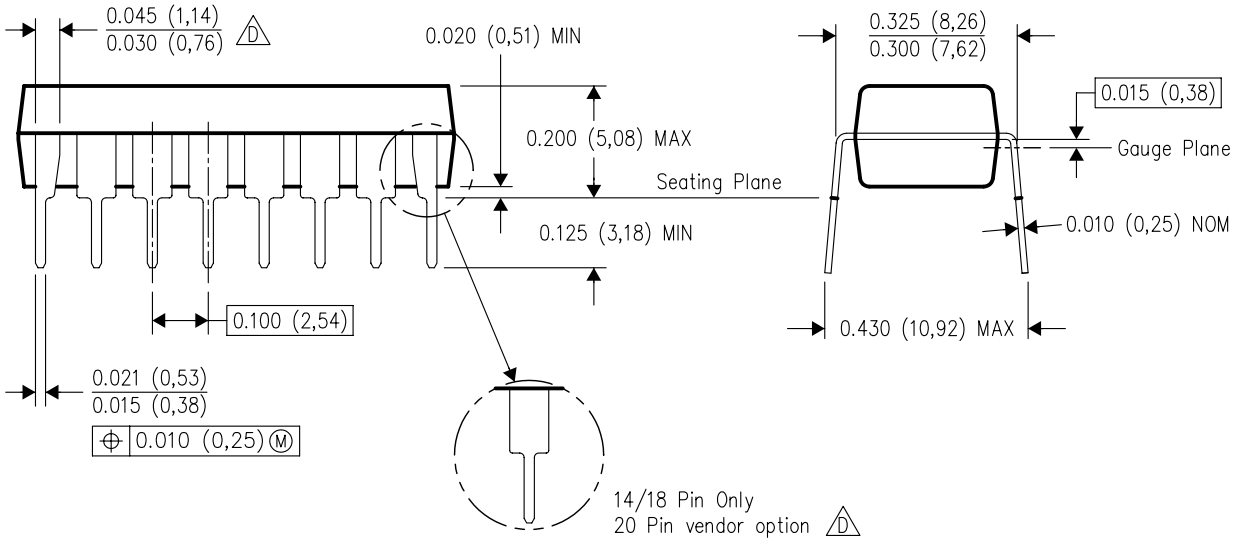
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

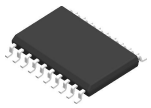


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

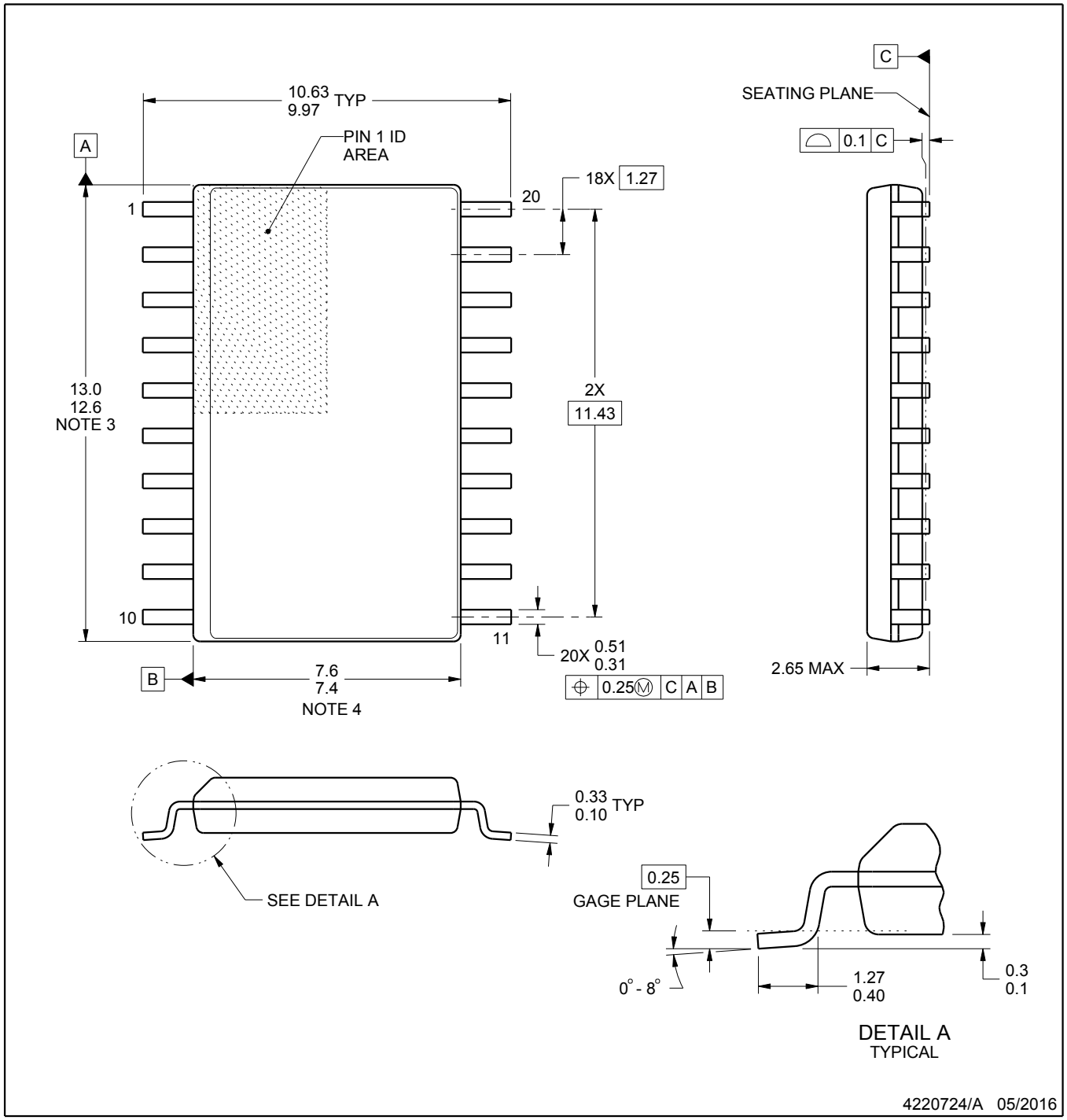


PACKAGE OUTLINE

DW0020A

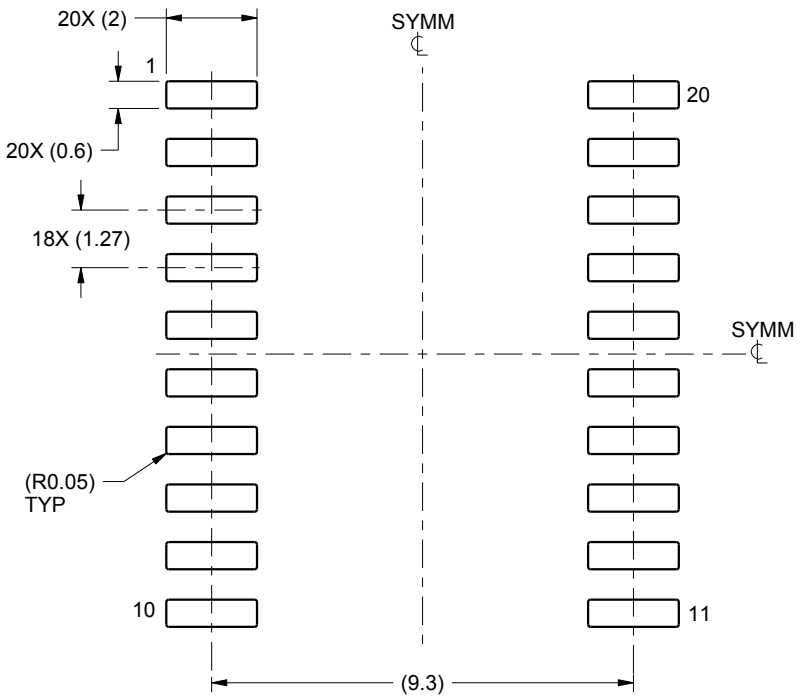
SOIC - 2.65 mm max height

SOIC

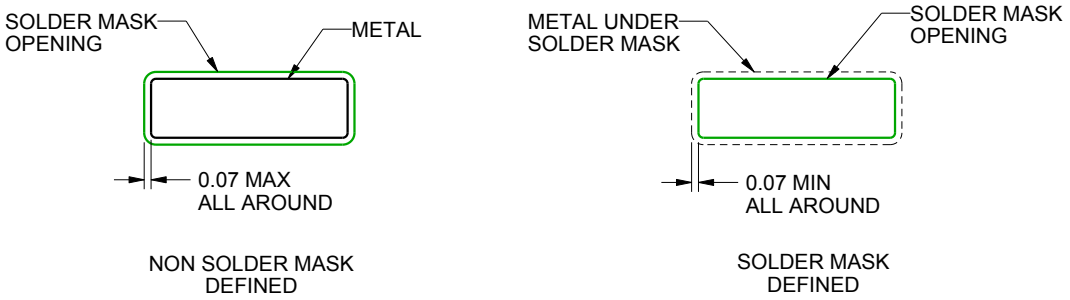


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

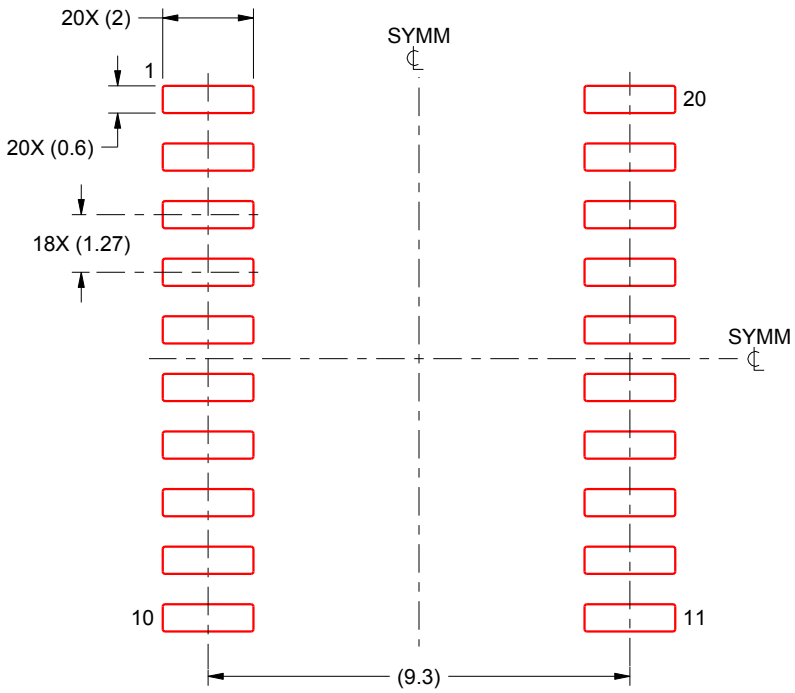


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



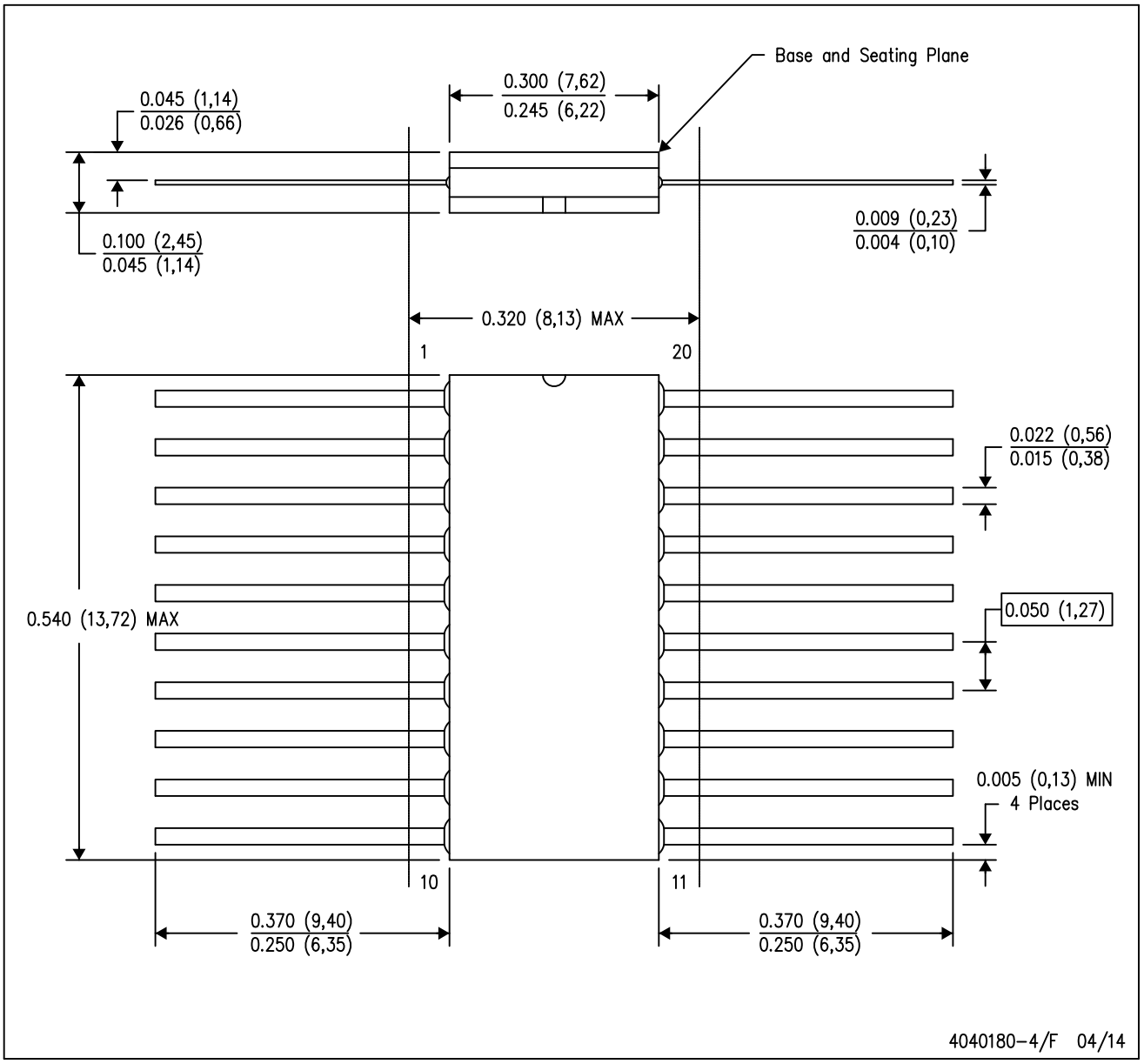
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



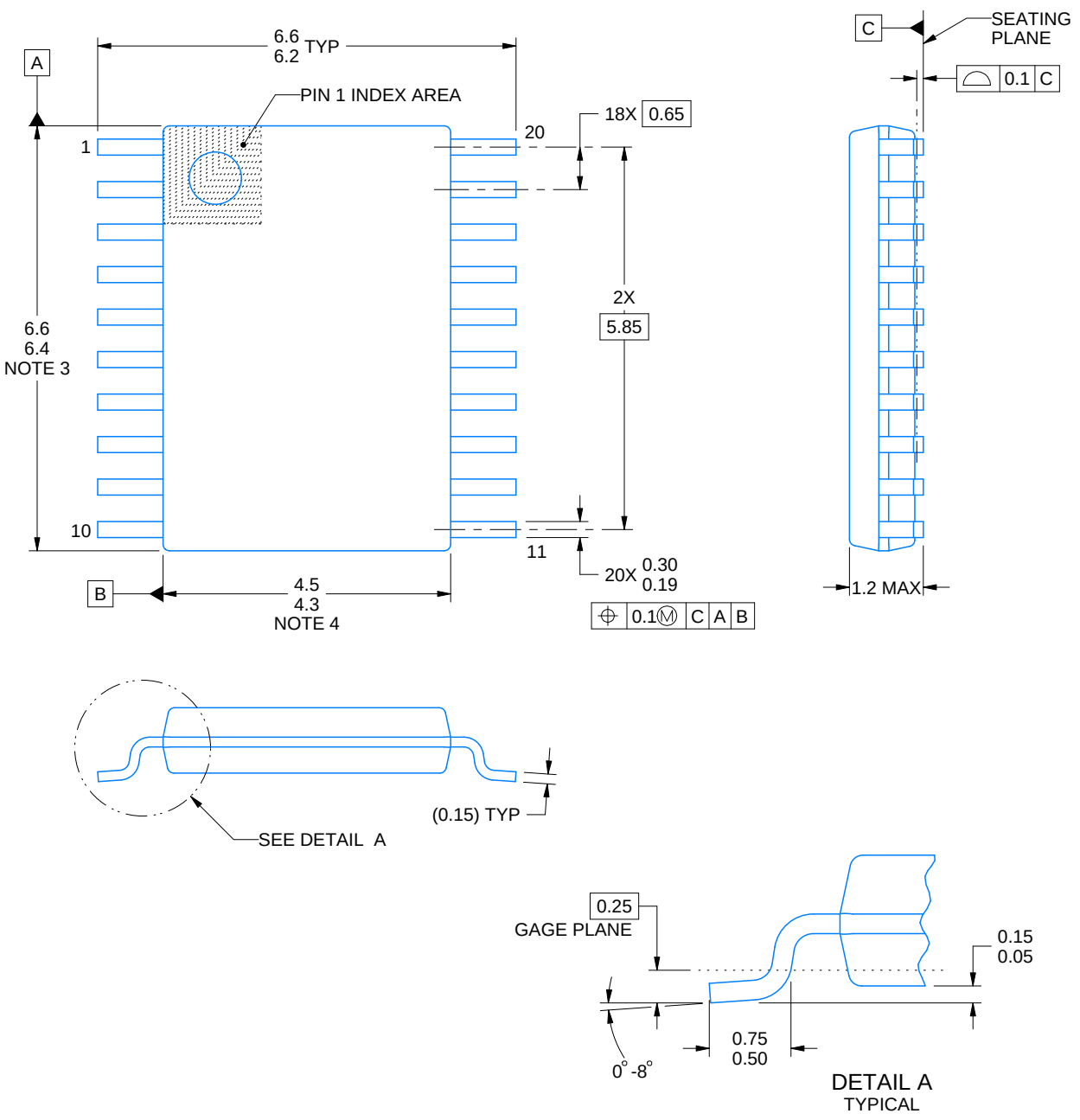
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

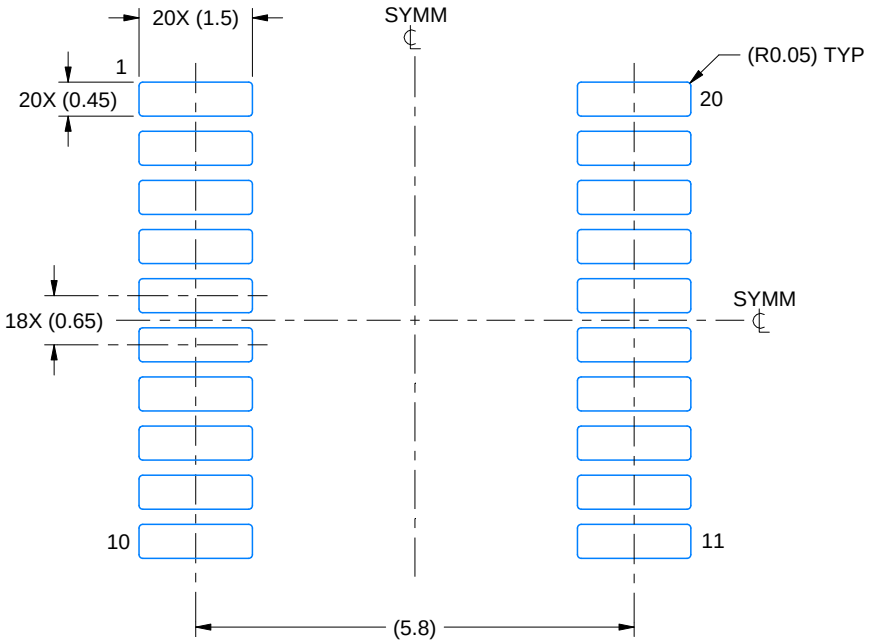
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



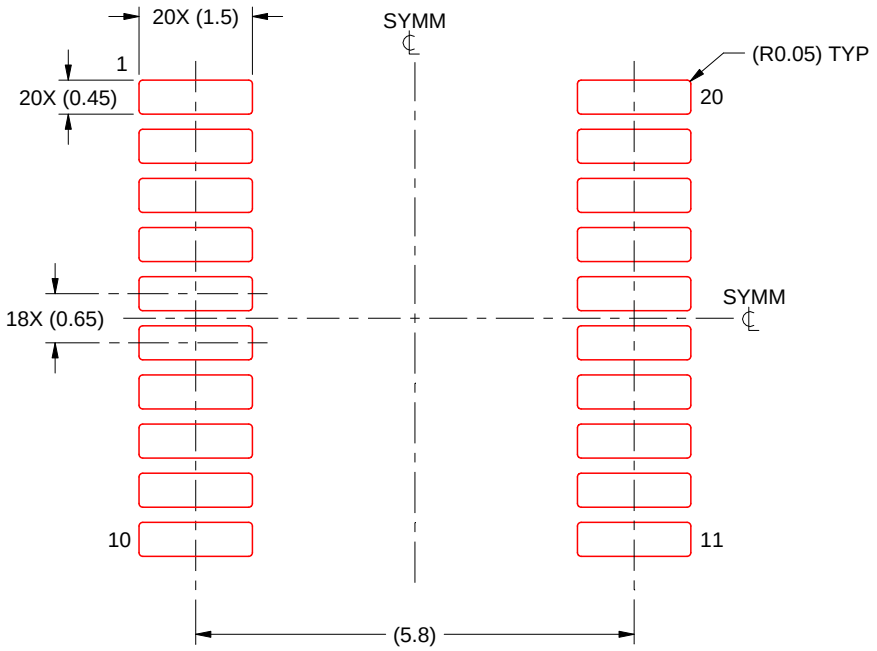
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

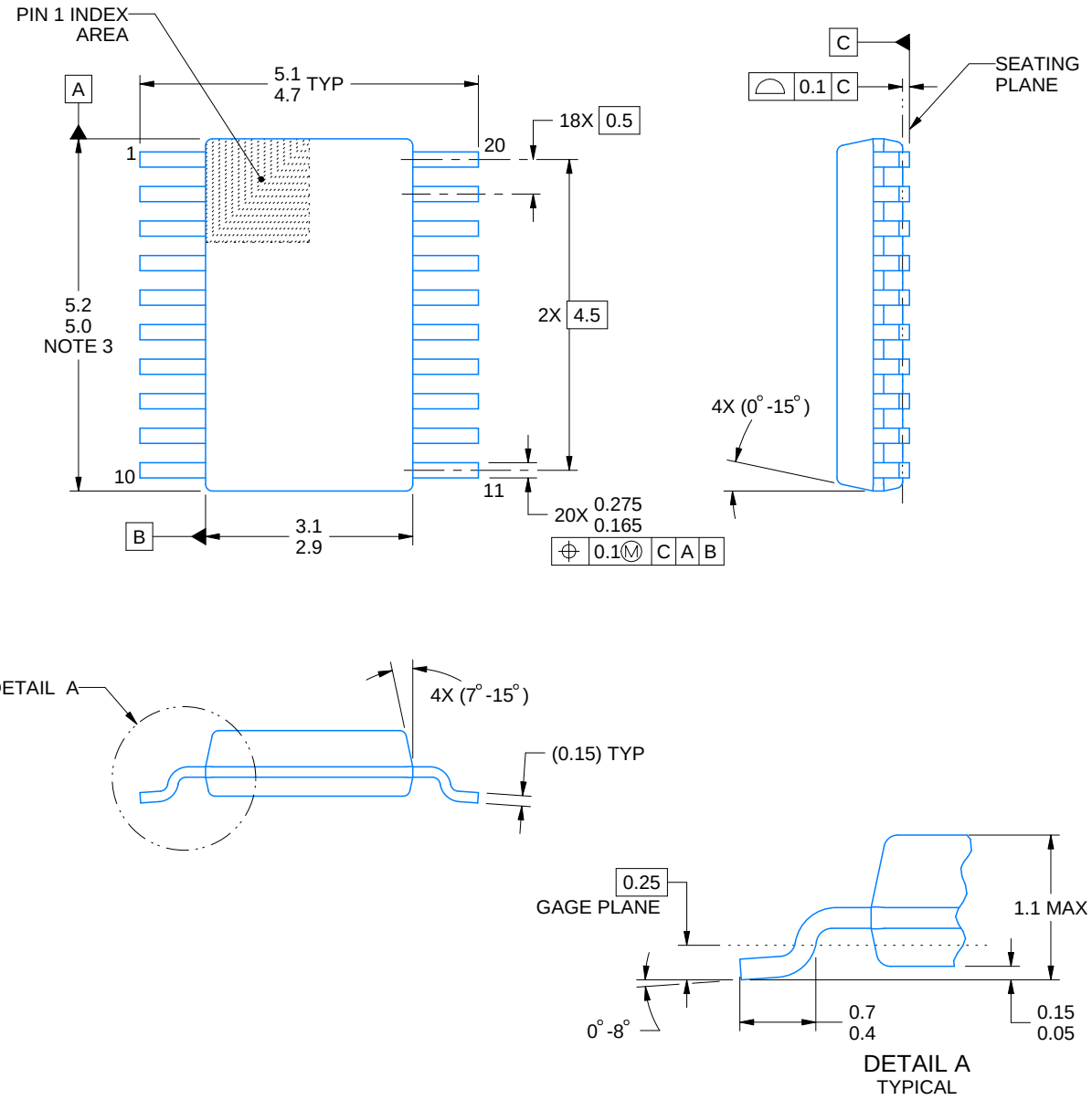
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

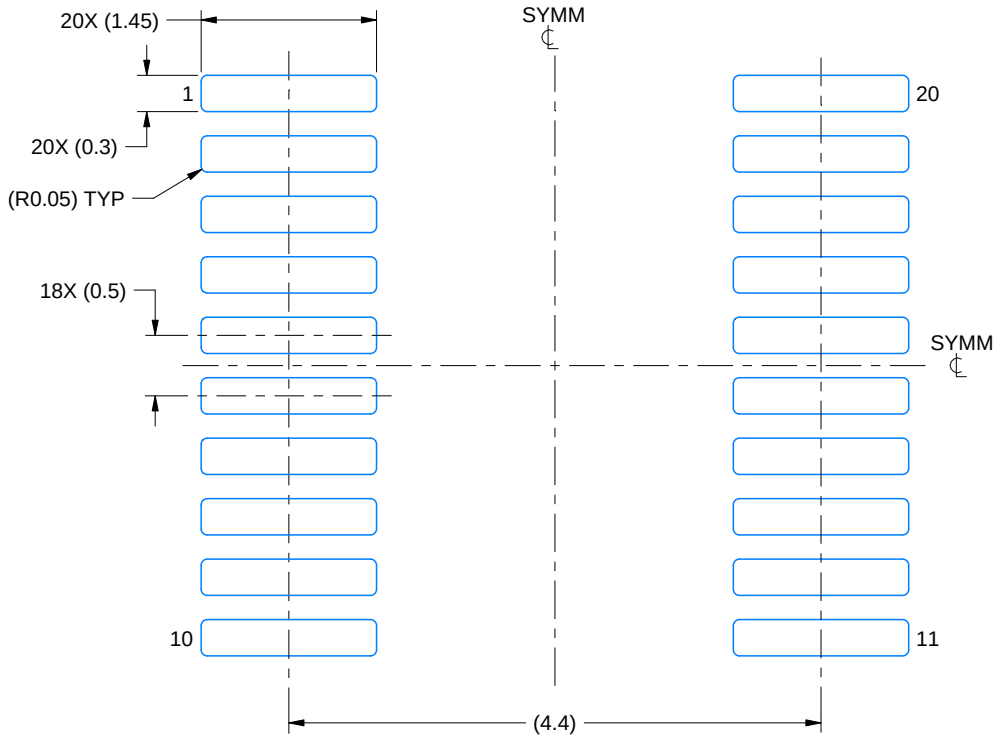
SMALL OUTLINE PACKAGE



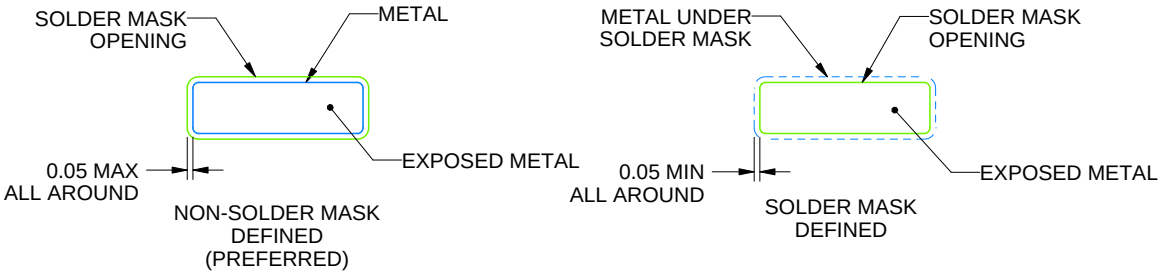
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

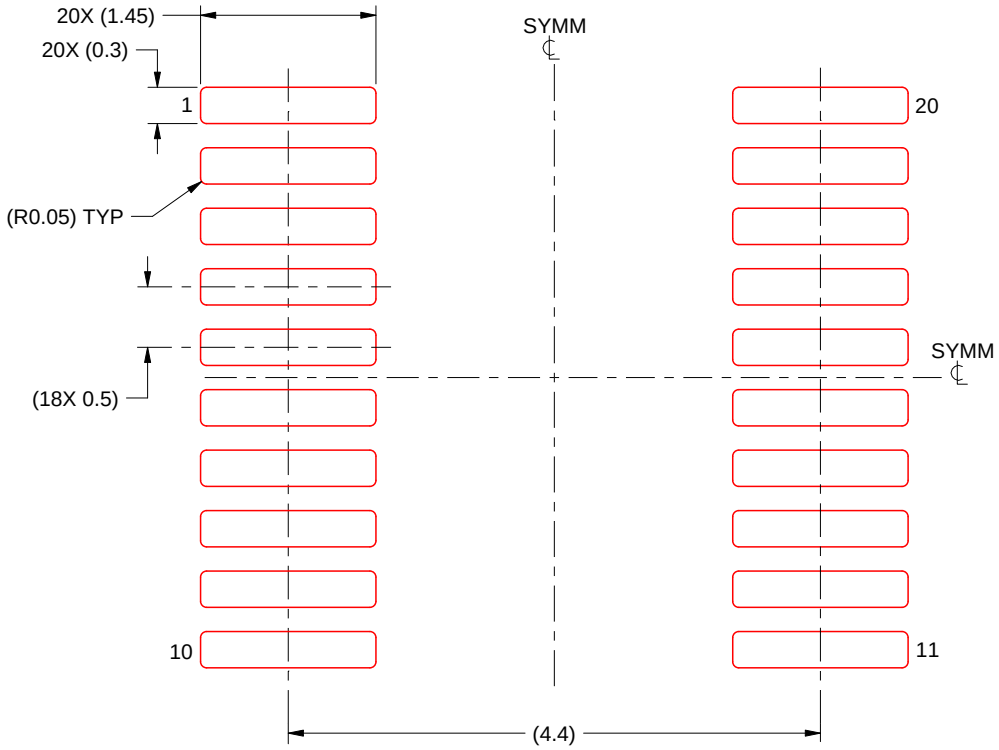


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

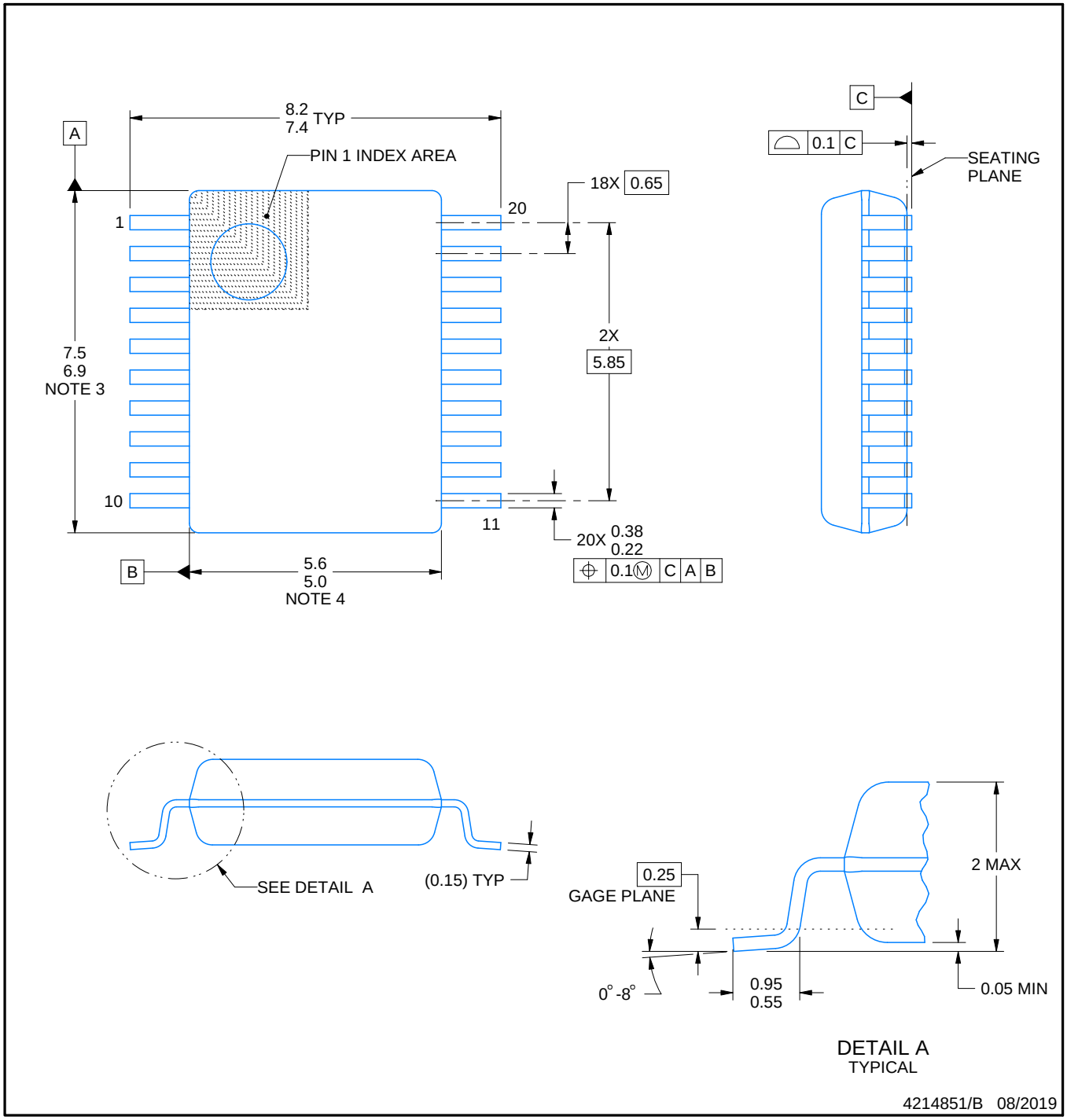
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

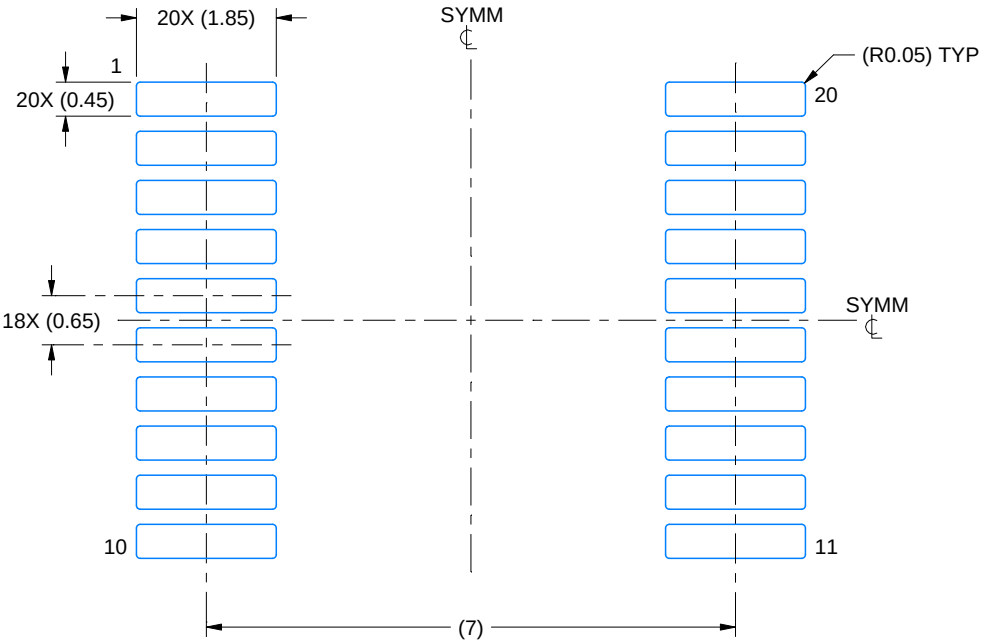
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

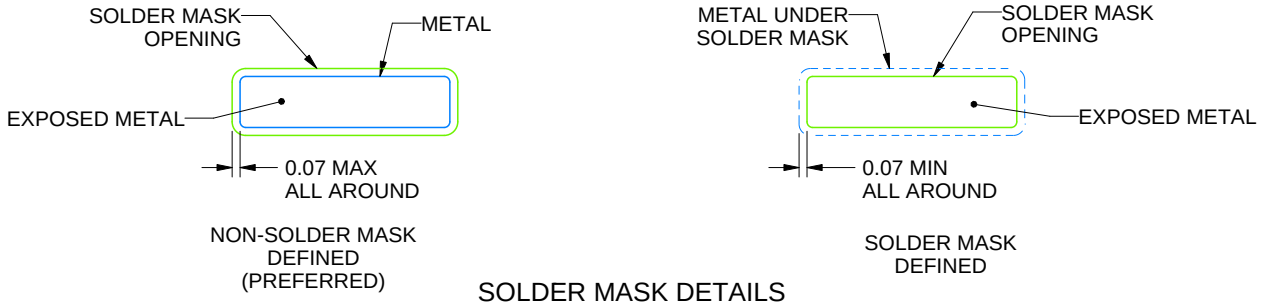


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

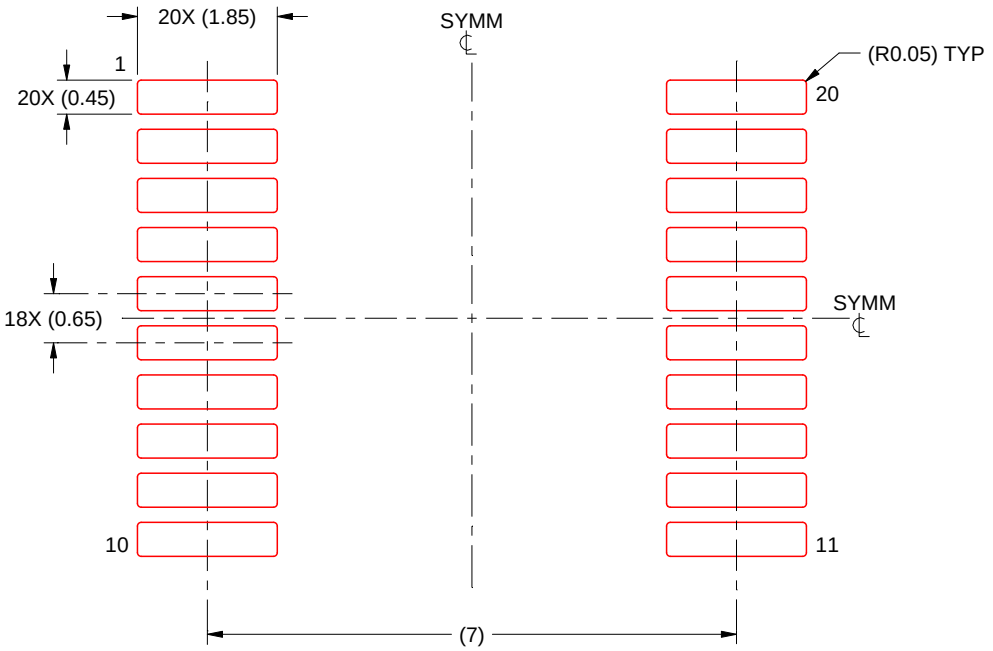
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

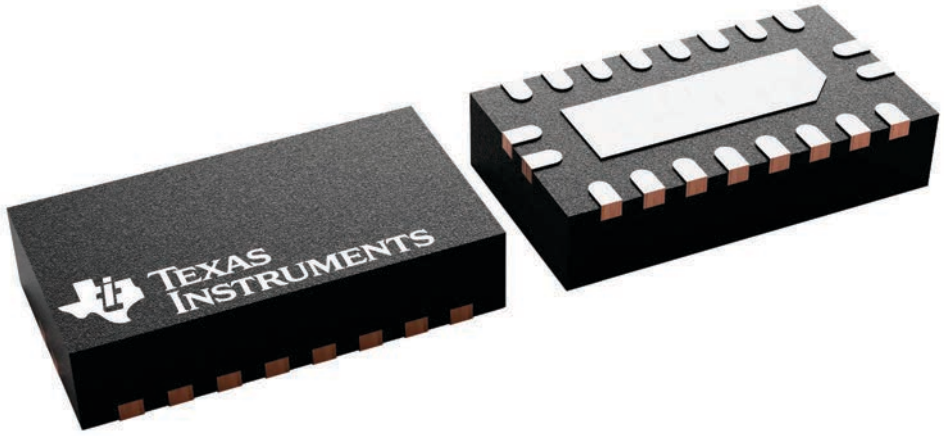
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

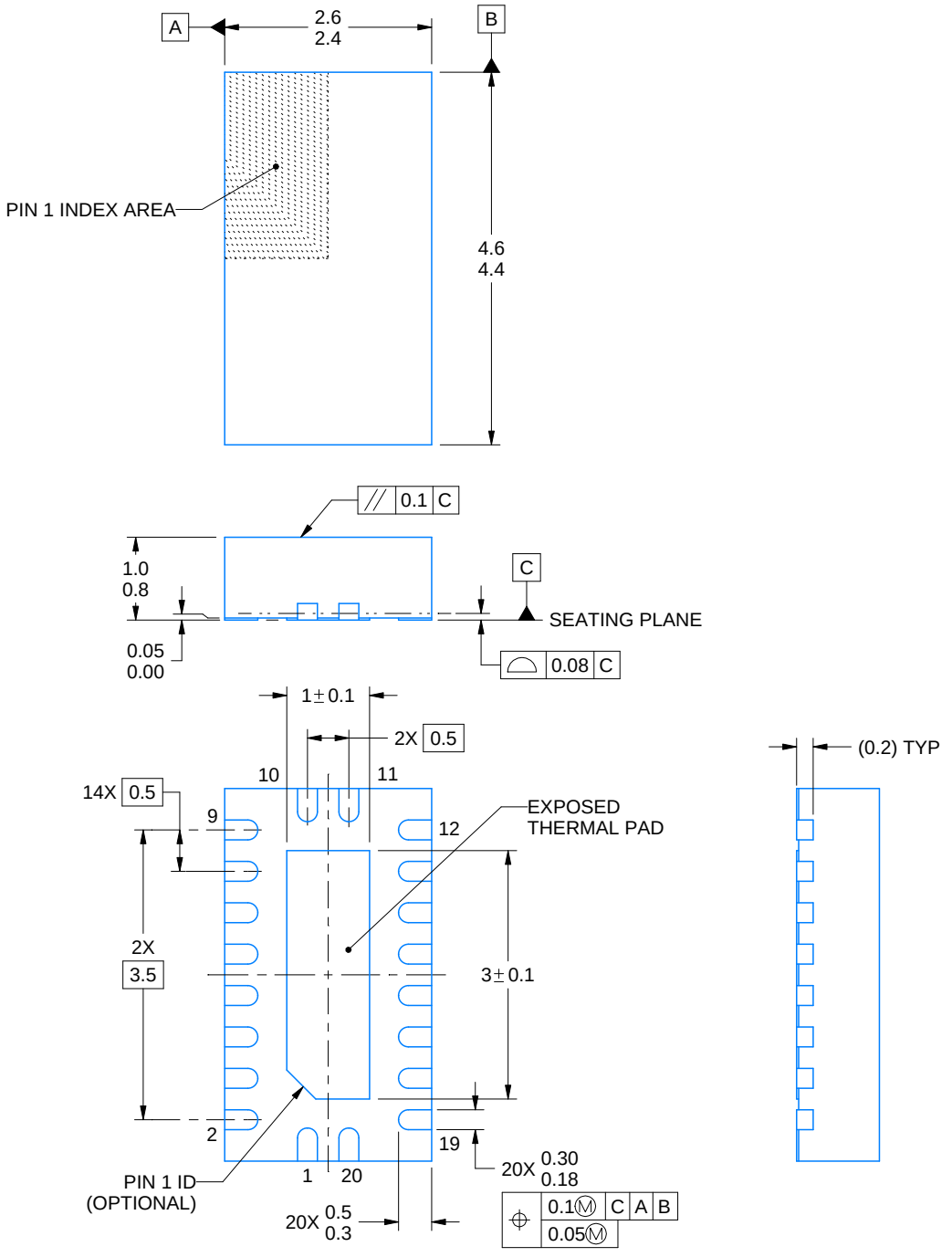


PACKAGE OUTLINE

RKS0020A

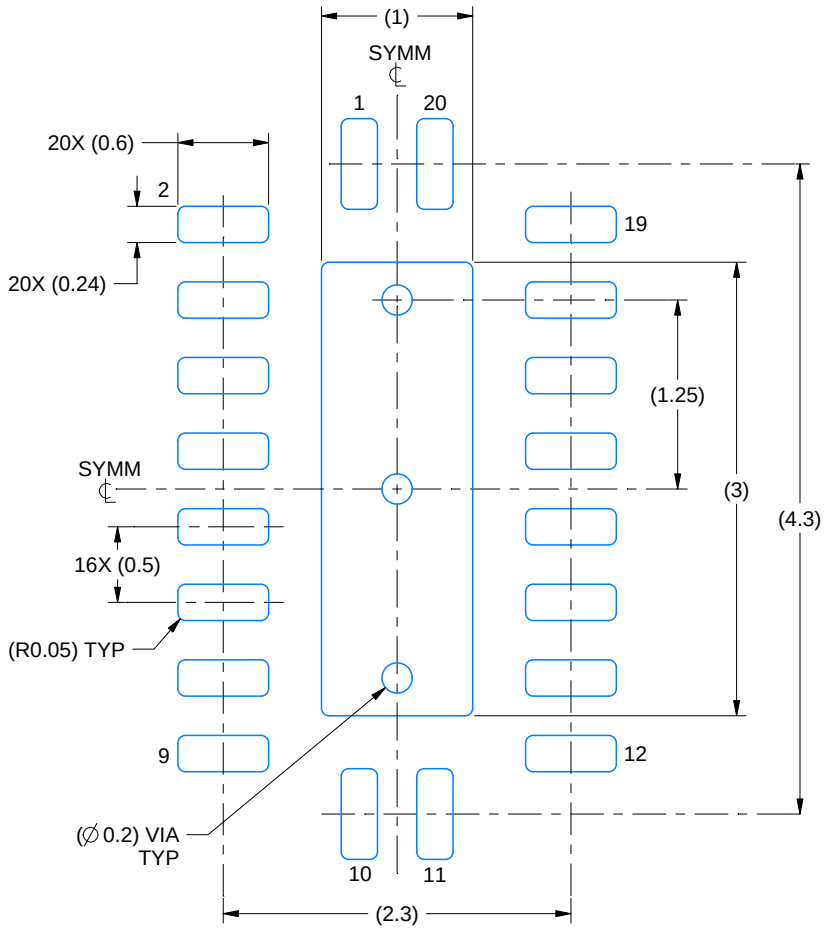
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

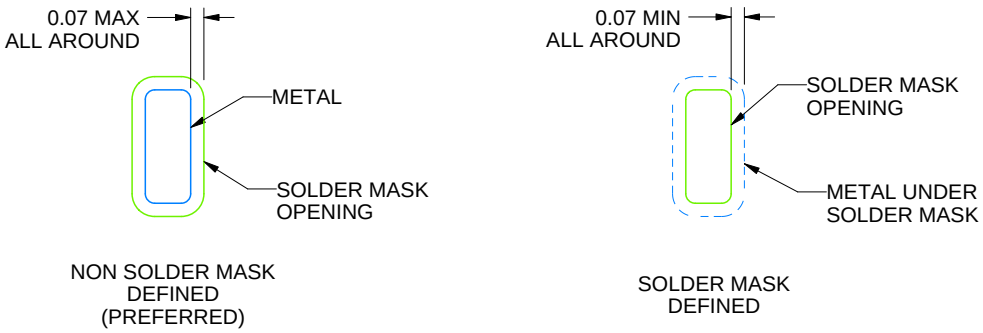


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

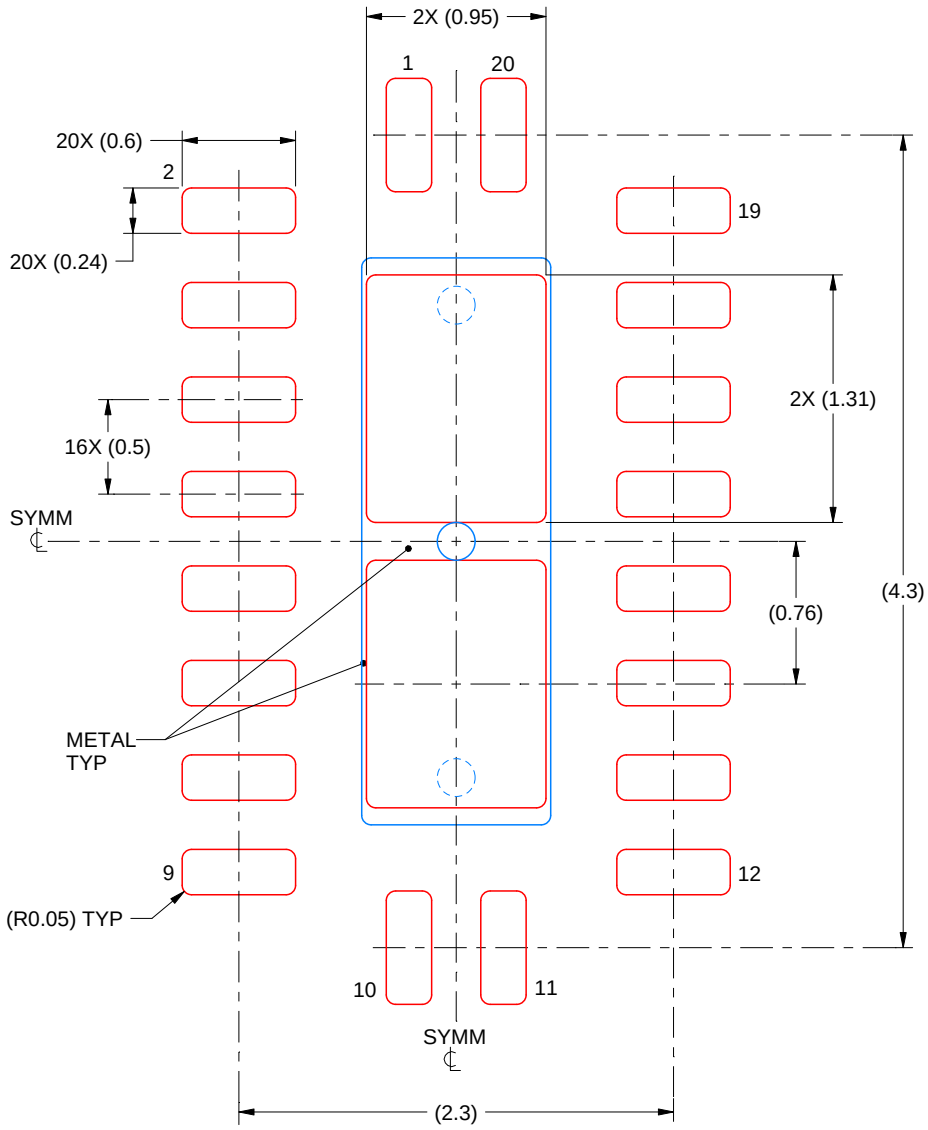


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

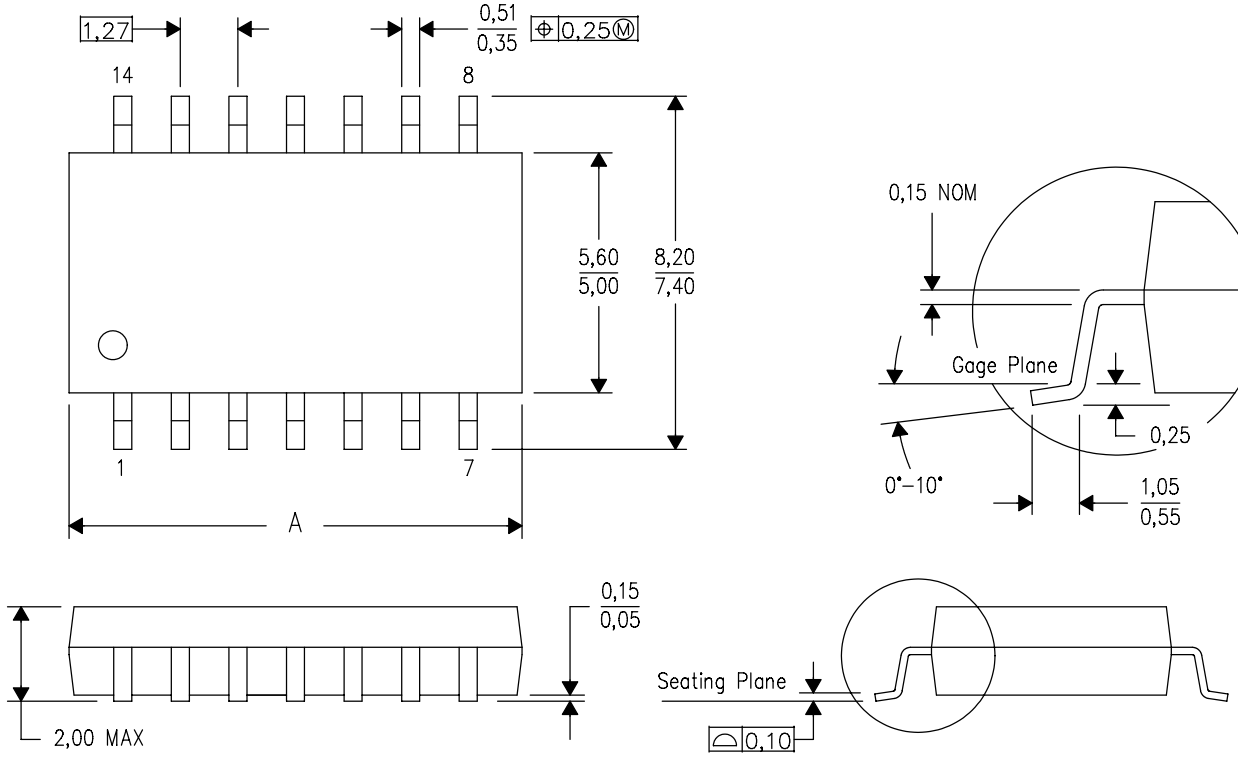
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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最后更新日期：2025 年 10 月