

# SN54ALS561A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

SDAS225A – DECEMBER 1982 – REVISED JANUARY 1995

- Carry Output for n-Bit Cascading
- Buffer-Type Outputs Drive Bus Lines Directly
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

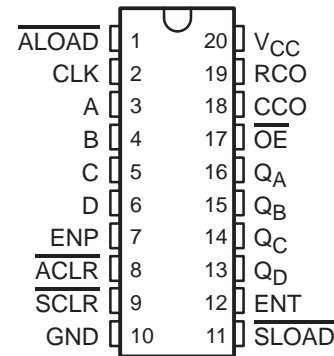
These binary counters are programmable and offer synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either asynchronous clear ( $\overline{\text{ACLR}}$ ) or synchronous clear ( $\text{SCLR}$ ).  $\overline{\text{ACLR}}$  (direct clear) overrides all other functions of the device, while  $\text{SCLR}$  overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to asynchronous load ( $\overline{\text{ALOAD}}$ ) or by the combination of a low level at synchronous load ( $\overline{\text{SLOAD}}$ ) and a positive-going clock transition. The counting function is enabled only when enable P (ENP), enable T (ENT),  $\overline{\text{ACLR}}$ ,  $\overline{\text{ALOAD}}$ ,  $\text{SCLR}$ , and  $\overline{\text{SLOAD}}$  are all high.

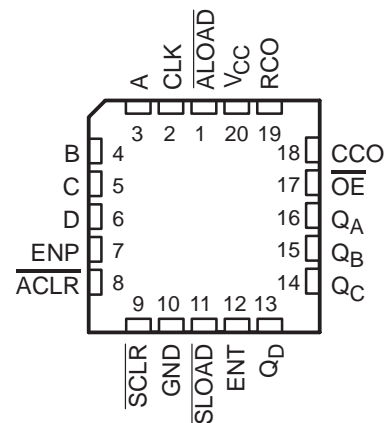
A high level at the output-enable ( $\overline{\text{OE}}$ ) input forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of  $\overline{\text{OE}}$ . ENT is fed forward to enable the ripple-carry output (RCO) to produce a high-level pulse while the count is maximum (15). The clocked carry output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the first counter to ENT of the next counter. However, for very high-speed counting, RCO should be used for cascading because CCO does not become active until the clock returns to the low level.

The SN54ALS561A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS561A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS561A ... J PACKAGE  
SN74ALS561A ... DW OR N PACKAGE  
(TOP VIEW)



SN54ALS561A ... FK PACKAGE  
(TOP VIEW)



# SN54ALS561A, SN74ALS561A

## SYNCHRONOUS 4-BIT COUNTERS

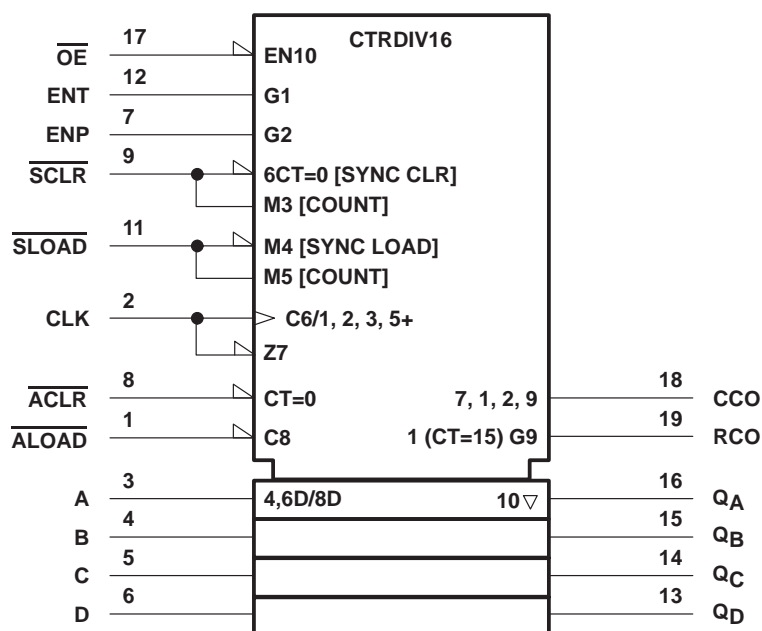
### WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS								OPERATION
$\overline{OE}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	H	H	L	X	X	X	↑	Synchronous clear
L	H	H	H	L	X	X	↑	Synchronous load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit counting
L	H	H	H	H	X	L	X	Inhibit counting

logic symbol†

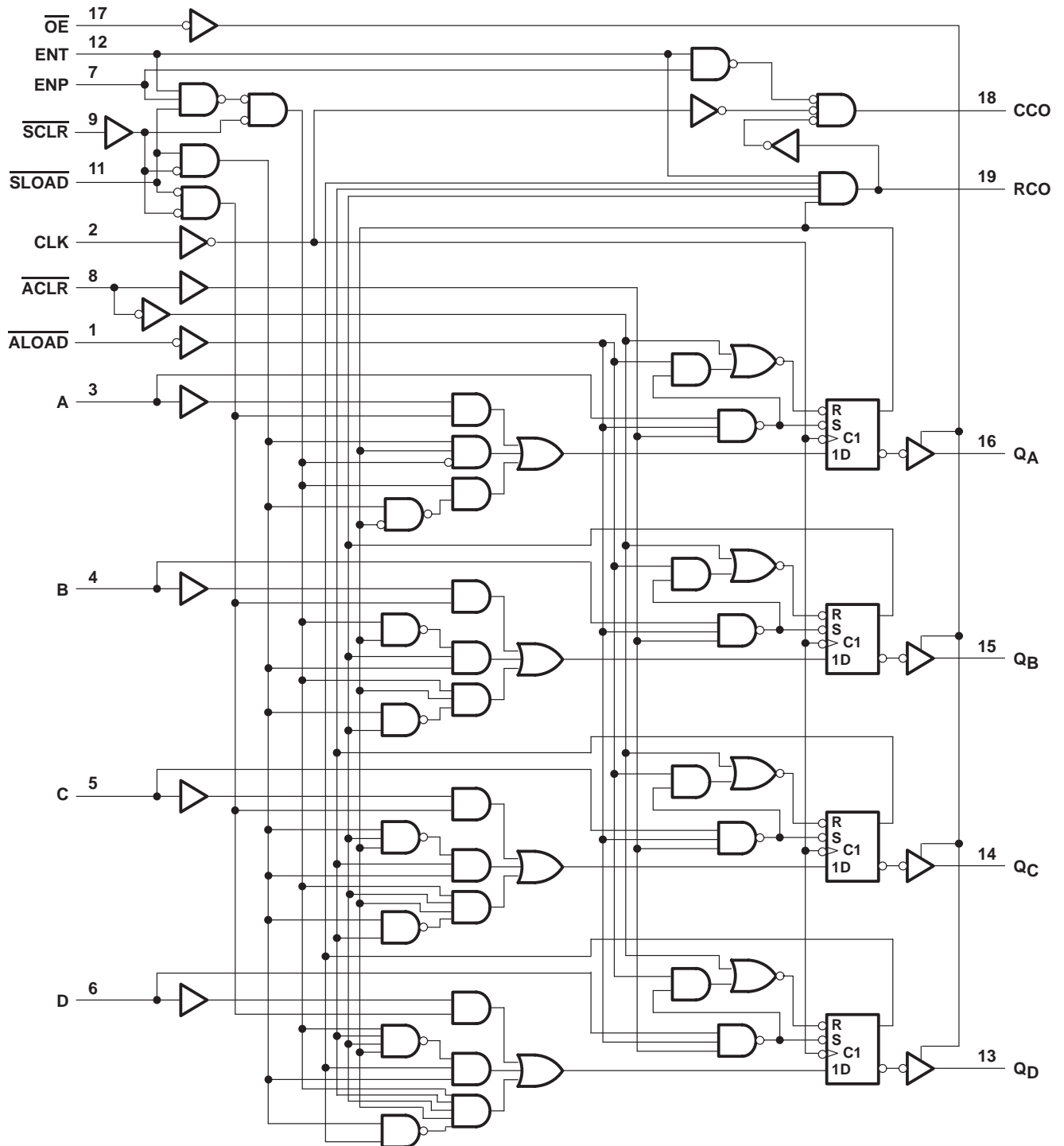


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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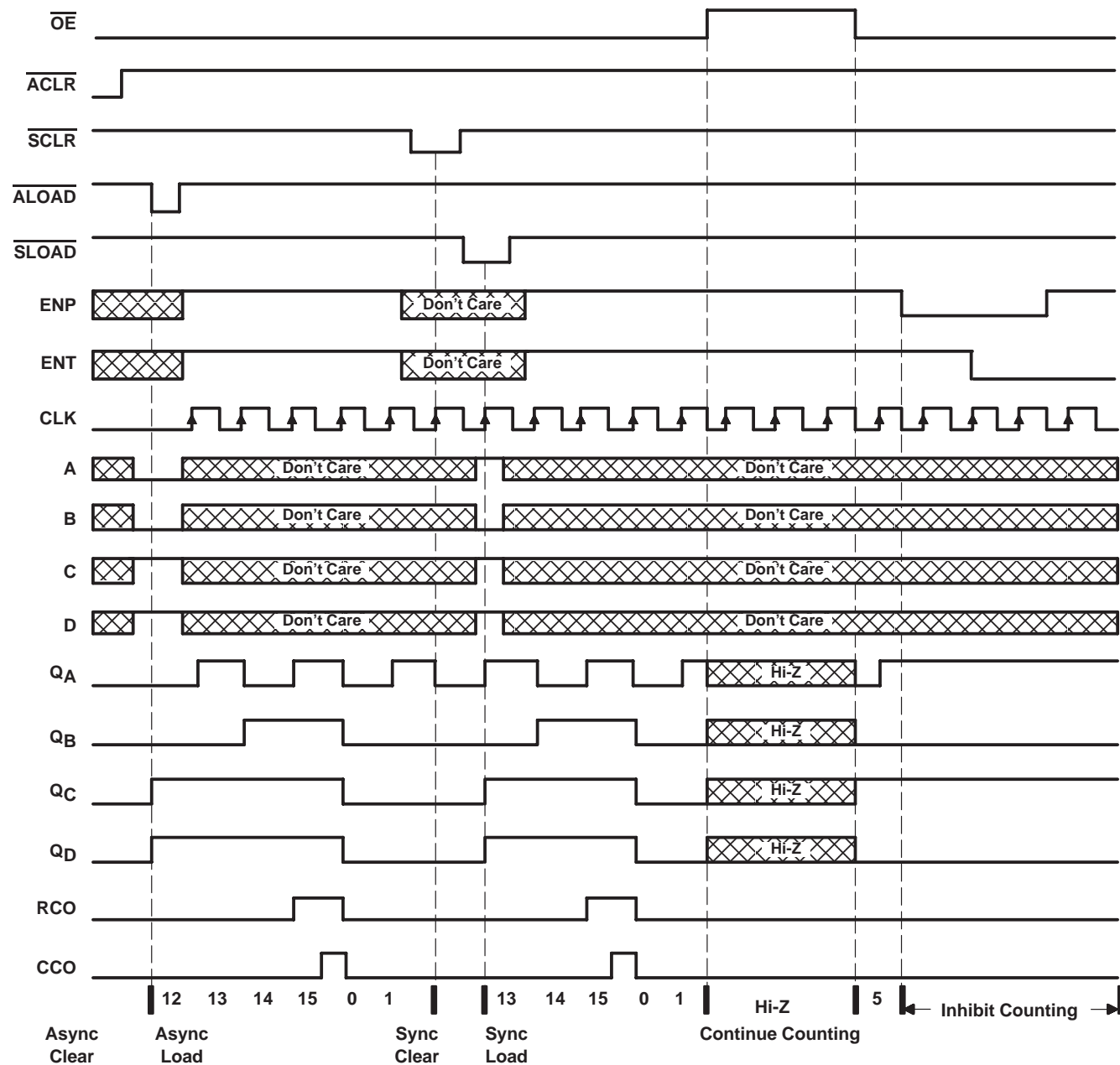
logic diagram (positive logic)



# SN54ALS561A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

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## typical load, count, and inhibit sequences



# SN54ALS561A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS561A	–55°C to 125°C
SN74ALS561A	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

				SN54ALS561A			SN74ALS561A			UNIT		
				MIN	NOM	MAX	MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage			4.5	5	5.5	4.5	5	5.5	V		
V <sub>IH</sub>	High-level input voltage			2			2			V		
V <sub>IL</sub>	Low-level input voltage			0.7			0.8			V		
I <sub>OH</sub>	High-level output current	Q outputs		−1			−2.6			mA		
		CCO and RCO		−0.4			−0.4					
I <sub>OL</sub>	Low-level output current	Q outputs		12			24			mA		
		CCO and RCO		4			8					
f <sub>clock</sub>	Clock frequency			0		20	0		30	MHz		
t <sub>w</sub>	Pulse duration	$\overline{ACL R}$ or $\overline{ALOAD}$ low		20			15			ns		
		CLK high		20			16.5					
		CLK low		25			16.5					
t <sub>su</sub>	Setup time before CLK↑	ENP, ENT	High	25			20			ns		
			Low	25			20					
		Data at A, B, C, D		25			20					
		$\overline{SCLR}$	Low	21			15					
			High (inactive)	35			30					
		$\overline{SLOAD}$	Low	20			15					
			High (inactive)	35			30					
		$\overline{ACL R}$ or $\overline{ALOAD}$ inactive		12			10					
t <sub>h</sub>	Hold time after CLK↑ for data, ENP, ENT, $\overline{SCLR}$ , or $\overline{SLOAD}$			0			0			ns		
T <sub>A</sub>	Operating free-air temperature			−55			125			0	70	°C

# SN54ALS561A, SN74ALS561A

## SYNCHRONOUS 4-BIT COUNTERS

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALS561A		SN74ALS561A		UNIT
				MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA	−1.5		−1.5		V
V <sub>OH</sub>	All outputs	V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = −0.4 mA	V <sub>CC</sub> − 2		V <sub>CC</sub> − 2		V
	Q outputs	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −1 mA	2.4	3.3			
			I <sub>OH</sub> = −2.6 mA			2.4	3.2	
V <sub>OL</sub>	Q outputs	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V
			I <sub>OL</sub> = 24 mA			0.35	0.5	
	CCO and RCO	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4	
			I <sub>OL</sub> = 8 mA			0.35	0.5	
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	20		20		μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V	−20		−20		μA
I <sub>I</sub>	ENP and ENT	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.2		0.2		mA
	Other inputs			0.1		0.1		
I <sub>IH</sub>	ENP and ENT	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	40		40		μA
	Other inputs			20		20		
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V	−0.2		−0.2		mA
I <sub>O‡</sub>	CCO and RCO	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	−15	−70	−15	−70	mA
	Q			−20	−112	−30	−112	
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V	Outputs high	17	27	17	27	mA
			Outputs low	21	33	21	33	
			Outputs disabled	22	36	22	36	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# SN54ALS561A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

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## switching characteristics (see Figure 1)

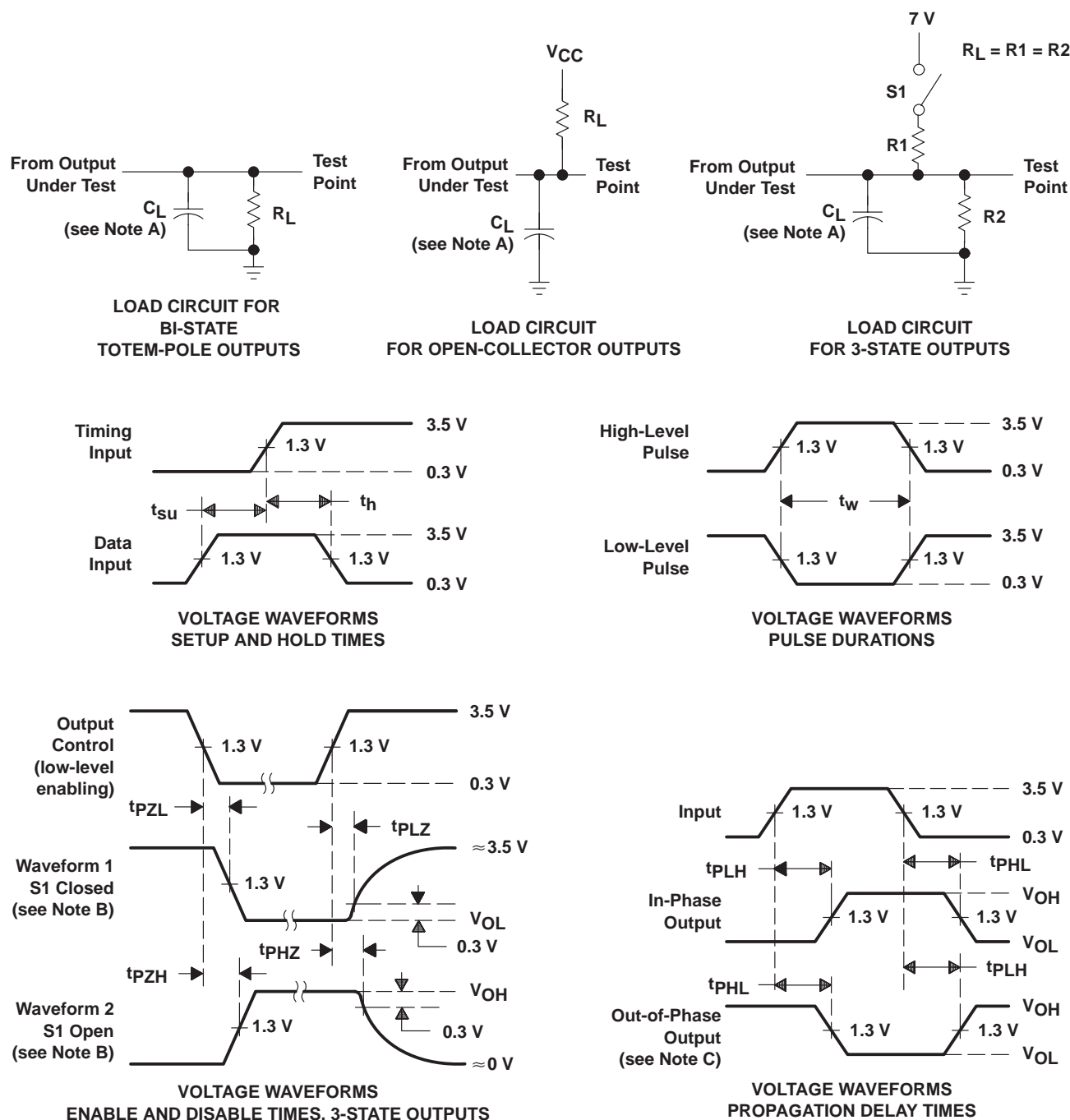
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS561A		SN74ALS561A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			20		30		MHz
t <sub>PLH</sub>	CLK	Any Q	4	15	4	12	ns
t <sub>PHL</sub>			5	21	5	18	
t <sub>PLH</sub>	CLK	RCO	9	35	9	29	ns
t <sub>PHL</sub>			8	29	8	24	
t <sub>PLH</sub>	CLK	CCO	8	35	8	26	ns
t <sub>PHL</sub>			5	20	5	16	
t <sub>PLH</sub>	$\overline{\text{ALOAD}}$	Any Q	10	38	10	35	ns
t <sub>PHL</sub>			7	27	7	23	
t <sub>PLH</sub>	$\overline{\text{ALOAD}}$	RCO	15	50	15	40	ns
t <sub>PHL</sub>			12	35	12	30	
t <sub>PLH</sub>	$\overline{\text{ALOAD}}$	CCO	25	65	25	55	ns
t <sub>PHL</sub>			12	42	12	33	
t <sub>PLH</sub>	A, B, C, or D	Any Q	8	35	8	30	ns
t <sub>PHL</sub>			7	27	7	22	
t <sub>PLH</sub>	ENT	RCO	5	20	5	16	ns
t <sub>PHL</sub>			4	18	4	14	
t <sub>PLH</sub>	ENT	CCO	12	35	12	32	ns
t <sub>PHL</sub>			4	15	4	12	
t <sub>PLH</sub>	ENP	CCO	5	22	5	18	ns
t <sub>PHL</sub>			4	14	4	12	
t <sub>PHL</sub>	$\overline{\text{ACLR}}$	Any Q	7	28	7	22	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any Q	5	24	5	19	ns
t <sub>PZL</sub>			8	28	8	23	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any Q	2	12	2	10	ns
t <sub>PLZ</sub>			2	20	4	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS561A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74ALS561AN</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS561AN
SN74ALS561AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS561AN

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

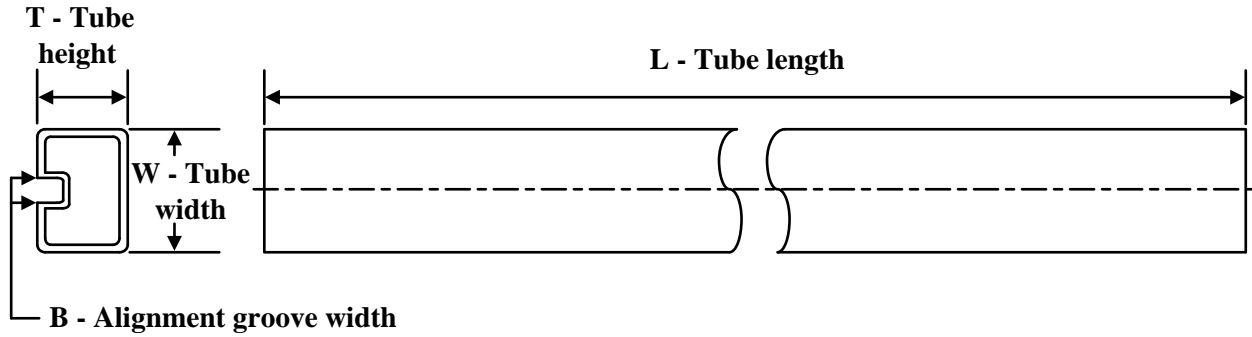
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TUBE



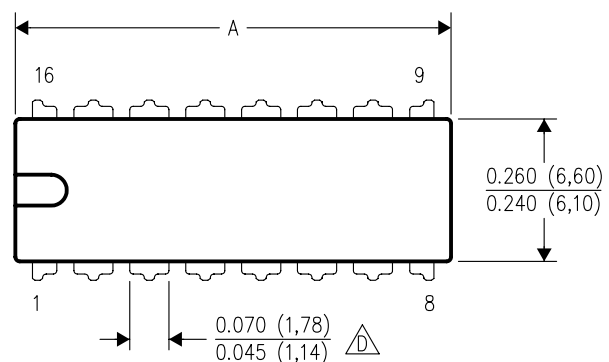
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS561AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS561AN.A	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

16 PINS SHOWN



## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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