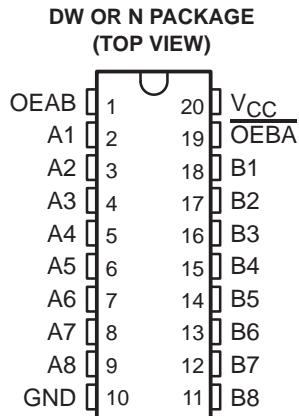


SN74ALS620A, SN74ALS621A, SN74ALS623A, SN74AS623 OCTAL BUS TRANSCEIVERS

SDAS226A – DECEMBER 1982 – REVISED JANUARY 1995

- Local Bus-Latch Capability
- Choice of True or Inverting Logic
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DEVICE	OUTPUT	LOGIC
SN74ALS620A	3 state	Inverting
SN74ALS621A	Open collector	True
SN74ALS623A, SN74AS623	3 state	True



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

The output-enable inputs disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and OEBA. Each output reinforces its input in this transceiver configuration. When both OEAB and OEBA are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical for the SN74ALS621A, SN74ALS623A, and SN74AS623 or complementary for the SN74ALS620A.

The -1 versions of the SN74ALS620A and SN74ALS621A are identical to the standard versions, except that the recommended maximum I_{OL} is increased to 48 mA in the -1 versions.

The SN74ALS620A, SN74ALS621A, SN74ALS623A, and SN74AS623 are characterized for operation from 0°C to 70°C.

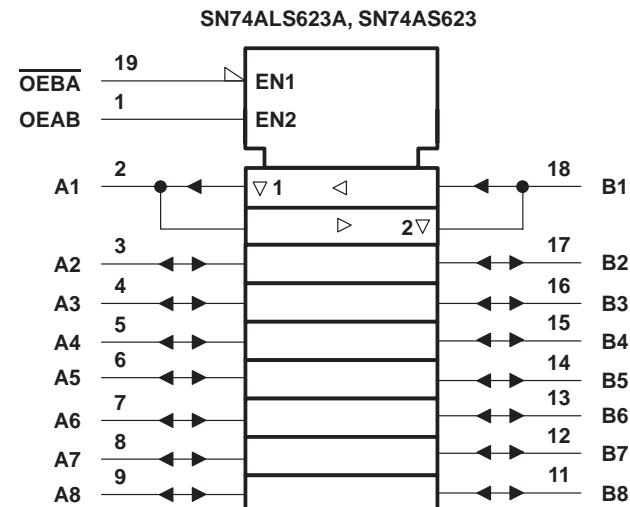
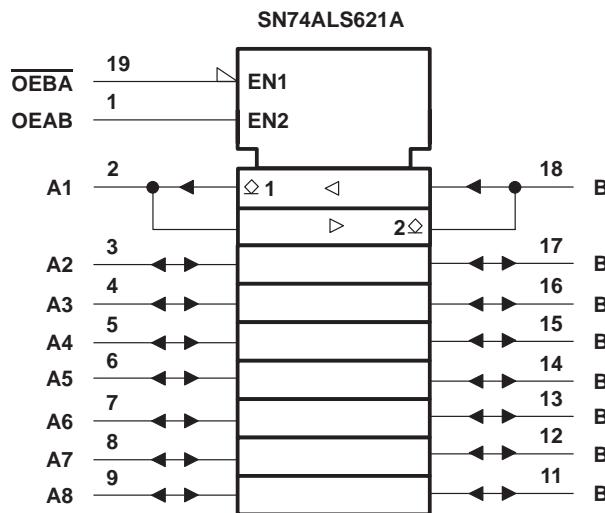
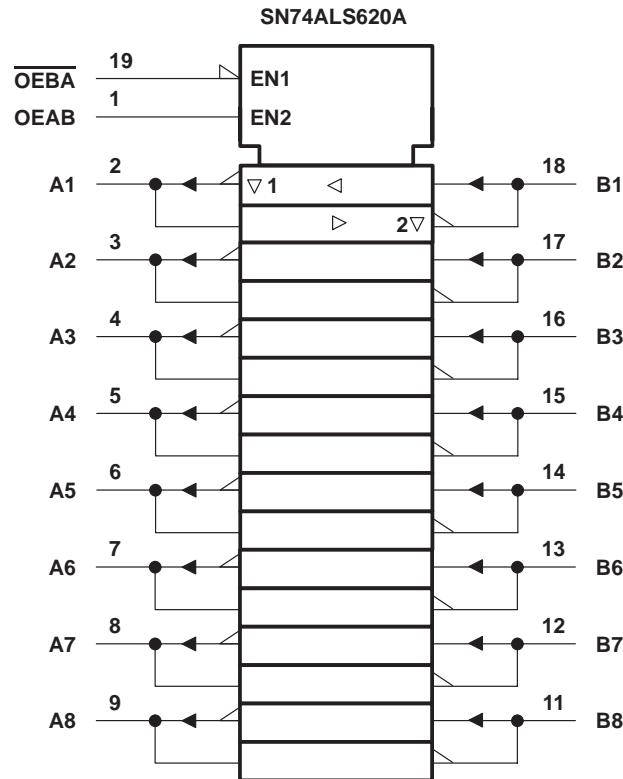
FUNCTION TABLE

INPUTS		OPERATION	
OEBA	OEAB	SN74ALS620A	SN74ALS621A SN74ALS623A SN74AS623
L	L	\bar{B} data to A bus	B data to A bus
H	H	\bar{A} data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	\bar{B} data to A bus, A data to B bus	B data to A bus, A data to B bus

SN74ALS620A, SN74ALS621A, SN74ALS623A, SN74AS623 OCTAL BUS TRANSCEIVERS

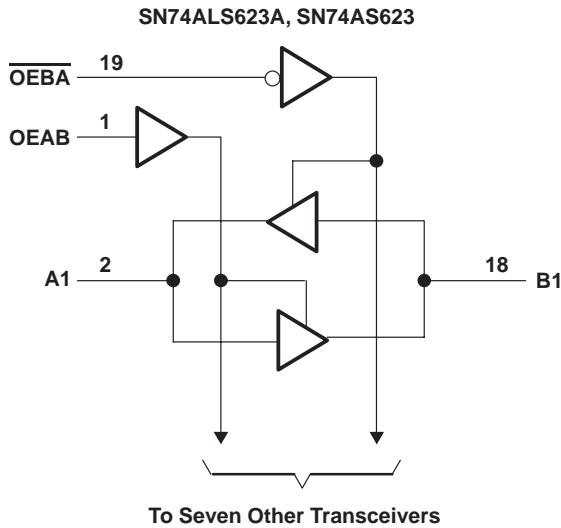
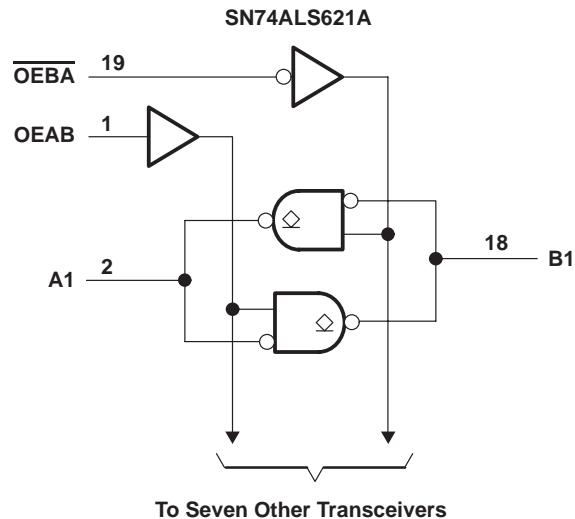
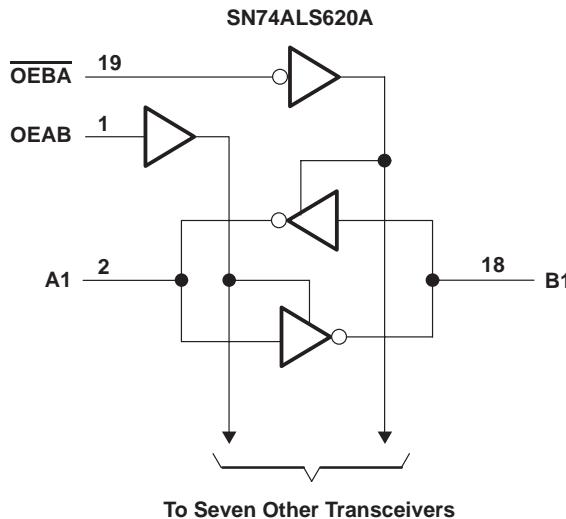
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logic symbols[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN74ALS620A, SN74ALS623A	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS620A, SN74ALS621A, SN74ALS623A, SN74AS623 OCTAL BUS TRANSCEIVERS

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recommended operating conditions

		SN74ALS620A SN74ALS623A			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2		V	
V _{IL}	Low-level input voltage	0.8		V	
I _{OH}	High-level output current	-15		mA	
I _{OL}	Low-level output current	24		mA	
T _A	Operating free-air temperature	0	70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			UNIT
		MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA		-1.2	V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} = 2		V
		V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4 3.2	
			I _{OH} = -15 mA	2	
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25 0.4	V
			I _{OL} = 24 mA‡	0.35 0.5	
I _I	Control inputs	V _{CC} = 5.5 V	V _I = 7 V	0.1	mA
	A or B ports		V _I = 5.5 V	0.1	
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V		20	μA
	A or B ports§			20	
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V		-0.1	mA
	A or B ports§			-0.1	
I _O ¶		V _{CC} = 5.5 V, V _O = 2.25 V		-30 -112	mA
I _{CC}	SN74ALS620A	V _{CC} = 5.5 V	Outputs high	24 34	mA
			Outputs low	31 44	
			Outputs disabled	33 47	
	SN74ALS623A	V _{CC} = 5.5 V	Outputs high	32 43	
			Outputs low	39 50	
			Outputs disabled	42 55	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN74ALS620A		SN74ALS623A			
			MIN	MAX	MIN	MAX		
t_{PLH}	A	B	2	10	2	13	ns	
t_{PHL}			2	10	3	11		
t_{PLH}	B	A	2	10	2	13	ns	
t_{PHL}			2	10	3	11		
t_{PZH}	OEBA	A	3	17	5	22	ns	
t_{PZL}			5	25	5	22		
t_{PHZ}	OEBA	A	2	12	2	16	ns	
t_{PLZ}			3	18	2	19		
t_{PZH}	OEAB	B	3	18	5	22	ns	
t_{PZL}			5	25	5	22		
t_{PHZ}	OEAB	B	2	12	2	16	ns	
t_{PLZ}			3	18	2	19		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs and I/O ports	7 V
Operating free-air temperature range, T_A : SN74ALS621A	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS621A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
				48 [§]	mA
T_A	Operating free-air temperature	0		70	°C

[§] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

SN74ALS620A, SN74ALS621A, SN74ALS623A, SN74AS623 OCTAL BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ALS621A			UNIT
		MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5	V
I_{OH}	$V_{CC} = 4.5 \text{ V}$, $V_{OH} = 5.5 \text{ V}$			0.1	mA
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 24 \text{ mA}$	0.35	0.5	V
		$I_{OL} = 48 \text{ mA}^{\ddagger}$	0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 7 \text{ V}$	0.1	mA
	A or B ports		$V_I = 5.5 \text{ V}$	0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		20	μA
	A or B ports \S			20	
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.1	mA
	A or B ports \S			-0.1	
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	29	40	mA
		Outputs low	35	48	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

\S For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 680 \Omega$, $T_A = \text{MIN to MAX}^{\dagger}$		UNIT	
			SN74ALS621A			
			MIN	MAX		
t_{PLH}	A	B	10	33	ns	
			5	20		
t_{PLH}	B	A	10	33	ns	
			5	20		
t_{PLH}	\overline{OEBA}	A	10	39	ns	
			12	35		
t_{PLH}	OEAB	B	10	39	ns	
			12	35		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN74AS623	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74AS623			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS623			UNIT
			MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC} = 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		
		$I_{OH} = -15$ mA	2			
V_{OL}	$V_{CC} = 4.5$ V,	$I_{OL} = 64$ mA	0.35	0.55		V
I_I	Control inputs	$V_{CC} = 5.5$ V	$V_I = 7$ V		0.1	mA
	A or B ports		$V_I = 5.5$ V		0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V		20	μ A
	A or B ports§				70	
I_{IL}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V		-0.5	mA
	A or B ports§				-0.75	
I_O ¶	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	-30	-150		mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high	57	93		mA
		Outputs low	16	189		
		Outputs disabled	71	116		

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS620A, SN74ALS621A, SN74ALS623A, SN74AS623 OCTAL BUS TRANSCEIVERS

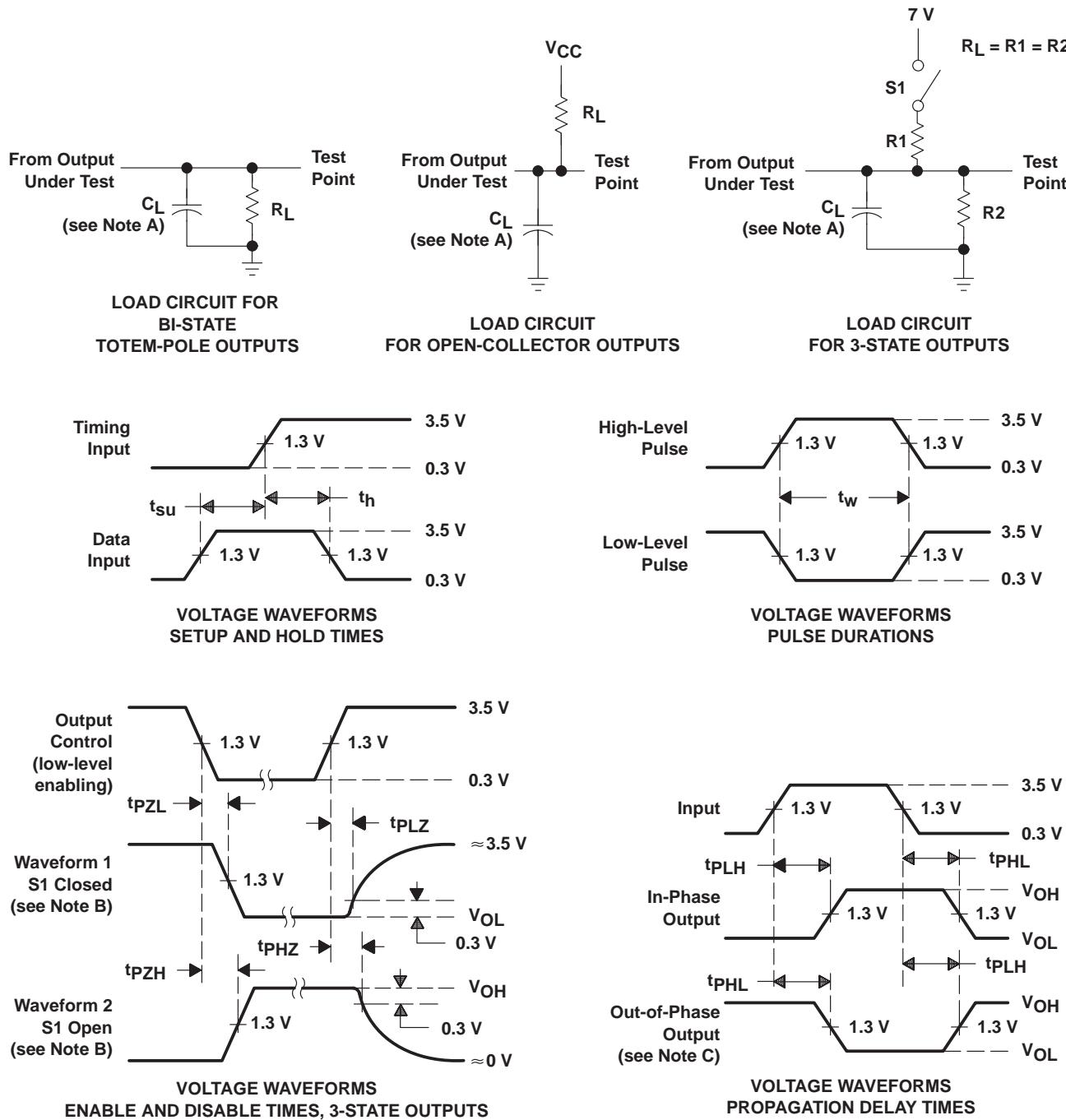
SDAS226A – DECEMBER 1982 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R1 = 500\text{ }\Omega,$ $R2 = 500\text{ }\Omega,$ $T_A = \text{MIN to MAX}^{\dagger}$	UNIT	
			SN74AS623		
			MIN	MAX	
t_{PLH}	A	B	1	9	ns
t_{PHL}			1	8	
t_{PLH}	B	A	1	9	ns
t_{PHL}			1	8.5	
t_{PZH}	$\overline{\text{OEBA}}$	A	2	11	ns
t_{PZL}			2	10	
t_{PHZ}	$\overline{\text{OEBA}}$	A	1	7.5	ns
t_{PLZ}			1	11.5	
t_{PZH}	$\overline{\text{OEAB}}$	B	2	11.5	ns
t_{PZL}			2	11	
t_{PHZ}	$\overline{\text{OEAB}}$	B	1	7	ns
t_{PLZ}			1	9	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- When measuring propagation delay items of 3-state outputs, switch S1 is open.
- All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS620ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS620A
SN74ALS620ADW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS620A
SN74ALS620AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS620AN
SN74ALS620AN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS620AN
SN74ALS621A-1N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621A-1N
SN74ALS621A-1N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621A-1N
SN74ALS621ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS621A
SN74ALS621ADW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS621A
SN74ALS621AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621AN
SN74ALS621AN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621AN
SN74ALS623ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A
SN74ALS623ADW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A
SN74ALS623AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS623AN
SN74ALS623AN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS623AN
SN74ALS623ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A
SN74ALS623ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

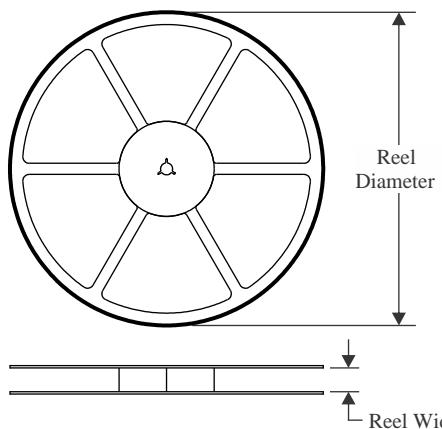
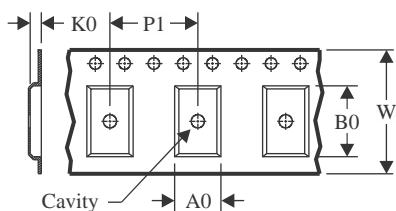
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

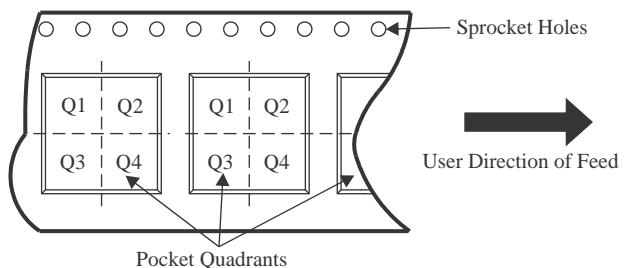
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


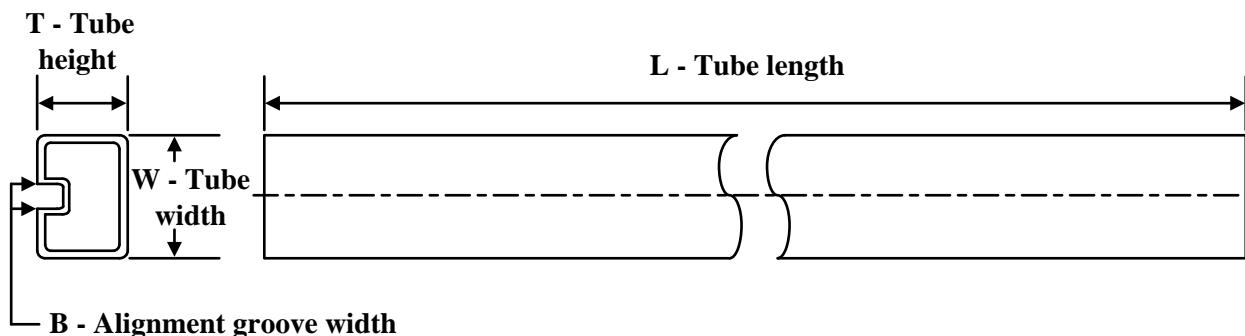
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS623ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS623ANSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE


*All dimensions are nominal

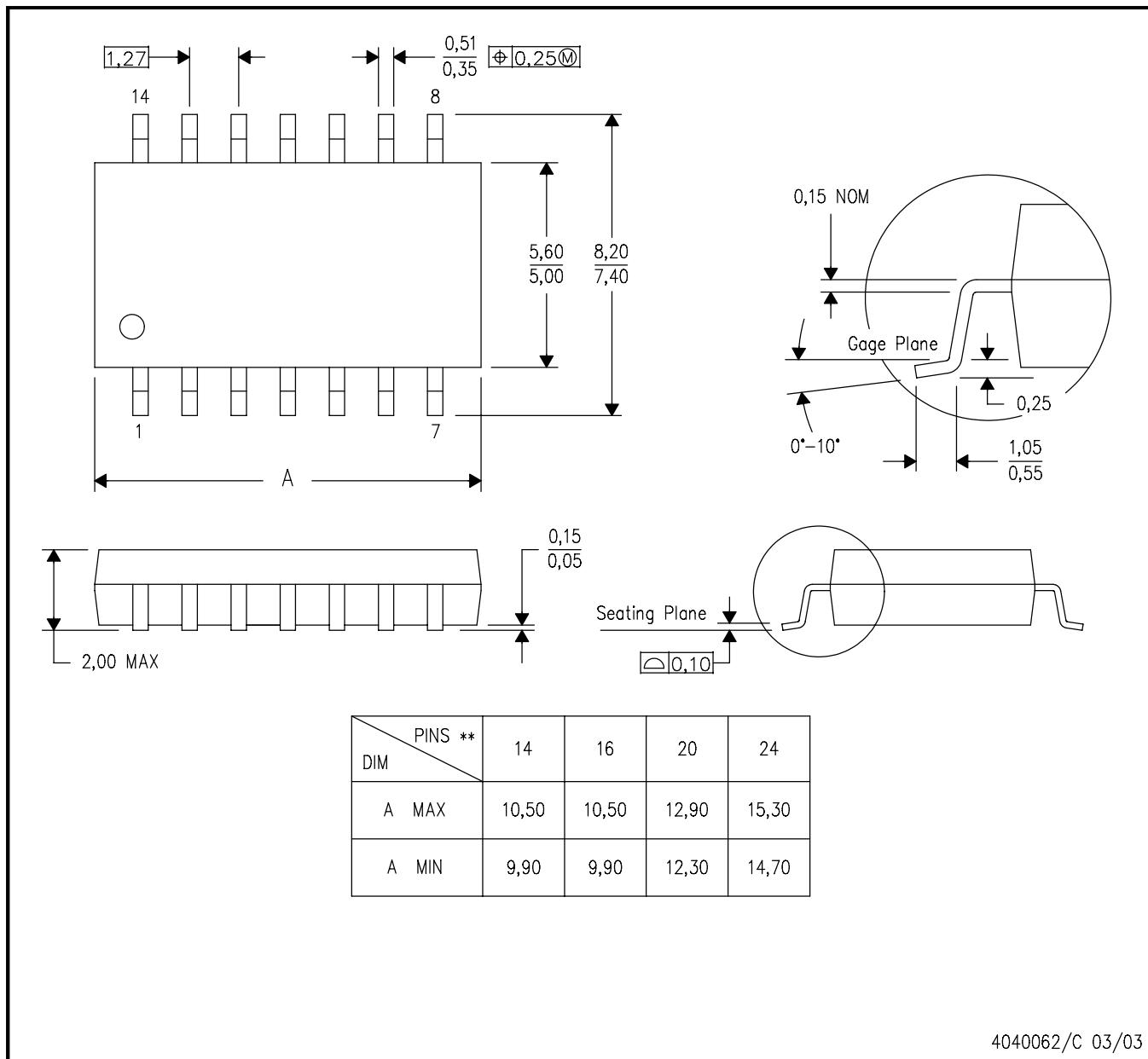
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS620ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS620ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS620AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS620AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621A-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621A-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS621ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS621AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS623ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS623ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS623AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS623AN.A	N	PDIP	20	20	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

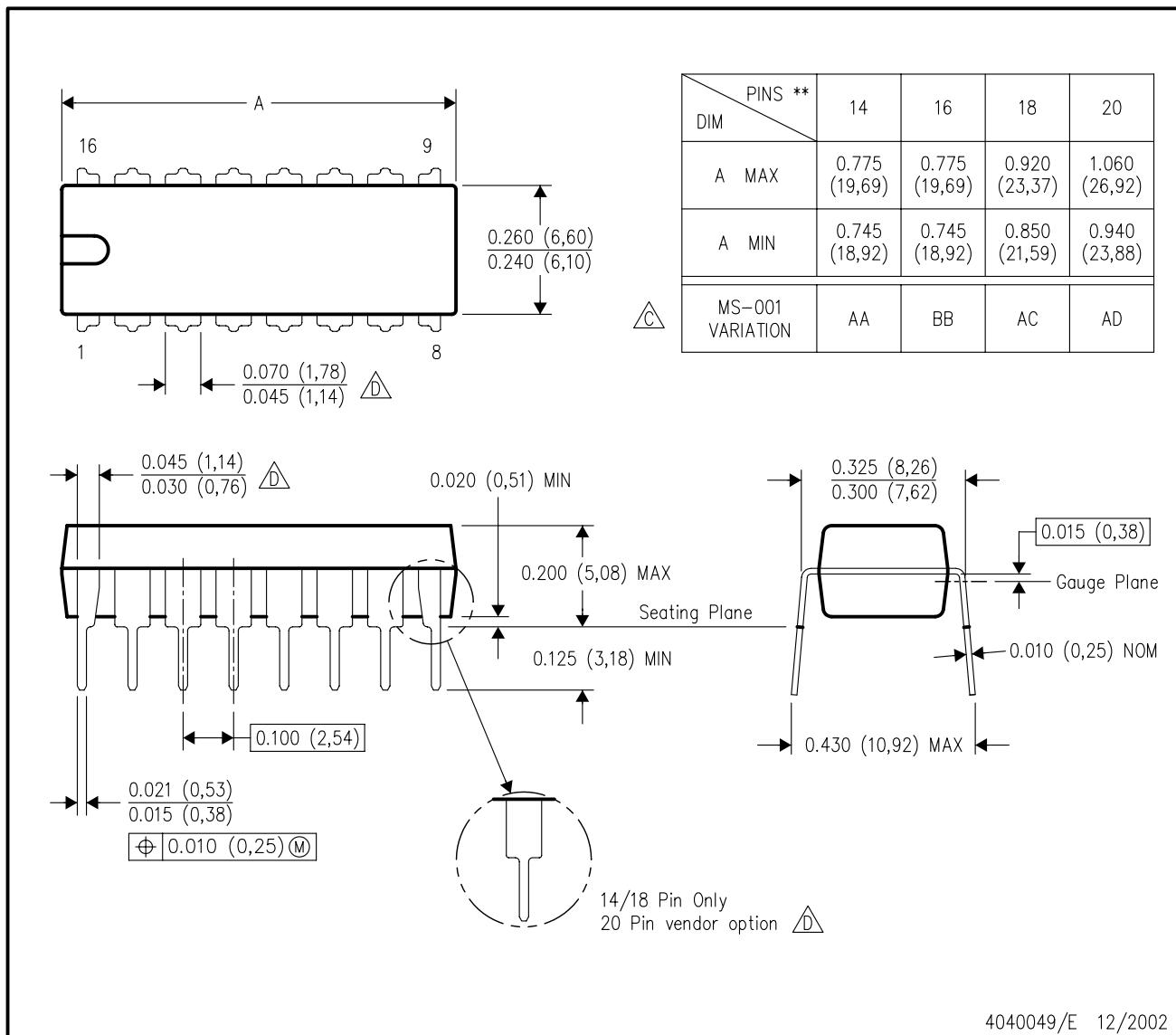


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

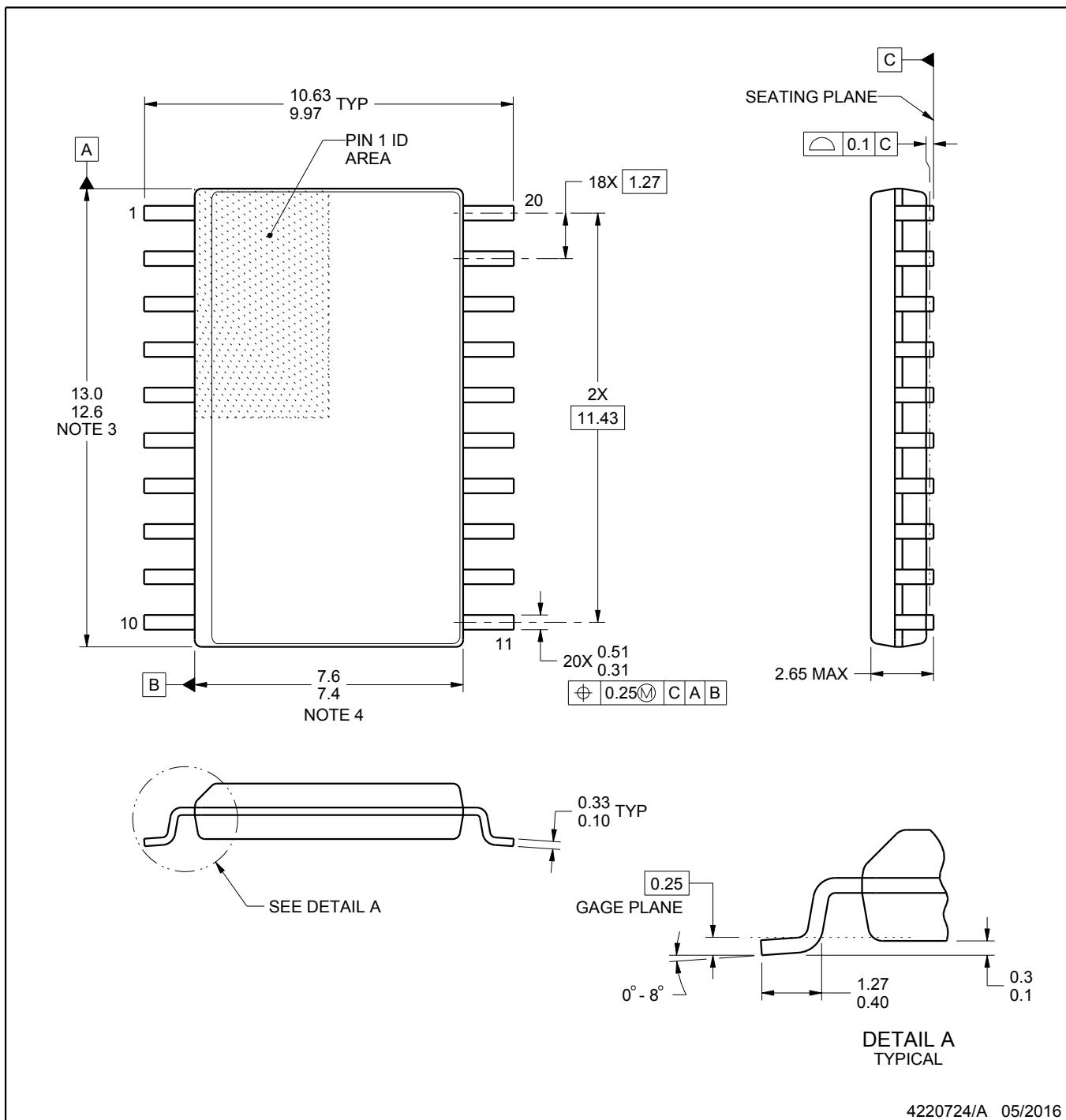
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

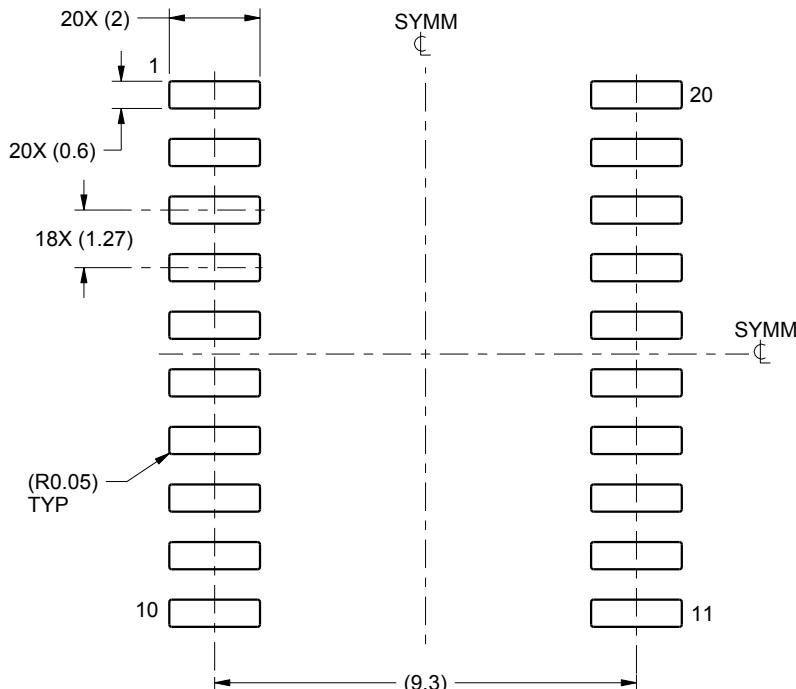
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

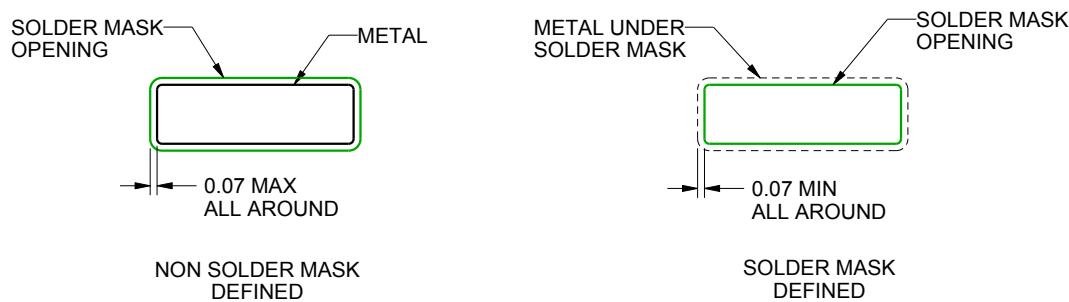
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

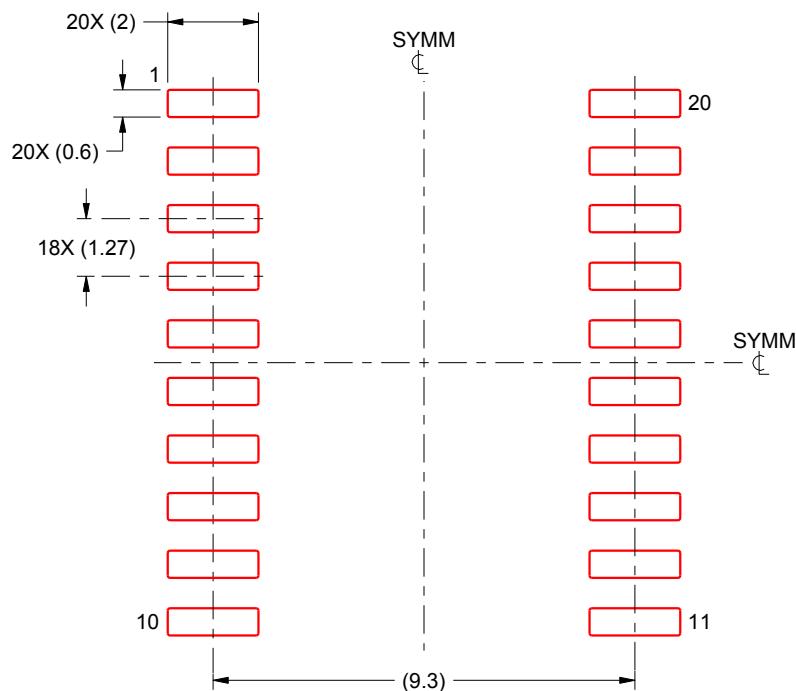
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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