

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 3.2 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Ideal for Use in PC100 Register DIMM
- Designed to Comply With JEDEC 168-Pin and 200-Pin SDRAM Buffered DIMM Specification
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

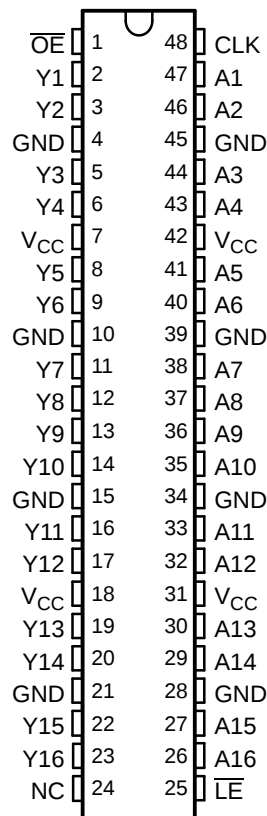
DESCRIPTION/ORDERING INFORMATION

This 16-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is low. When $\overline{LE}$ is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVC16334DL	ALVC16334
		Tape and reel	SN74ALVC16334DLR	
	TSSOP - DGG	Tape and reel	SN74ALVC16334DGGR	ALVC16334
	TVSOP - DGV	Tape and reel	SN74ALVC16334DGVR	VC334

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Widebus is a trademark of Texas Instruments.

SN74ALVC16334

16-BIT UNIVERSAL BUS DRIVER

WITH 3-STATE OUTPUTS

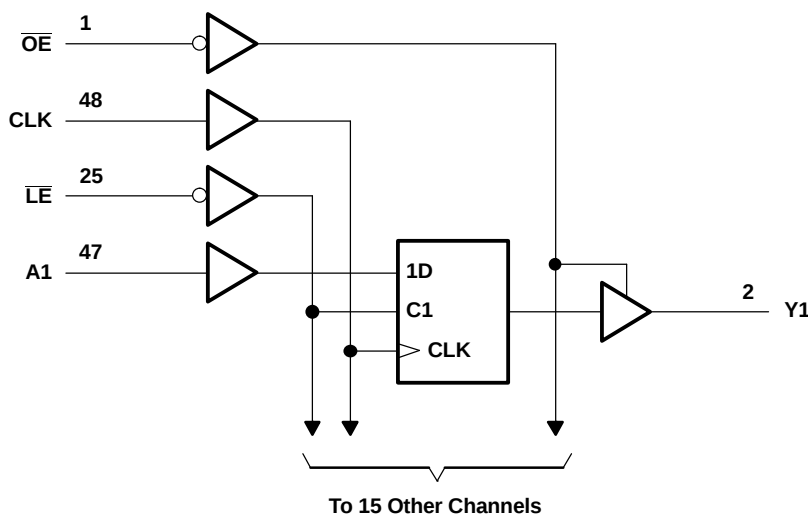
SCES128E—FEBRUARY 1998—REVISED SEPTEMBER 2004

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{OE}$	$\overline{LE}$	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	$\uparrow$	L	L
L	H	$\uparrow$	H	H
L	H	L or H	X	$Y_0^{(1)}$

(1) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage range		-0.5	4.6	V	
V _I	Input voltage range ⁽²⁾		-0.5	4.6	V	
V _O	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0			-50	mA
I _{OK}	Output clamp current	V _O < 0			-50	mA
I _O	Continuous output current				±50	mA
Continuous current through each V _{CC} or GND					±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package			58	°C/W
		DGV package			48	
		DL package			63	
T _{stg}	Storage temperature range		-65	150	°C	

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 4.6 V maximum.
- The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-4	mA
		V _{CC} = 2.3 V	-12	
		V _{CC} = 2.7 V	-12	
		V _{CC} = 3 V	-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	12	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V
		I _{OH} = -4 mA	1.65 V	1.2			
		I _{OH} = -6 mA	2.3 V	2			
	I _{OH} = -12 mA		2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
	I _{OH} = -24 mA	3 V	2				
V _{OL}		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 6 mA	2.3 V			0.4	
	I _{OL} = 12 mA		2.3 V			0.7	
			2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND		3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND		3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0		3.6 V			40	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	5			pF
	Data inputs			5.5			
C _o	Outputs	V _O = V _{CC} or GND	3.3 V	7.5			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVC16334

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCES128E—FEBRUARY 1998—REVISED SEPTEMBER 2004

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency			(1)		150		150		150		MHz	
t_w	Pulse duration	$\overline{LE}$ low		(1)		3.3		3.3		3.3		ns	
		CLK high or low		(1)		3.3		3.3		3.3			
t_{su}	Setup time	Data before CLK $\uparrow$		(1)		1.4		1.7		1.5		ns	
		Data before $\overline{LE}\uparrow$	CLK high		(1)		1.2		1.6		1.3		
			CLK low		(1)		1.4		1.5		1.2		
t_h	Hold time	Data after CLK $\uparrow$		(1)		0.9		0.9		0.9		ns	
		Data after $\overline{LE}\uparrow$	CLK high or low		(1)		1.1		1.1		1.1		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		150		150		150		MHz
t_{pd}	A	Y	(1)		1	3.7	3.6		1.1	3.3	ns
	$\overline{LE}$		(1)		1	4.8	5		1.3	4.4	
	CLK		(1)		1	4.4	4.5		1	4.1	
t_{en}	$\overline{OE}$	Y	(1)		1	5.4	5.4		1.1	4.6	ns
t_{dis}	$\overline{OE}$	Y	(1)		1	4.1	4.5		1.7	4.4	ns

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

from 0°C to 65°C, $C_L = 50\text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_{pd}	A	Y	1.2	3.2	ns
	CLK		1.1	4	

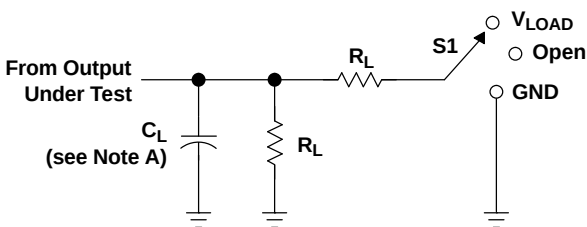
OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Outputs enabled	$C_L = 0, \quad f = 10\text{ MHz}$	(1)	31	36	pF
	Outputs disabled		(1)	7	11	

(1) This information was not available at the time of publication.

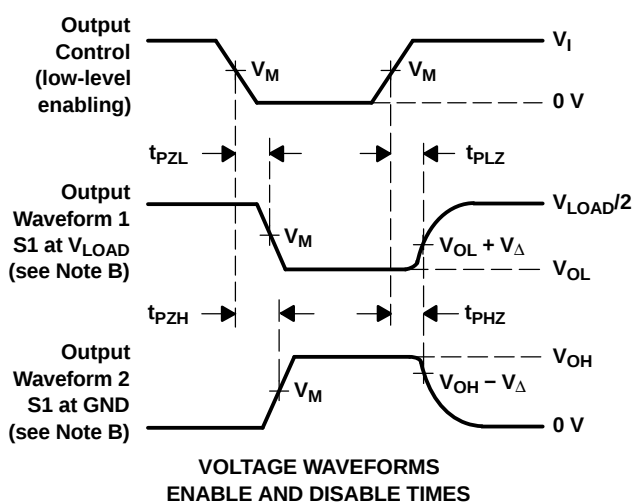
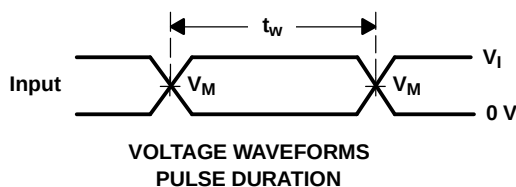
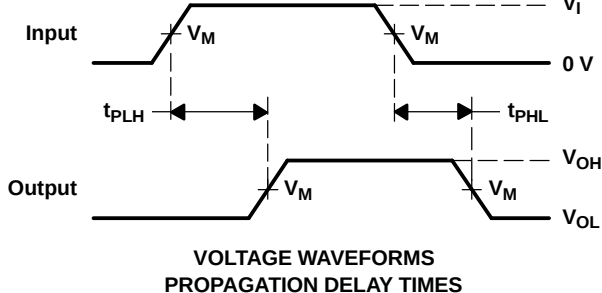
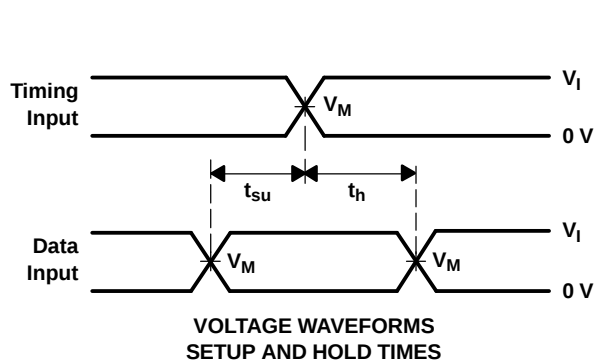
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3 V $\pm$ 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50$ Ω .
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVC16334DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16334
SN74ALVC16334DGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16334
SN74ALVC16334DGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VC334
SN74ALVC16334DGVR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VC334
SN74ALVC16334DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16334
SN74ALVC16334DL.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16334

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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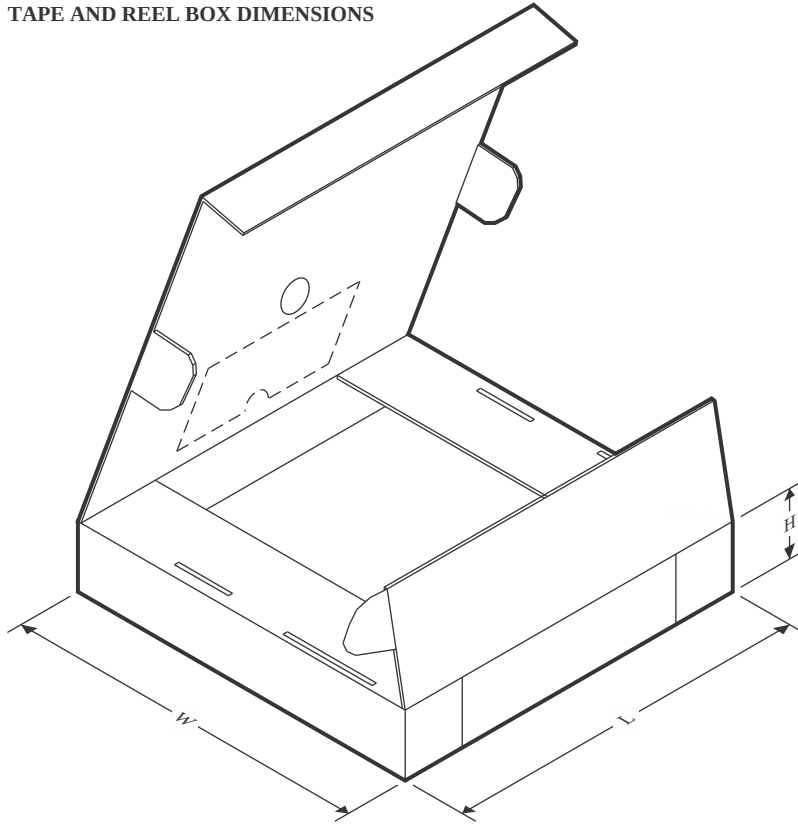
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVC16334DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVC16334DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVC16334DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74ALVC16334DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0

TUBE

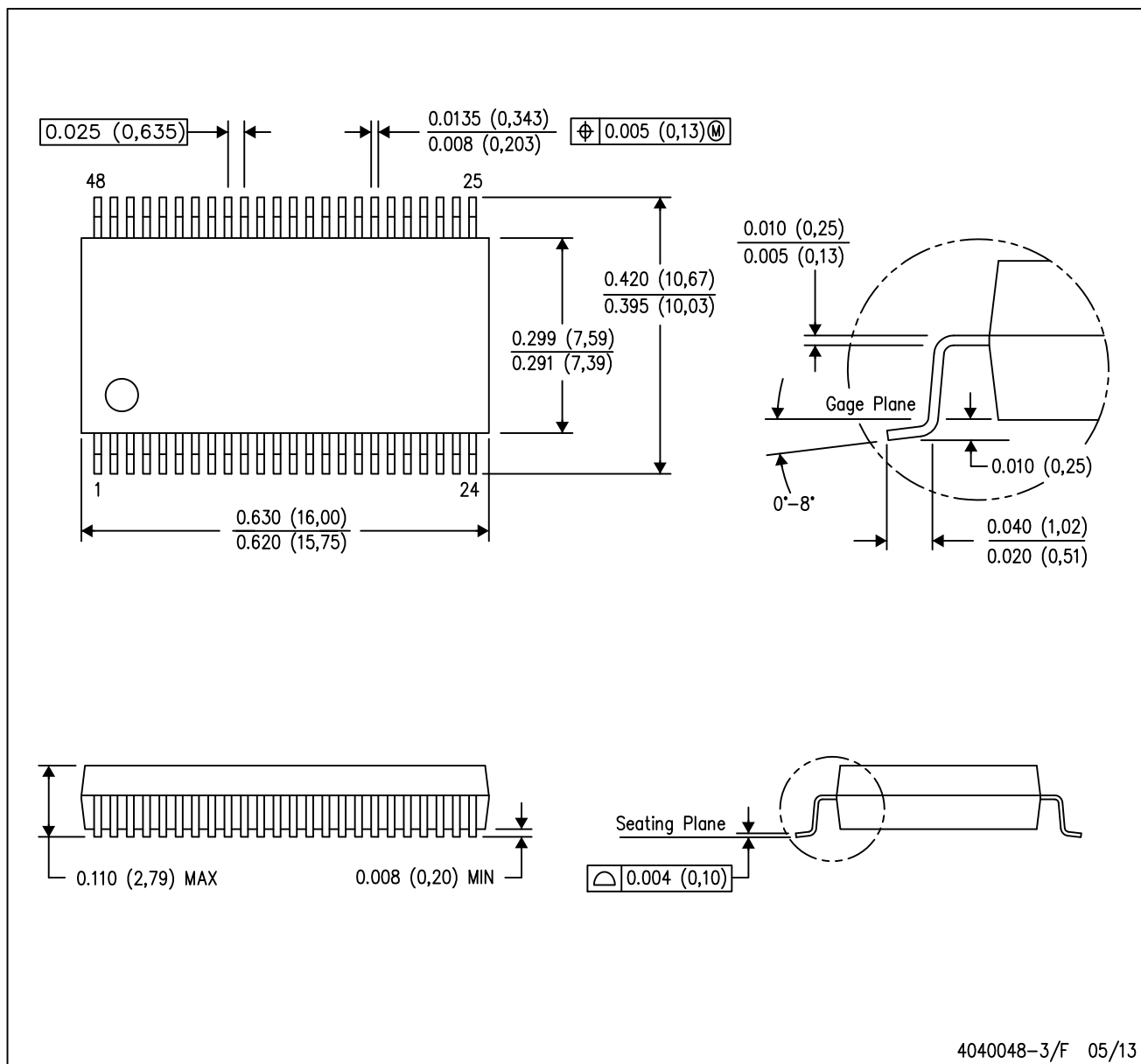


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALVC16334DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ALVC16334DL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

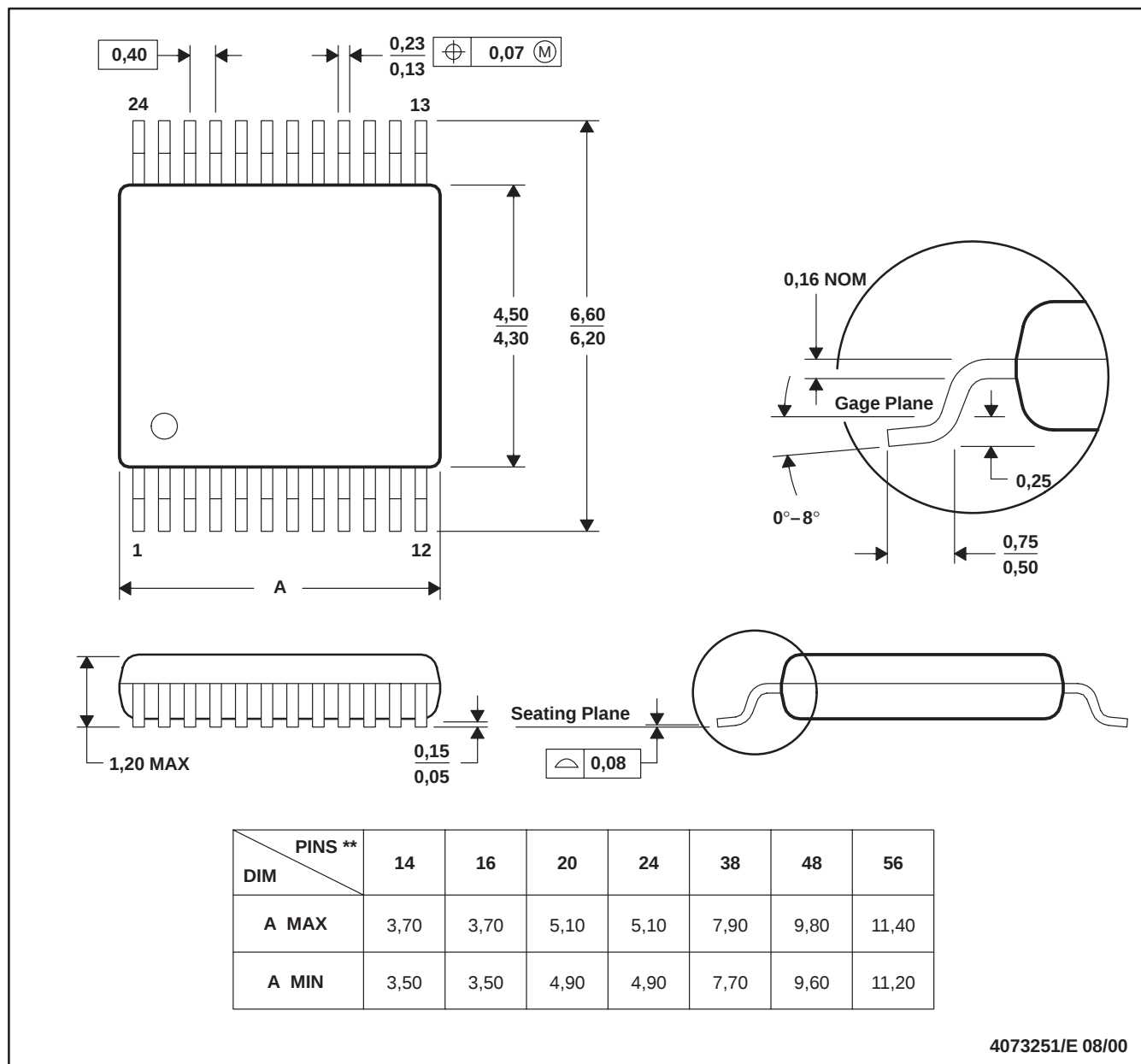


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

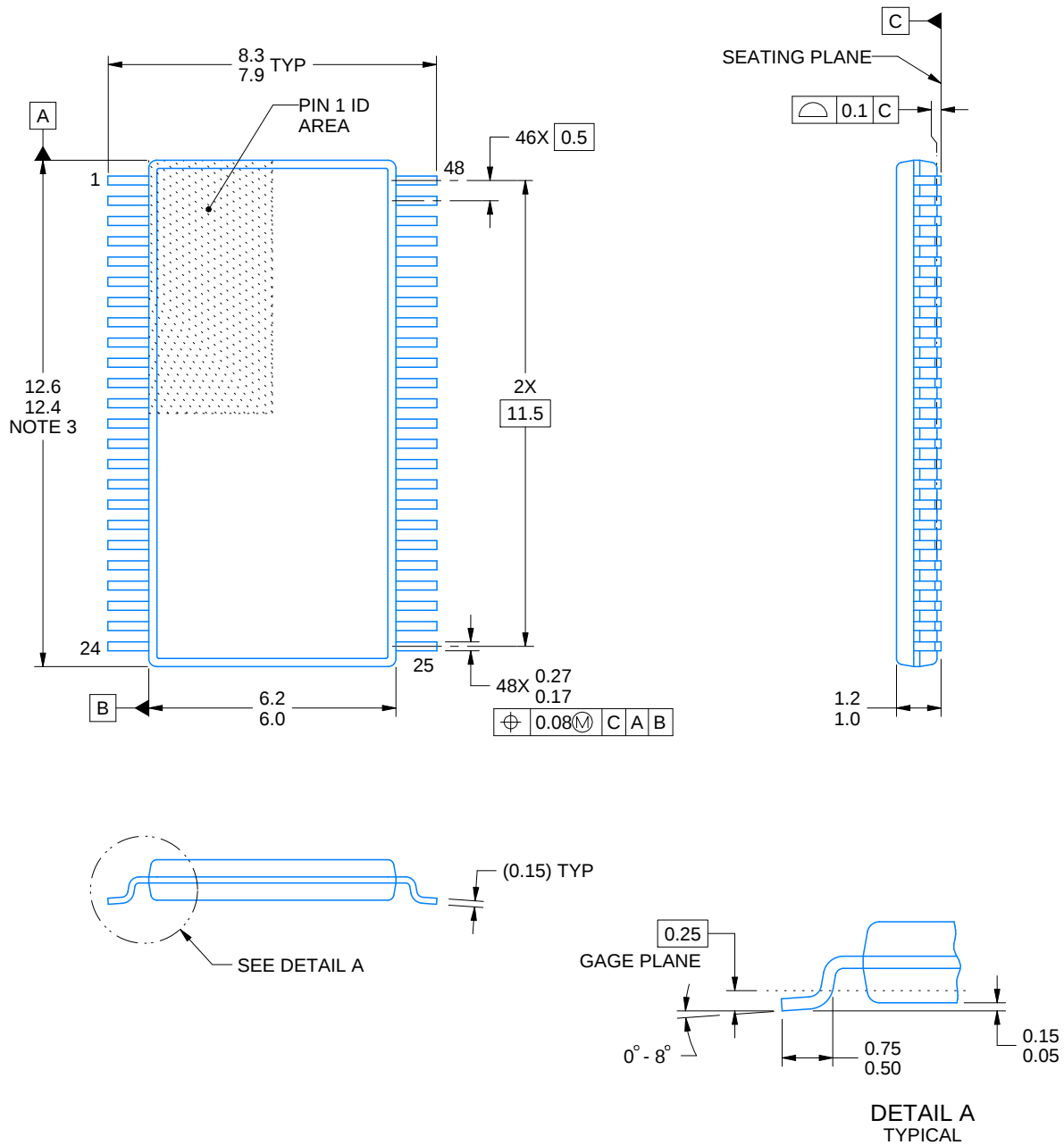
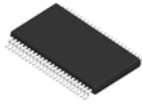
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

NOTES:

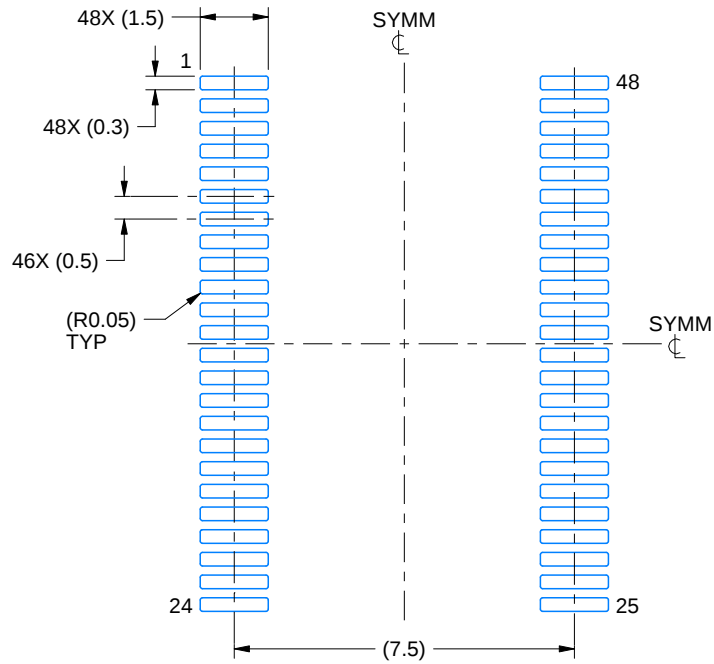
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

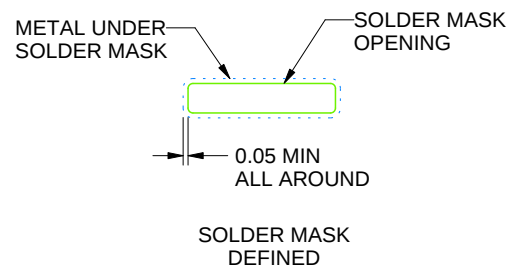
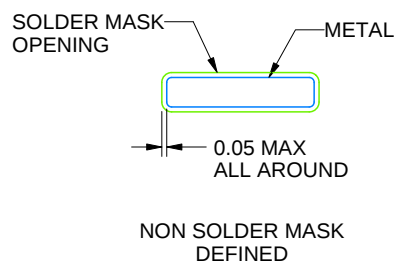
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

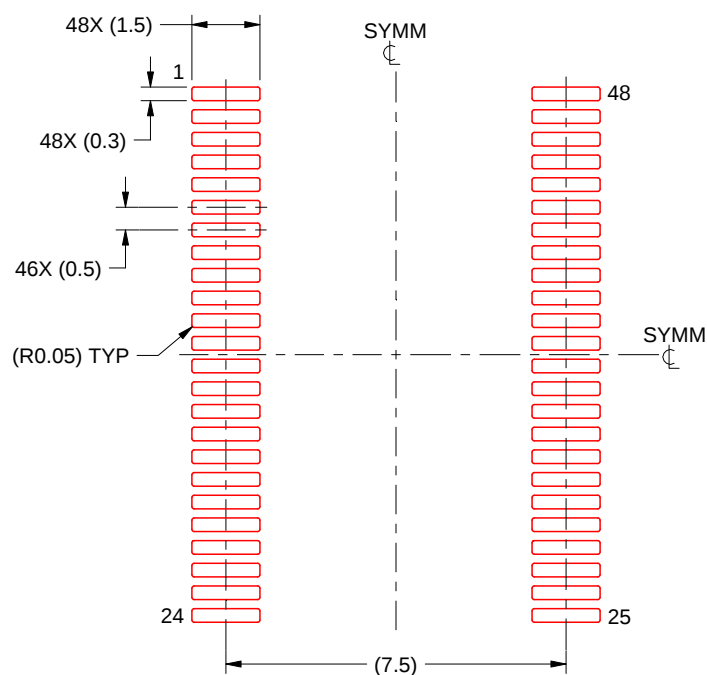
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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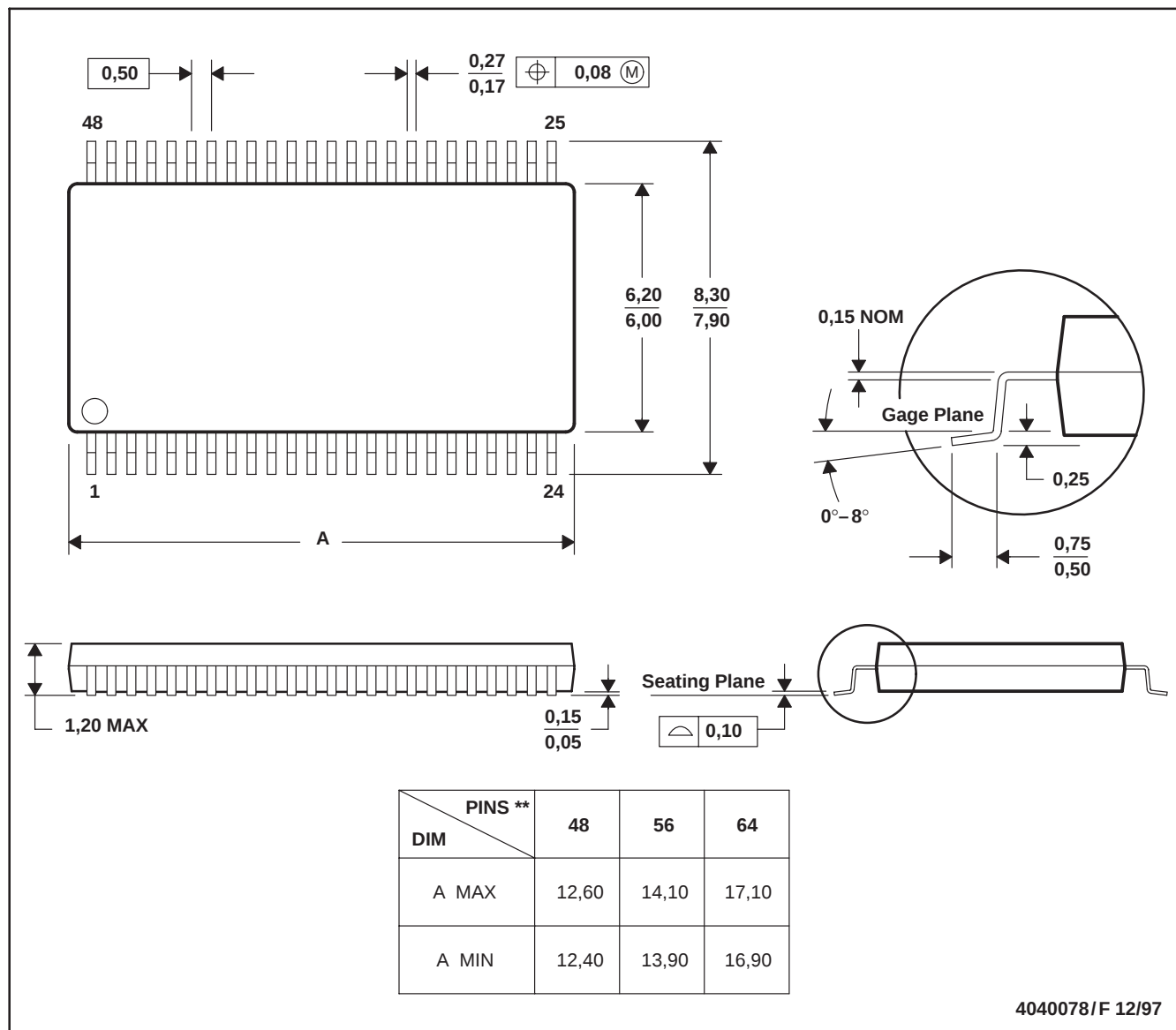
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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