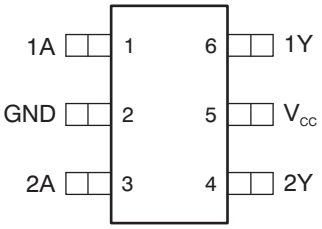
# SN74AUC2G34
# DUAL BUFFER GATE

SCES514B – NOVEMBER 2003 – REVISED JANUARY 2007

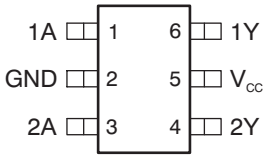
## FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Sub-1-V Operable**
- **Max $t_{pd}$ of 1.6 ns at 1.8 V**
- **Low Power Consumption, 10 μA at 1.8 V**
- **±8-mA Output Drive at 1.8 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

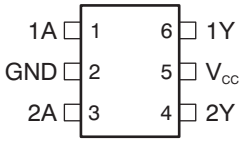
**DBV PACKAGE**
**(TOP VIEW)**



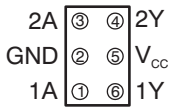

**DCK PACKAGE**
**(TOP VIEW)**




**DRL PACKAGE**
**(TOP VIEW)**




**YZP PACKAGE**
**(BOTTOM VIEW)**




## DESCRIPTION/ORDERING INFORMATION

This dual buffer gate is operational at 0.8-V to 2.7-V $V_{CC}$, but is designed specifically for 1.65-V to 1.95-V $V_{CC}$ operation.

The SN74AUC2G34 performs the Boolean function Y = A in positive logic.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING(2) |
|---|---|---|---|---|
| –40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74AUC2G34YZPR | _ _ _U9_ |
| | SOT-563 – DRL | Reel of 4000 | SN74AUC2G34DRLR | U9_ |
| | SOT-23 – DBV | Reel of 3000 | SN74AUC2G34DBVR | U34_ |
| | SC-70 – DCK | Reel of 3000 | SN74AUC2G34DCKR | U9_ |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

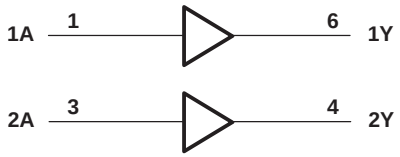
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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### FUNCTION TABLE (EACH GATE)

| INPUT A | OUTPUT Y |
|---|---|
| H | H |
| L | L |

### LOGIC DIAGRAM (POSITIVE LOGIC)




## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 3.6 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 4.1 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 4.1 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±20 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(3) | DBV package | | 165 | °C/W |
| | | DCK package | | 259 | |
| | | DRL package | | 142 | |
| | | YZP package | | 123 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.8 | 2.7 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 0.8 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | 0.65 × $V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 0.8 V | | 0 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | | 0.35 × $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 0.8 V | | –0.7 | mA |
| | | $V_{CC}$ = 1.1 V | | –3 | |
| | | $V_{CC}$ = 1.4 V | | –5 | |
| | | $V_{CC}$ = 1.65 V | | –8 | |
| | | $V_{CC}$ = 2.3 V | | –9 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 0.8 V | | 0.7 | mA |
| | | $V_{CC}$ = 1.1 V | | 3 | |
| | | $V_{CC}$ = 1.4 V | | 5 | |
| | | $V_{CC}$ = 1.65 V | | 8 | |
| | | $V_{CC}$ = 2.3 V | | 9 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 0.8 V to 1.65 V[2] | | 20 | ns/V |
| | | $V_{CC}$ = 1.65 V to 1.95 V[3] | | 20 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V[3] | | 10 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) The data was taken at $C_L$ = 15 pF, $R_L$ = 2 kΩ (see Figure 1).
(3) The data was taken at $C_L$ = 30 pF, $R_L$ = 500 Ω (see Figure 1).

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 µA | 0.8 V to 2.7 V | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –0.7 mA | 0.8 V | | 0.55 | | |
| | | $I_{OH}$ = –3 mA | 1.1 V | 0.8 | | | |
| | | $I_{OH}$ = –5 mA | 1.4 V | 1 | | | |
| | | $I_{OH}$ = –8 mA | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = –9 mA | 2.3 V | 1.8 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | 0.8 V to 2.7 V | | | 0.2 | V |
| | | $I_{OL}$ = 0.7 mA | 0.8 V | | 0.25 | | |
| | | $I_{OL}$ = 3 mA | 1.1 V | | | 0.3 | |
| | | $I_{OL}$ = 5 mA | 1.4 V | | | 0.4 | |
| | | $I_{OL}$ = 8 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 9 mA | 2.3 V | | | 0.6 | |
| $I_I$ | A inputs | $V_I$ = $V_{CC}$ or GND | 0 to 2.7 V | | | ±5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 2.7 V | 0 | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 0.8 V to 2.7 V | | | 10 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 2.5 V | | 2 | | pF |

(1) All typical values are at $T_A$ = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 6.4 | 0.7 | 3.4 | 0.6 | 2.3 | 0.6 | 1 | 1.6 | 0.5 | 1.2 | ns |

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 30 pF (unless otherwise noted) (see Figure 1)

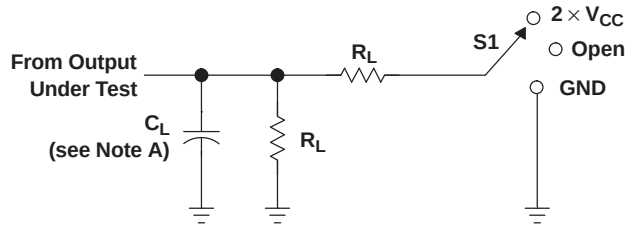
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 0.7 | 1.3 | 2.4 | 0.6 | 1.8 | ns |

## Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V | $V_{CC}$ = 1.5 V | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 12 | 12 | 12 | 13 | 14 | pF |

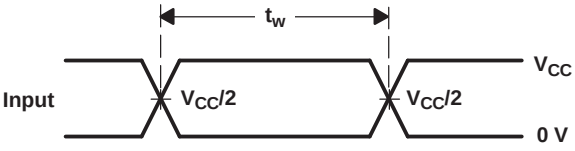
## PARAMETER MEASUREMENT INFORMATION



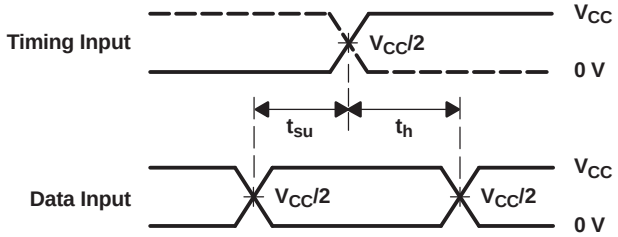

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

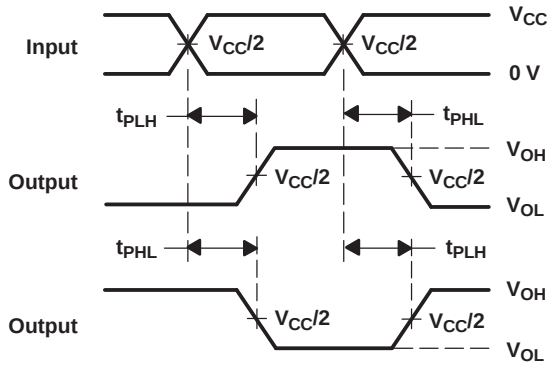
| $V_{CC}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|
| 0.8 V | 15 pF | 2 kΩ | 0.1 V |
| 1.2 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.5 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | 15 pF | 2 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 15 pF | 2 kΩ | 0.15 V |
| 1.8 V ± 0.15 V | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 30 pF | 500 Ω | 0.15 V |



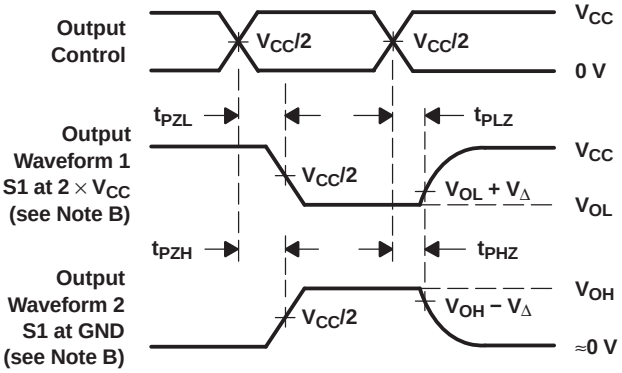

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AUC2G34DBVR | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U34R |
| SN74AUC2G34DBVR.B | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U34R |
| SN74AUC2G34DCKR | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U95, U9F, U9R) |
| SN74AUC2G34DCKR.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U95, U9F, U9R) |
| SN74AUC2G34DCKRE4 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U95, U9F, U9R) |
| SN74AUC2G34DRLR | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (1KB, U97, U9R) |
| SN74AUC2G34DRLR.B | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (1KB, U97, U9R) |
| SN74AUC2G34DRLRG4 | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 1KB |
| SN74AUC2G34DRLRG4.B | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 1KB |
| SN74AUC2G34YZPR | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | U9N |
| SN74AUC2G34YZPR.B | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | U9N |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

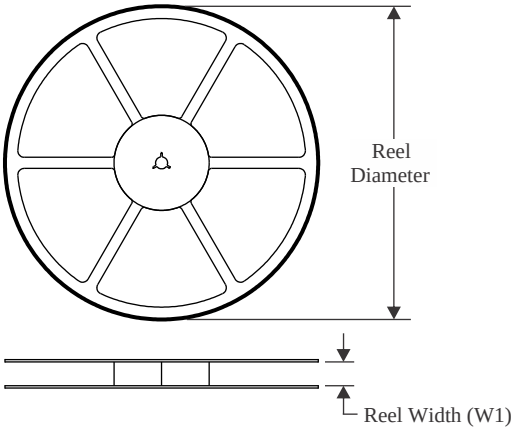
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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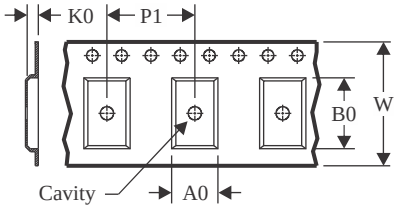
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

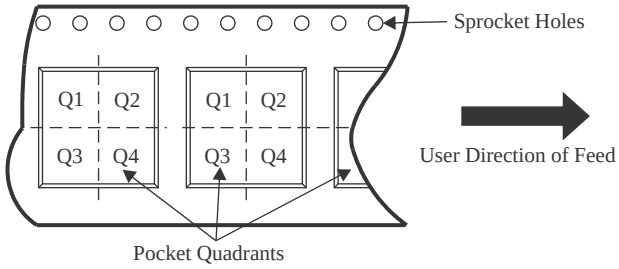



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

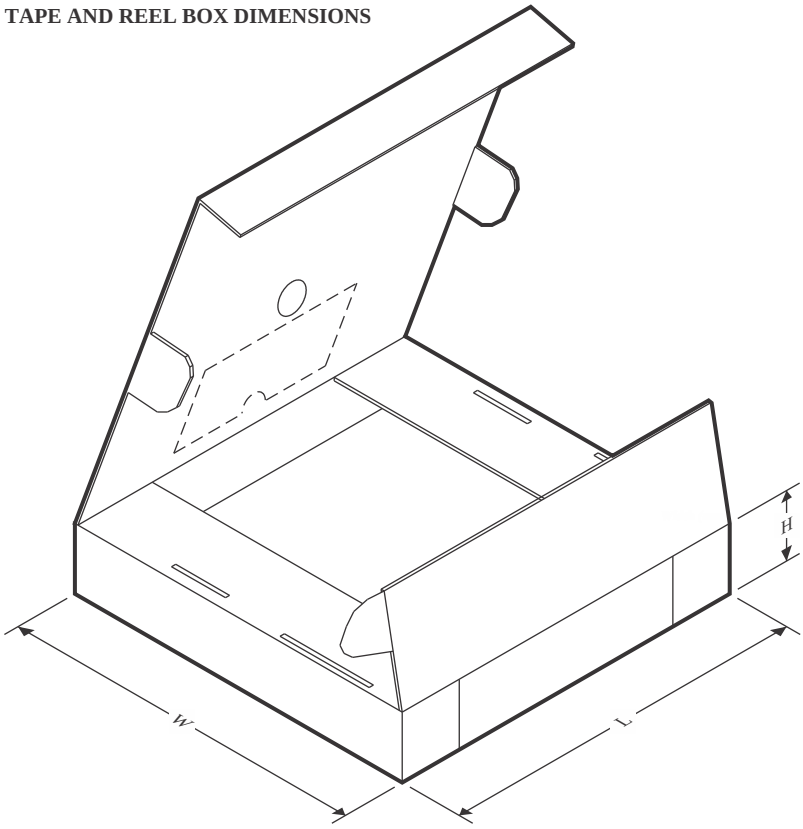
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUC2G34DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC2G34DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUC2G34DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUC2G34DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUC2G34DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74AUC2G34DRLRG4 | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74AUC2G34YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUC2G34DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC2G34DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC2G34DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC2G34DRLR | SOT-5X3 | DRL | 6 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AUC2G34DRLR | SOT-5X3 | DRL | 6 | 4000 | 210.0 | 185.0 | 35.0 |
| SN74AUC2G34DRLRG4 | SOT-5X3 | DRL | 6 | 4000 | 210.0 | 185.0 | 35.0 |
| SN74AUC2G34YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

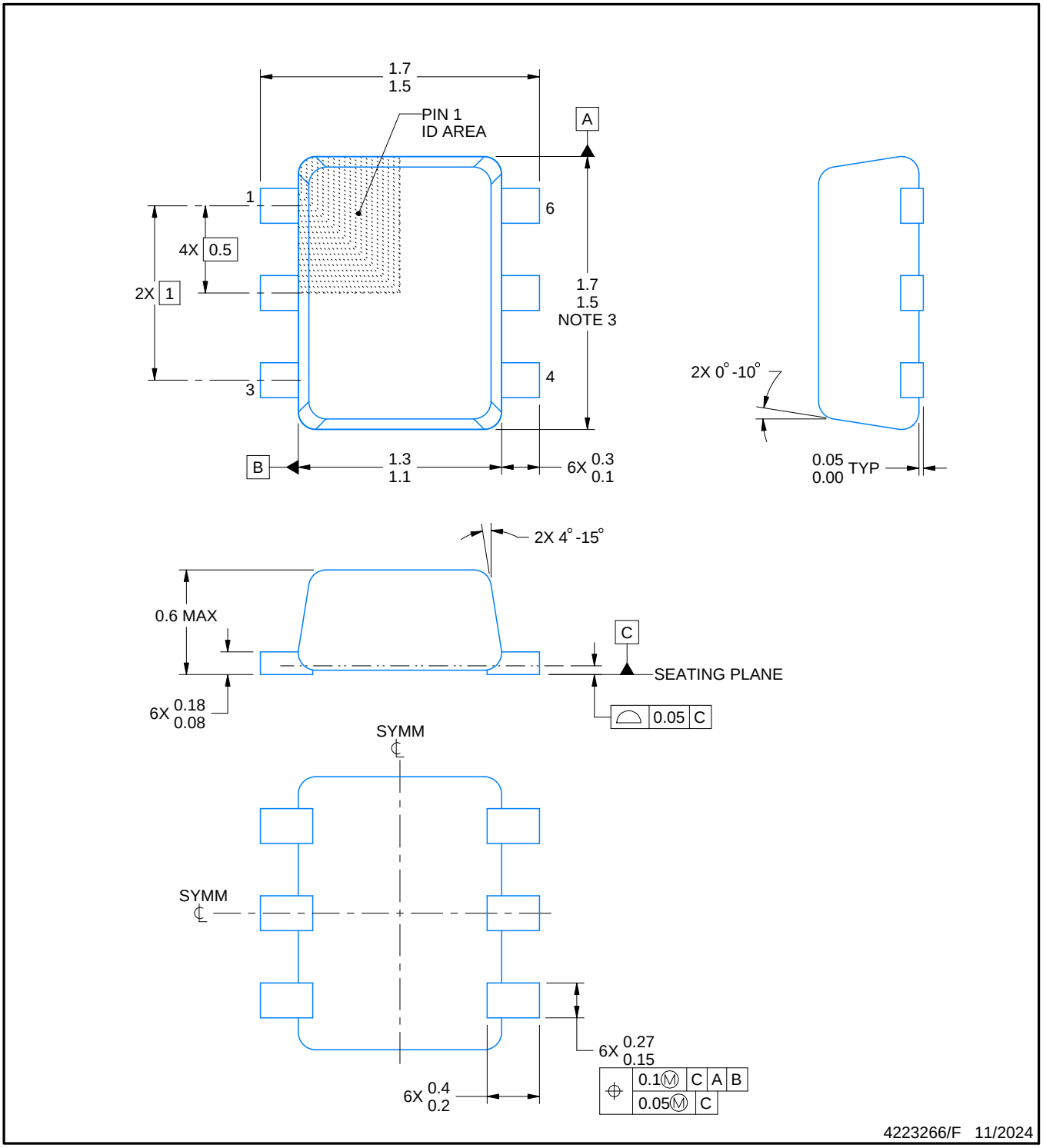


# PACKAGE OUTLINE

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




NOTES:

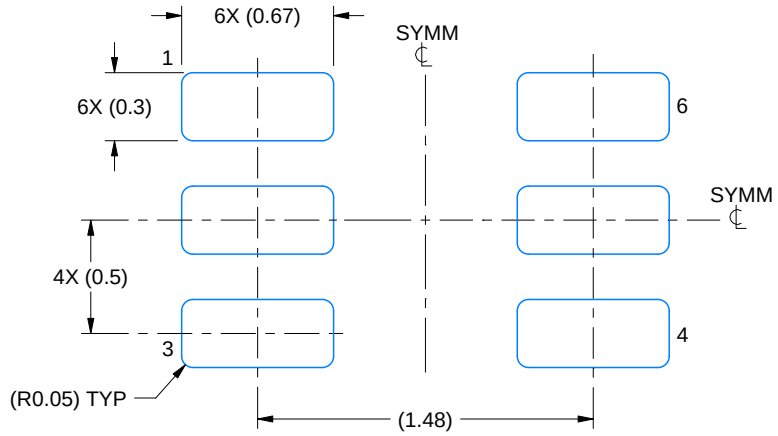
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

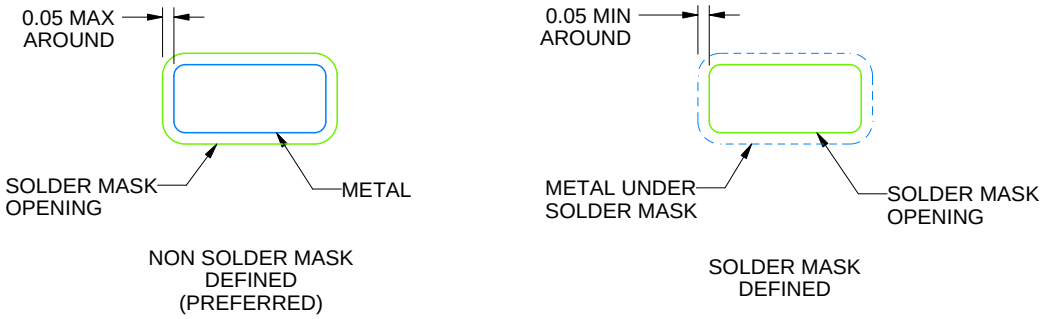
## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
SCALE:30X




SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

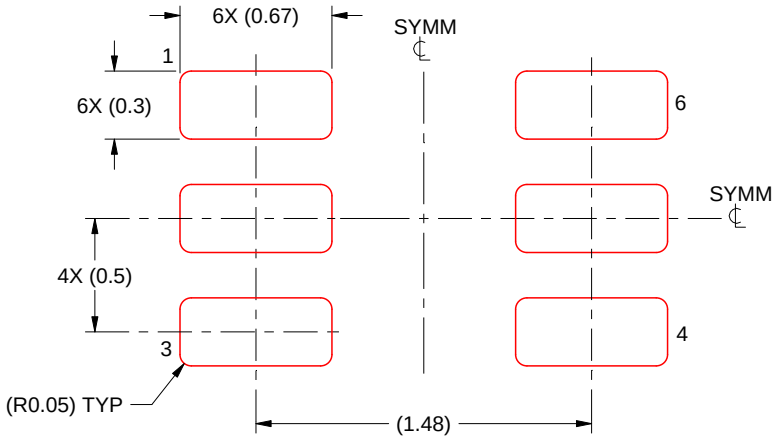
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

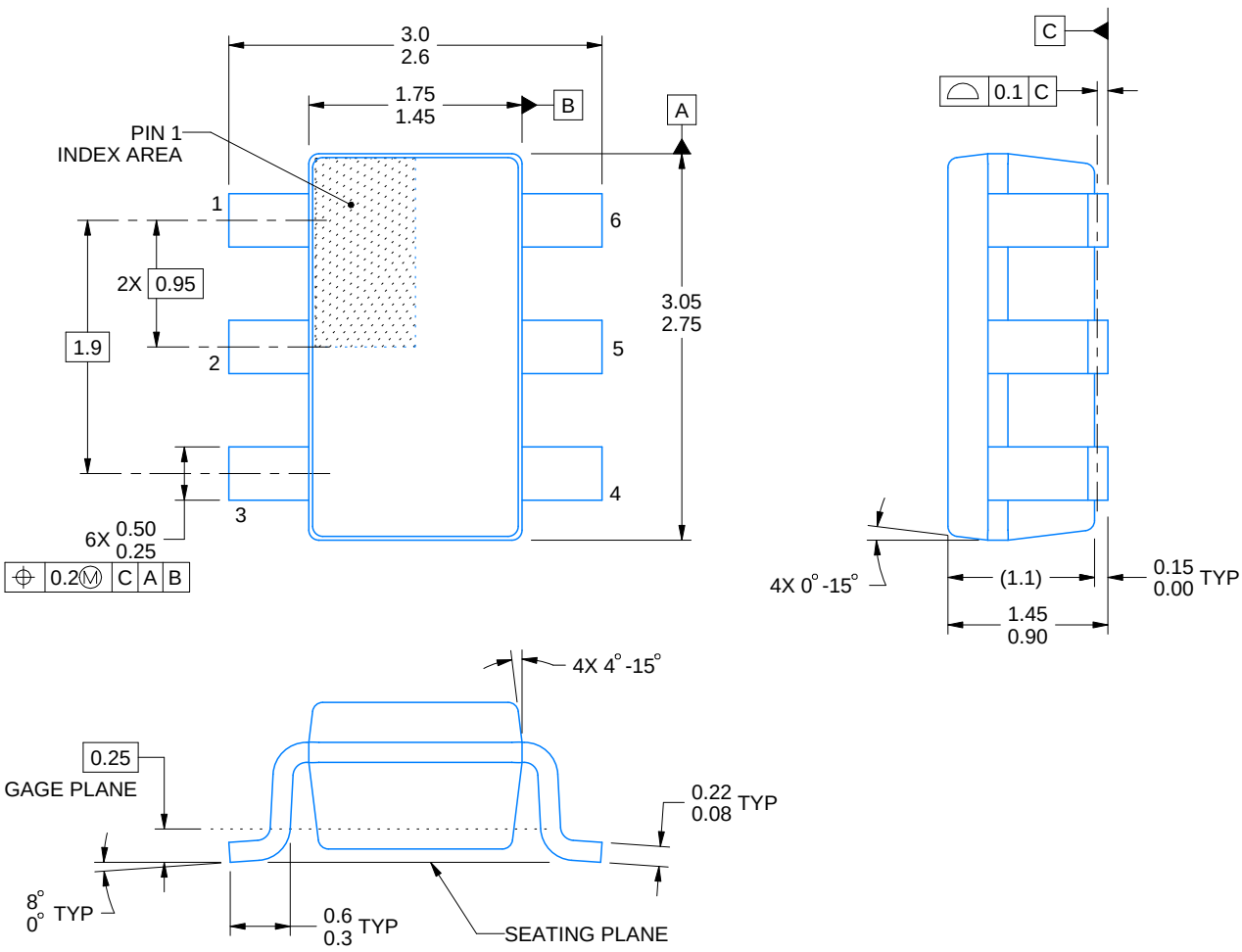
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

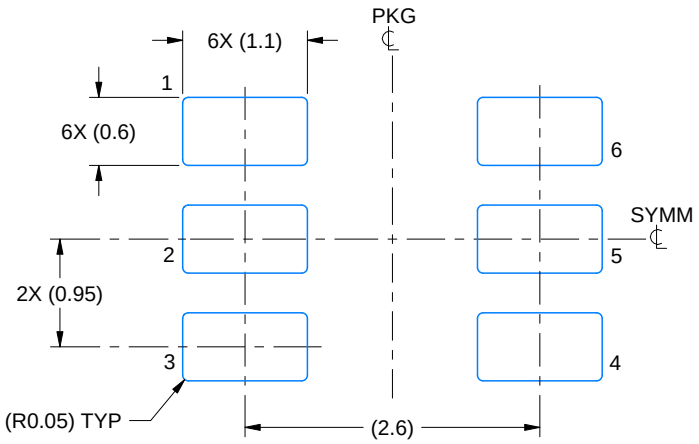
SMALL OUTLINE TRANSISTOR



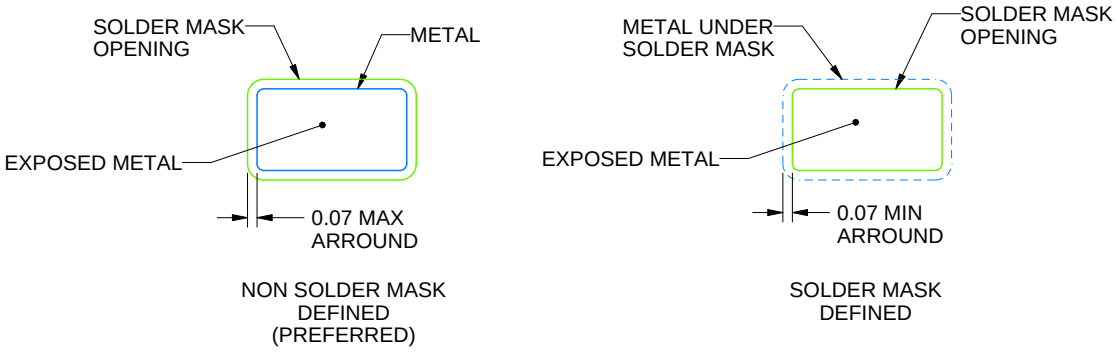

4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

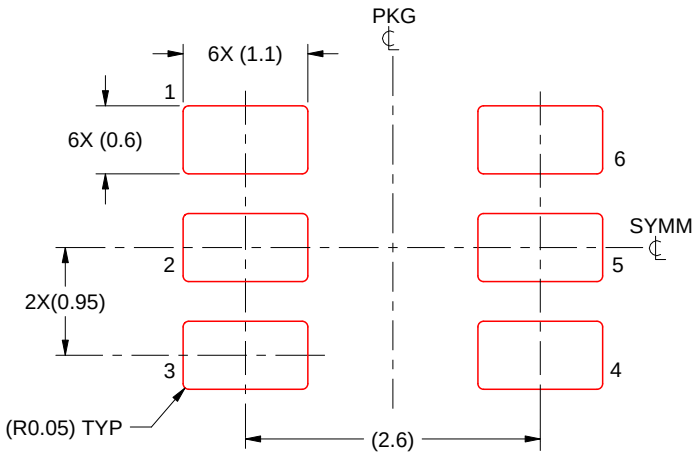



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

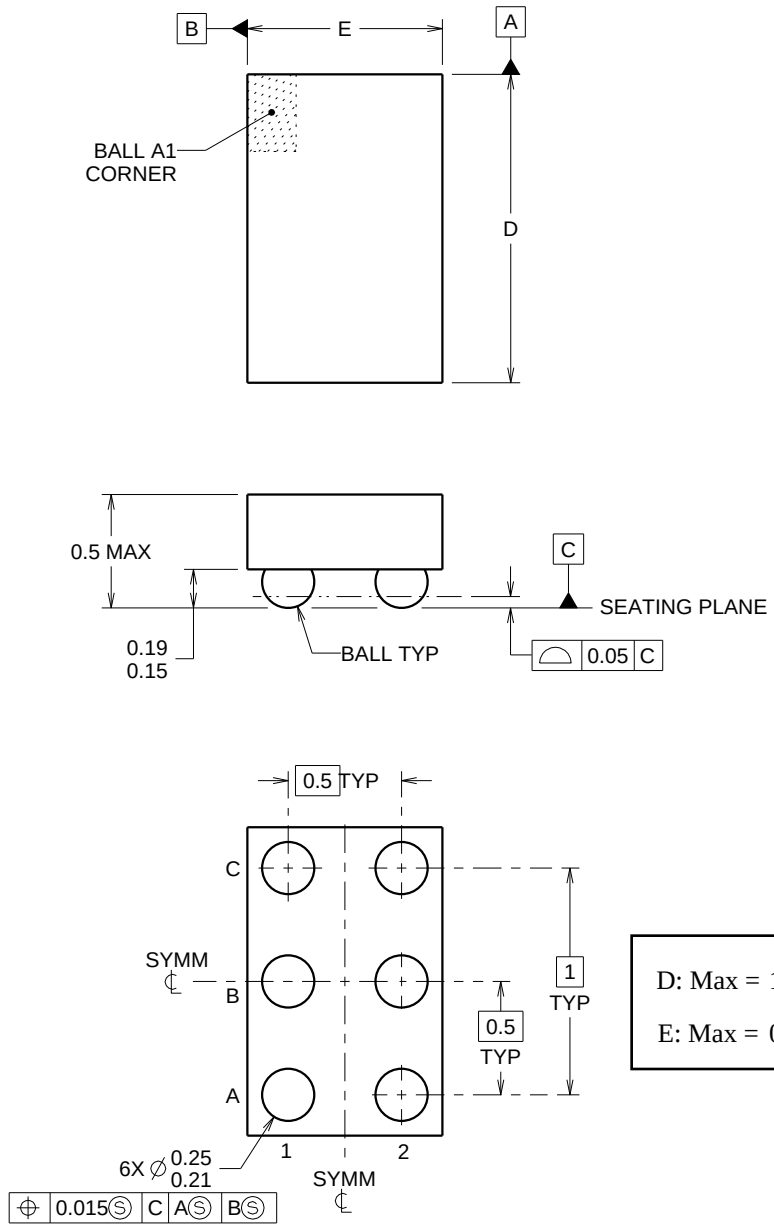
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## YZP0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




D: Max = 1.418 mm, Min =1.357 mm

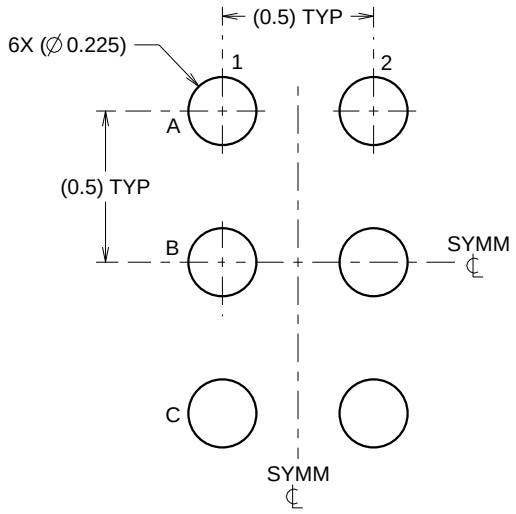
E: Max = 0.918 mm, Min =0.857 mm

4219524/A 06/2014

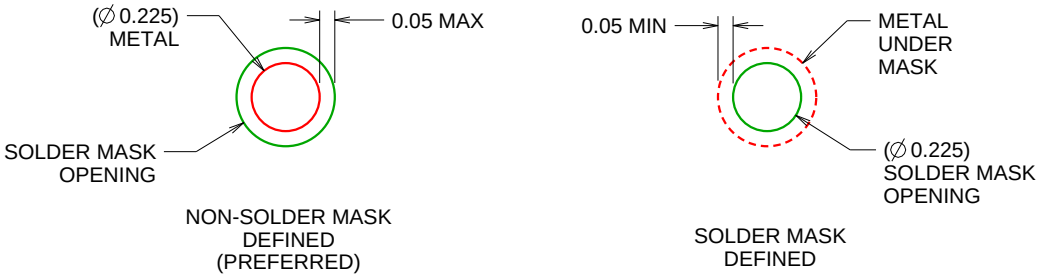
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
SCALE:40X

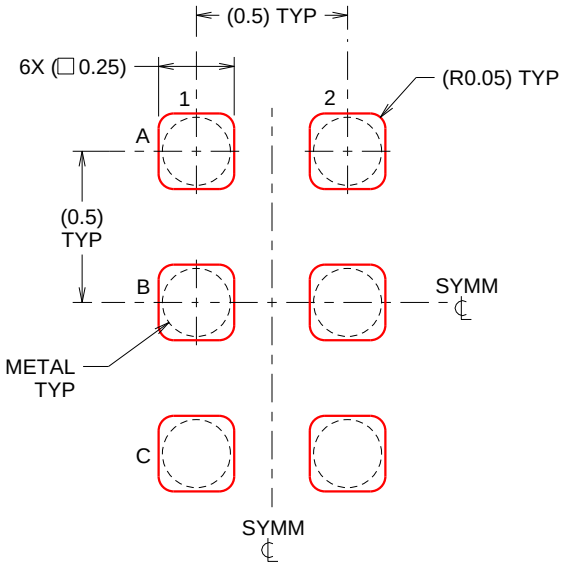



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

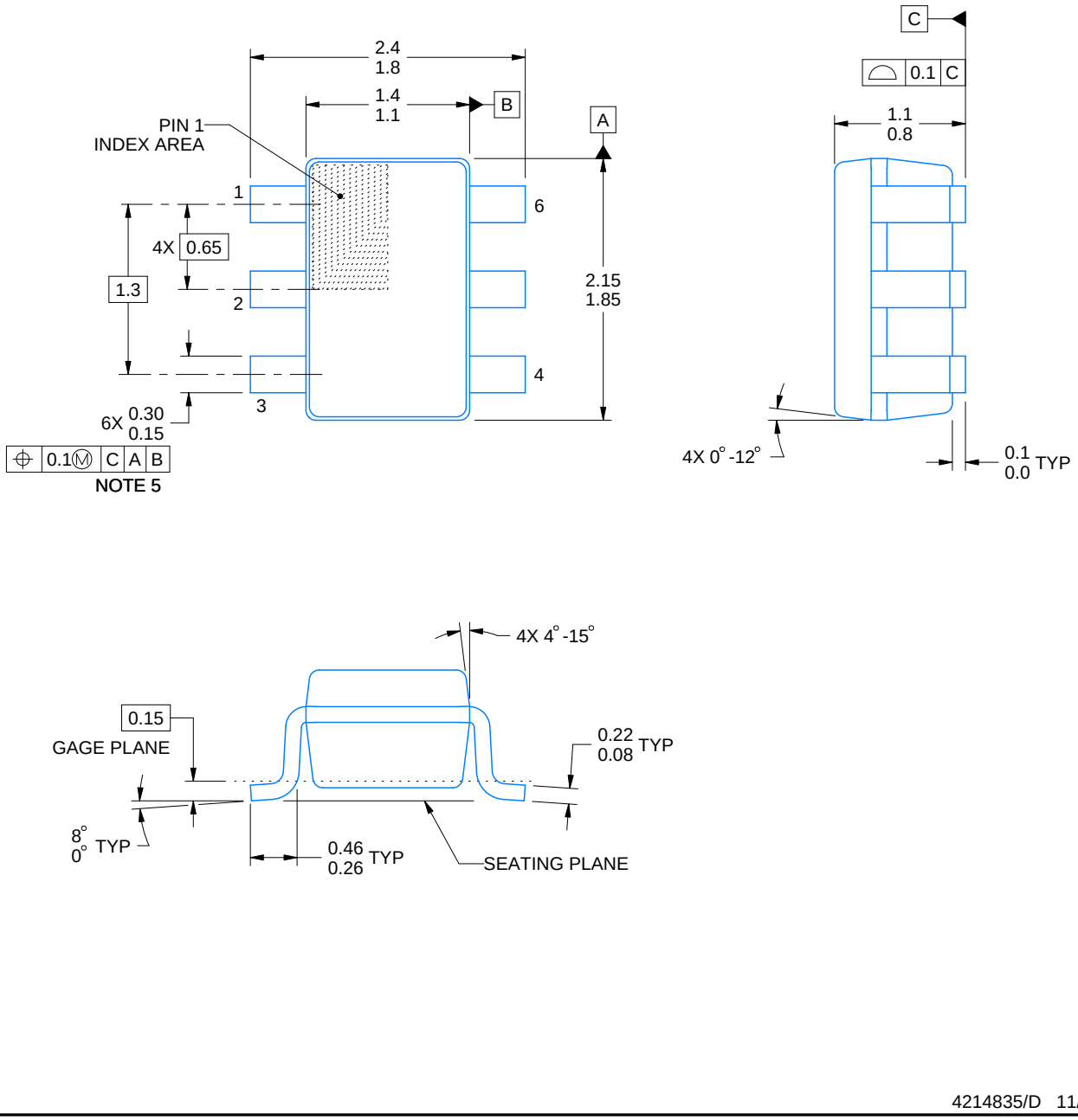
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DCK0006A

## SOT - 1.1 max height

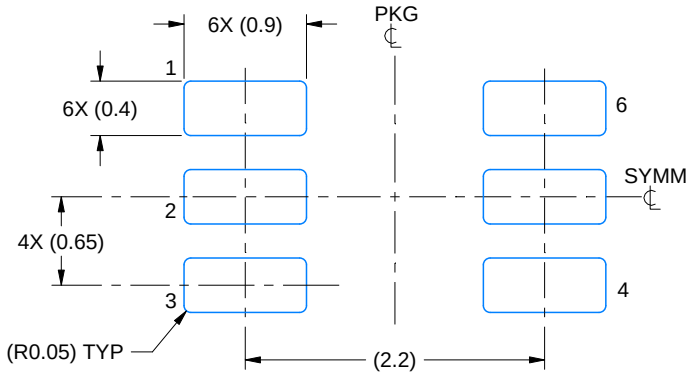
SMALL OUTLINE TRANSISTOR



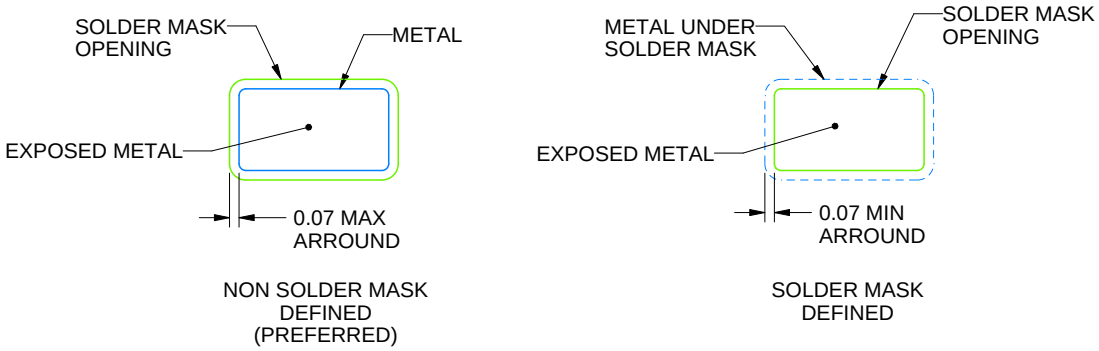

4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

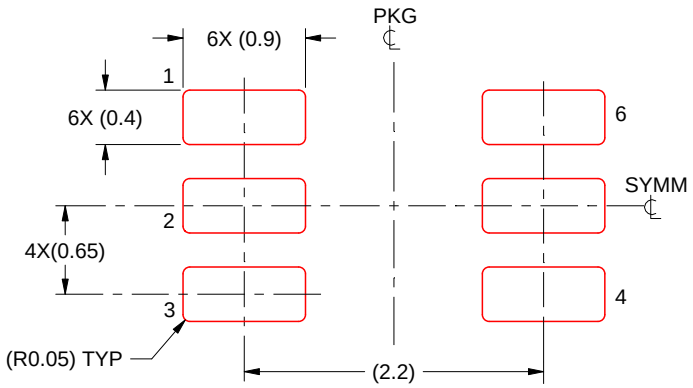



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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