具有可配置电压转换、三态输出和总线保持电路的 SN74AXCH8T245 8 位双电源总线收发器

1 特性

- 通过认证且完全可配置的双电源轨设计可允许各个端口在 0.65V 至 3.6V 的电源电压范围内运行
- 工作温度范围 -40°C 至 +125°C
- 总线保持数据输入消除了对外部上拉或下拉电阻的需求
- 多向控制引脚，支持同步升降转换
- 从 1.8V 转换到 3.3V 时，支持高达 380Mbps 的转换速率
- V_{CC} 隔离功能可在断电情况下有效隔离两条总线
- 局部断电模式可在断电情况下限制回流电流
- 兼容 SN74AVCH8T245 和 74AVCH8T245 电平转换器
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 8000V 人体放电模型
  - 1000V 充电器件模型

2 应用

- 企业与通信
- 无线基础设施
- 楼宇自动化
- 数据中心交换机
- 企业级固态硬盘
- 机架式服务器
- 电子销售点 (EPOS)

3 说明

SN74AXCH8T245 器件是一款 8 位同相总线收发器，可用于解决在最新电压节点（0.7V、0.8V、0.9V）上运行的器件与在行业标准电压节点（1.8V、2.5V、3.3V）上运行的器件之间的电压电平不匹配问题。

该器件通过两条独立电源轨（V_{CCA} 和 V_{CCB}）。数据引脚 A1 至 A8 均用于跟踪 V_{CCA}，可承受 0.65V-3.6V 范围内的任何电源电压。数据引脚 B1 至 B8 均用于跟踪 V_{CCB}，可承受 0.65V-3.6V 范围内的任何电源电压。此外，SN74AXCH8T245 还与单电源系统兼容。

SN74AXCH8T245 器件旨在实现数据总线间的异步通信。根据方向控制输入（DIR1 和 DIR2）的逻辑电平，此器件将数据从 A 总线传输至 B 总线，或者将数据从 B 总线传输至 A 总线。输出使能 ($\overline{OE}$) 输入可用于禁用输出，从而有效隔离总线。

SN74AXCH8T245 器件旨在使控制引脚（DIR 和 $\overline{OE}$）以 V_{CCA} 为基准。

有源总线保持电路会将未使用或未驱动的输入保持在有效逻辑状态。不建议在总线保持电路上使用上拉或下拉电阻器。如果 V_{CCA} 或 V_{CCB} 连上电源，则总线保持电路在所有 A 端口和 B 端口上均始终保持工作状态，与方向控制或输出使能无关。

该器件完全 适用于 使用 I_{off} 的不完全断电应用。当器件断电时，I_{off} 电路将会禁用输出。这会抑制电流反流到器件中，从而防止损坏器件。

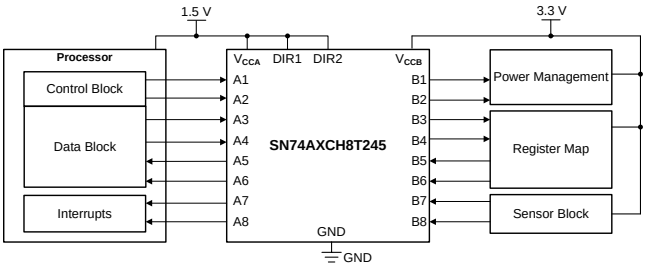
V_{CC} 隔离功能可确保当任一 V_{CC} 输入电源低于 100mV 时，所有电平转换器输出都将禁用并处于高阻抗状态。为了确保电平转换器 I/O 在上电或掉电期间处于高阻抗状态，应将 $\overline{OE}$ 通过上拉电阻器接到 V_{CCA}；该电阻器的最小值取决于驱动器的灌电流能力。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
SN74AXCH8T245PW	TSSOP (24)	7.80mm × 4.40mm
SN74AXCH8T245RHL	VQFN (24)	5.50mm × 3.50mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

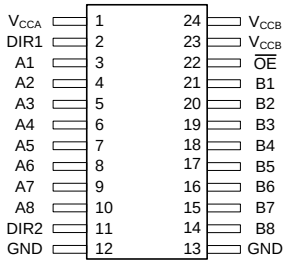
Changes from Original (August 2018) to Revision A **Page**

- 已添加 向器件信息表添加了 RHL 封装 ... 1
- Added RHL package pinout ... 3
- Added RHL package to Thermal Information table ... 5

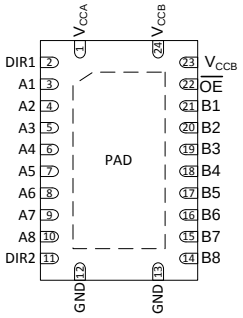
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5 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



RHL Package(1)
24-Pin VQFN
Top View



(1) PAD - may be grounded (recommended) or left floating.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	PW, RHL		
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR1	2	I	Direction-control signal. Referenced to V_{CCA}.
DIR2	11	I	Direction-control signal. Referenced to V_{CCA}. See *Multiple Direction Control Pins* for additional details. Tie to GND to maintain backwards compatibility with the SN74AVCH8T245 device.
GND	12	—	Ground
	13	—	Ground
$\overline{OE}$	22	I	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 0.65 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	23	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V
	24	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		–0.5	4.2	V
Supply voltage, V_{CCB}		–0.5	4.2	V
Input voltage, V_I(2)	I/O ports (A port)	–0.5	4.2	V
	I/O ports (B port)	–0.5	4.2	
	Control inputs	–0.5	4.2	
Voltage applied to any output in the high-impedance or power-off state, V_O(2)	A port	–0.5	4.2	V
	B port	–0.5	4.2	
Voltage applied to any output in the high or low state, V_O(2) (3)	A port	–0.5	V_{CCA} + 0.2	V
	B port	–0.5	V_{CCB} + 0.2	
Input clamp current, I_{IK}	V_I < 0	–50		mA
Output clamp current, I_{OK}	V_O < 0	–50		mA
Continuous output current, I_O		–50	50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage			0.65	3.6	V
V_{CCB}	Supply voltage			0.65	3.6	V
V_{IH}	High-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} × 0.70		V
			V_{CCI} = 0.76 V - 1 V	V_{CCI} × 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} × 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} × 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} × 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} × 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} × 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} × 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} × 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} × 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} × 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} × 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active state		0	V_{CCO} (2)	V
		Tri-state		0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information

THERMAL METRIC (1)		SN74AXCH8T245		UNIT
		PW (TSSOP)	RHL (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.7	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.0	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.4	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	–40°C to 85°C			–40°C to 125°C			UNIT
						MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = –50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = –200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = –500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_{BHL}	Bus-hold low sustaining current (3)	V_I= 0.20 V		0.65 V	0.65 V	4			4			µA
		V_I= 0.23 V		0.76 V	0.76 V	8			7			
		V_I= 0.26 V		0.85 V	0.85 V	10			10			
		V_I= 0.39 V		1.1 V	1.1 V	20			20			
		V_I= 0.49 V		1.4 V	1.4 V	40			30			
		V_I= 0.58 V		1.65 V	1.65 V	55			45			
		V_I= 0.7 V		2.3 V	2.3 V	90			80			
		V_I= 0.8 V		3 V	3 V	145			135			
I_{BHH}	Bus-hold high sustaining current (4)	V_I= 0.45 V		0.65 V	0.65 V	–4			–4			µA
		V_I= 0.53 V		0.76 V	0.76 V	–8			–7			
		V_I= 0.59 V		0.85 V	0.85 V	–10			–10			
		V_I= 0.71 V		1.1 V	1.1 V	–20			–20			
		V_I= 0.91 V		1.4 V	1.4 V	–40			–30			
		V_I= 1.07 V		1.65 V	1.65 V	–55			–45			
		V_I= 1.6 V		2.3 V	2.3 V	–90			–80			
		V_I= 2.0 V		3 V	3 V	–145			–135			
I_{BHLO}	Bus-hold low overdrive current (5)	V_I= 0 to V_{CC}		0.75 V	0.75 V	40			40			µA
				0.84 V	0.84 V	50			50			
				0.95 V	0.95 V	65			65			
				1.3 V	1.3 V	105			105			
				1.6 V	1.6 V	150			150			
				1.95 V	1.95 V	205			205			
				2.7 V	2.7 V	335			335			
				3.6V	3.6V	480			480			

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) All typical values are for T_A = 25°C.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}(MAX). I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL}(MAX).
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}(MIN). I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH}(MIN).
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.

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Electrical Characteristics (continued)

Over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	–40°C to 85°C			–40°C to 125°C			UNIT
					MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
I_{BHHO}	Bus-hold high overdrive current (6)	V_I= 0 to V_{CC}	0.75 V	0.75 V	–40			–40			µA
			0.84 V	0.84 V	–50			–50			
			0.95 V	0.95 V	–65			–65			
			1.3 V	1.3 V	–105			–105			
			1.6 V	1.6 V	–150			–150			
			1.95 V	1.95 V	–205			–205			
			2.7 V	2.7 V	–335			–335			
			3.6V	3.6V	–480			–480			
I_I	Input leakage current	Control Inputs (DIR, $\overline{OE}$): $V_I = V_{CCA}$ or GND	0.65 V - 3.6 V	0.65 V - 3.6 V	–0.5		0.5	–1		1	µA
I_{off}	Partial power down current	A Port: V_I or V_O = 0 V - 3.6 V	0 V	0 V - 3.6 V	–8		8	–12		12	µA
		B Port: V_I or V_O = 0 V - 3.6 V	0 V - 3.6 V	0 V	–8		8	–12		12	
I_{OZ}	High-impedance state output current	A Port: $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$	3.6 V	3.6 V	–8		8	–12		12	µA
		B Port: $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$	3.6 V	3.6 V	–8		8	–12		12	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			20			42	µA
			0 V	3.6 V	–2			–12			
			3.6 V	0 V			13			27	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			20			40	µA
			0 V	3.6 V			13			27	
			3.6 V	0 V	–2			–12			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			30			60	µA
C_i	Input capacitance	Control Inputs (DIR, $\overline{OE}$): V_I = 3.3 V or GND	3.3 V	3.3 V		4.5			4.5		pF
C_{io}	Data I/O capacitance	Ports A and B: $\overline{OE} = V_{CCA}$, V_O = 1.65V DC + 1 MHz -16 dBm sine wave	3.3 V	3.3 V		7.3			7.3		pF

(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

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6.6 Switching Characteristics, V_{CCA} = 0.7 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	178	0.5	115	0.5	83	0.5	49	ns
			–40°C to 125°C	0.5	178	0.5	115	0.5	83	0.5	49	
		B input to A output	–40°C to 85°C	0.5	178	0.5	159	0.5	132	0.5	94	
			–40°C to 125°C	0.5	178	0.5	159	0.5	132	0.5	94	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	194	0.5	194	0.5	194	0.5	194	ns
			–40°C to 125°C	0.5	194	0.5	194	0.5	194	0.5	194	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	216	0.5	179	0.5	158	0.5	78	
			–40°C to 125°C	0.5	216	0.5	179	0.5	158	0.5	78	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	240	0.5	240	0.5	240	0.5	240	ns
			–40°C to 125°C	0.5	240	0.5	240	0.5	240	0.5	240	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	292	0.5	180	0.5	125	0.5	76	
			–40°C to 125°C	0.5	292	0.5	180	0.5	125	0.5	76	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	47	0.5	50	0.5	62	0.5	151	ns
			–40°C to 125°C	0.5	47	0.5	50	0.5	62	0.5	151	
		B input to A output	–40°C to 85°C	0.5	89	0.5	88	0.5	87	0.5	86	
			–40°C to 125°C	0.5	89	0.5	88	0.5	87	0.5	86	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	194	0.5	194	0.5	194	0.5	194	ns
			–40°C to 125°C	0.5	194	0.5	194	0.5	194	0.5	194	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	70	0.5	69	0.5	67	0.5	101	
			–40°C to 125°C	0.5	70	0.5	69	0.5	67	0.5	101	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	240	0.5	240	0.5	240	0.5	240	ns
			–40°C to 125°C	0.5	240	0.5	240	0.5	240	0.5	240	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	69	0.5	69	0.5	84	0.5	552	
			–40°C to 125°C	0.5	69	0.5	69	0.5	84	0.5	552	

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6.7 Switching Characteristics, V_{CCA} = 0.8 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	159	0.5	96	0.5	64	0.5	33	ns
			–40°C to 125°C	0.5	159	0.5	96	0.5	64	0.5	33	
		B input to A output	–40°C to 85°C	0.5	117	0.5	97	0.5	79	0.5	54	
			–40°C to 125°C	0.5	117	0.5	97	0.5	79	0.5	54	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	154	0.5	154	0.5	154	0.5	154	ns
			–40°C to 125°C	0.5	154	0.5	154	0.5	154	0.5	154	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	202	0.5	165	0.5	144	0.5	65	
			–40°C to 125°C	0.5	202	0.5	165	0.5	144	0.5	65	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	137	0.5	137	0.5	137	0.5	137	ns
			–40°C to 125°C	0.5	137	0.5	137	0.5	137	0.5	137	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	270	0.5	160	0.5	104	0.5	55	
			–40°C to 125°C	0.5	270	0.5	160	0.5	104	0.5	55	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	27	0.5	26	0.5	26	0.5	35	ns
			–40°C to 125°C	0.5	27	0.5	26	0.5	26	0.5	35	
		B input to A output	–40°C to 85°C	0.5	44	0.5	43	0.5	42	0.5	41	
			–40°C to 125°C	0.5	44	0.5	43	0.5	42	0.5	41	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	154	0.5	154	0.5	154	0.5	154	ns
			–40°C to 125°C	0.5	154	0.5	154	0.5	154	0.5	154	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	57	0.5	55	0.5	50	0.5	52	
			–40°C to 125°C	0.5	57	0.5	55	0.5	50	0.5	52	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	137	0.5	137	0.5	137	0.5	137	ns
			–40°C to 125°C	0.5	137	0.5	137	0.5	137	0.5	137	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	46	0.5	44	0.5	46	0.5	59	
			–40°C to 125°C	0.5	46	0.5	44	0.5	46	0.5	59	

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6.8 Switching Characteristics, V_{CCA} = 0.9 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to output	–40°C to 85°C	0.5	133	0.5	79	0.5	53	0.5	23	ns
			–40°C to 125°C	0.5	133	0.5	79	0.5	53	0.5	23	
		B input to A output	–40°C to 85°C	0.5	84	0.5	64	0.5	53	0.5	41	
			–40°C to 125°C	0.5	84	0.5	64	0.5	53	0.5	41	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	130	0.5	130	0.5	130	0.5	130	ns
			–40°C to 125°C	0.5	130	0.5	130	0.5	130	0.5	130	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	193	0.5	157	0.5	137	0.5	57	
			–40°C to 125°C	0.5	193	0.5	157	0.5	137	0.5	57	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	128	0.5	128	0.5	128	0.5	128	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	257	0.5	149	0.5	94	0.5	45	
			–40°C to 125°C	0.5	257	0.5	149	0.5	94	0.5	45	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	18	0.5	16	0.5	15	0.5	18	ns
			–40°C to 125°C	0.5	18	0.5	16	0.5	15	0.5	18	
		B input to A output	–40°C to 85°C	0.5	29	0.5	25	0.5	23	0.5	22	
			–40°C to 125°C	0.5	29	0.5	25	0.5	23	0.5	22	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	130	0.5	130	0.5	130	0.5	130	ns
			–40°C to 125°C	0.5	130	0.5	130	0.5	130	0.5	130	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	50	0.5	48	0.5	42	0.5	43	
			–40°C to 125°C	0.5	50	0.5	48	0.5	42	0.5	43	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	128	0.5	128	0.5	128	0.5	128	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	37	0.5	34	0.5	32	0.5	36	
			–40°C to 125°C	0.5	37	0.5	34	0.5	32	0.5	36	

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6.9 Switching Characteristics, V_{CCA} = 1.2 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	95	0.5	54	0.5	40	0.5	15	ns
			–40°C to 125°C	0.5	95	0.5	54	0.5	40	0.5	15	
		B input to A output	–40°C to 85°C	0.5	49	0.5	33	0.5	23	0.5	15	
			–40°C to 125°C	0.5	49	0.5	33	0.5	23	0.5	15	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	47	0.5	47	0.5	47	0.5	47	ns
			–40°C to 125°C	0.5	47	0.5	47	0.5	47	0.5	47	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	181	0.5	147	0.5	127	0.5	49	
			–40°C to 125°C	0.5	181	0.5	147	0.5	127	0.5	49	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	40	0.5	40	0.5	40	0.5	40	ns
			–40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	221	0.5	132	0.5	81	0.5	34	
			–40°C to 125°C	0.5	221	0.5	132	0.5	81	0.5	34	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	11	0.5	9	0.5	8	0.5	8	ns
			–40°C to 125°C	0.5	11	0.5	9	0.5	8	0.5	8	
		B input to A output	–40°C to 85°C	0.5	12	0.5	10	0.5	8	0.5	8	
			–40°C to 125°C	0.5	12	0.5	10	0.5	8	0.5	8	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	47	0.5	47	0.5	47	0.5	47	ns
			–40°C to 125°C	0.5	47	0.5	47	0.5	47	0.5	47	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	42	0.5	40	0.5	34	0.5	34	
			–40°C to 125°C	0.5	42	0.5	40	0.5	34	0.5	34	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	39	0.5	40	0.5	40	0.5	40	ns
			–40°C to 125°C	0.5	39	0.5	40	0.5	40	0.5	40	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	25	0.5	22	0.5	20	0.5	19	
			–40°C to 125°C	0.5	25	0.5	22	0.5	20	0.5	19	

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6.10 Switching Characteristics, V_{CCA} = 1.5 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	90	0.5	44	0.5	29	0.5	12	ns
			–40°C to 125°C	0.5	90	0.5	44	0.5	29	0.5	12	
		B input to A output	–40°C to 85°C	0.5	47	0.5	27	0.5	18	0.5	11	
			–40°C to 125°C	0.5	47	0.5	27	0.5	18	0.5	11	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	176	0.5	142	0.5	122	0.5	44	
			–40°C to 125°C	0.5	176	0.5	142	0.5	122	0.5	44	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	25	0.5	25	0.5	25	0.5	25	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	214	0.5	114	0.5	71	0.5	29	
			–40°C to 125°C	0.5	214	0.5	114	0.5	71	0.5	29	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	9	0.5	8	0.5	6	0.5	6	ns
			–40°C to 125°C	0.5	9	0.5	8	0.5	6	0.5	6	
		B input to A output	–40°C to 85°C	0.5	9	0.5	8	0.5	6	0.5	5	
			–40°C to 125°C	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	38	0.5	37	0.5	31	0.5	31	
			–40°C to 125°C	0.5	38	0.5	37	0.5	31	0.5	31	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	25	0.5	25	0.5	25	0.5	25	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	21	0.5	18	0.5	15	0.5	13	
			–40°C to 125°C	0.5	21	0.5	18	0.5	15	0.5	13	

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6.11 Switching Characteristics, V_{CCA} = 1.8 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	88	0.5	43	0.5	25	0.5	10	ns
			–40°C to 125°C	0.5	88	0.5	43	0.5	25	0.5	10	
		B input to A output	–40°C to 85°C	0.5	50	0.5	26	0.5	16	0.5	9	
			–40°C to 125°C	0.5	50	0.5	26	0.5	16	0.5	9	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	35	0.5	35	0.5	35	0.5	35	ns
			–40°C to 125°C	0.5	35	0.5	35	0.5	35	0.5	35	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	174	0.5	139	0.5	119	0.5	42	
			–40°C to 125°C	0.5	174	0.5	139	0.5	119	0.5	42	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	ns
			–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	213	0.5	111	0.5	67	0.5	27	
			–40°C to 125°C	0.5	213	0.5	111	0.5	67	0.5	27	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	8	0.5	7	0.5	6	0.5	5	ns
			–40°C to 125°C	0.5	8	0.5	7	0.5	6	0.5	5	
		B input to A output	–40°C to 85°C	0.5	7	0.5	6	0.5	5	0.5	4	
			–40°C to 125°C	0.5	7	0.5	7	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	35	0.5	35	0.5	35	0.5	35	ns
			–40°C to 125°C	0.5	35	0.5	35	0.5	35	0.5	35	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	36	0.5	35	0.5	30	0.5	29	
			–40°C to 125°C	0.5	36	0.5	35	0.5	30	0.5	29	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	ns
			–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	19	0.5	16	0.5	13	0.5	11	
			–40°C to 125°C	0.5	19	0.5	16	0.5	13	0.5	11	

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6.12 Switching Characteristics, V_{CCA} = 2.5 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	87	0.5	42	0.5	23	0.5	8	ns
			–40°C to 125°C	0.5	87	0.5	42	0.5	23	0.5	8	
		B input to A output	–40°C to 85°C	0.5	62	0.5	26	0.5	15	0.5	8	
			–40°C to 125°C	0.5	62	0.5	26	0.5	15	0.5	8	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	173	0.5	137	0.5	117	0.5	40	
			–40°C to 125°C	0.5	173	0.5	137	0.5	117	0.5	40	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	211	0.5	107	0.5	63	0.5	24	
			–40°C to 125°C	0.5	211	0.5	107	0.5	63	0.5	24	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	6	0.5	6	0.5	5	0.5	5	ns
			–40°C to 125°C	0.5	6	0.5	6	0.5	5	0.5	5	
		B input to A output	–40°C to 85°C	0.5	6	0.5	6	0.5	5	0.5	4	
			–40°C to 125°C	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	34	0.5	33	0.5	28	0.5	28	
			–40°C to 125°C	0.5	34	0.5	33	0.5	28	0.5	28	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	16	0.5	14	0.5	10	0.5	9	
			–40°C to 125°C	0.5	16	0.5	14	0.5	10	0.5	9	

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6.13 Switching Characteristics, V_{CCA} = 3.3 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	87	0.5	41	0.5	22	0.5	8	ns
			–40°C to 125°C	0.5	87	0.5	41	0.5	22	0.5	8	
		B input to A output	–40°C to 85°C	0.5	151	0.5	36	0.5	18	0.5	8	
			–40°C to 125°C	0.5	151	0.5	36	0.5	18	0.5	8	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	27	0.5	27	0.5	27	0.5	27	ns
			–40°C to 125°C	0.5	27	0.5	27	0.5	27	0.5	27	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	172	0.5	136	0.5	116	0.5	39	
			–40°C to 125°C	0.5	172	0.5	136	0.5	116	0.5	39	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	210	0.5	106	0.5	62	0.5	23	
			–40°C to 125°C	0.5	210	0.5	106	0.5	62	0.5	23	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	5	0.5	5	0.5	4	0.5	4	ns
			–40°C to 125°C	0.5	5	0.5	5	0.5	4	0.5	4	
		B input to A output	–40°C to 85°C	0.5	6	0.5	5	0.5	5	0.5	4	
			–40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	27	0.5	27	0.5	27	0.5	27	ns
			–40°C to 125°C	0.5	27	0.5	27	0.5	27	0.5	27	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	33	0.5	32	0.5	27	0.5	27	
			–40°C to 125°C	0.5	33	0.5	32	0.5	27	0.5	27	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	15	0.5	13	0.5	10	0.5	8	
			–40°C to 125°C	0.5	15	0.5	13	0.5	10	0.5	8	

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6.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		3.0		pF
			V_{CCA} = V_{CCB} = 0.8 V		3.0		
			V_{CCA} = V_{CCB} = 0.9 V		3.0		
			V_{CCA} = V_{CCB} = 1.2 V		3.1		
			V_{CCA} = V_{CCB} = 1.5 V		3.0		
			V_{CCA} = V_{CCB} = 1.8 V		3.2		
			V_{CCA} = V_{CCB} = 2.5 V		3.7		
			V_{CCA} = V_{CCB} = 3.3 V		4.4		
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.5		pF
			V_{CCA} = V_{CCB} = 0.8 V		2.5		
			V_{CCA} = V_{CCB} = 0.9 V		2.6		
			V_{CCA} = V_{CCB} = 1.2 V		2.6		
			V_{CCA} = V_{CCB} = 1.5 V		2.6		
			V_{CCA} = V_{CCB} = 1.8 V		2.7		
			V_{CCA} = V_{CCB} = 2.5 V		3.2		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		12.6		pF
			V_{CCA} = V_{CCB} = 0.8 V		12.3		
			V_{CCA} = V_{CCB} = 0.9 V		12.4		
			V_{CCA} = V_{CCB} = 1.2 V		12.4		
			V_{CCA} = V_{CCB} = 1.5 V		12.7		
			V_{CCA} = V_{CCB} = 1.8 V		13.6		
			V_{CCA} = V_{CCB} = 2.5 V		17.4		
			V_{CCA} = V_{CCB} = 3.3 V		20.9		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.2		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.1		
			V_{CCA} = V_{CCB} = 0.9 V		1.1		
			V_{CCA} = V_{CCB} = 1.2 V		1.0		
			V_{CCA} = V_{CCB} = 1.5 V		1.0		
			V_{CCA} = V_{CCB} = 1.8 V		0.9		
			V_{CCA} = V_{CCB} = 2.5 V		0.9		
			V_{CCA} = V_{CCB} = 3.3 V		0.9		

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Operating Characteristics: T_A = 25°C (continued)

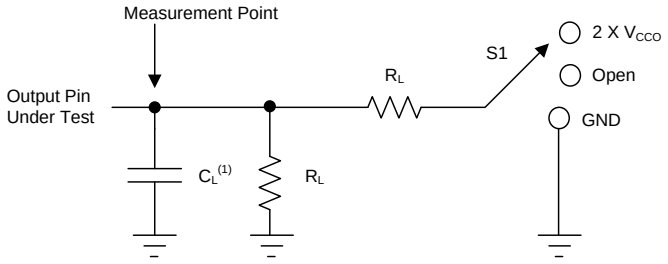
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		12.6		pF
			V_{CCA} = V_{CCB} = 0.8 V		12.4		
			V_{CCA} = V_{CCB} = 0.9 V		12.4		
			V_{CCA} = V_{CCB} = 1.2 V		12.4		
			V_{CCA} = V_{CCB} = 1.5 V		12.6		
			V_{CCA} = V_{CCB} = 1.8 V		13.6		
			V_{CCA} = V_{CCB} = 2.5 V		17.2		
			V_{CCA} = V_{CCB} = 3.3 V		20.8		
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.4		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.3		
			V_{CCA} = V_{CCB} = 0.9 V		1.3		
			V_{CCA} = V_{CCB} = 1.2 V		1.2		
			V_{CCA} = V_{CCB} = 1.5 V		1.1		
			V_{CCA} = V_{CCB} = 1.8 V		1.1		
			V_{CCA} = V_{CCB} = 2.5 V		1.1		
			V_{CCA} = V_{CCB} = 3.3 V		1.0		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		3.3		pF
			V_{CCA} = V_{CCB} = 0.8 V		3.3		
			V_{CCA} = V_{CCB} = 0.9 V		3.3		
			V_{CCA} = V_{CCB} = 1.2 V		3.2		
			V_{CCA} = V_{CCB} = 1.5 V		3.2		
			V_{CCA} = V_{CCB} = 1.8 V		3.3		
			V_{CCA} = V_{CCB} = 2.5 V		3.6		
			V_{CCA} = V_{CCB} = 3.3 V		4.4		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.8		pF
			V_{CCA} = V_{CCB} = 0.8 V		2.8		
			V_{CCA} = V_{CCB} = 0.9 V		2.8		
			V_{CCA} = V_{CCB} = 1.2 V		2.8		
			V_{CCA} = V_{CCB} = 1.5 V		2.7		
			V_{CCA} = V_{CCB} = 1.8 V		2.8		
			V_{CCA} = V_{CCB} = 2.5 V		3.1		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		

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7 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f =1 MHz
- Z_0 = 50 Ω
- dv / dt ≤ 1 ns/V



(1) C_L includes probe and jig capacitance.

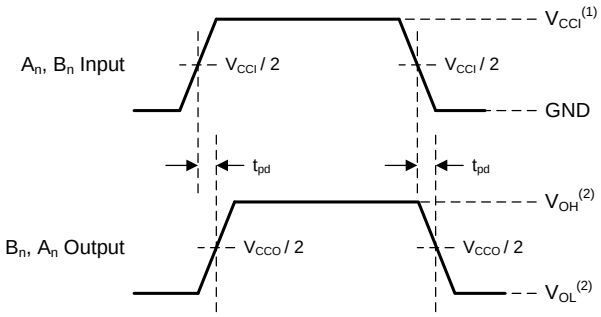
图 1. Load Circuit

Parameter	V_{CCO}	R_L	C_L	S1	V_{TP}
t_{pd}	1.1 V - 3.6 V	2 kΩ	15 pF	Open	N/A
	0.65 V - 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}(1), t_{dis}(1)	3 V - 3.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.3 V
	1.65 V - 2.7 V	2 kΩ	15 pF	2 X V_{CCO}	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	2 X V_{CCO}	0.1 V
t_{en}(2), t_{dis}(2)	3 V - 3.6 V	2 kΩ	15 pF	GND	0.3 V
	1.65V - 2.7 V	2 kΩ	15 pF	GND	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	GND	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	GND	0.1 V

(1) Output waveform on the conditions that input is driven to a valid Logic Low.

(2) Output waveform on the condition that input is driven to a valid Logic High.

图 2. Load Circuit Conditions



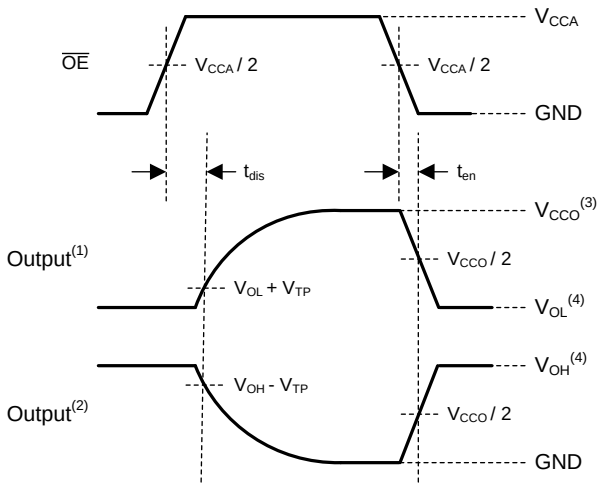
(1) V_{CCI} is the supply pin associated with the input port.

(2) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

图 3. Propagation Delay

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Parameter Measurement Information (接下页)



(1) Output waveform on the condition that input is driven to a valid Logic Low.

(2) Output waveform on the condition that input is driven to a valid Logic High.

(3) V_{CCO} is the supply pin associated with the output port.

(4) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

图 4. Enable Time And Disable Time

8 Detailed Description

8.1 Overview

The SN74AXCH8T245 device is an 8-bit, dual-supply non-inverting transceiver with bidirectional voltage level translation. The I/O pins labeled with A and the control pins (DIR1, DIR2, and $\overline{OE}$) are supported by V_{CCA}, and the I/O pins labeled with B are supported by V_{CCB}. Both the A port and the B port are able to accept I/O voltages ranging from 0.65 V to 3.6 V.

8.2 Functional Block Diagram

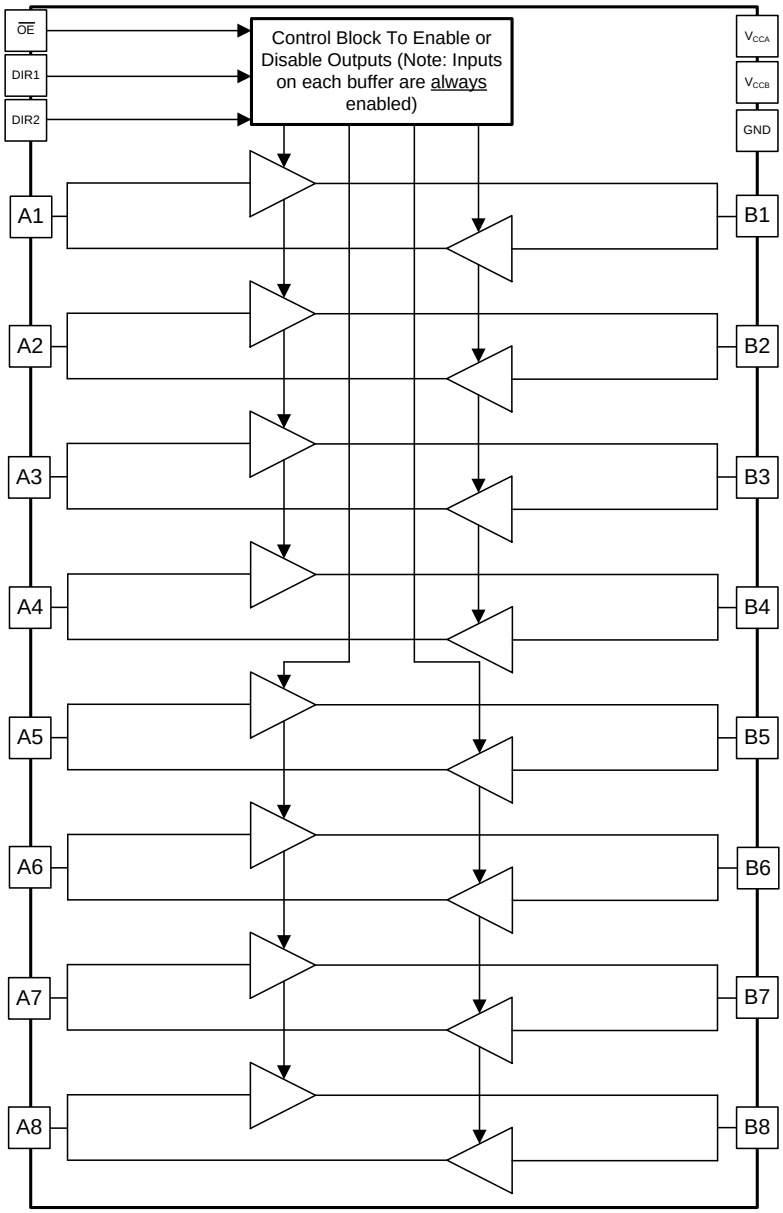


图 5. Functional Block Diagram

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8.3 Feature Description

8.3.1 Up-Translation and Down-Translation From 0.65 V to 3.6 V

Both supply pins are configurable over the full 0.65 V to 3.6 V voltage range, which makes the device suitable for translating between any of the low voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Multiple Direction Control Pins

Two control pins are used to configure the 8 data I/Os. I/O channels 1 through 4 are grouped together and I/O channels 5 through 8 are banked together. The benefit of this is to permit simultaneous up-translation and down-translation within one device. This eliminates the need for multiple devices, where each device can only provide up-translation or down-translation sequentially. Simultaneous up and down translation is supported when both V_{CCA} and V_{CCB} are at least 1.40 V.

8.3.3 Bus-Hold Circuitry

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state, which helps with board space savings and reduced component costs. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. See the Bus-Hold Circuit application note for more details. (SCLA015).

Note that the bus-hold circuitry always remains active when the corresponding supply is present (i.e. B port bus-hold circuits are active when V_{CCB} is present, and A port bus-hold circuits are active when V_{CCA} is present). The bus hold circuitry is also active even when the device is in a partial power down state or when the output enable pin is used to place all outputs into high impedance.

8.3.4 I_{off} Supports Partial-Power-Down Mode Operation

This feature is to limit the leakage current of an I/O pin being driven to a voltage as large as 3.6 V while having its corresponding power supply rail powered down. This is represented by the I_{off} parameter in the *Electrical Characteristics* table.

8.4 Device Functional Modes

All control inputs are referenced to V_{CCA} and must be driven to a valid Logic High or Logic Low (that is, not floating) to assure proper device operation and to prevent excessive power consumption. 表 1 summarizes the possible modes of device operation based on the configuration of the control inputs.

表 1. Function Table(1)

CONTROL INPUTS			Signal Direction	
$\overline{OE}$	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	
L	L	H	B to A	A to B
L	H	L	A to B	
L	H	H	A to B	B to A

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different voltage nodes. 图 6 depicts an application in which the SN74AXCH8T245 device is up-translating a 0.7 V input to a 3.3 V output to interface between a system controller and a peripheral device.

9.2 Typical Application

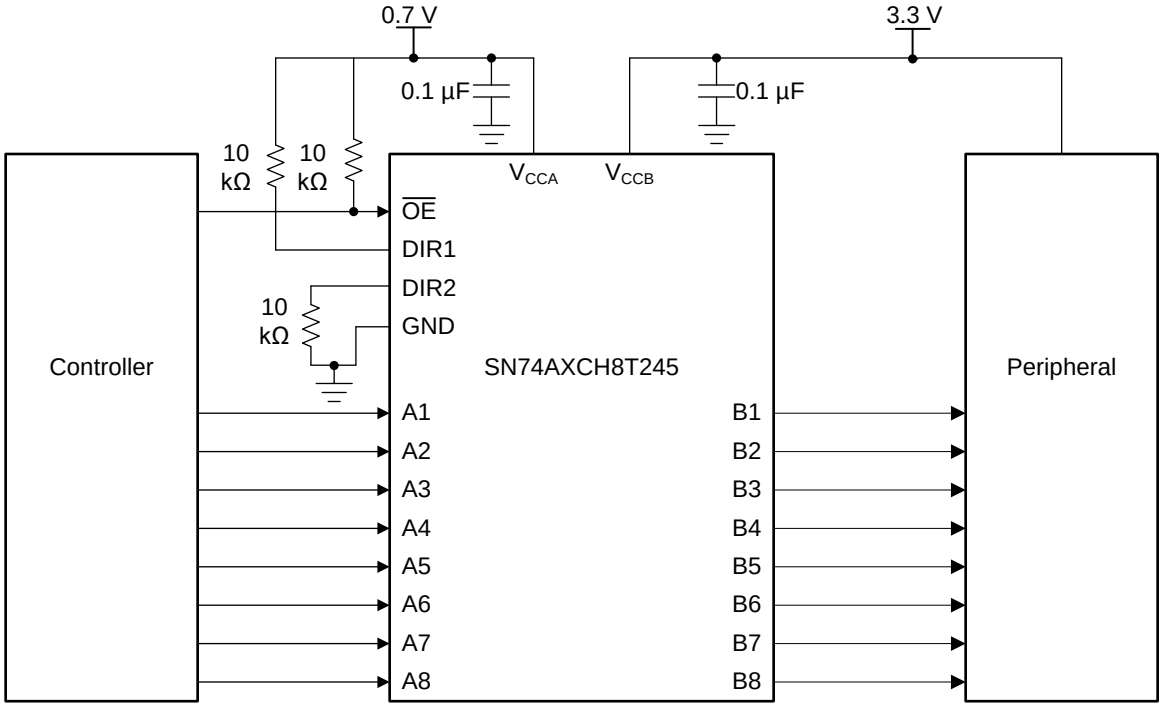


图 6. Typical Application Schematic

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Typical Application (接下页)

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 2.

表 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXCH8T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXCH8T245 device is driving to determine the output voltage range.

9.2.3 Application Curve

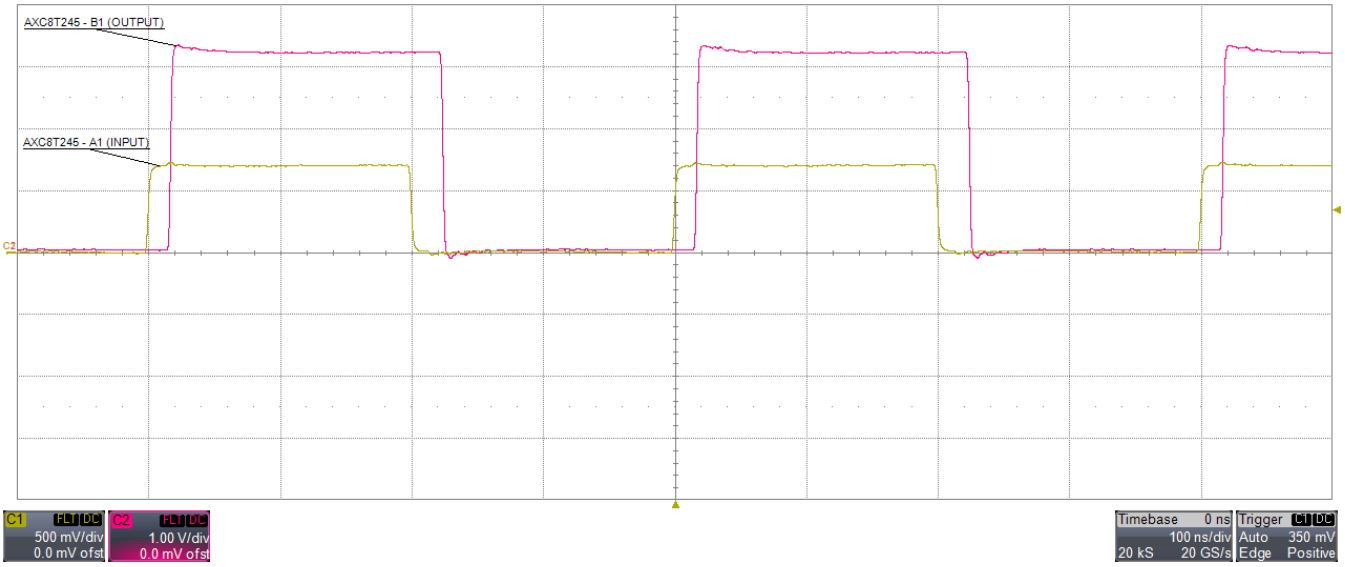


图 7. Translation Up (0.7 V to 3.3 V) at 2.5 MHz

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. However, there are no additional requirements for power supply sequencing.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Power Sequencing for AXC Family of Devices* application report.

11 Layout

11.1 Layout Guidelines

To assure reliability of the device, follow common printed-circuit board layout guidelines.

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

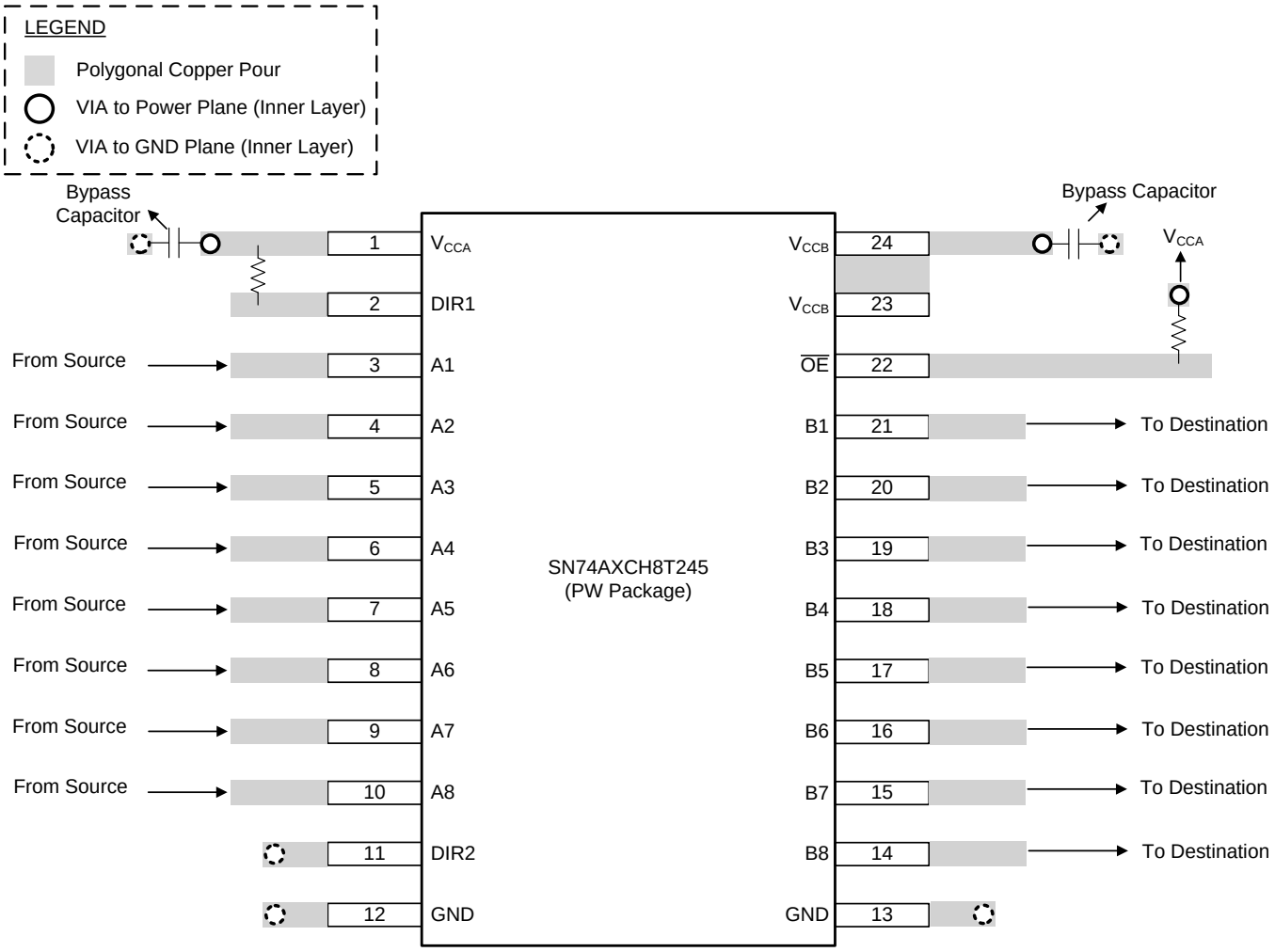


图 8. SN74AXCH8T245 Device Layout Example

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

德州仪器 (TI)，*《慢速或浮点 CMOS 输入的影响》*应用报告

德州仪器 (TI)，*《AXC 系列器件电源定序》* 应用报告

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AXCH8T245RHLRG4	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
74AXCH8T245RHLRG4.B	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245PWR.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245PWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245PWRG4.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245RHLR	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245RHLR.B	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AH8T245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

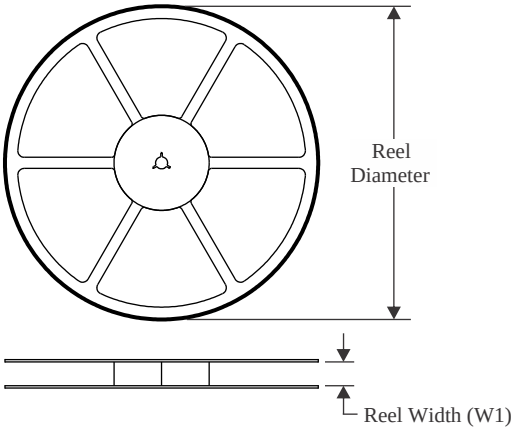
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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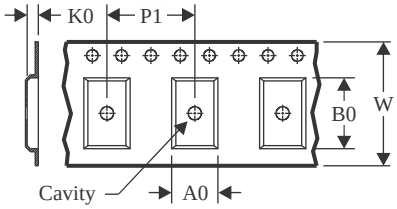
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

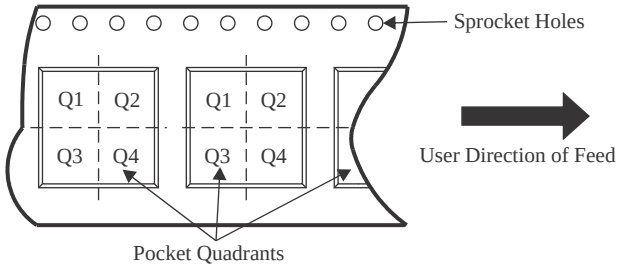


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

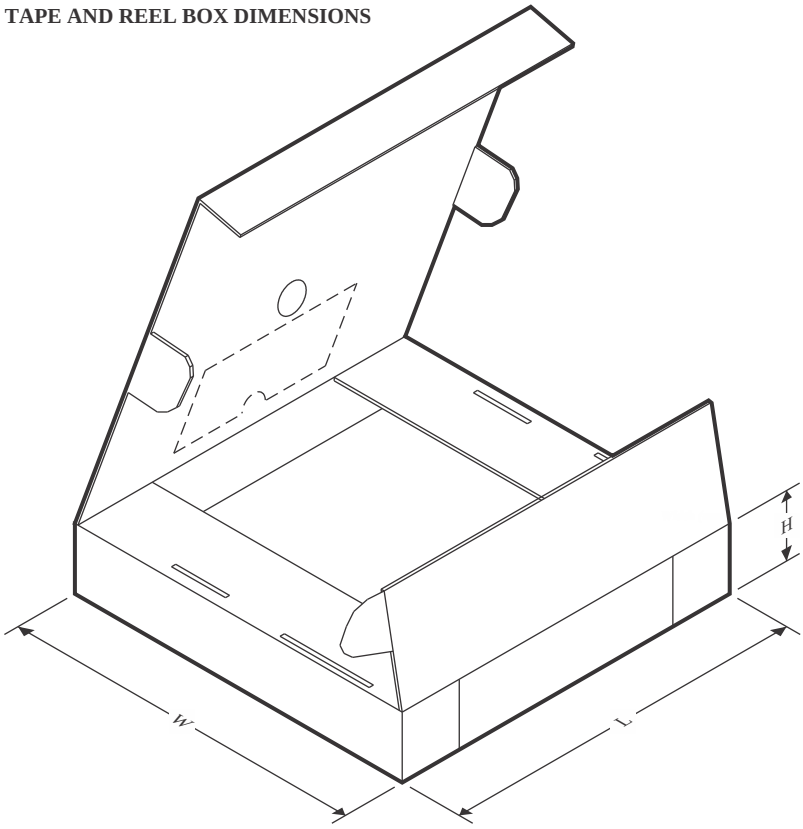
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

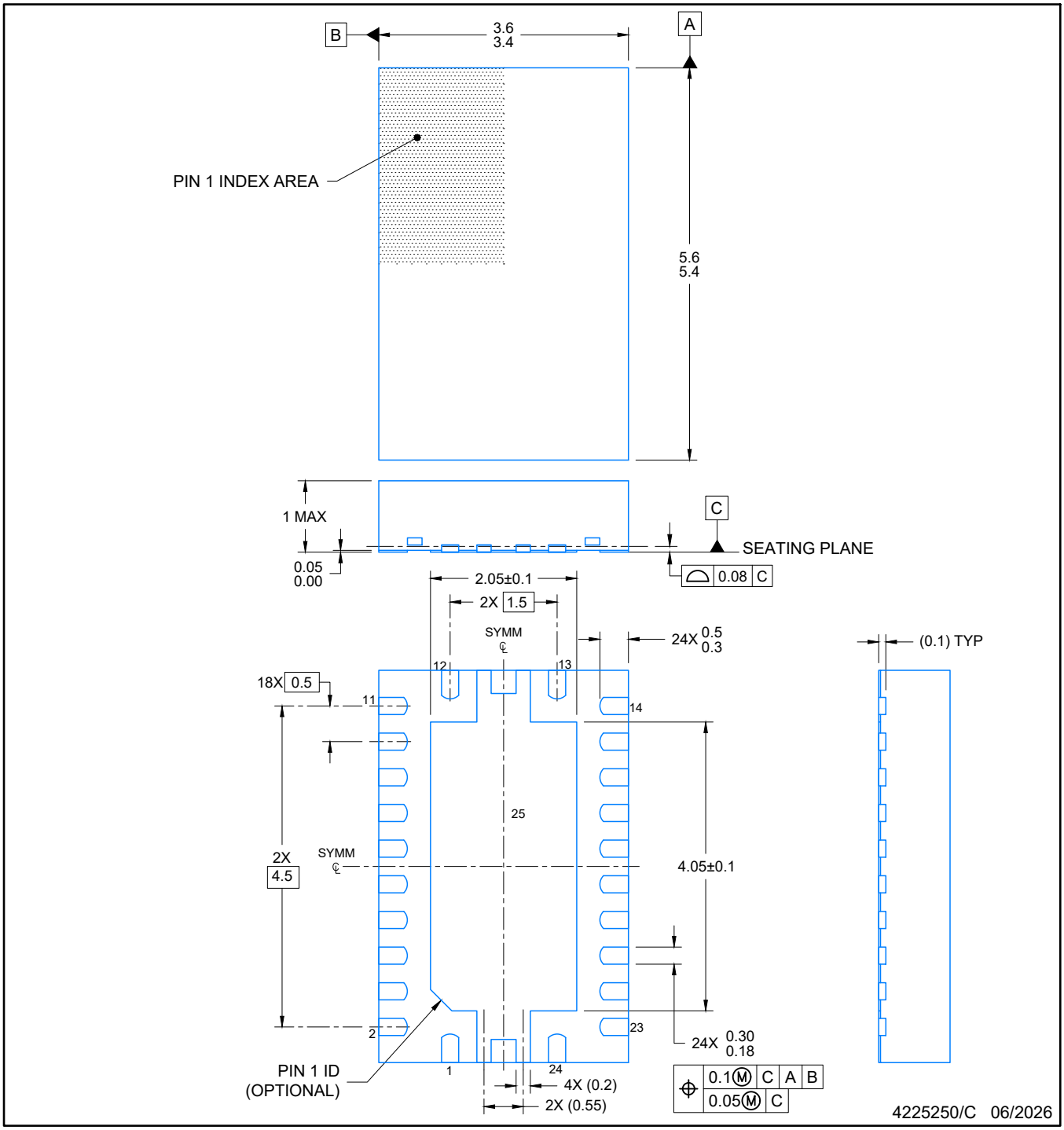
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AXCH8T245RHLRG4	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74AXCH8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AXCH8T245PWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AXCH8T245RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



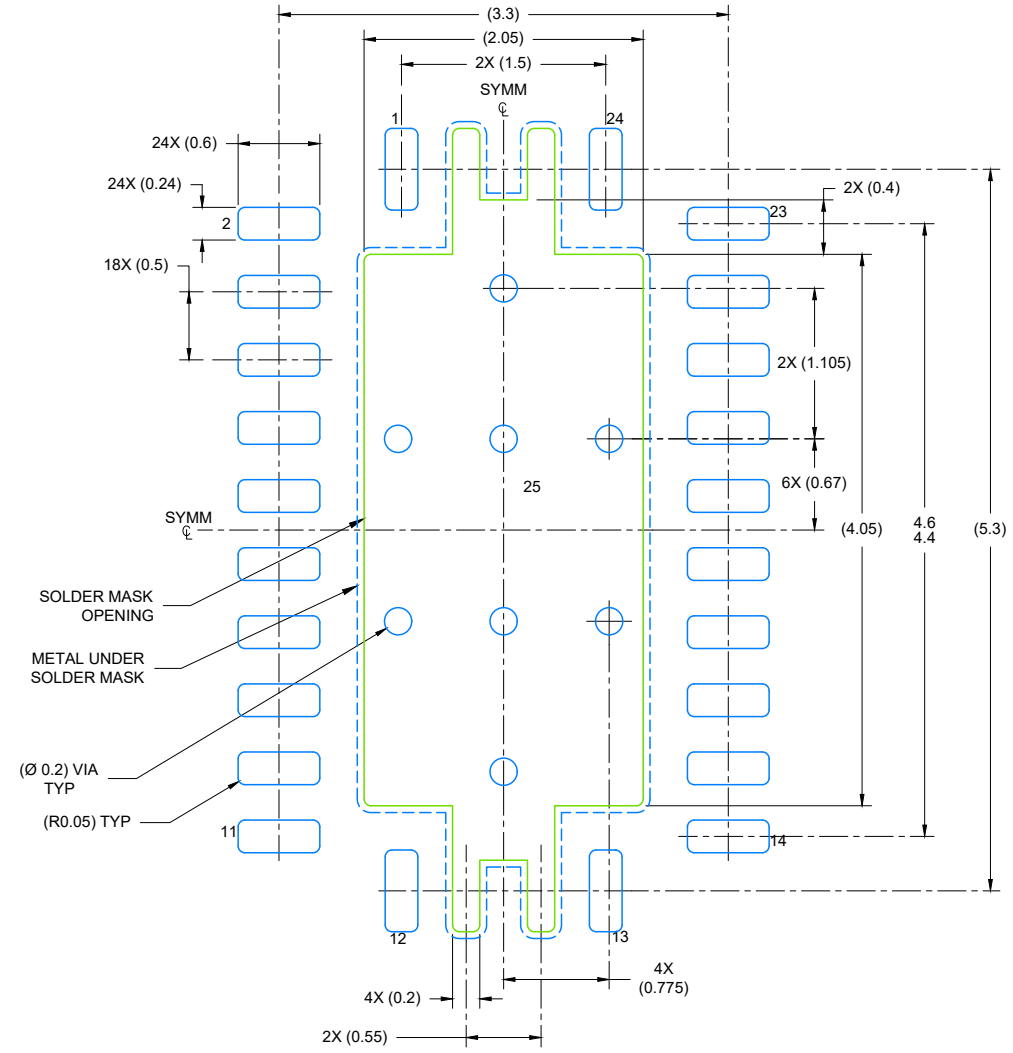
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AXCH8T245RHLRG4	VQFN	RHL	24	3000	367.0	367.0	35.0
SN74AXCH8T245PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
SN74AXCH8T245PWRG4	TSSOP	PW	24	2000	353.0	353.0	32.0
SN74AXCH8T245RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0

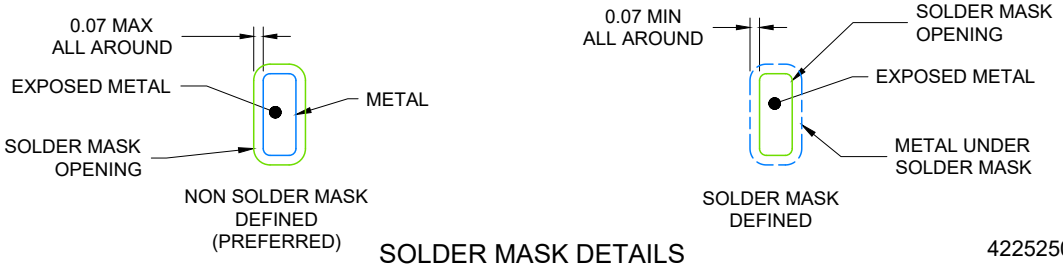


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

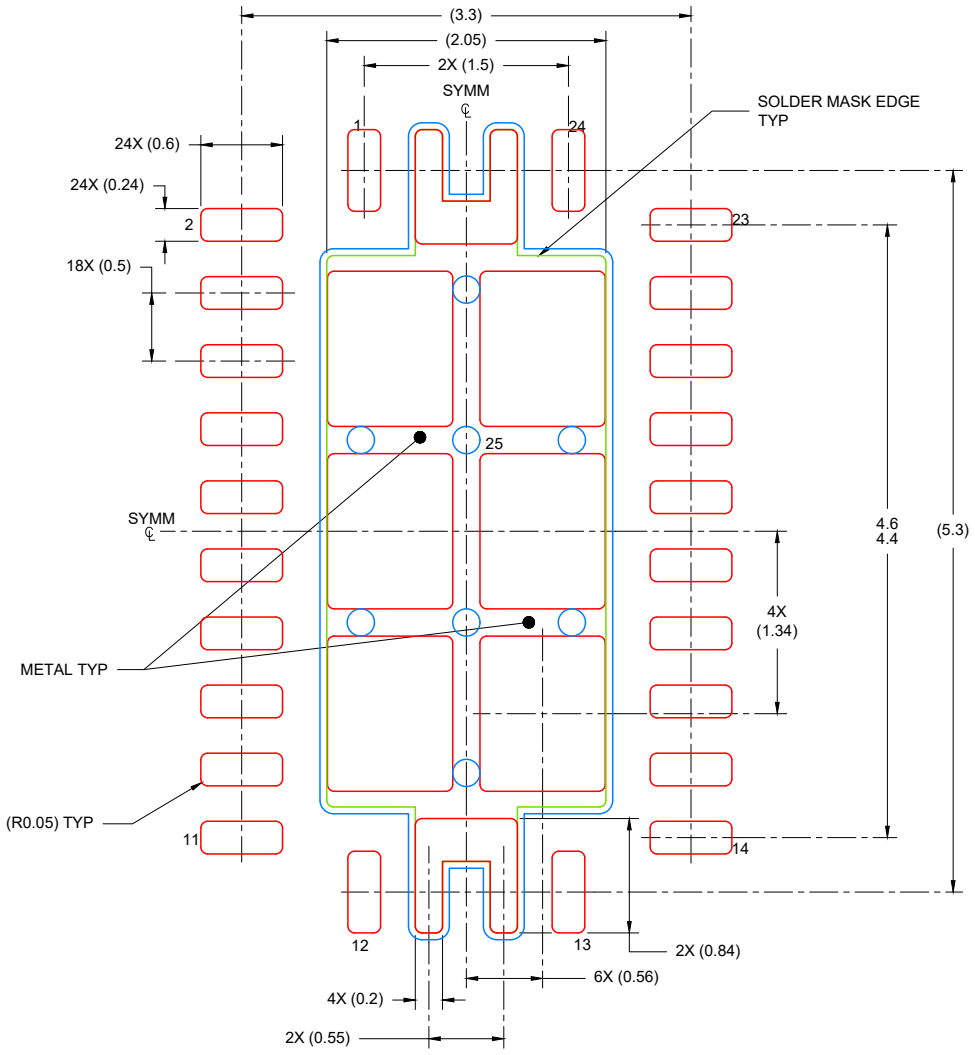


SOLDER MASK DETAILS

4225250/C 06/2026

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/C 06/2026

NOTES: (continued)

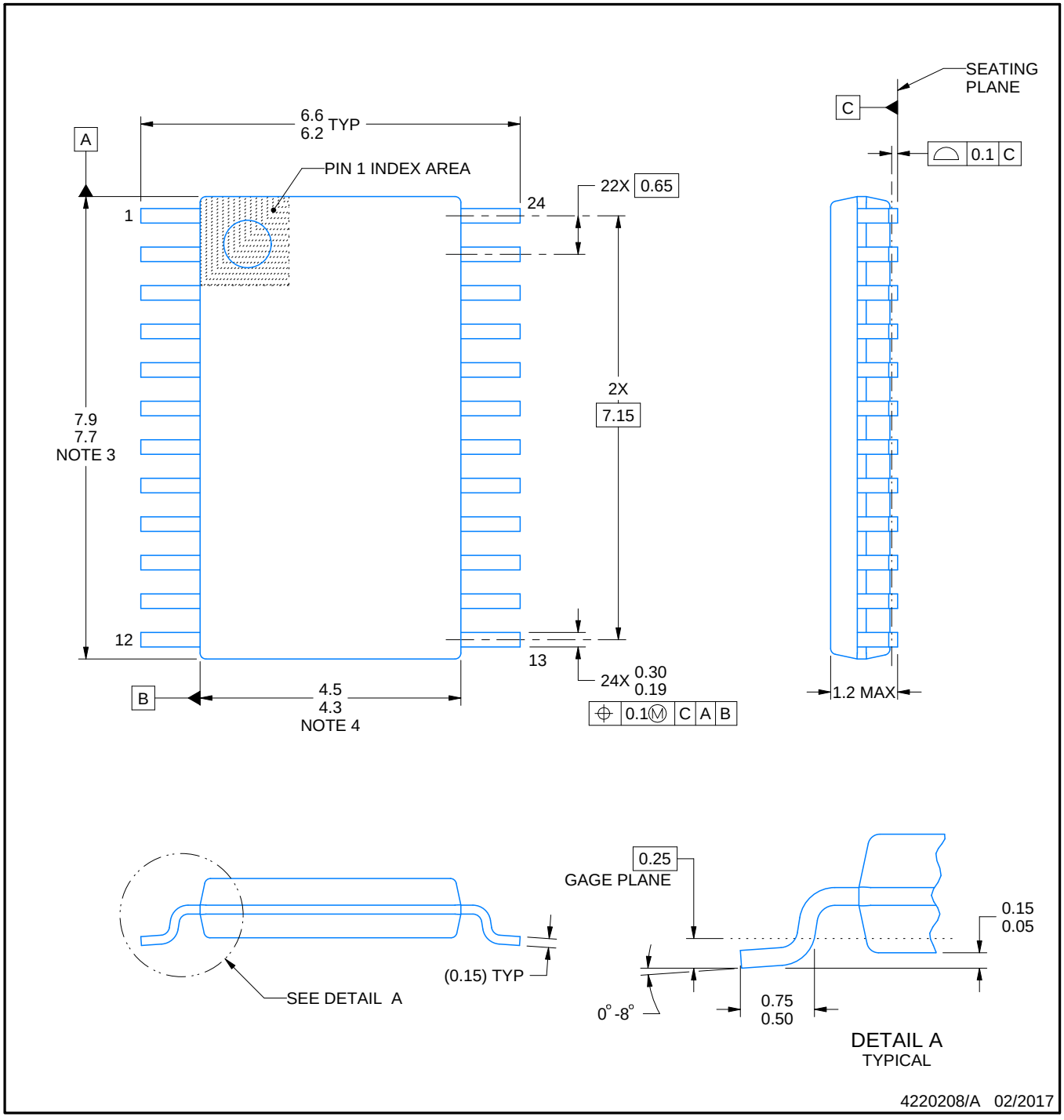
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0024A

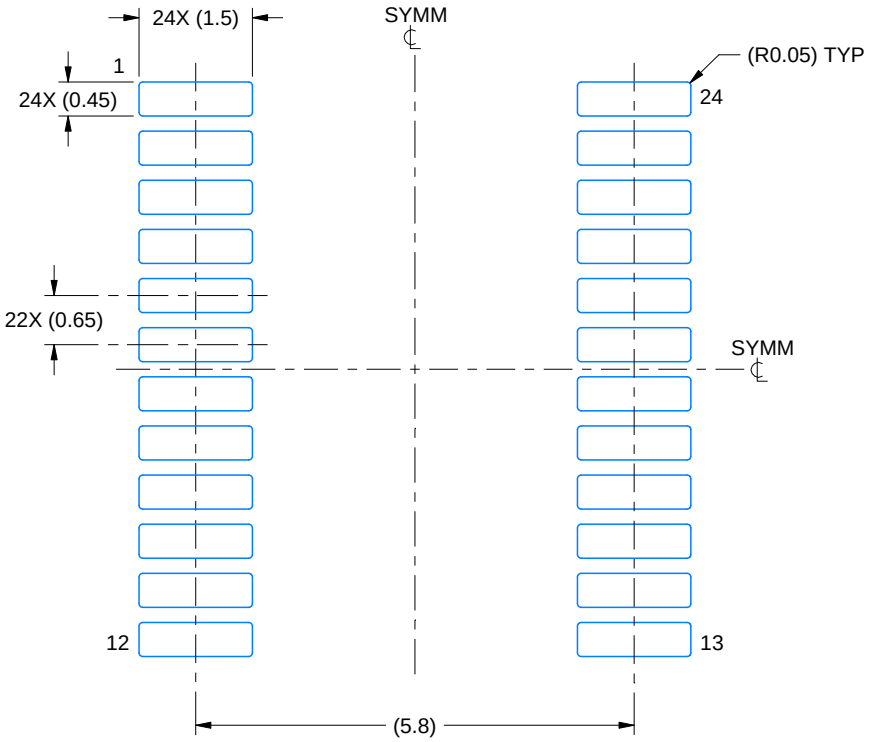
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

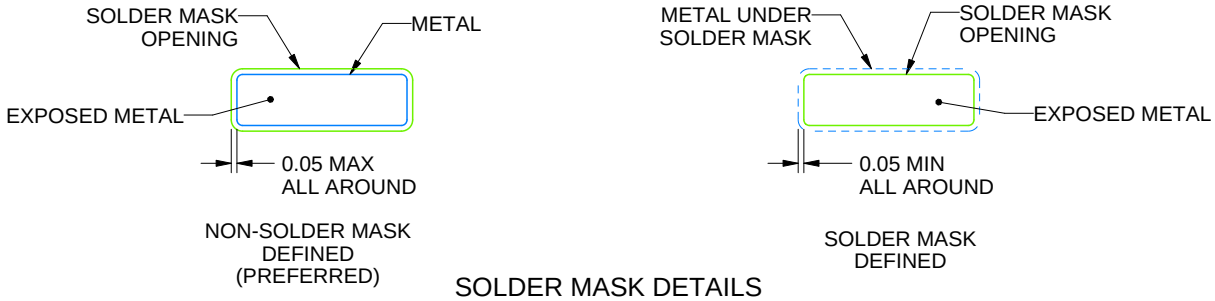


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

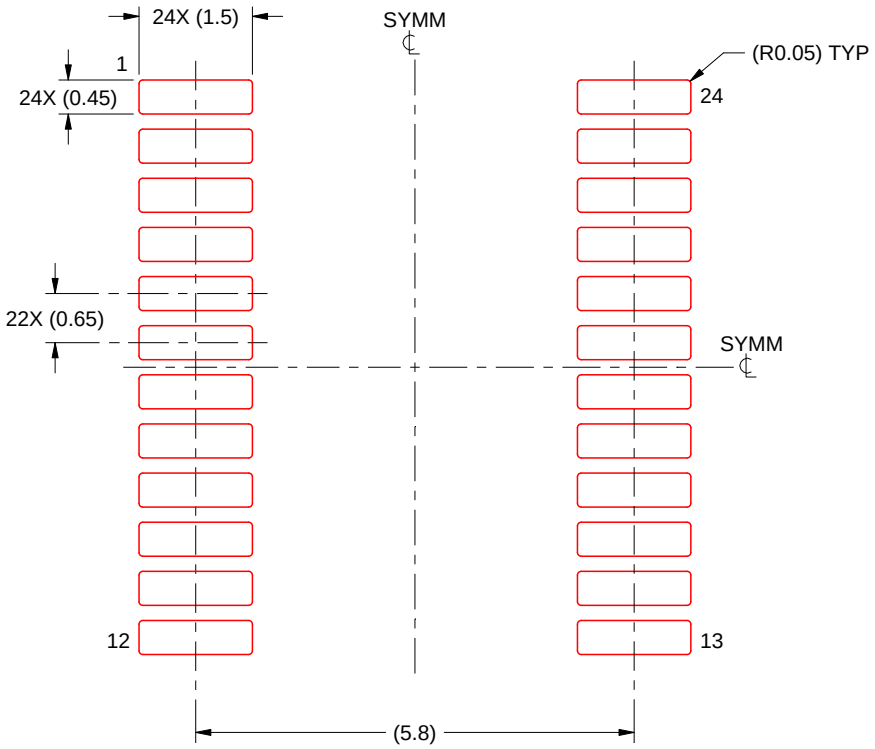


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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