SN74CB3Q3306A Dual FET Bus Switch 2.5V/3.3V Low-Voltage High-Bandwidth Bus Switch

1 Features

- High-Bandwidth Data Path (up to 500MHz)
- 5V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4Ω Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0 to 5V Switching With 3.3V V_{CC}
  - 0 to 3.3V Switching With 2.5V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input and Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5pF Typ)
- Fast Switching Frequency ($f_{\overline{OE}}$ = 20MHz Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 0.25mA Typ)
- V_{CC} Operating Range From 2.3V to 3.6V
- Data I/Os Support 0 to 5V Signaling Levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control Inputs Can Be Driven by TTL or 5V/3.3V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000V Human-Body Model (A114-B, Class II)
  - 1000V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating

2 Description

The SN74CB3Q3306A device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3306A device provides an optimized interface option appropriate for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3306A device is organized as two 1-bit switches with separate output-enable (1 $\overline{OE}$, 2 $\overline{OE}$) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

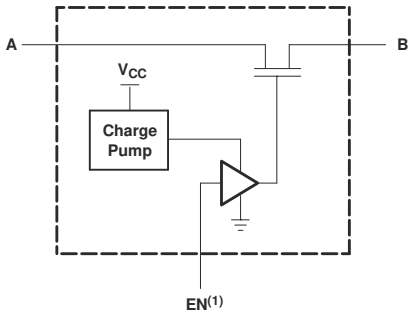
The SN74CB3Q3306A device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To confirm the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74CB3Q3306A	VSSOP (8)	2.00mm × 3.10mm
	TSSOP (8)	3.00mm × 6.10mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



(1) EN is the internal enable signal applied to the switch.

Simplified Schematic, Each FET Switch (SW)

Table of Contents

3 Pin Configuration and Functions

DCU PACKAGE
(TOP VIEW)

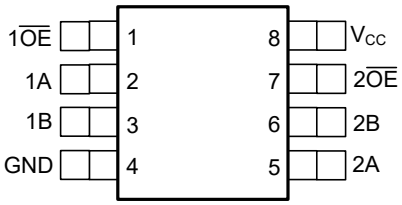


Figure 3-1. DCU Package 8-Pin Top View

PW PACKAGE
(TOP VIEW)

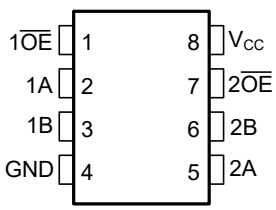


Figure 3-2. PW Package 8-Pin Top View

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 A port
1B	3	I/O	Channel 1 B port
1$\overline{OE}$	1	I	Output Enable for switch 1
2A	5	I/O	Channel 2 A port
2B	6	I/O	Channel 2 B port
2$\overline{OE}$	7	I	Output Enable for switch 2
GND	4	P	Ground
V_{cc}	8	P	Power supply

(1) I = input, O = output, I/O = input and output, P = power

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)	DCU		205.3	°C/W
		PW		173.7	
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

4.2 Recommended Operating Conditions

(1)			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7	5.5	V
		V_{CC} = 2.7V to 3.6V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.7	V
		V_{CC} = 2.7V to 3.6V	0	0.8	
$V_{I/O}$	Data input or output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

4.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

4.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3305 DCU (VSSOP) 8 PINS	SN74CB3Q3305 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.3	173.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.8	85.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	118	109.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.1	27.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	117.2	108.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the application note, *Semiconductor and IC Package Thermal Metrics*.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6V,	I_I = –18mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6V,	V_{IN} = 0 to 5.5V				±1	µA
I_{OZ}[3]		V_{CC} = 3.6V,	V_O = 0 to 5.5V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.25	0.7	mA
ΔI_{CC}[4]	Control inputs	V_{CC} = 3.6V,	One input at 3V,	Other inputs at V_{CC} or GND			25	µA
I_{CCD}[5]	Per control input	V_{CC} = 3.6V, Control input switching at 50% duty cycle	A and B ports open,			0.06	0.1	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3V,	V_{IN} = 5.5V, 3.3V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		8	10.5	pF
r_{on}[6]		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0,	I_O = 30mA		4	8	Ω
			V_I = 1.7V,	I_O = –15mA		5	9	
		V_{CC} = 3V	V_I = 0,	I_O = 30mA		4	6	
			V_I = 2.4V,	I_O = –15mA		5	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 4-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$(1)	$\overline{OE}$	A or B		10		20	MHz
t_{pd}(2)	A or B	B or A		0.2		0.2	ns
t_{en}	$\overline{OE}$	A or B	1.5	11.2	1.5	11.5	ns
t_{dis}	$\overline{OE}$	A or B	1	14.2	1	11	ns

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5V, $R_L \geq 1M\Omega$, C_L = 0)
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

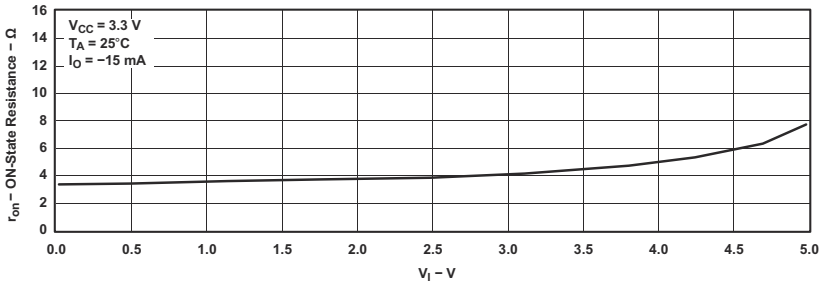


Figure 4-1. Typical r_{on} vs V_I

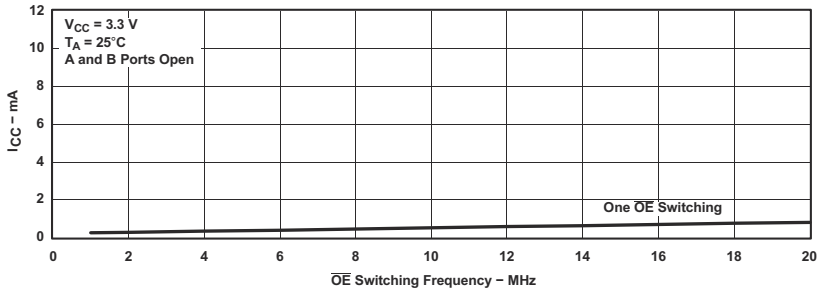
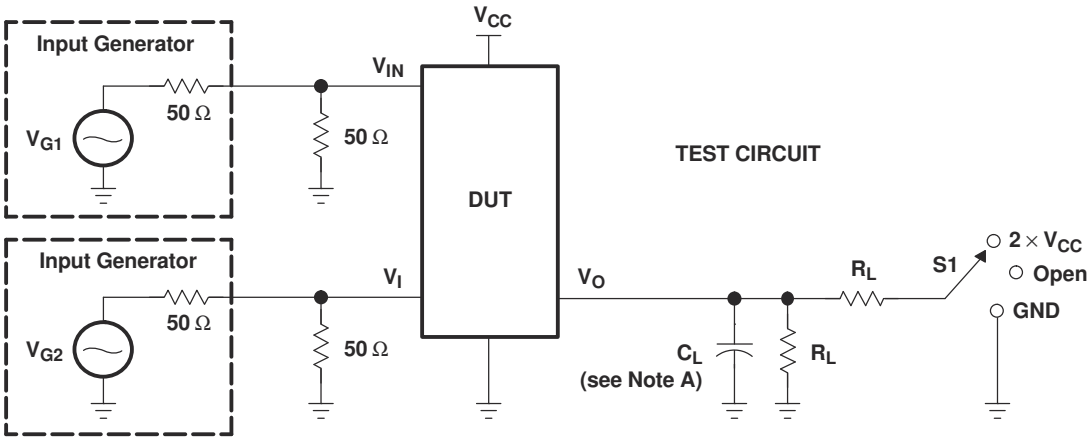
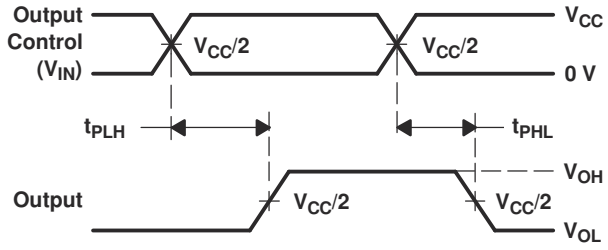


Figure 4-2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency

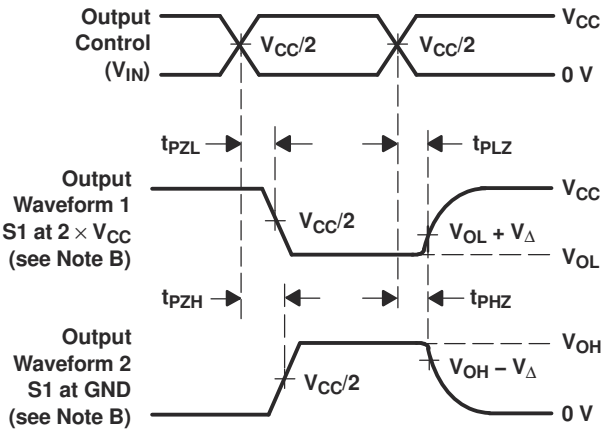
5 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



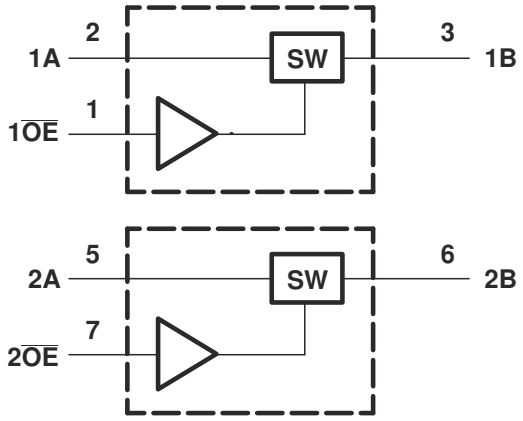
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Functional Block Diagram



6.2 Device Functional Modes

Table 6-1. Function Table

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Hi-Z	Disconnect

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2011) to Revision F (September 2026)	Page
• Removed ordering information	1
• Added package diagram	1
• Added Pin Configuration and Functions	3
• Updated Thermal Information	5
• Updated Electrical Characteristics	5
• Updated Switching Characteristics	6

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CB3Q3306ADCURE4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GA6R
74CB3Q3306ADCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GA6R
74CB3Q3306ADCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GA6R
SN74CB3Q3306ADCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(A6, GA6Q, GA6R) GZ
SN74CB3Q3306ADCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(A6, GA6Q, GA6R) GZ
SN74CB3Q3306ADCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(A6, GA6Q, GA6R) GZ
SN74CB3Q3306APW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	BU306A
SN74CB3Q3306APWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BU306A
SN74CB3Q3306APWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU306A
SN74CB3Q3306APWR.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU306A
SN74CB3Q3306APWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU306A
SN74CB3Q3306APWRG4.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU306A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74CB3Q3306A :

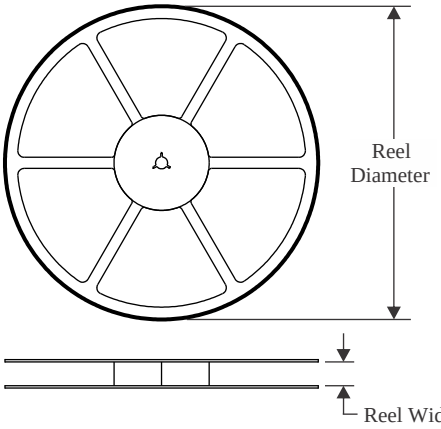
- Enhanced Product : SN74CB3Q3306A-EP

NOTE: Qualified Version Definitions:

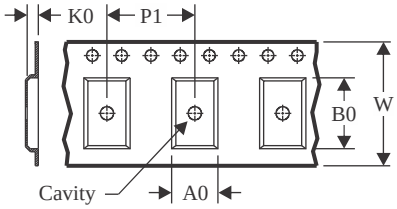
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

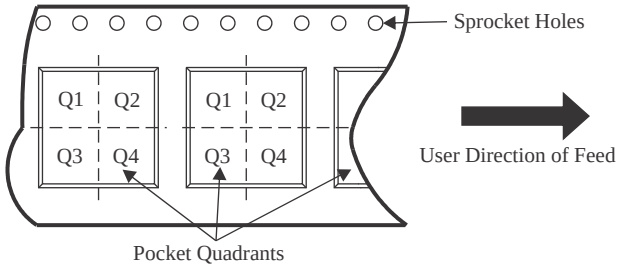


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

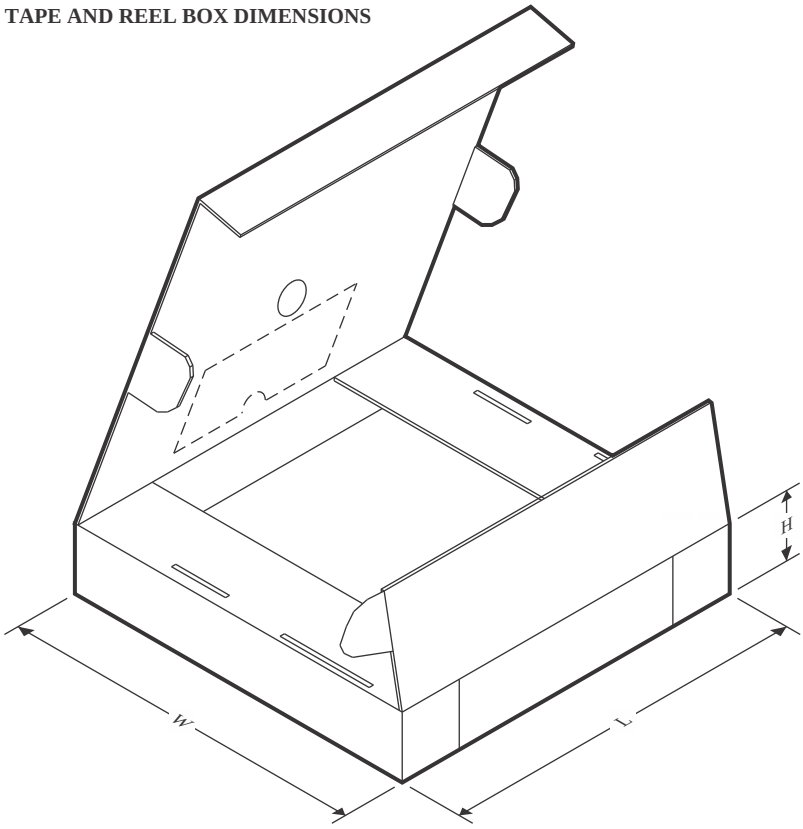
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3Q3306ADCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3306ADCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3306ADCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3306APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3306APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3306APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

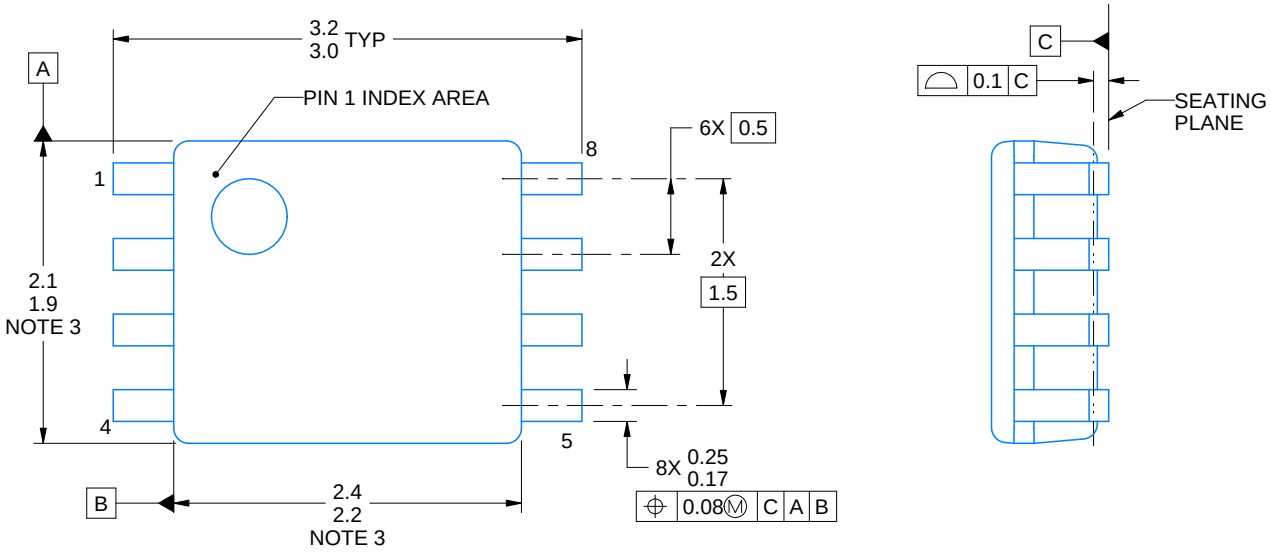
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3Q3306ADCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3306ADCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3306ADCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74CB3Q3306APWR	TSSOP	PW	8	2000	353.0	353.0	32.0
SN74CB3Q3306APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
SN74CB3Q3306APWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0

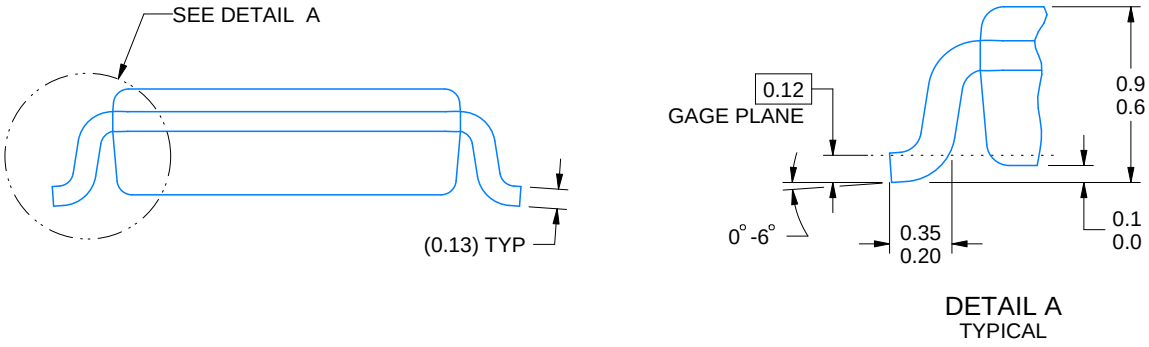
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

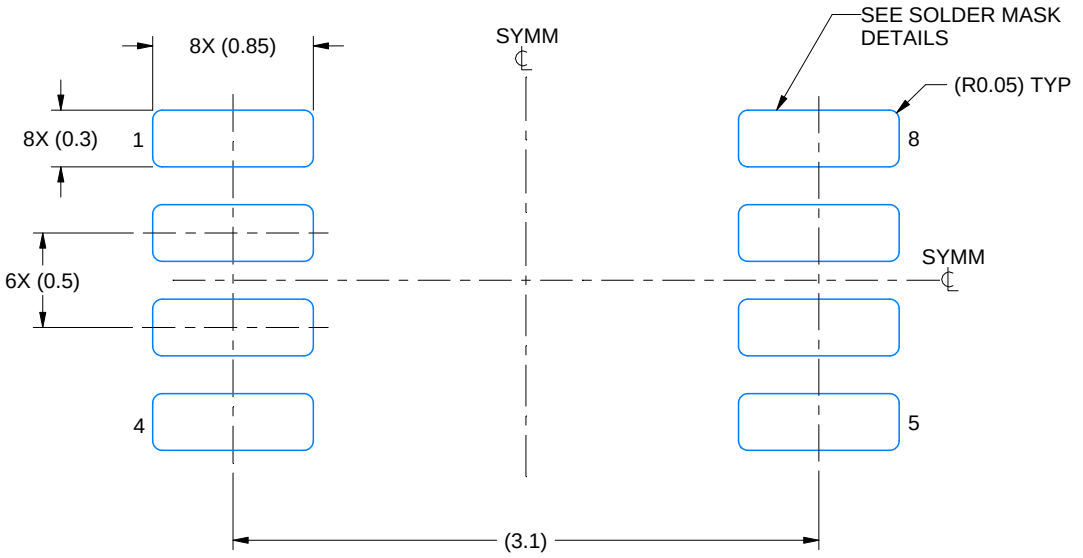




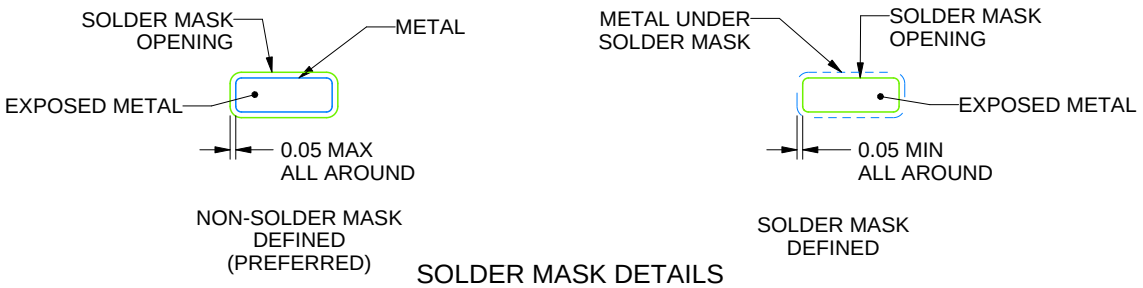
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

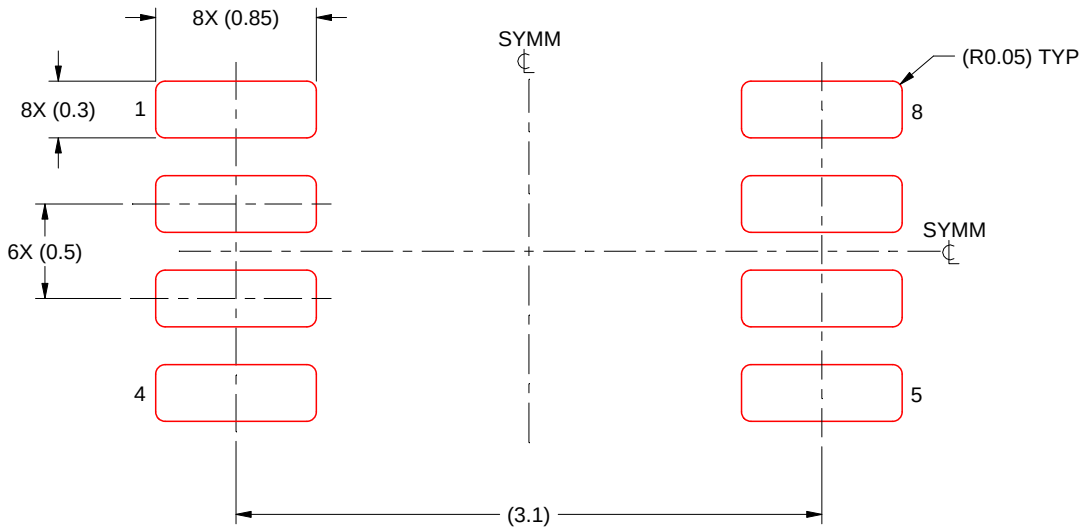


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

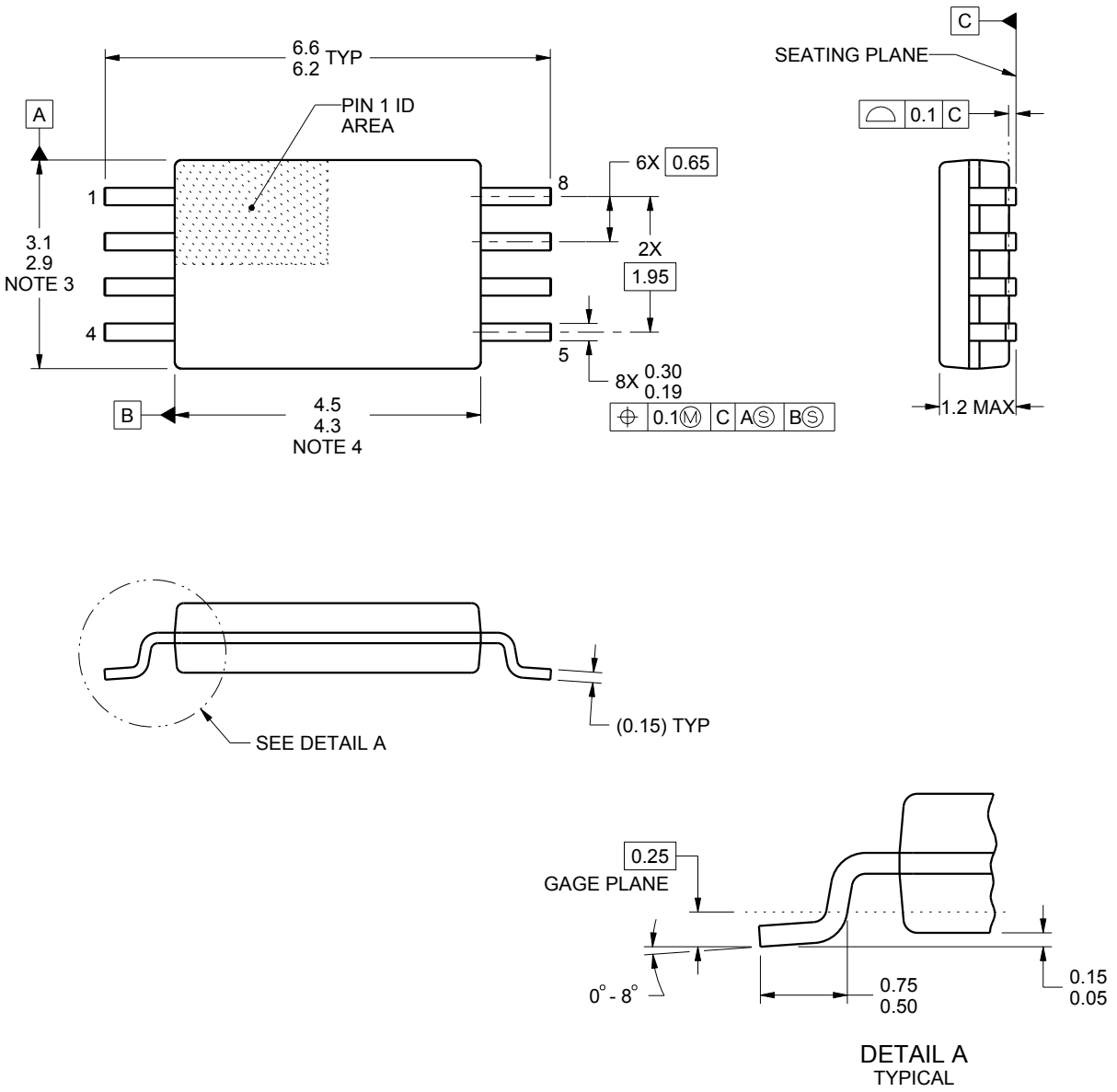
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

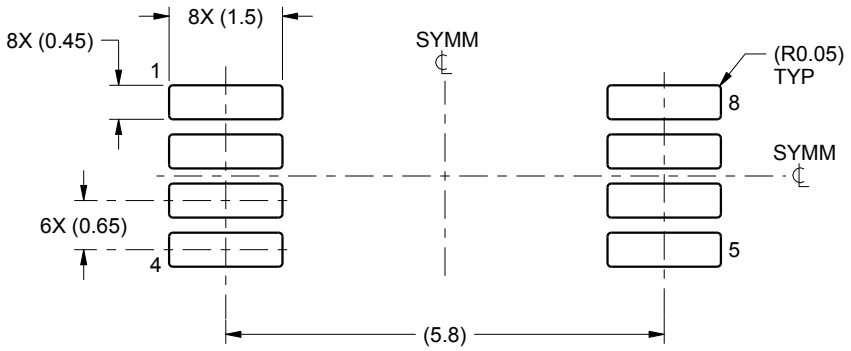
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

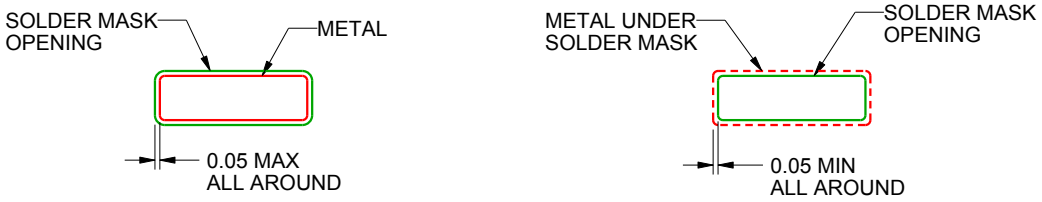


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

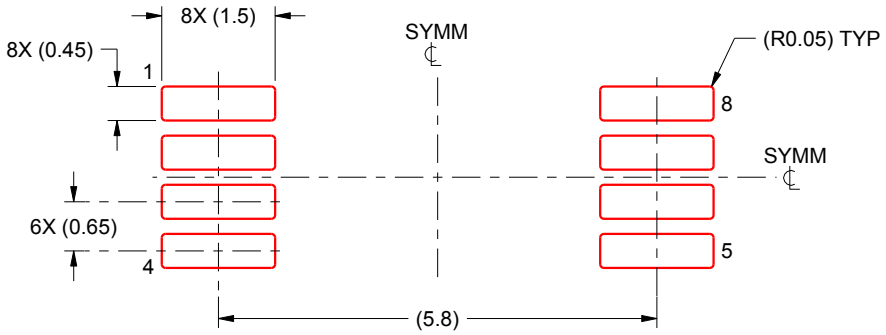


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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