

SN54CBT16209, SN74CBT16209A 18-BIT FET BUS-EXCHANGE SWITCHES

SCDS0060 – NOVEMBER 1992 – REVISED NOVEMBER 2004

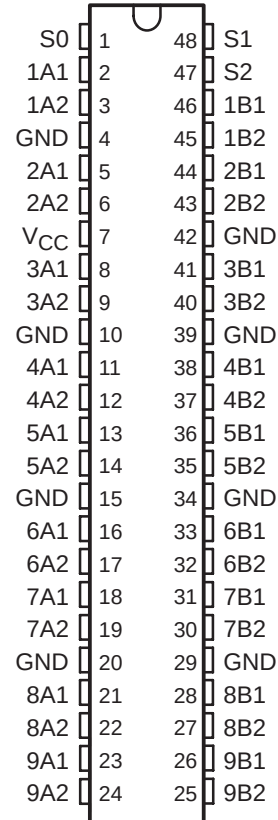
- Members of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

description/ordering information

The SN54CBT16209 and SN74CBT16209A devices provide 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switches allows connections to be made with minimal propagation delay.

The devices operate as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

SN54CBT16209 . . . WD PACKAGE
SN74CBT16209A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16209ADL	CBT16209A
		Tape and reel	SN74CBT16209ADLR	
	TSSOP – DGG	Tape and reel	SN74CBT16209ADGGR	CBT16209A
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74CBT16209ADGVR	CY209A
	CFP – WD	Tube	SNJ54CBT16209WD	SNJ54CBT16209WD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

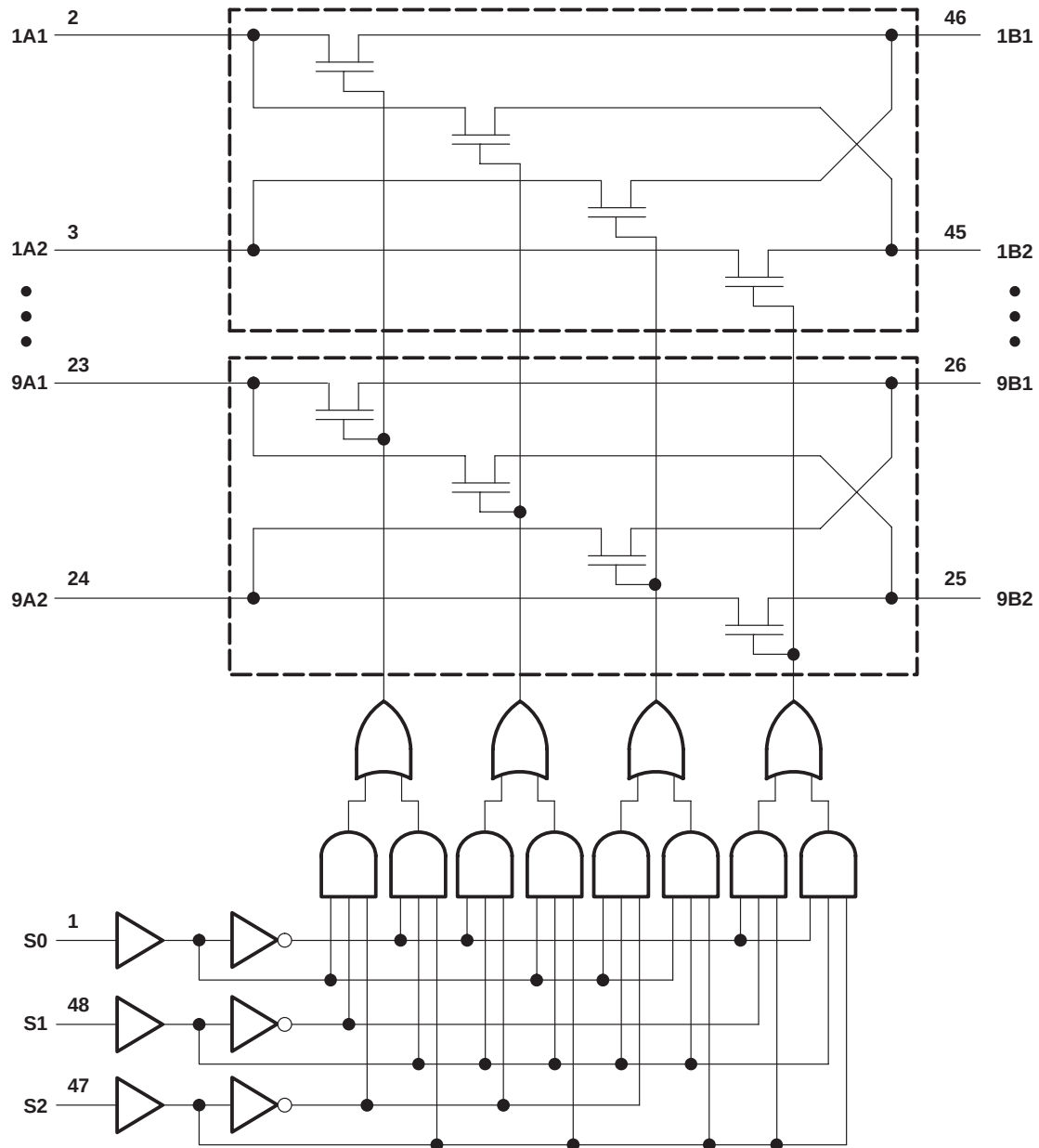
SN54CBT16209, SN74CBT16209A
18-BIT FET BUS-EXCHANGE SWITCHES

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FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port

logic diagram (positive logic)



SN54CBT16209, SN74CBT16209A

18-BIT FET BUS-EXCHANGE SWITCHES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54CBT16209		SN74CBT16209A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4	5.5	4	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2	V
I_I		$V_{CC} = 0$,	$V_I = 5.5$ V			10	μA
		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V or GND			±1	
I_{CC}		$V_{CC} = 5.5$ V,	$I_O = 0$, $V_I = V_{CC}$ or GND			3	μA
ΔI_{CC} [§]	Control inputs	$V_{CC} = 5.5$ V,	One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3$ V or 0				4	pF
$C_{io(OFF)}$		$V_O = 3$ V or 0, S_0, S_1 , and $S_2 = GND$				7.5	pF
r_{on} [¶]		$V_{CC} = 4$ V TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V, $I_I = 15$ mA			14 20	Ω
		$V_{CC} = 4.5$ V	$V_I = 0$, $I_I = 64$ mA			4 8	
			$I_I = 30$ mA			4 8	
			$V_I = 2.4$ V, $I_I = 15$ mA			6 15	

[‡] All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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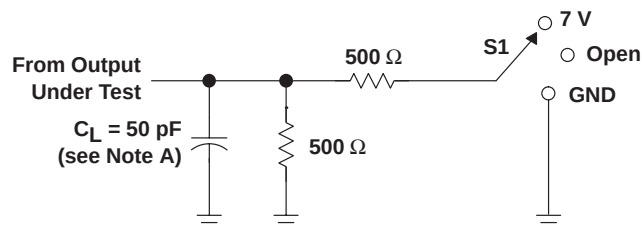
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16209				SN74CBT16209A				UNIT
			V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} [†]	A or B	B or A			0.8*		0.35		0.25		ns
t _{pd}	S	A or B	14		2	13.1	9.9		1.5	9	ns
t _{en}	S	A or B	16		1.7	15.3	10.3		1.5	9.8	ns
t _{dis}	S	A or B	14.5		1	13.2	9.3		1.5	8.8	ns

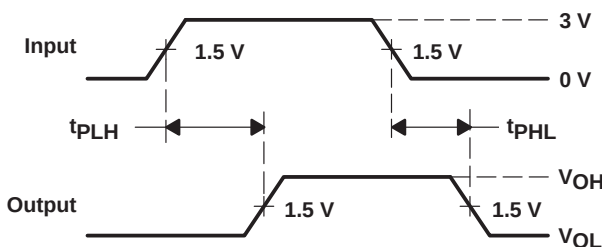
* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

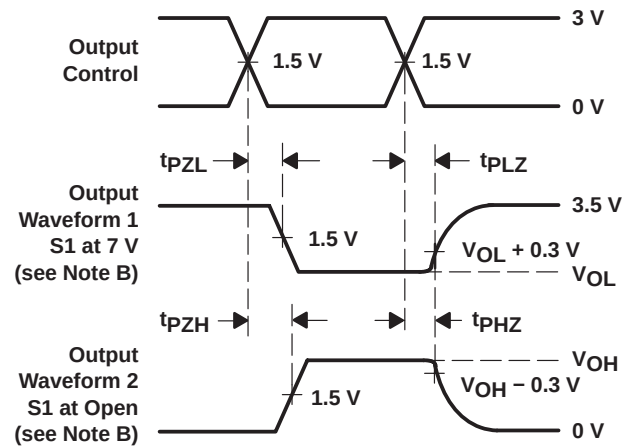


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PHZ}	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50$ Ω , $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT16209ADGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16209A
SN74CBT16209ADGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16209A
SN74CBT16209ADGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY209A
SN74CBT16209ADGVR.A	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY209A
SN74CBT16209ADL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16209A
SN74CBT16209ADL.A	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16209A
SN74CBT16209ADLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16209A
SN74CBT16209ADLR.A	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16209A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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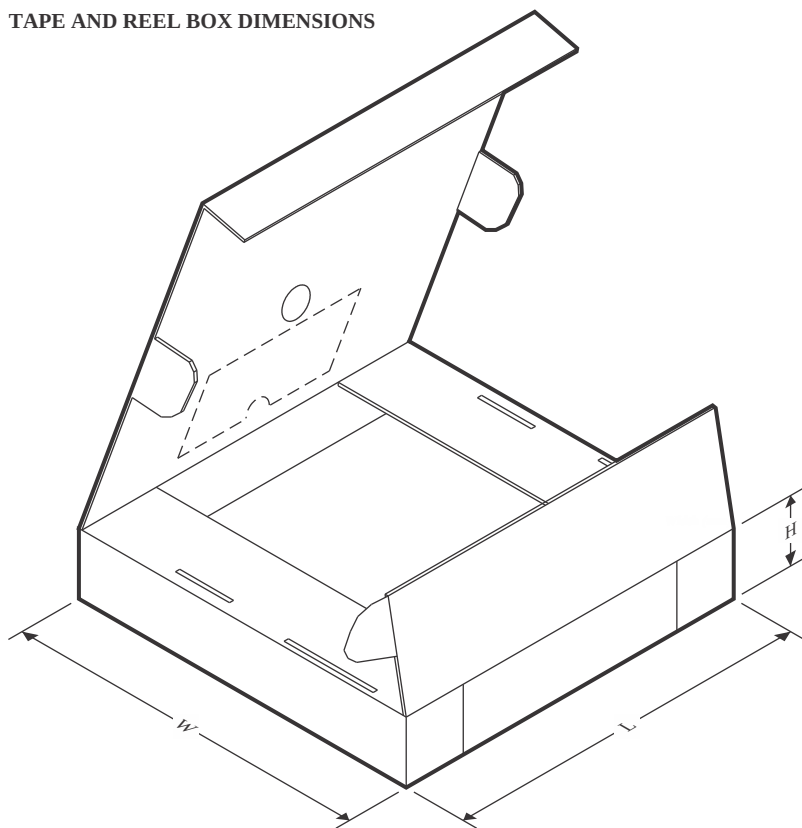
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16209ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74CBT16209ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74CBT16209ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

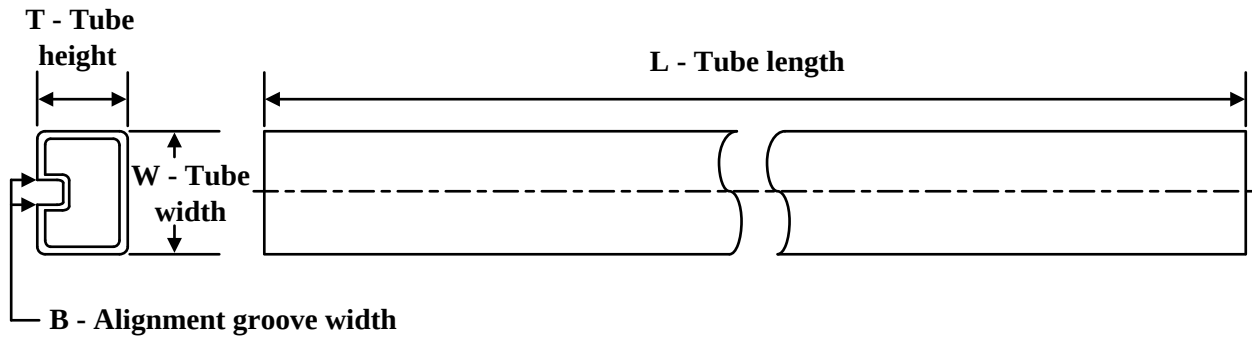
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16209ADGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74CBT16209ADGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74CBT16209ADLR	SSOP	DL	48	1000	356.0	356.0	53.0

TUBE

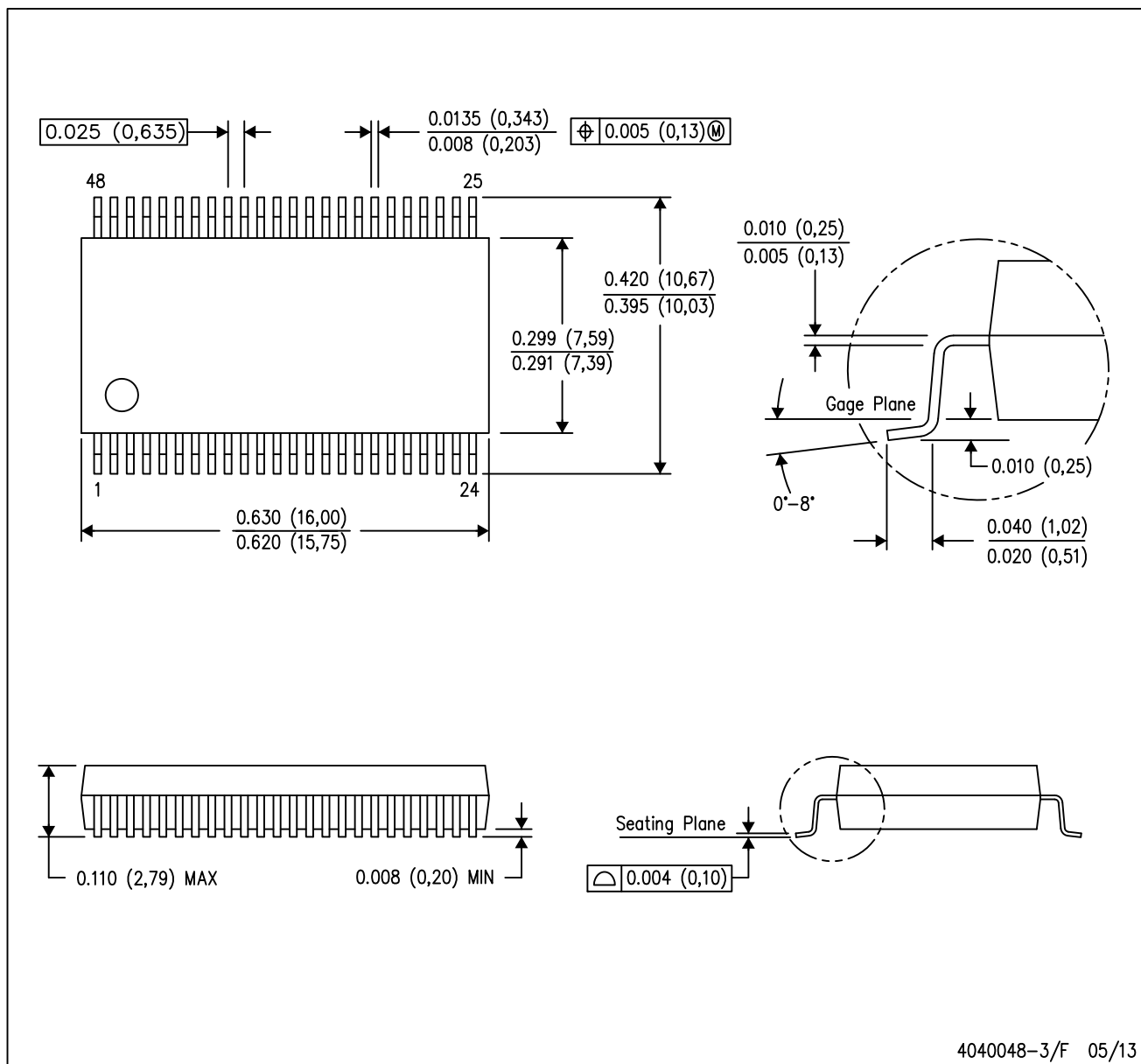


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT16209ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74CBT16209ADL.A	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

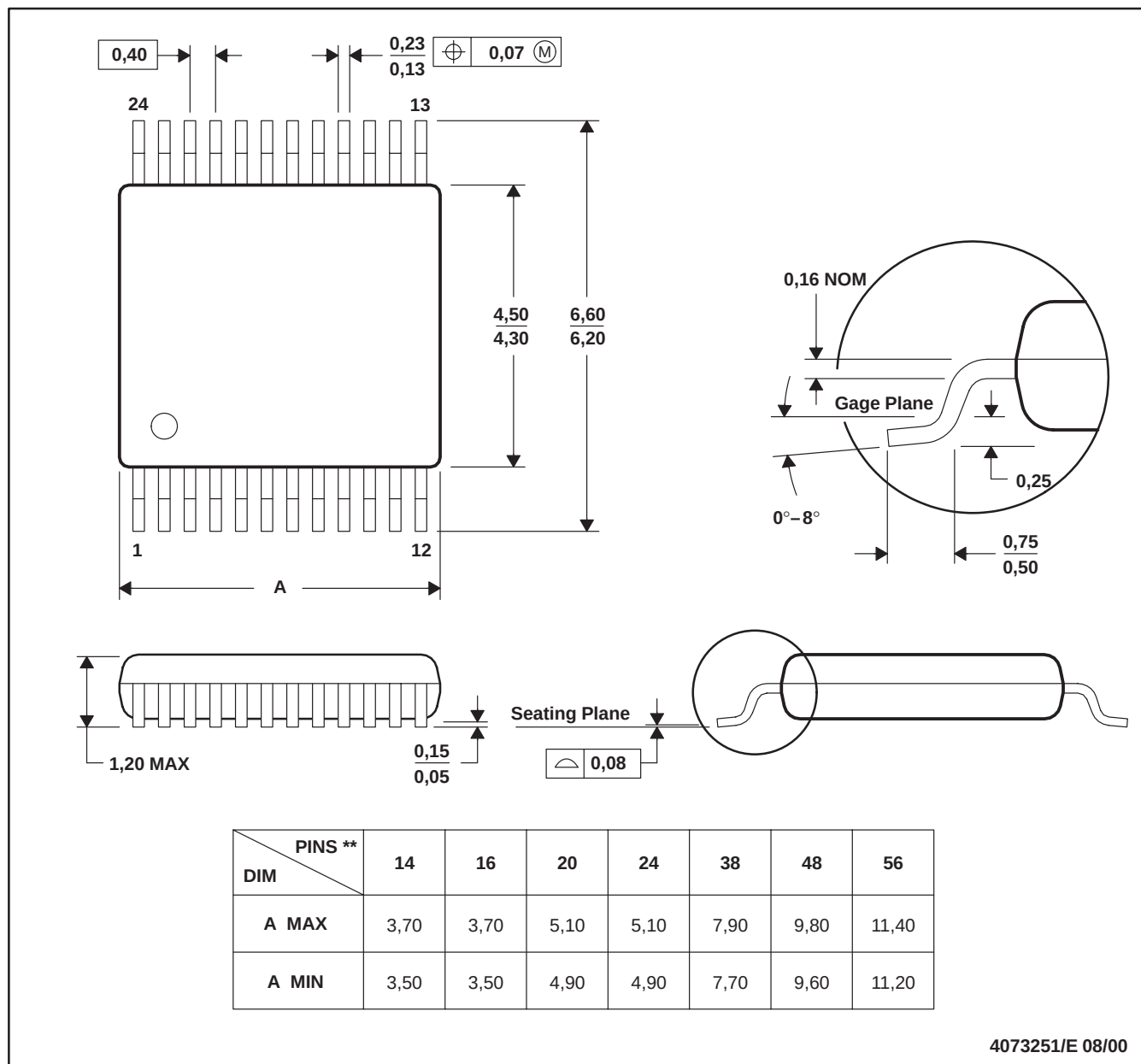


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

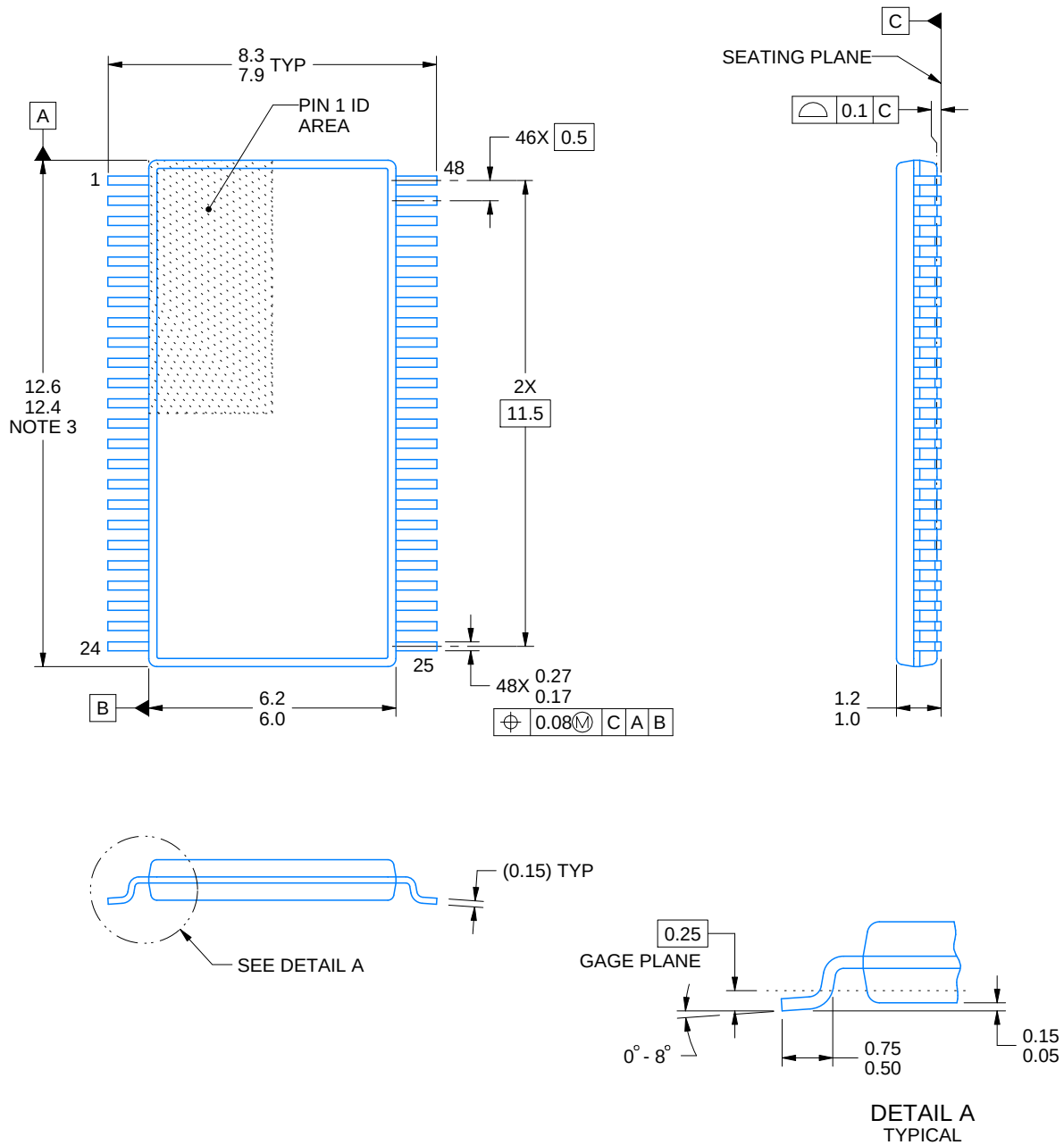
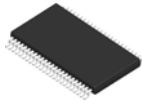
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



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NOTES:

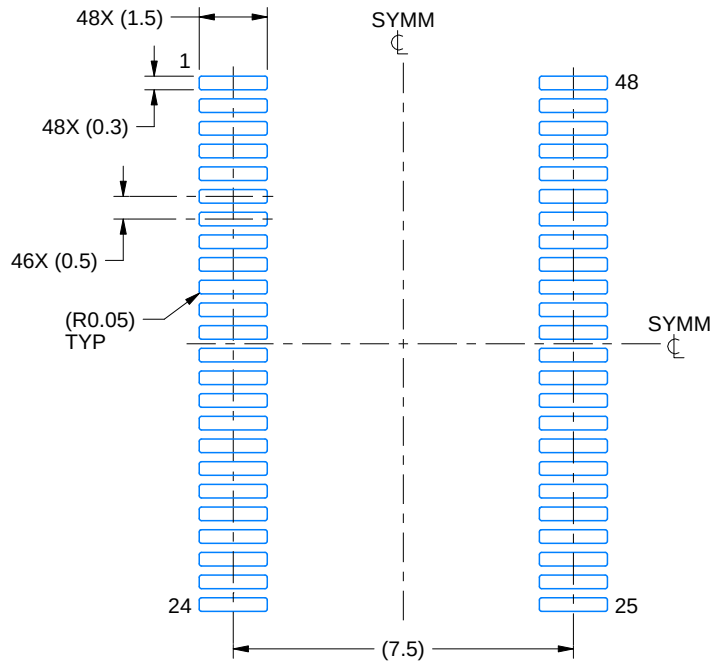
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

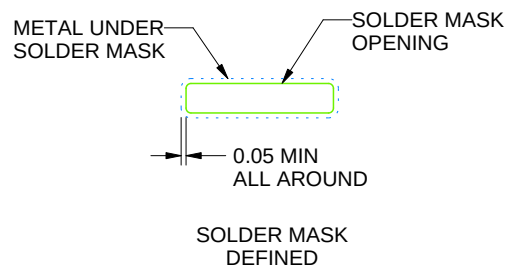
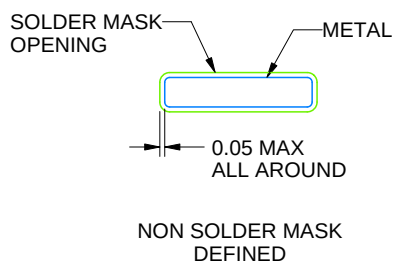
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

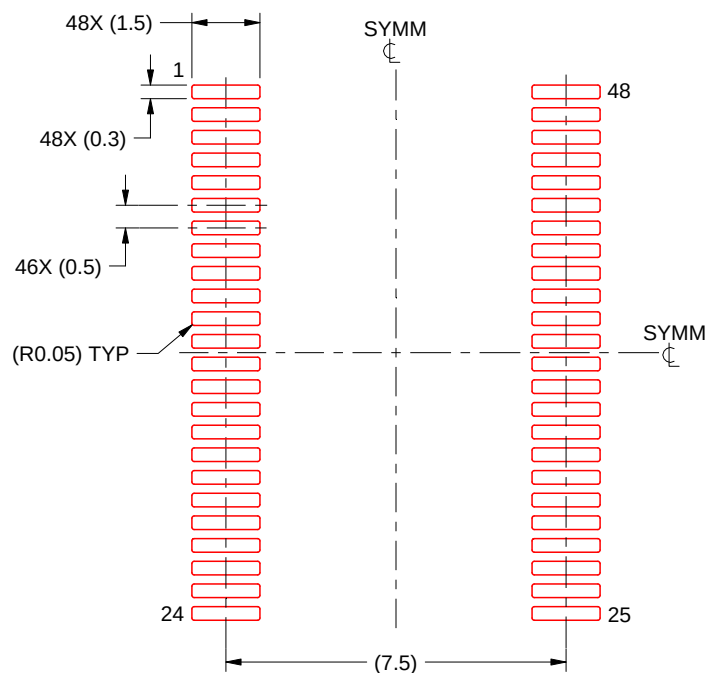
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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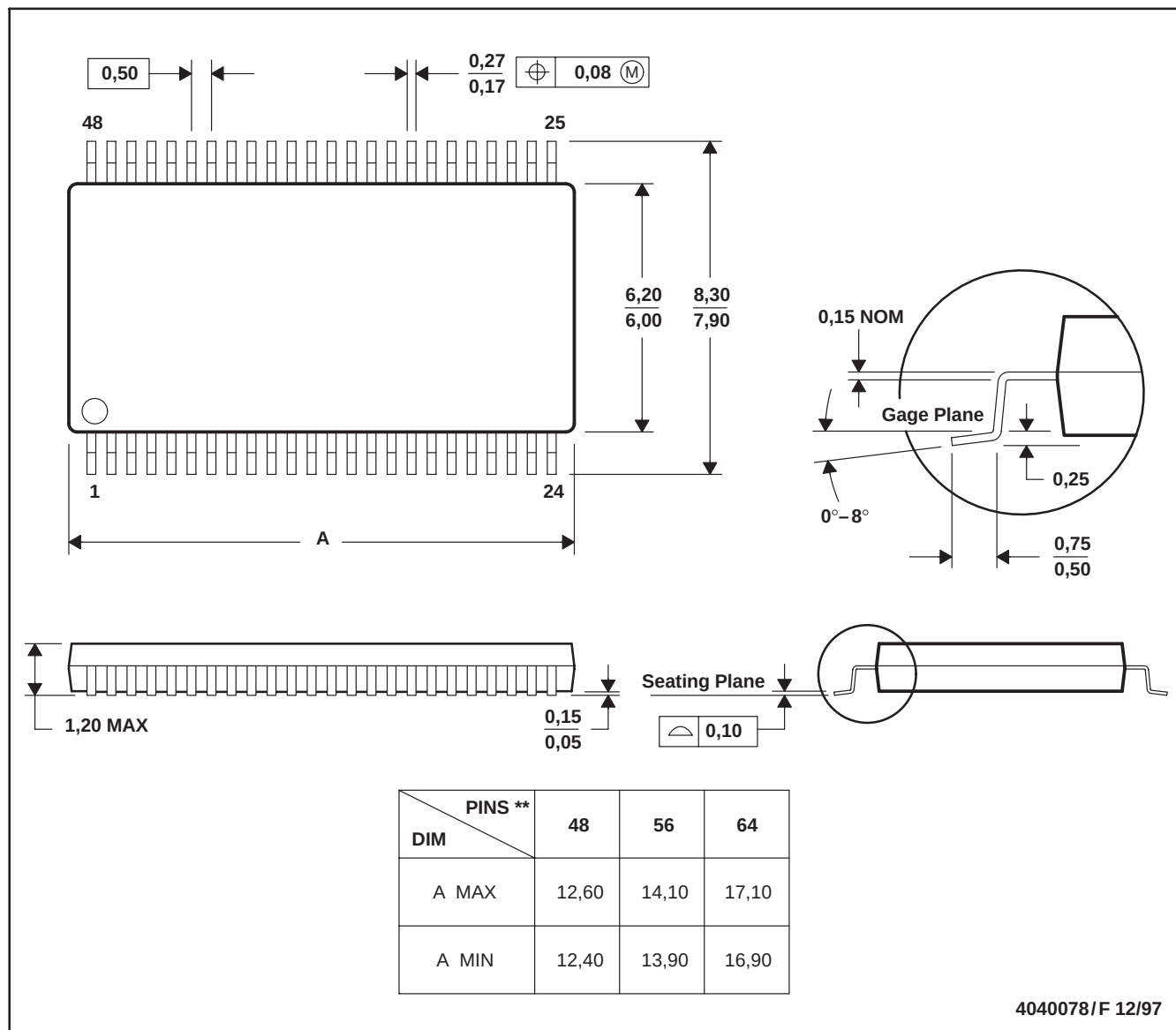
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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