SN74CBTLV3253 低压双路 1:4 FET 多路复用器/多路解复用器

1 特性

- 在功能上与 QS3253 等效
- 两个端口之间具有 5Ω 开关连接
- 支持在数据 I/O 端口进行轨到轨开关
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 数据中心和企业计算
- 宽带固定线路接入
- 楼宇自动化
- 有线网络
- 电机驱动器
- 视频广播：基于 IP 的多格式转码器
- 视频通信系统

3 说明

SN74CBTLV3253 器件是一款双路、1:4 高速 FET 多路复用器和多路解复用器。此开关具有低导通状态电阻，可以最短传播延迟建立连接。

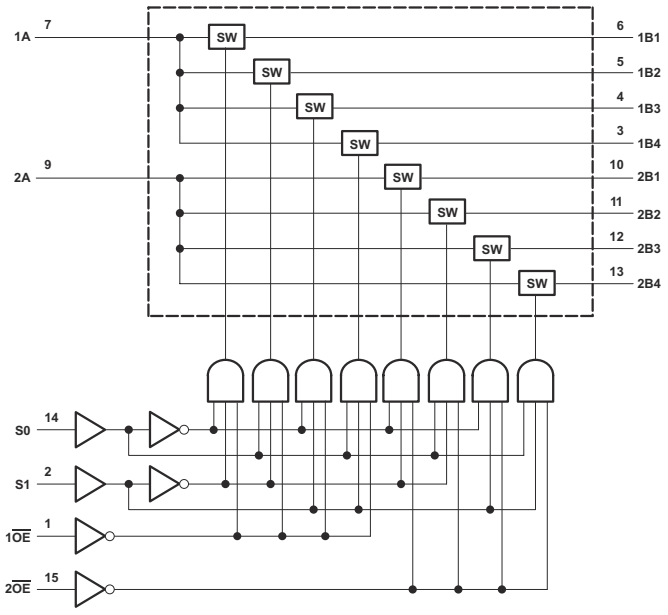
选择 (S0, S1) 输入端控制数据流。当关联的输出使能 ($\overline{OE}$) 输入端为高电平时，FET 多路复用器/多路解复用器将被禁用。

SN74CBTLV3253 器件完全符合使用 I_{off} 的部分断电应用的规范要求。I_{off} 特性确保在关断时，损坏电流不能通过器件回流。该器件可在关断时提供隔离。

封装信息

器件型号	封装 (1)	封装尺寸
SN74CBTLV3253D	SOIC (16)	9.90mm × 3.90mm
SN74CBTLV3253DBQ	SSOP (16)	4.90mm × 3.90mm
SN74CBTLV3253DGV	TVSOP (16)	3.60mm × 4.40mm
SN74CBTLV3253RGY	VQFN (16)	4.00mm × 3.50mm
SN74CBTLV3253PW	TSSOP (16)	5.00mm × 4.40mm
SN74CBTLV3253DYY	SOT (16)	4.20mm × 2.00mm
SN74CBTLV3253BQB	WQFN (16)	3.50mm × 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

内容

4 引脚配置和功能

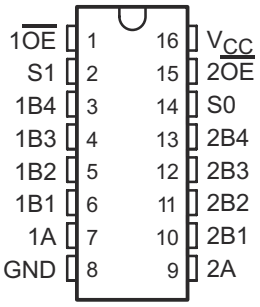


图 4-1. D、DBQ、DGV、PW 或 DYY 封装 16 引脚 SOIC、SSOP、TVSOP、TSSOP 或 SOT 顶视图

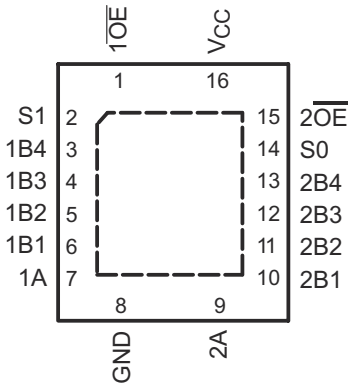


图 4-2. RGY 或 BQB 封装 16 引脚 VQFN 顶视图

表 4-1. 引脚功能

引脚		类型	说明
名称	编号		
1 $\overline{OE}$	1	I	输出使能 1，低电平有效
S1	2	I	选择“引脚 1”
1B4	3	I/O	通道 1 I/O 4
1B3	4	I/O	通道 1 I/O 3
1B2	5	I/O	通道 1 I/O 2
1B1	6	I/O	通道 1 I/O 1
1A	7	I/O	通道 1 公共
GND	8	—	接地
2A	9	I/O	通道 2 公共
2B1	10	I/O	通道 2 I/O 1
2B2	11	I/O	通道 2 I/O 2
2B3	12	I/O	通道 2 I/O 3
2B4	13	I/O	通道 2 I/O 4
S0	14	I	选择“引脚 0”
2 $\overline{OE}$	15	I	输出使能 2，低电平有效
V_{CC}	16	—	电源

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压		-0.5	4.6	V
V_{IN}	控制输入电压(2)		-0.5	4.6	V
$V_{I/O}$	开关 I/O 电压(2)		-0.5	4.6	V
I_{IK}	控制输入钳位电流	V_{IN} < 0		-50	mA
$I_{I/OK}$	I/O 端口钳位电流	$V_{I/O}$ < 0		-50	mA
	通过 V_{CC} 或 GND 的持续电流			±128	mA
T_J	结温			150	°C
T_{stg}	贮存温度		-65	150	°C

(1) 超出“绝对最大额定值”运行可能会对器件造成永久损坏。“绝对最大额定值”并不表示器件在这些条件下或在“建议运行条件”以外的任何其他条件下能够正常运行。如果超出“建议运行条件”但在“绝对最大额定值”范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。
(2) 如果遵守输入和输出钳位电流额定值，则可能会超过输入和输出负电压额定值。

5.2 ESD 等级

			值	单位
V_{ESD}	静电放电	人体放电模式 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准，所有引脚(1)	+2000	V
		充电器件模式 (CDM)，符合 JEDEC 规范 JESD22-C101，所有引脚(2)	+1000	V

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压		2.3	3.6	V
V_{IH}	高电平控制输入电压	V_{CC} = 2.3V 至 2.7V	1.7		V
		V_{CC} = 2.7V 至 3.6V	2		
V_{IL}	低电平控制输入电压	V_{CC} = 2.3V 至 2.7V		0.7	V
		V_{CC} = 2.7V 至 3.6V		0.8	
T_A	自然通风条件下的工作温度	PKG = RGY、DBQ、D、PW、DGV	-40	85	°C
T_A	自然通风条件下的工作温度	PKG = BQB、DYY	-40	125	°C

(1) 器件所有的未使用控制输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅*慢速或浮点 CMOS 输入影响*应用说明。

5.4 热性能信息

热指标(1)		SN74CBTLV3253							单位
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	DYY (SOT)	BQB (WQFN)	
		16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	
$R_{\theta JA}$	结至环境热阻	102.5	116.6	123.1	129.1	78.4	129.9	88.1	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	65.4	70	48.7	67	52.5	78.4	58.3	°C/W
$R_{\theta JB}$	结至电路板热阻	65.2	75	54.9	87.1	21.74	73.3	17.0	°C/W
ψ_{JT}	结至顶部特征参数	25.5	17	5.2	14.5	52.5	17.2	58.3	°C/W
ψ_{JB}	结至电路板特征参数	64.6	74.1	54.3	86.3	76.6	72.4	85.1	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	37.3	不适用	37.5	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用手册。

5.5 电气特性 - 仅限 D、DBQ、DGV、PW 和 RGY

在自然通风条件下的建议运行温度范围（-40°C 至 85°C）内测得（除非另有说明）

参数		测试条件			最小值	典型值(1)	最大值	单位
V_{IK}		V_{CC} = 3V，	I_I = -18mA				-1.2	V
I_I		V_{CC} = 3.6V，	V_I = V_{CC} 或 GND				±1	μA
I_{off}		V_{CC} = 0，	V_I 或 V_O = 0V 至 3.6V				15	μA
I_{CC}		V_{CC} = 3.6V，	I_O = 0，	V_I = V_{CC} 或 GND			10	μA
ΔI_{CC} (2)	控制输入	V_{CC} = 3.6V，	一个输入为 3V，	其他输入电压为 V_{CC} 或 GND			300	μA
C_i	控制输入	V_I = 3V 或 0V				3		pF
$C_{io(OFF)}$	A 端口	V_O = 3V 或 0V，	$\overline{OE}$ = V_{CC}			20.5		pF
	B 端口					5.5		
r_{on} (3)		V_{CC} = 2.3V，V_{CC} = 2.5V 时的典型值	V_I = 0	I_I = 64mA		5	8	Ω
				I_I = 24mA		5	8	
			V_I = 1.7V，	I_I = 15mA		27	40	
		V_{CC} = 3V	V_I = 0	I_I = 64mA		5	7	
				I_I = 24mA		5	7	
			V_I = 2.4V，	I_I = 15mA		10	15	

(1) 所有典型值均在 V_{CC} = 3.3V（除非另外注明）、T_A = 25°C 时测得。
(2) 这是每个输入在指定电压电平（而不是 V_{CC} 或 GND 下）的电源电流增加情况。
(3) 在流经开关的指示电流下，由 A 和 B 端子之间的压降测量。导通状态电阻由两个（A 或 B）端子的较低电压决定。

5.6 电气特性 - 仅限 DYY 和 BQB 封装

在自然通风条件下的建议运行温度范围（-40°C 至 125°C）内测得（除非另有说明）

参数		测试条件			最小值	典型值(1)	最大值	单位
V_{IK}		V_{CC} = 3V，	I_I = -18mA				-1.2	V
I_I		V_{CC} = 3.6V，	V_I = V_{CC} 或 GND				±1	μA
I_{off}		V_{CC} = 0，	V_I 或 V_O = 0V 至 3.6V				20	μA
I_{CC}		V_{CC} = 3.6V，	I_O = 0，	V_I = V_{CC} 或 GND			10	μA
ΔI_{CC} (2)	控制输入	V_{CC} = 3.6V，	一个输入为 3V，	其他输入电压为 V_{CC} 或 GND			300	μA
C_i	控制输入	V_I = 3V 或 0V				3		pF
$C_{io(OFF)}$	A 端口	V_O = 3V 或 0V，	$\overline{OE}$ = V_{CC}			20.5		pF
	B 端口					5.5		
r_{on} (3)		V_{CC} = 2.3V，V_{CC} = 2.5V 时的典型值	V_I = 0	I_I = 64mA		5	10	Ω
				I_I = 24mA		5	10	
			V_I = 1.7V，	I_I = 15mA		27	40	
		V_{CC} = 3V	V_I = 0	I_I = 64mA		5	9	
				I_I = 24mA		5	9	
			V_I = 2.4V，	I_I = 15mA		10	20	

(1) 所有典型值均在 V_{CC} = 3.3V（除非另外注明）、T_A = 25°C 时测得。
(2) 这是每个输入在指定电压电平（而不是 V_{CC} 或 GND 下）的电源电流增加情况。
(3) 在流经开关的指示电流下，由 A 和 B 端子之间的压降测量。导通状态电阻由两个（A 或 B）端子的较低电压决定。

5.7 开关特性 - 仅限 D、DBQ、DGV、PW 和 RGY

在自然通风条件下的建议运行温度范围（-40°C 至 85°C）内测得（除非另有说明）（请参阅图 6-1）

参数	从（输入）	至（输出）	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		单位
			最小值	最大值	最小值	最大值	
t_{pd}	A 或 B(1)	B 或 A		0.15		0.25	ns
	S	A 或 B	1	6.8	1	5.5	
t_{en}	S	A 或 B	1	4.3	1	4	ns
t_{dis}	S	A 或 B	1	5.1	1	5.5	ns
t_{en}	$\overline{OE}$	A 或 B	1	5	1	4.8	ns
t_{dis}	$\overline{OE}$	A 或 B	1	5.5	1	5.4	ns

(1) 当由一个理想电压源（零输出阻抗）驱动时，传播延迟是使用此开关通态电阻典型值和额定负载电容计算得出的 RC 时间常数。

5.8 开关特性 - 仅限 DYY 和 BQB 封装

在自然通风条件下的建议运行温度范围（-40°C 至 125°C）内测得（除非另有说明）（请参阅图 6-1）

参数	从（输入）	至（输出）	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		单位
			最小值	最大值	最小值	最大值	
t_{pd}	A 或 B[1]	B 或 A		3.1		1.7	ns
	S	A 或 B	1	6.8	1	5.5	
t_{en}	S	A 或 B	1	6.8	1	6.8	ns
t_{dis}	S	A 或 B	1	7	1	7	ns
t_{en}	$\overline{OE}$	A 或 B	1	6.5	1	6	ns
t_{dis}	$\overline{OE}$	A 或 B	1	6.5	1	6	ns

5.9 典型特性

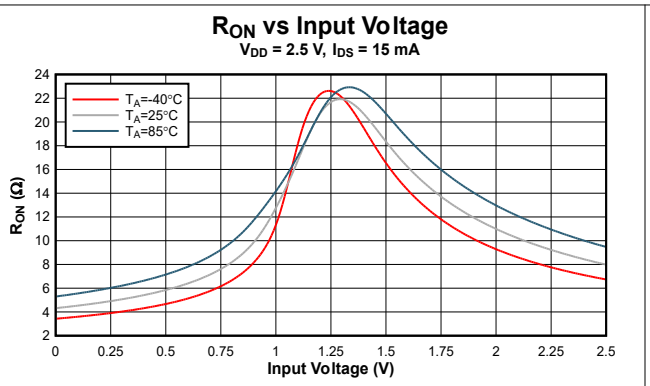


图 5-1. V_{DD} = 2.5V，I_{DS} = 15mA

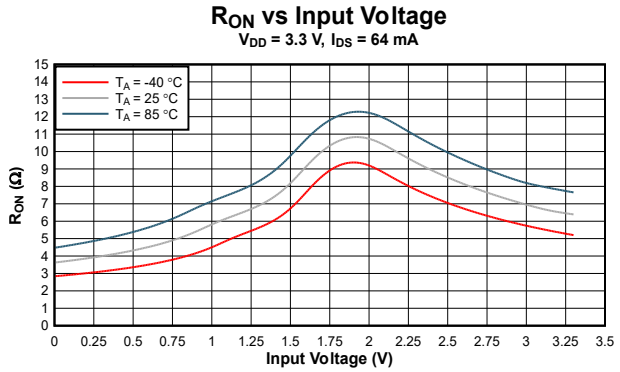


图 5-2. V_{DD} = 3.3V，I_{DS} = 64mA

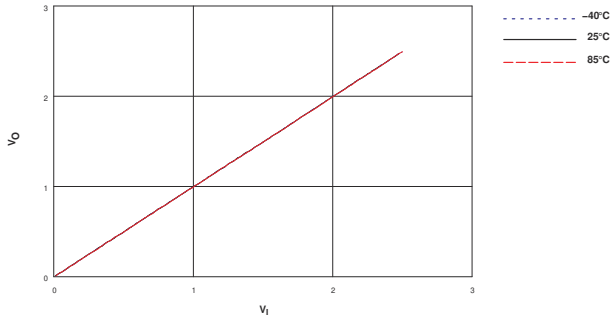
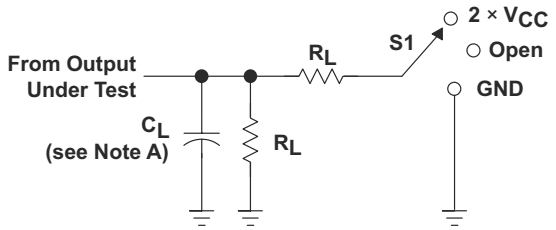


图 5-3. V_O 与 V_I 间的关系，V_{CC} = 2.5V

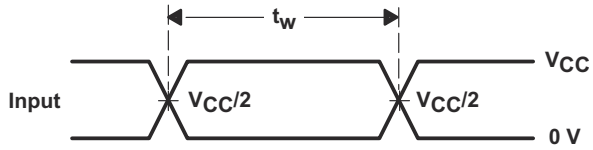
6 参数测量信息



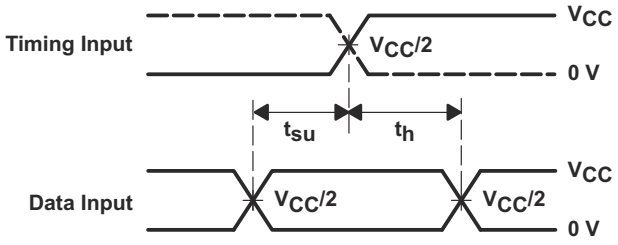
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

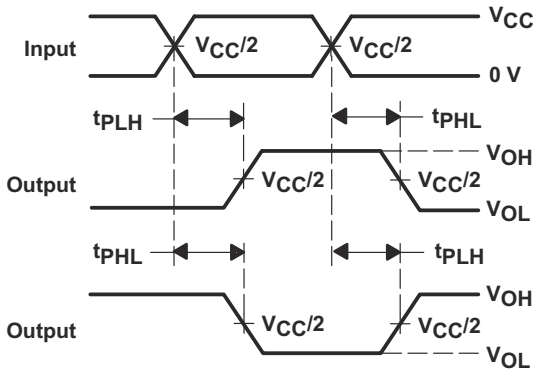
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V



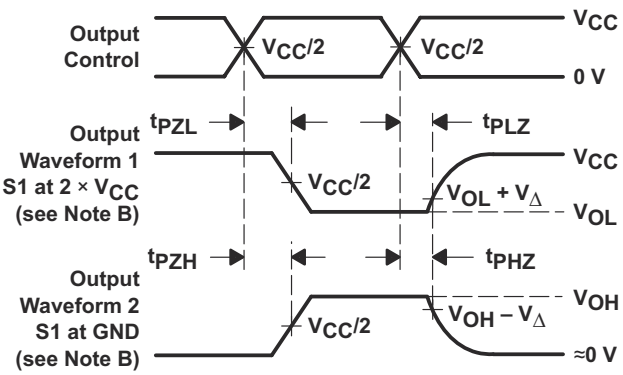
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

图 6-1. 测试电路和电压波形

7 详细说明

7.1 概述

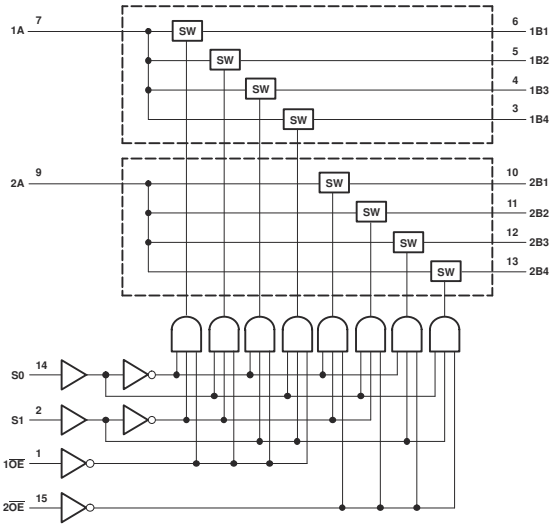
SN74CBTLV3253 器件是一款双路、1:4 高速 FET 多路复用器/多路解复用器。此开关具有低导通状态电阻，可以最短传播延迟建立连接。

选择 (S0, S1) 输入端控制数据流。当关联的输出使能 ($\overline{OE}$) 输入端为高电平时，FET 多路复用器和多路解复用器将被禁用。

SN74CBTLV3253 器件完全符合使用 I_{off} 的部分断电应用的规范要求。I_{off} 特性确保在关断时防止损坏电流通过器件回流。该器件可在关断时提供隔离。

为了确保加电或断电期间的高阻抗状态，$\overline{OE}$ 应通过一个上拉电阻器被连接至 V_{CC}；该电阻器的最小值由驱动器的电流吸收能力来决定。

7.2 功能方框图



7.3 特性说明

SN74CBTLV3253 器件在功能上与 QS3253 等效，并在两个端口之间具有 5Ω 交换机连接。该器件还在数据 I/O 端口以及 I_{off} 上提供轨到轨开关，支持局部断电模式运行。

7.4 器件功能模式

表 7-1 列出了 SN74CBTLV3253 器件的功能模式。

表 7-1. 功能表
(每个多路复用器/多路信号分离器)

输入			功能
$\overline{OE}$	S1	S0	
L	L	L	A 端口 = B1 端口
L	L	H	A 端口 = B2 端口
L	H	L	A 端口 = B3 端口
L	H	H	A 端口 = B4 端口
H	X	X	断开

8 应用和实施

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户应负责确定各元件是否适用于其应用。客户应验证并测试其设计是否能够实现，以确保系统功能。

8.1 应用信息

SN74CBTLV3253 可用于在 4:1 配置中同时对多达 2 个通道进行多路复用和多路信号分离。此处所示的应用是在两个器件之间进行多路复用的 2 位总线。$\overline{OE}$ 和 S 引脚用于从总线控制器控制芯片。这是非常通用的示例，适用于许多情况。

8.2 典型应用

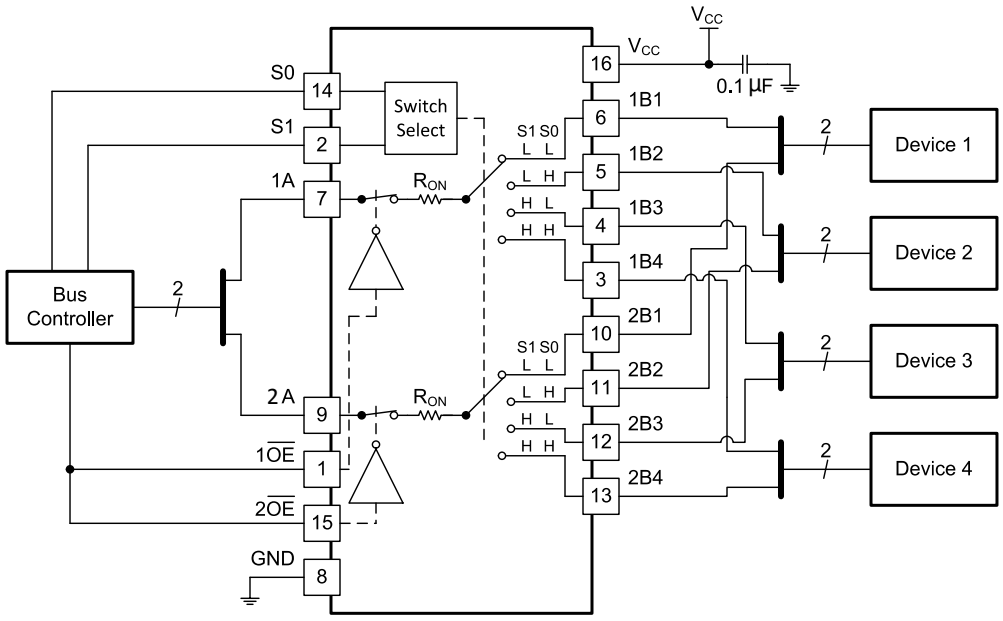


图 8-1. SN74CBTLV3253 典型应用

8.2.1 设计要求

0.1µF 电容器应尽量靠近器件放置。

8.2.2 详细设计过程

1. 建议的输入条件：
   - 有关指定的高电平和低电平，请参阅 节 5.3 中的 V_{IH} 和 V_{IL}。
   - 输入和输出具有过压容限，因此在任何有效 V_{CC} 下高达 4.6V。
2. 建议的输出条件：
   - 每个通道的负载电流不得超过 ±128mA。
3. 频率选择标准：
   - 增加布线电阻/电容可以降低最大频率能力；按照 节 10 中的说明使用布局实践。

8.2.3 应用曲线

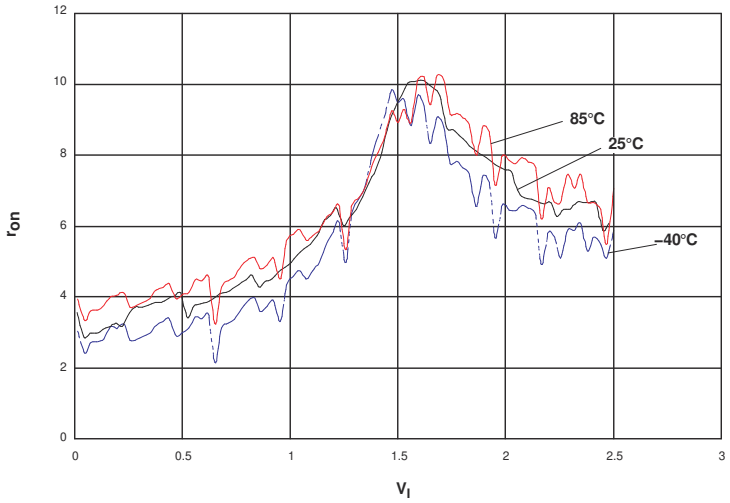


图 8-2. r_{on} 与 V_I 间的关系， V_{CC} = 2.5V

9 电源相关建议

电源可以是 节 5.3 表中列出的最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 µ F 旁路电容器。如果多个引脚被标记为 V_{CC}，鉴于 V_{CC} 引脚在电路内部彼此相连，建议为每个 V_{CC} 引脚配备一个 0.01 µ F 或 0.022 µ F 电容器。若器件具备 V_{CC} 和 V_{DD} 等在不同电压水平运作的双电源引脚，为保证稳定，建议为每个电源引脚配备一个 0.1µF 旁路电容器。要抑制不同的噪声频率，请并联多个旁路电容器。值为 0.1 µ F 和 1 µ F 的电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

10 布局

10.1 布局指南

反射和匹配问题与环路天线理论密切相关，但两者之间存在显著差异，故而需要独立于该理论框架外进行探讨。当 PCB 布线以 90° 角拐角时，会发生反射。反射的主要原因是布线宽度发生了变化。在拐角的顶点，布线宽度增加到原来宽度的 1.414 倍。这种增加会影响传输线特性，尤其是导致反射的布线的分布式电容和自感特性。并非所有 PCB 布线都是直线，因此某些布线必须拐角。图 10-1 展示了渐入佳境的圆角技术。只有最后一个示例（理想）保持恒定的布线宽度并能够更大限度地减少反射。

10.2 布局示例

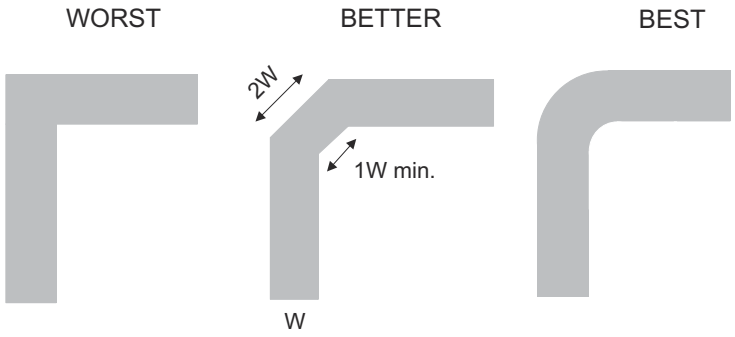


图 10-1. 布线示例

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

- 德州仪器 (TI)，CMOS 输入缓慢变化或悬空的影响

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 商标

所有商标均为其各自所有者的财产。

11.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision J (January 2018) to Revision K (July 2026)	Page
• 添加了具有 125°C 适应能力的新封装	4
• 更新了“热性能额定值”	5
• 为新封装添加了“电气规格”一节	6
• 为新封装添加了开关规格部分	7
• 添加了典型特曲线	7

Changes from Revision I (February 2014) to Revision J (January 2018)	Page
• 更改了 *热性能信息* 表	5

Changes from Revision H (February 2014) to Revision I (September 2015)	Page
• 添加了 *应用* 部分、*器件信息* 表、*引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 表、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分，以及 *机械、封装和可订购信息* 部分	1

Changes from Revision G (February 2014) to Revision H (February 2014)	Page
• 更新了数据表 – 无具体更改	1

Changes from Revision F (July 2012) to Revision G (February 2014)	Page
• 删除了 *订购信息* 表	1

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CBTLV3253DGVRG4	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
74CBTLV3253DGVRG4.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
74CBTLV3253RGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
74CBTLV3253RGYRG4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
74CBTLV3253RGYRG4.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253DBQR.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253DBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253
SN74CBTLV3253DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253
SN74CBTLV3253DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253
SN74CBTLV3253DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	CL253
SN74CBTLV3253PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253RGYR.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

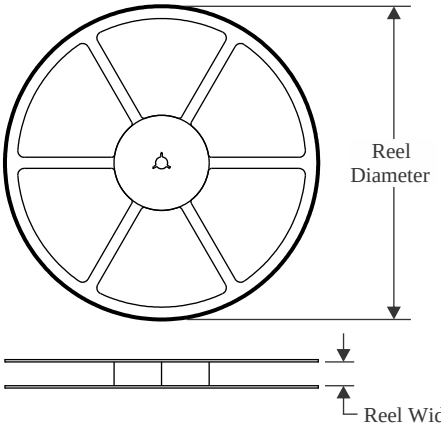
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

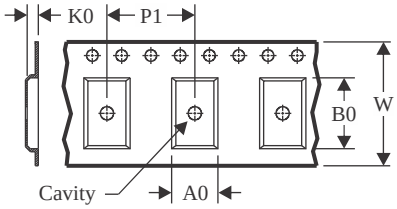
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

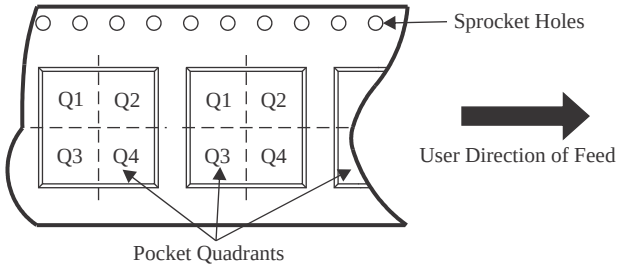


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

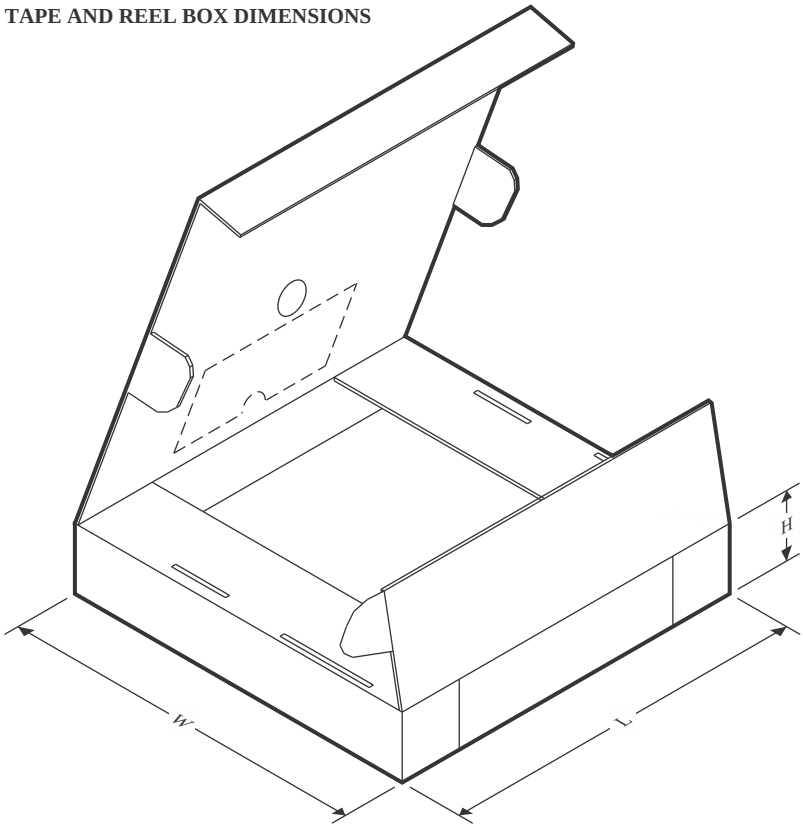
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV3253DGVRG4	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
74CBTLV3253RGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74CBTLV3253BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74CBTLV3253DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3253DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBTLV3253DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.5	3.56	1.35	8.0	12.0	Q3
SN74CBTLV3253PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3253RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

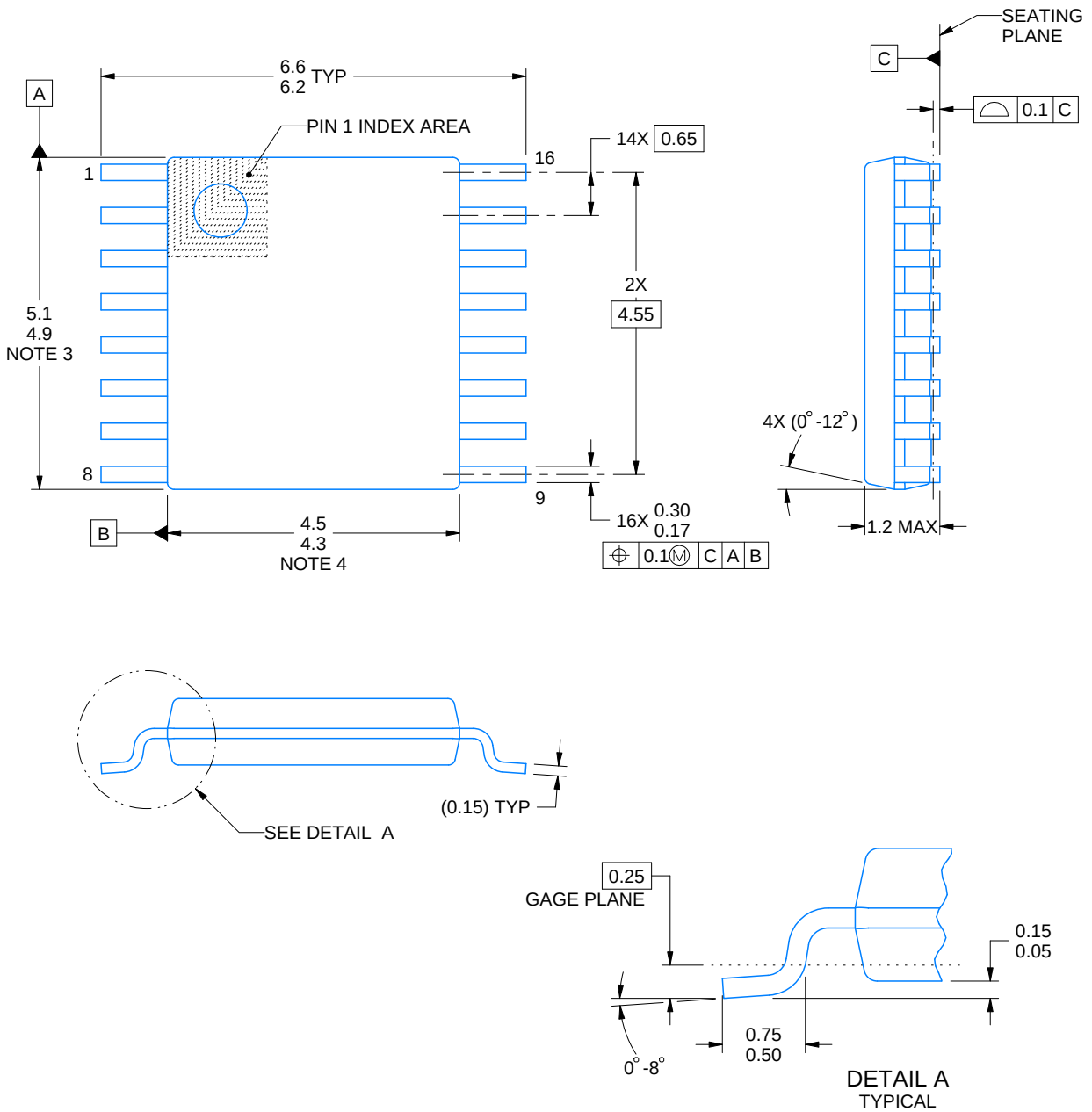
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV3253DGVRG4	TVSOP	DGV	16	2000	353.0	353.0	32.0
74CBTLV3253RGYRG4	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74CBTLV3253BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74CBTLV3253DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CBTLV3253DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74CBTLV3253DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74CBTLV3253DYYR	SOT-23-THIN	DYY	16	3000	360.0	360.0	36.0
SN74CBTLV3253PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CBTLV3253RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

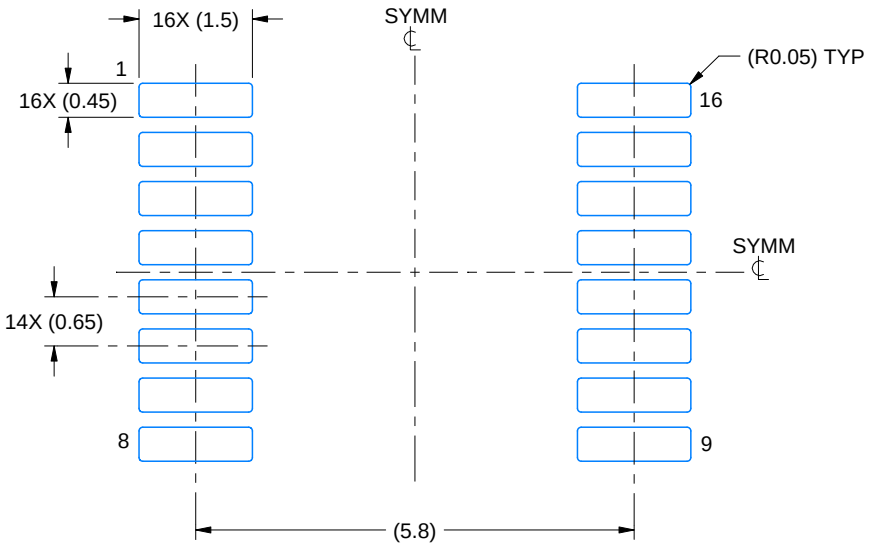
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



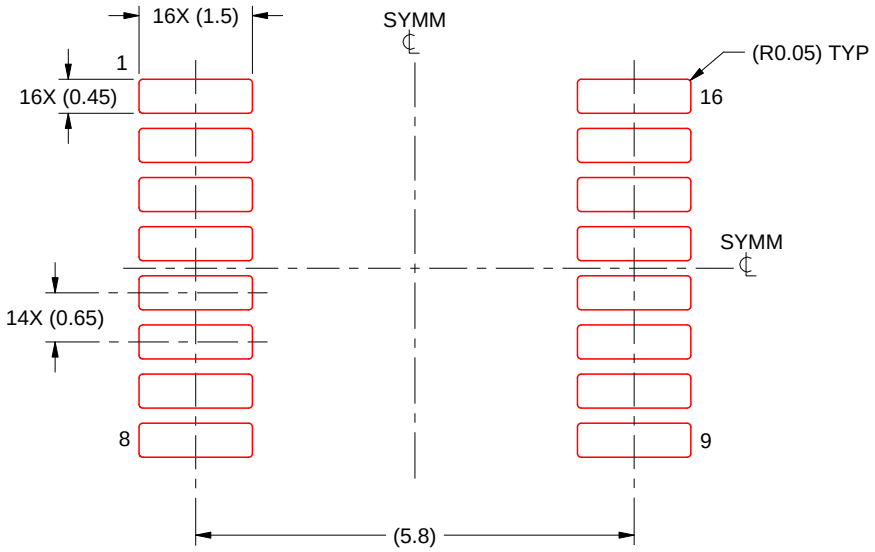
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

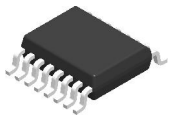


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

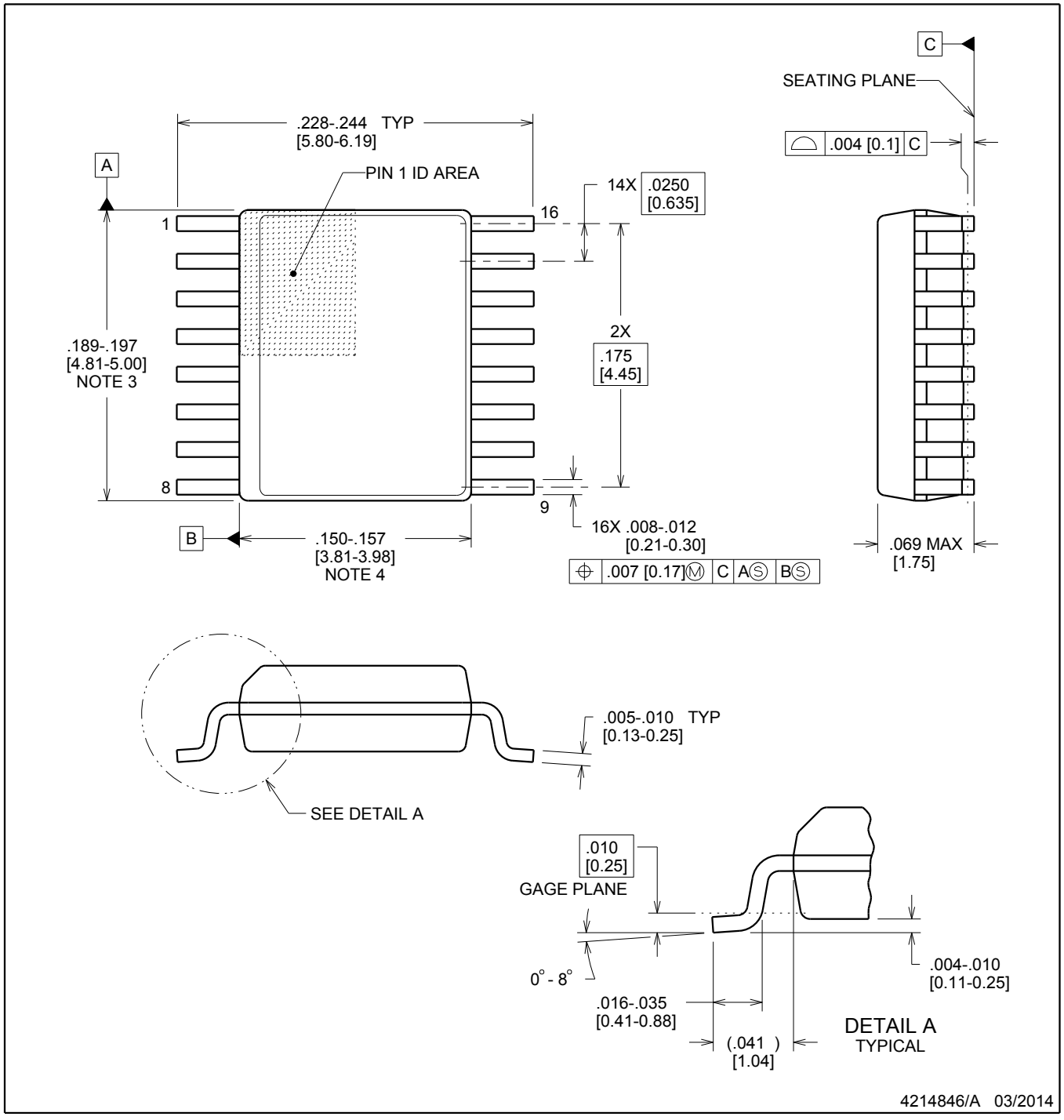


PACKAGE OUTLINE

DBQ0016A

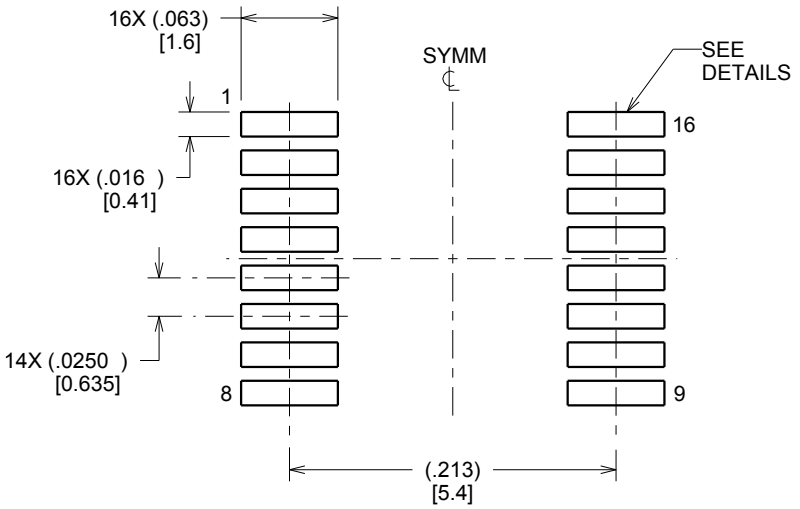
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

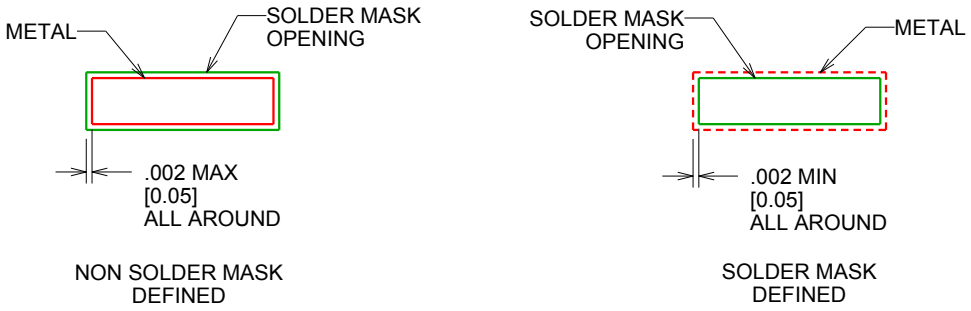


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

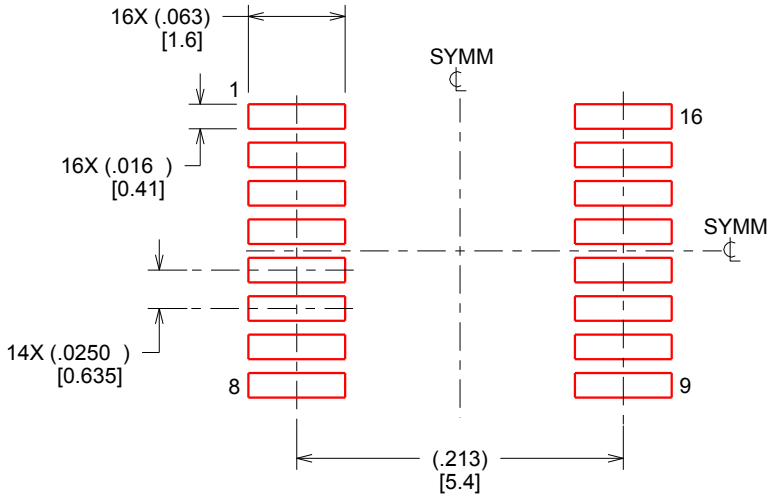
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

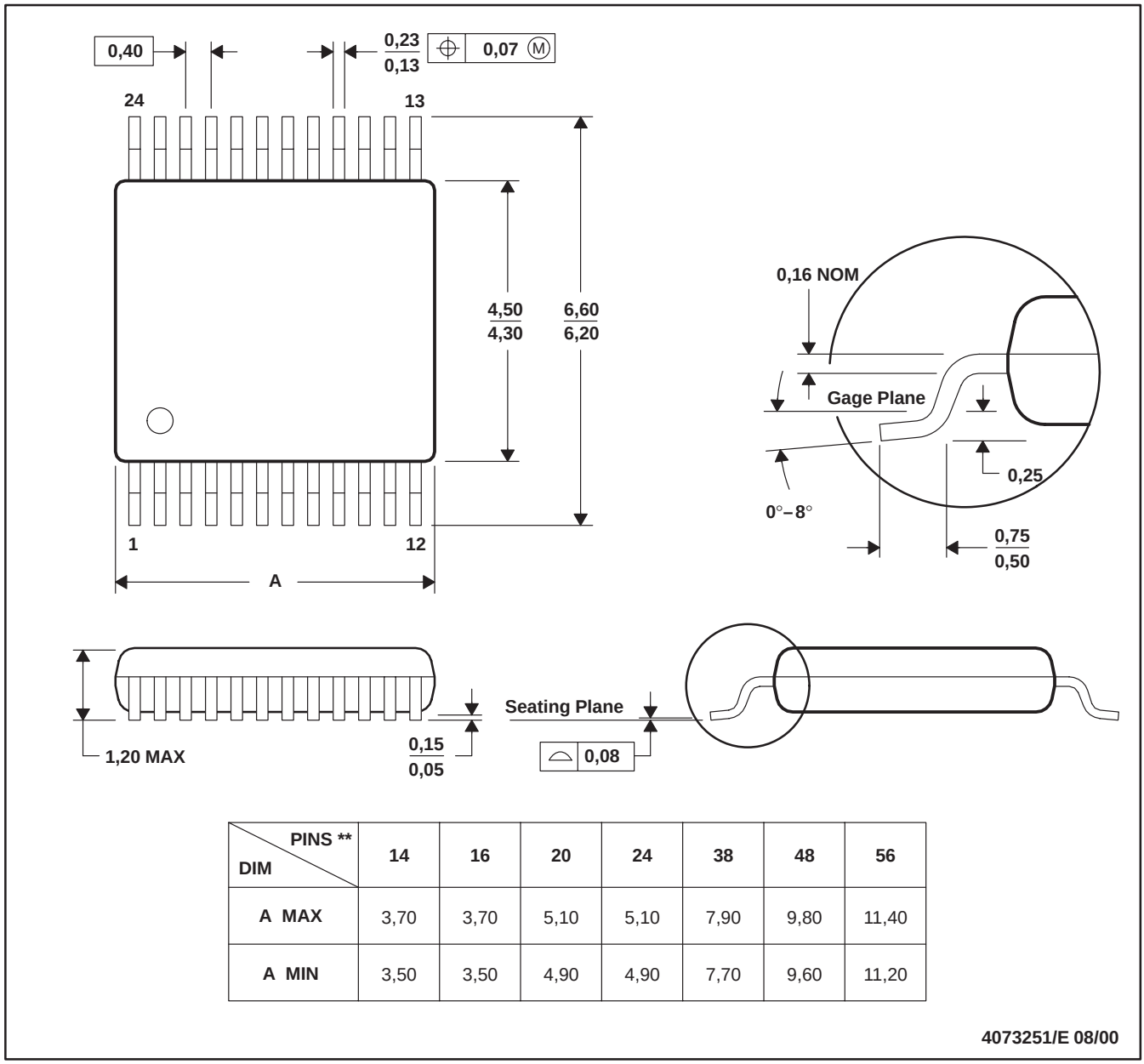
4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

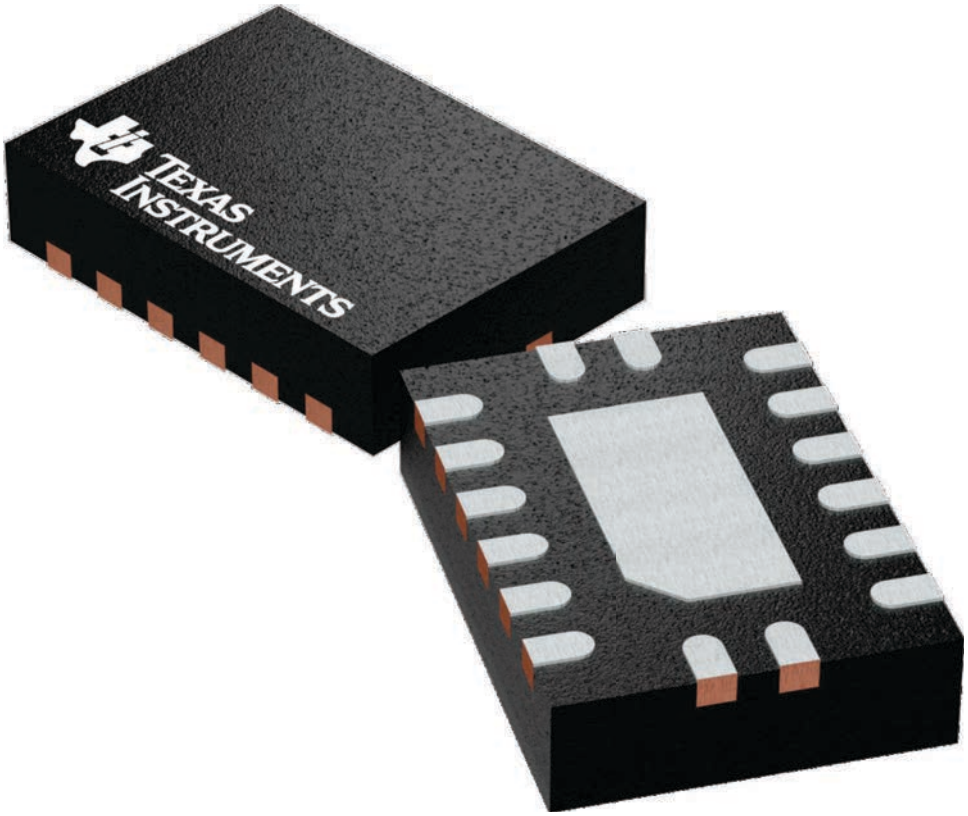
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



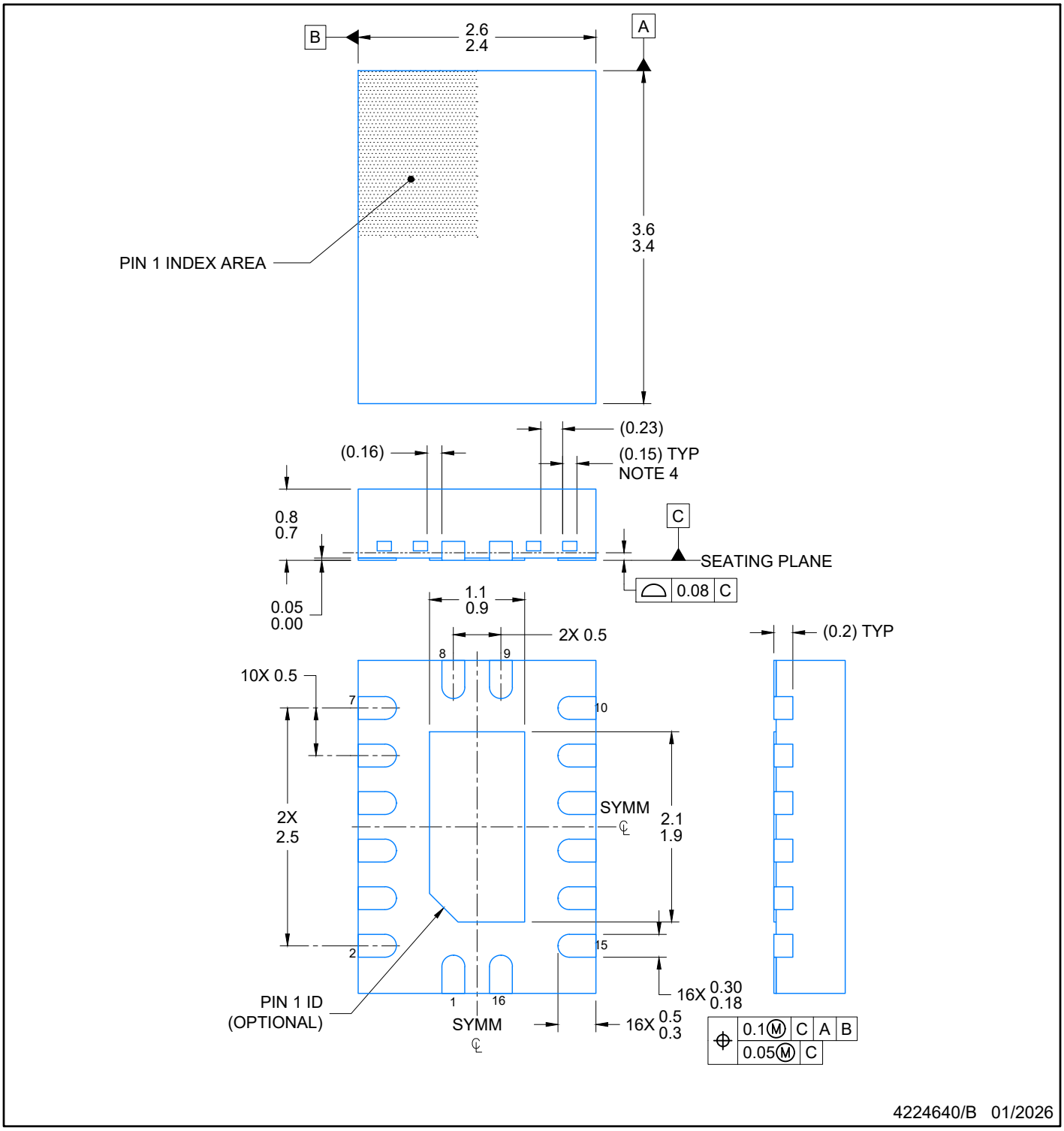
4226161/A

PACKAGE OUTLINE

BQB0016A

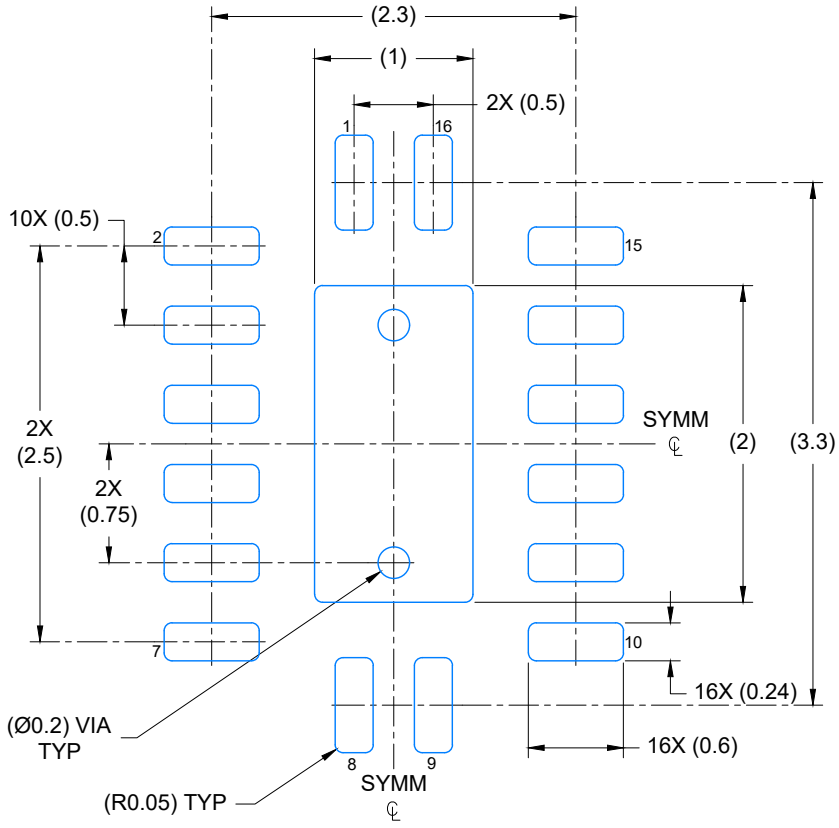
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

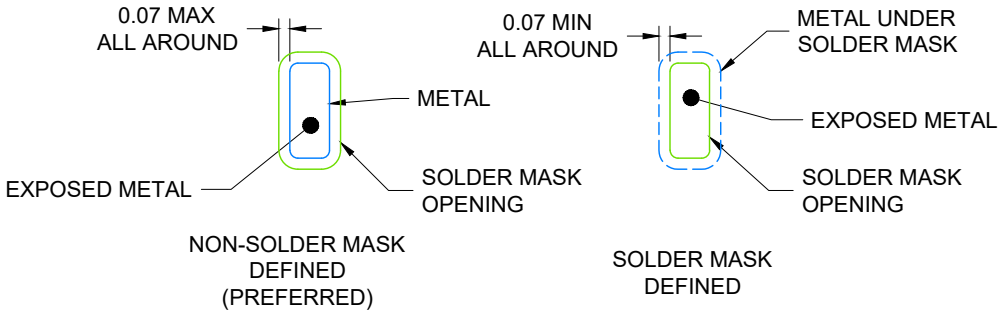


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

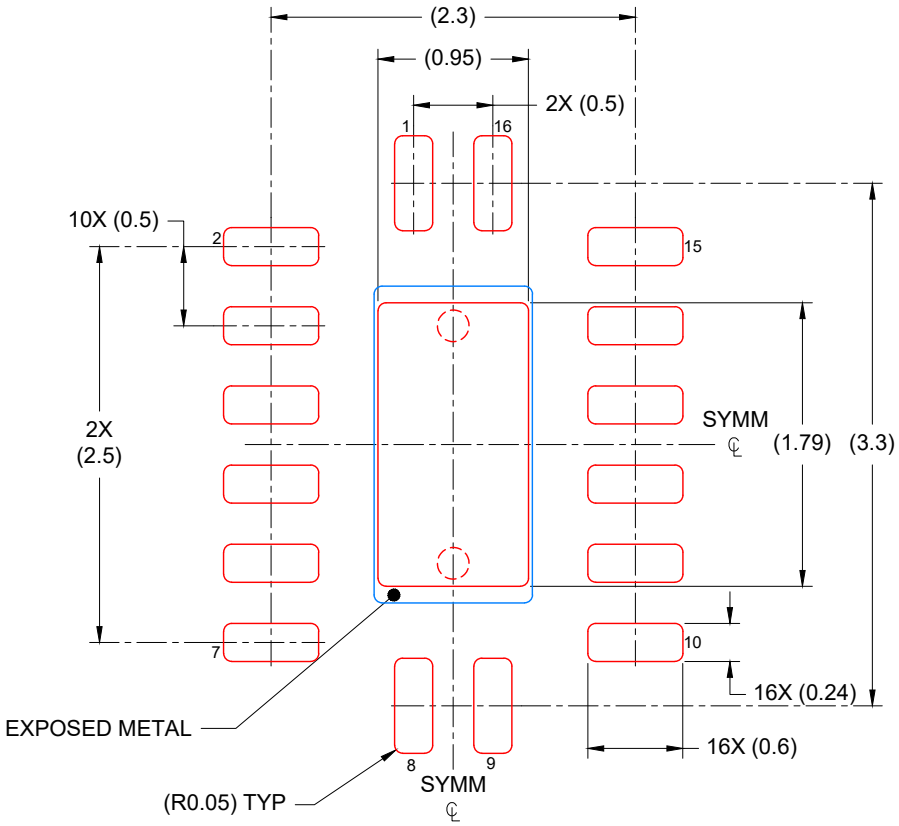


4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

NOTES: (continued)

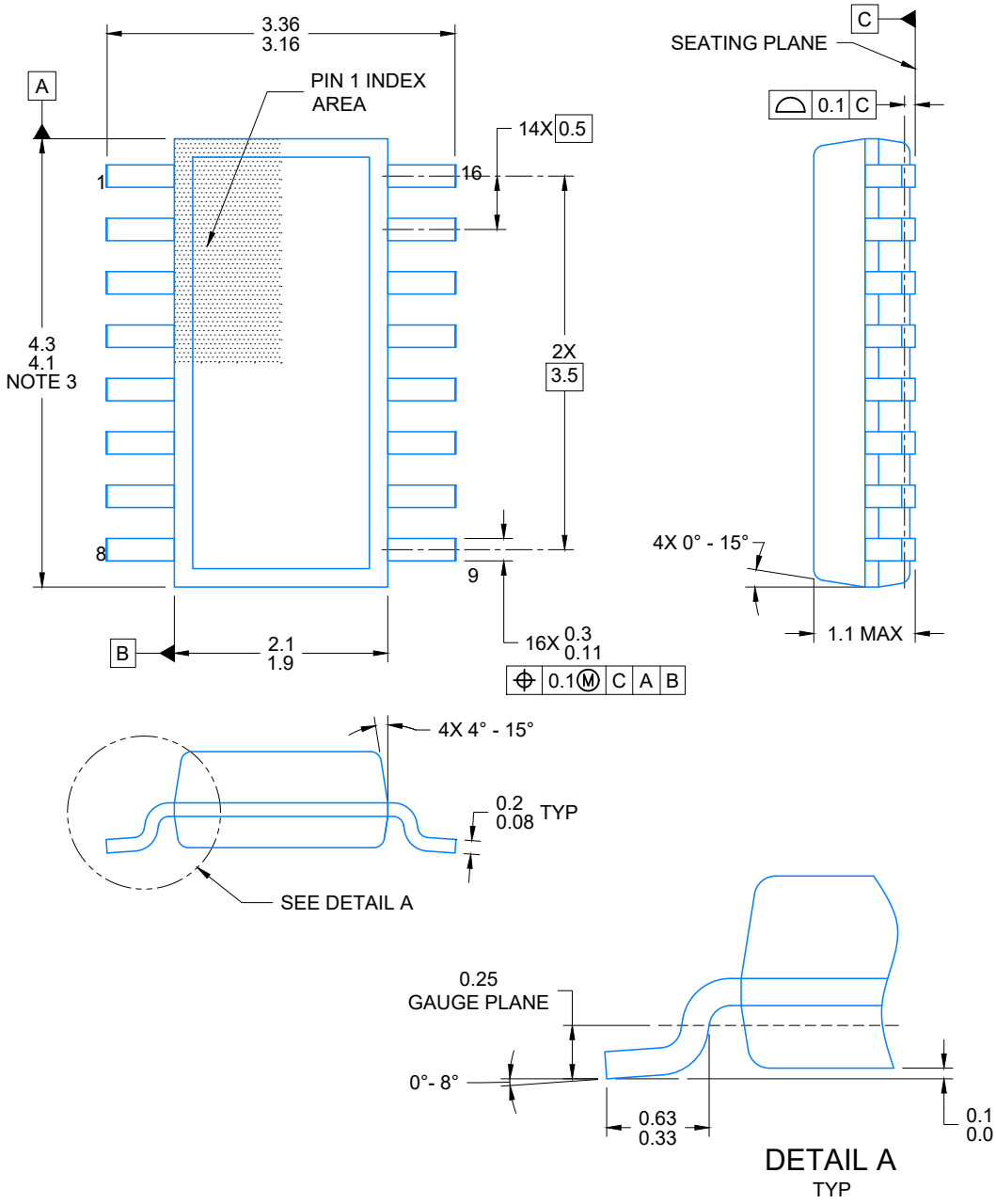
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

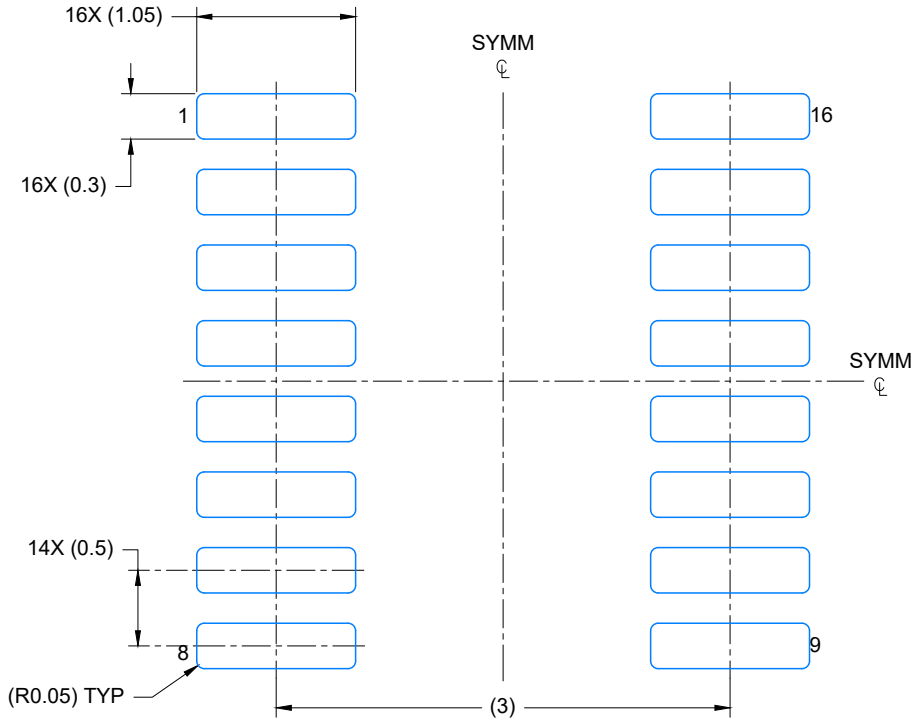
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

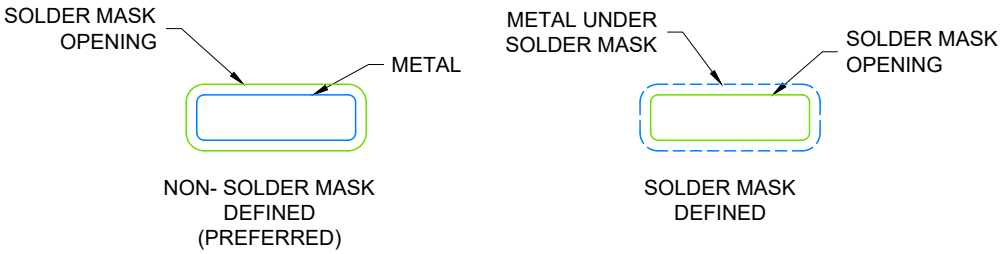


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

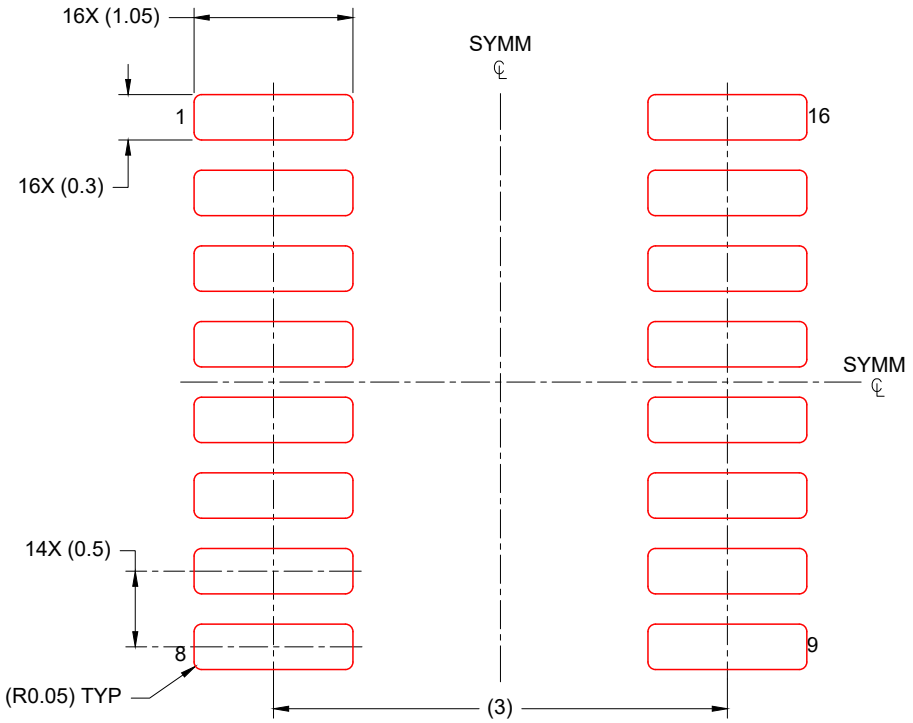
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

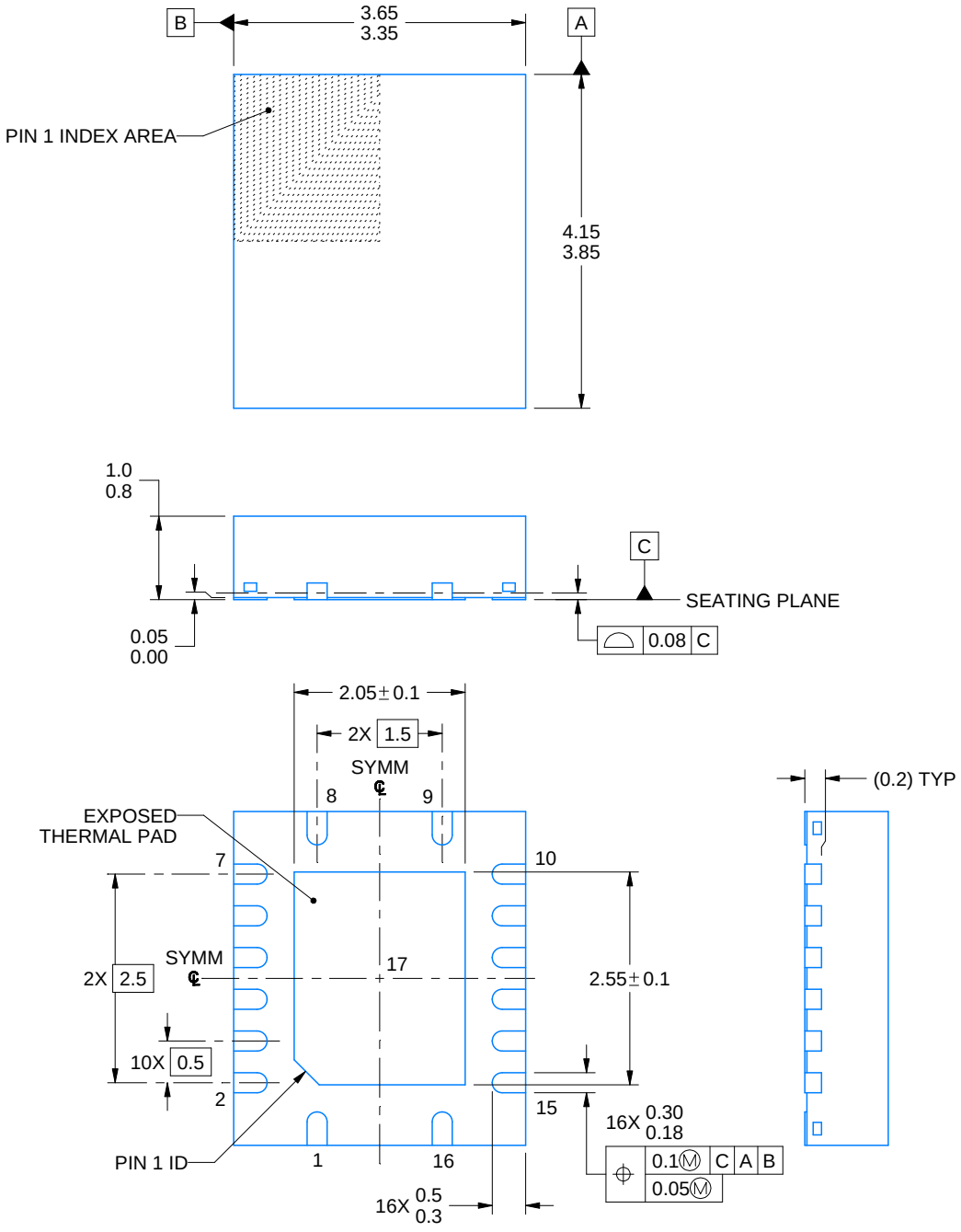
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY0016A

PACKAGE OUTLINE

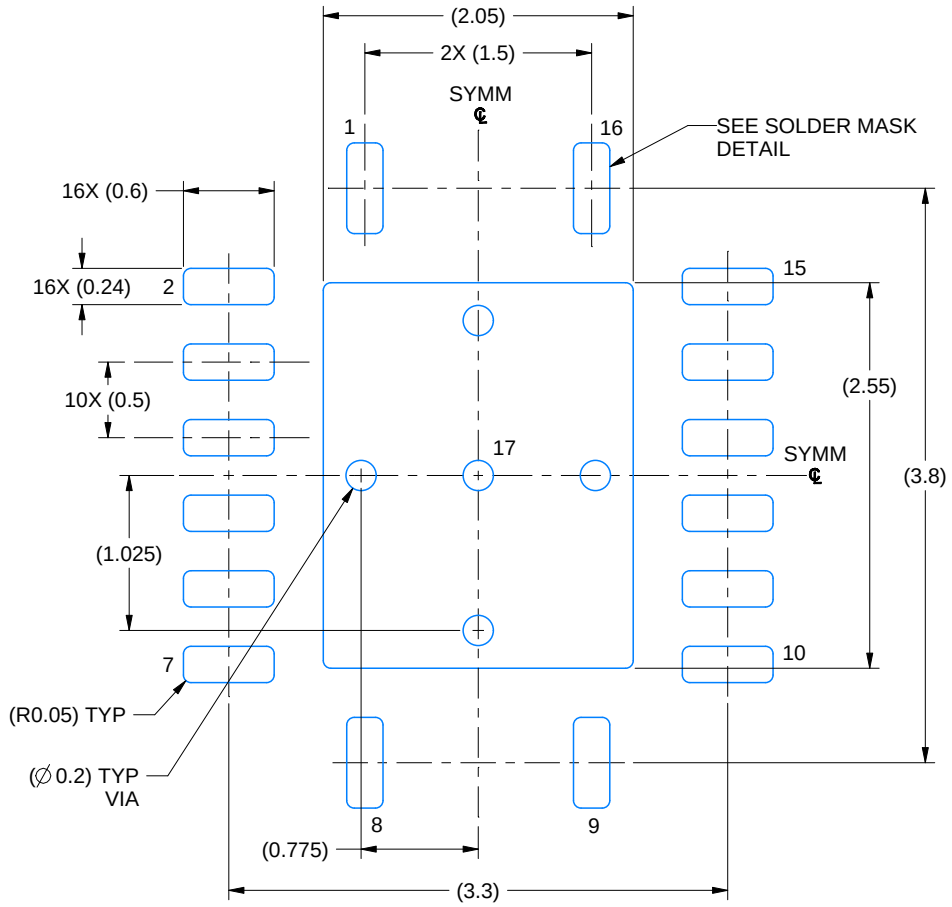
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

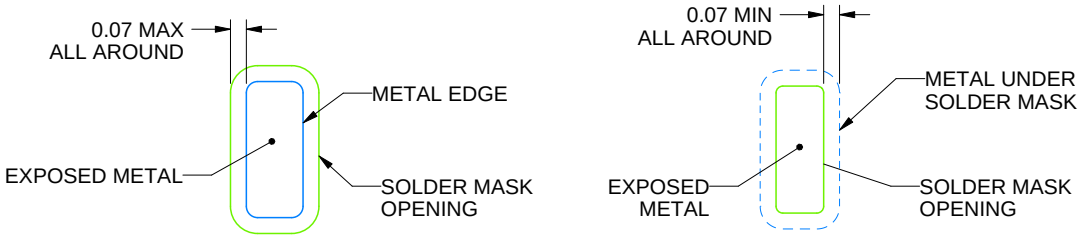


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

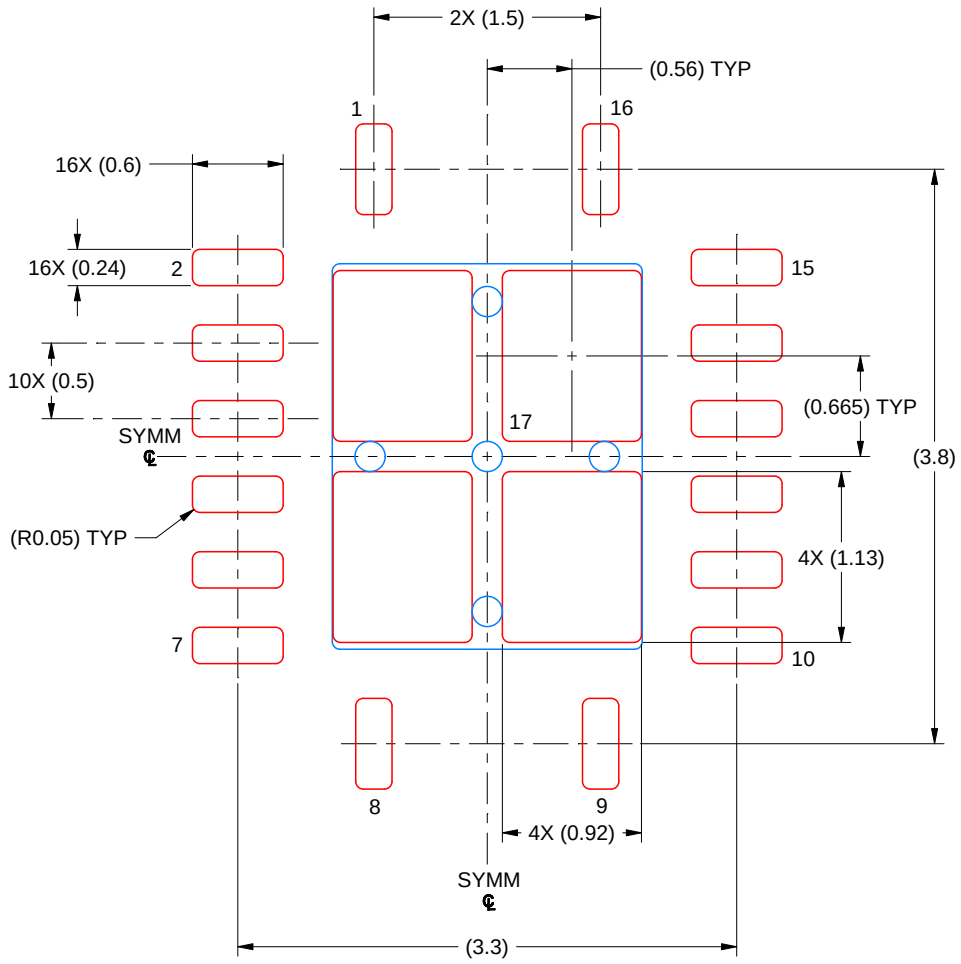


SOLDER MASK DETAILS

4225140/A 07/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

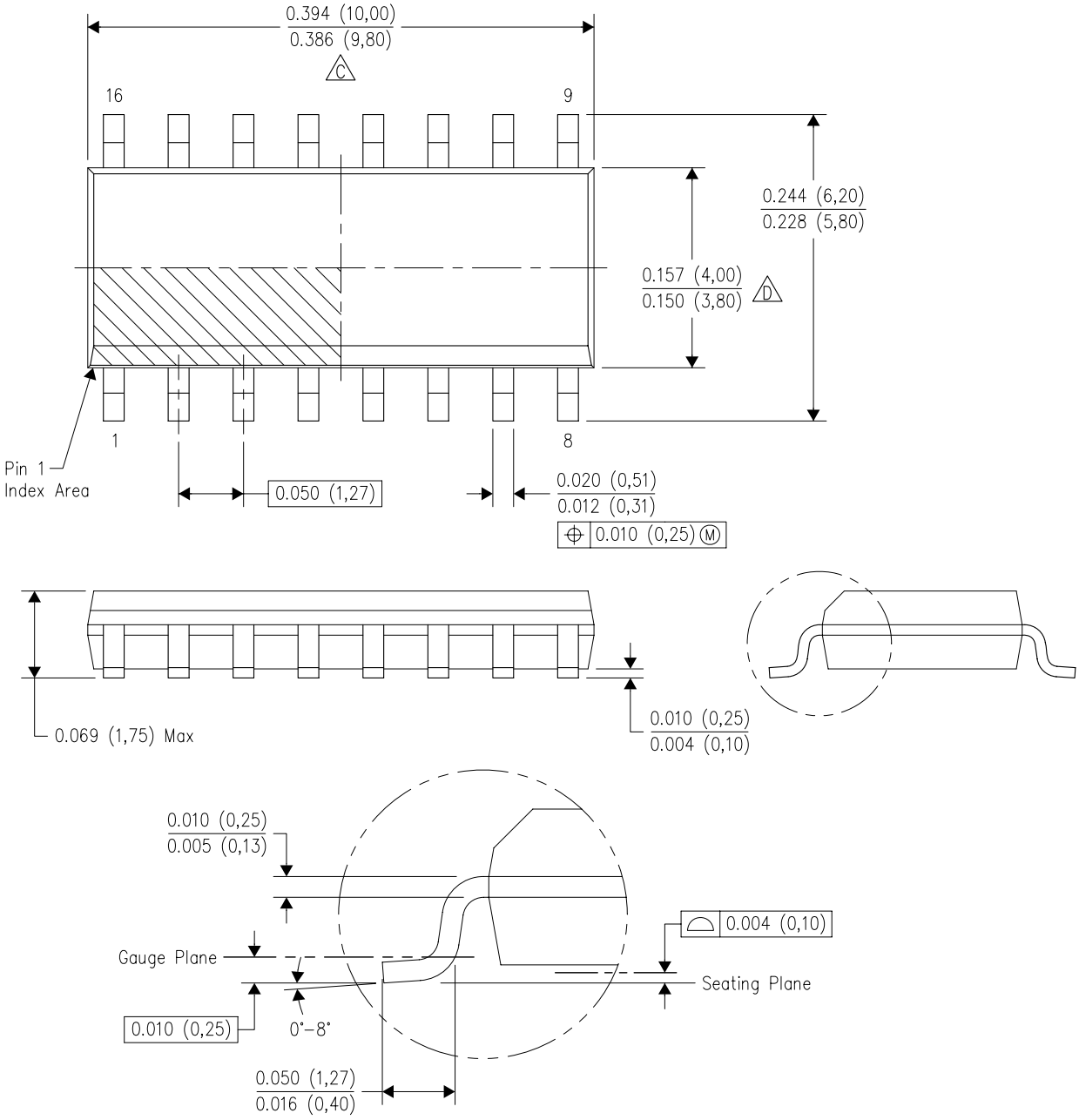
EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225140/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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最后更新日期：2025 年 10 月