

SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

- Combines 'F245 and 'F280B Functions in One Package
- High-Impedance N-P-N Inputs for Reduced Loading (70 μ A in Low and High States)
- High Output Drive and Light Bus Loading
- 3-State B Outputs Sink 64 mA and Source 15 mA
- Input Diodes for Termination Effects
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

description

The SN74F657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a specified current sinking capability of 24 mA at the A port and 64 mA at the B port.

The transmit/receive ($\overline{T/R}$) input determines the direction of the data flow through the bidirectional transceivers. When $\overline{T/R}$ is high, data is transmitted from the A port to the B port. When $\overline{T/R}$ is low, data is received at the A port from the B port.

When the output enable ($\overline{OE}$) input is high, both the A and B ports are placed in a high-impedance state (disabled). The $\overline{ODD/EVEN}$ input allows the user to select between odd or even parity systems. When transmitting from A port to B port ($\overline{T/R}$ high), PARITY is an output from the generator/checker. When receiving from B port to A port ($\overline{T/R}$ low), PARITY is an input.

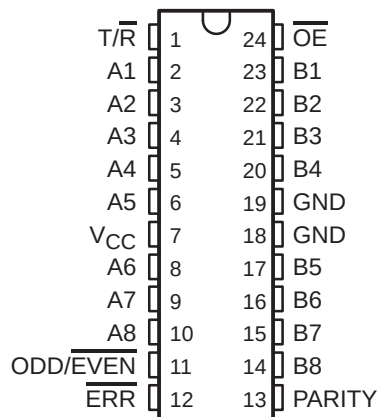
When transmitting ($\overline{T/R}$ high), the parity select ($\overline{ODD/EVEN}$) input is made high or low as appropriate. The A port is then polled to determine the number of high bits. The PARITY output goes to the logic state determined by $\overline{ODD/EVEN}$ and the number of high bits on A port. When $\overline{ODD/EVEN}$ is low (for even parity) and the number of high bits on A port is odd, the PARITY will be high, transmitting even parity. If the number of high bits on A port is even, the PARITY will be low, keeping even parity.

When in the receive mode ($\overline{T/R}$ low), the B port is polled to determine the number of high bits. If $\overline{ODD/EVEN}$ is low (for even parity) and the number of highs on B port is:

1. Odd and the PARITY input is high, then $\overline{ERR}$ will be high signifying no error.
2. Even and the PARITY input is high, then $\overline{ERR}$ will be low indicating an error.

The SN74F657 is characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE
(TOP VIEW)

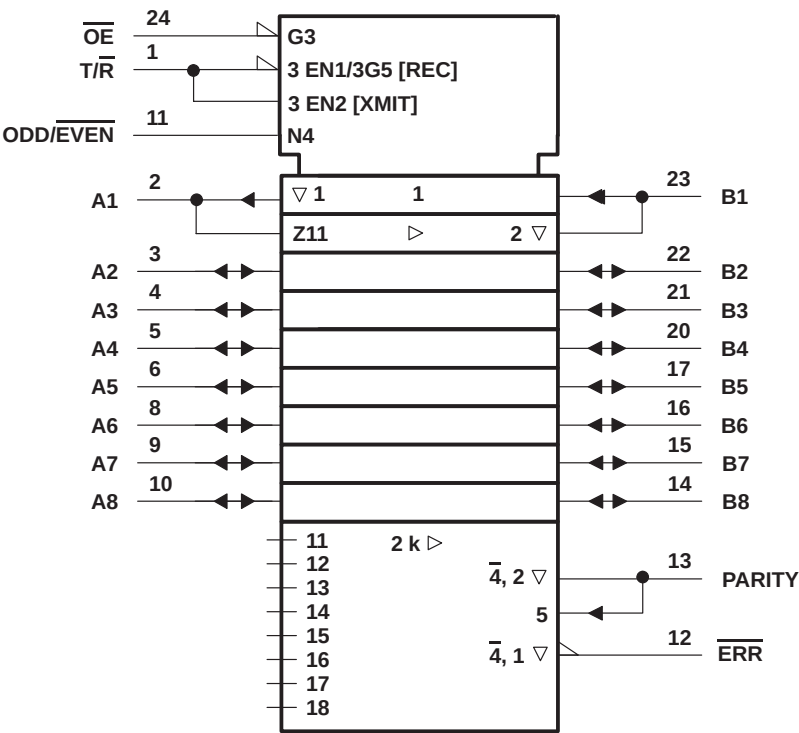


SN74F657
OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER
AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	$\overline{T/R}$	ODD/EVEN		ERR	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



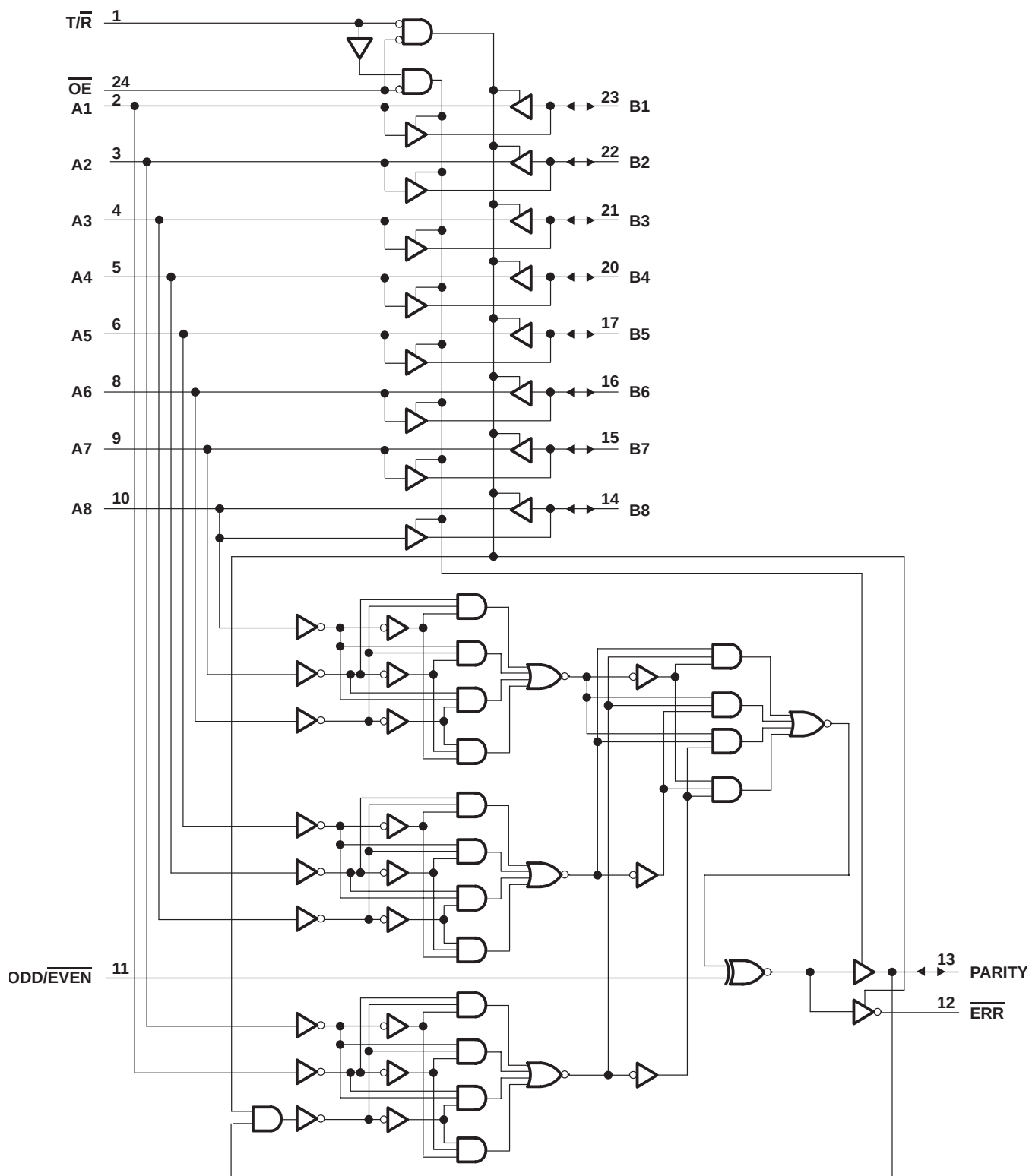
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

logic diagram (positive logic)



SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (excluding I/O ports) (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	–0.5 V to 5.5 V
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state: A1–A8	48 mA
B1–B8	128 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	A1–A8		–3	mA
		B1–B8, PARITY, $\overline{ERR}$		–12	
I_{OL}	Low-level output current	A1–A8		24	mA
		B1–B8, PARITY, $\overline{ERR}$		64	
T_A	Operating free-air temperature	0		70	°C



SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	Any output	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -3\text{ mA}$	2.4	3.3		V
	B1–B8, PARITY, $\overline{ERR}$	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -15\text{ mA}$	2	3.1		
	Any output	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -1\text{ mA to } -3\text{ mA}$	2.7			
V_{OL}	A1–A8	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 24\text{ mA}$		0.35	0.5	V
	B1–B8, PARITY, $\overline{ERR}$		$I_{OL} = 64\text{ mA}$		0.42	0.55	
I_I	$\overline{T/R}$	$V_{CC} = 0$,	$V_I = 7\text{ V}$,			0.1	mA
	$\overline{OE}$	$V_{CC} = 0$,	$V_I = 7\text{ V}$,			0.1	
	ODD/EVEN	$V_{CC} = 0$,	$V_I = 7\text{ V}$			0.1	
	A1–A8	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$			2	
	B1–B8					1	
$I_{IH}^{\ddagger}$	A, B, PARITY	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			70	μA
	$\overline{T/R}$, $\overline{OE}$					40	
	ODD/EVEN					20	
$I_{IL}^{\ddagger}$	A, B, PARITY	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-70	μA
	$\overline{T/R}$, $\overline{OE}$					-40	
	ODD/EVEN					-20	
$I_{OS}^{\S}$	A1–A8	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-60		-150	mA
	B1–B8			-100		-225	
I_{OZH}	$\overline{ERR}$	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			50	μA
I_{OZL}	$\overline{ERR}$	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-50	μA
I_{CCH}		$V_{CC} = 5.5\text{ V}$			90	125	mA
I_{CCL}		$V_{CC} = 5.5\text{ V}$			106	150	mA
I_{CCZ}		$V_{CC} = 5.5\text{ V}$			98	145	mA

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX [†]		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	2.5	4.2	7.5	2.5	8	ns
t _{PHL}			3	4	7.5	3	8	
t _{PLH}	A	PARITY	6	8.4	14	6	16	ns
t _{PHL}			6.8	8.5	15	6.8	16	
t _{PLH}	ODD/ $\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	4	6.4	11	4	12	ns
t _{PHL}			4.5	6.9	11.5	4.5	12.5	
t _{PLH}	B	$\overline{\text{ERR}}$	8	12.7	20.5	7.5	22.5	ns
t _{PHL}			8	13.4	20.5	7.5	22.5	
t _{PLH}	PARITY	$\overline{\text{ERR}}$	6	8.1	15.5	6	16.5	ns
t _{PHL}			7.5	8.8	15.5	7.5	17	
t _{PZH}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$ [‡]	3	5.3	8	3	9	ns
t _{PZL}			4	5.4	9.5	4	11	
t _{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$ [‡]	2	4.2	7.5	2	8	ns
t _{PLZ}			2	3.7	6	2	6.5	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] These delay times reflect the 3-state recovery time only and not the signal through the buffers or parity check circuitry. To assure valid information at the $\overline{\text{ERR}}$ output pin, time must be allowed for the signal to propagate through the drivers (B to A), and to the $\overline{\text{ERR}}$ output. Valid data at the $\overline{\text{ERR}}$ output is greater than or equal to (B to A) + (A to PARITY).

NOTE 2: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74F657DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F657
SN74F657DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F657

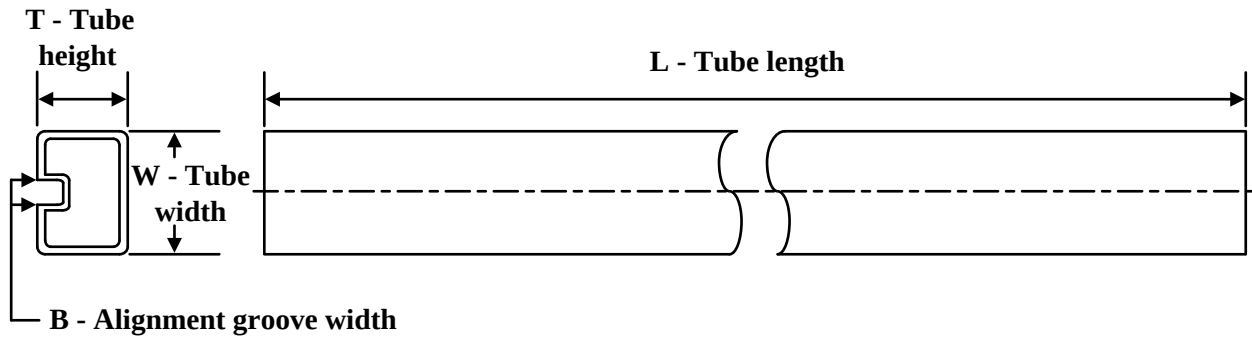
- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE

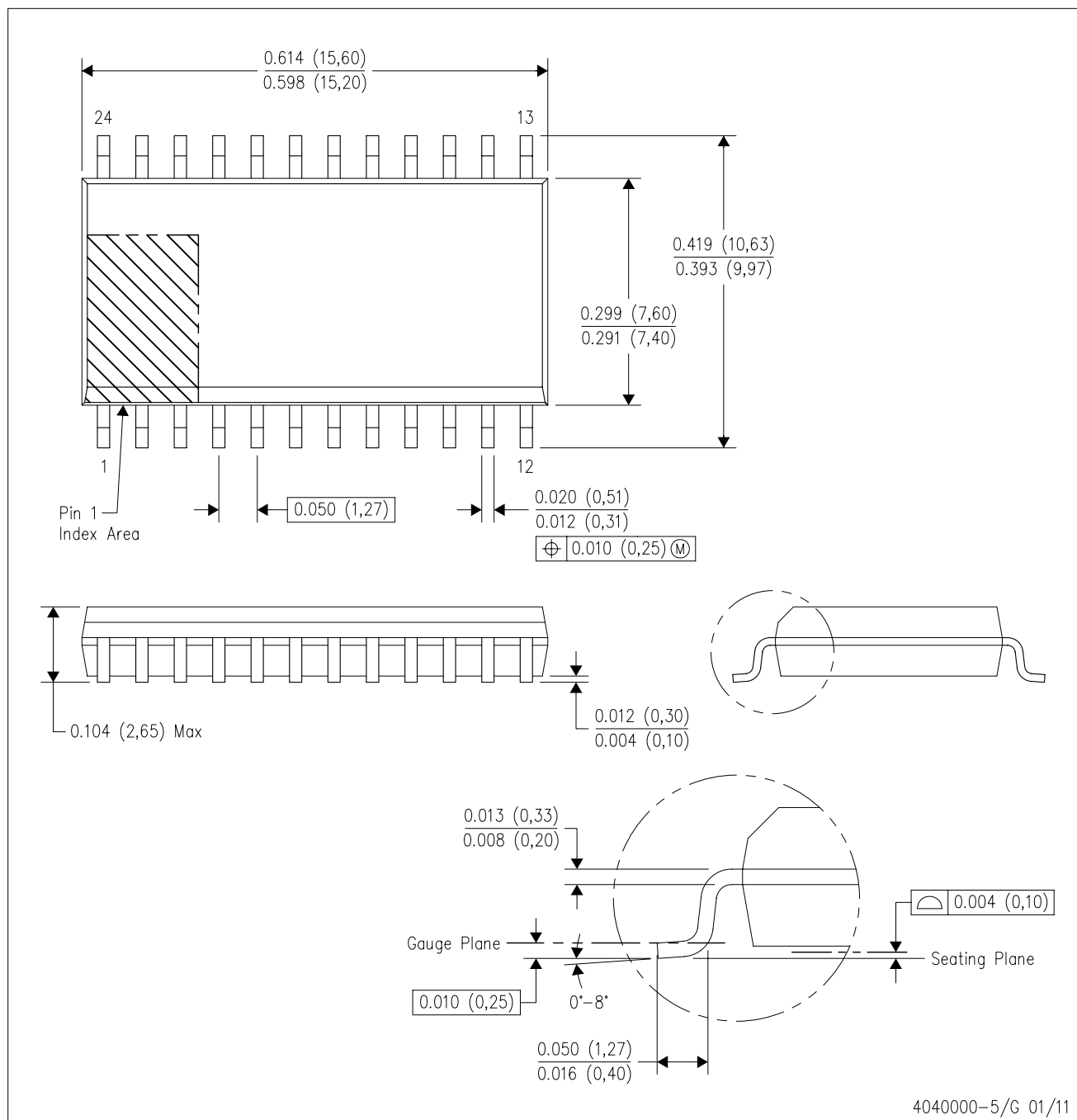


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F657DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74F657DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025