SNx4HC240 具有三态输出的八路缓冲器和线路驱动器

1 特性

- 2V 至 6V 的宽工作电压范围
- 高电流输出可驱动多达 15 个 LSTTL 负载
- 低功耗，I_{CC} 最大值为 80 μA
- t_{pd} 典型值 = 9ns
- 5V 时，输出驱动为 ±6mA
- 低输入电流，最大值 1μA
- 三态输出驱动总线或缓冲存储器地址寄存器

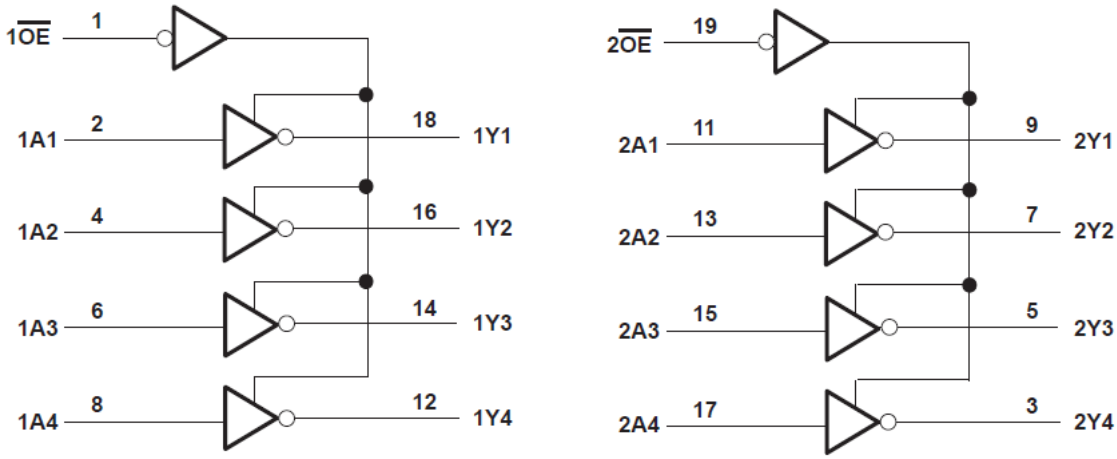
2 说明

这些八路缓冲器和线路驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。’HC240 器件配置为两个具有独立输出使能 ($\overline{OE}$) 输入的 4 位缓冲器/驱动器。当 $\overline{OE}$ 为低电平时，该器件将来自 A 输入的反相数据传递到 Y 输出。当 $\overline{OE}$ 为高电平时，输出处于高阻态。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SN74HC240	DW（SOIC，20）	12.80mm x 10.3mm	12.80mm x 7.50mm
	DB（SSOP，20）	7.2mm x 7.8mm	7.2mm x 5.30mm
	DGS（VSSOP，20）	5.1mm × 4.9mm	5.1mm × 3mm
	PDIP (20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	NS（SOP，20）	12.6mm x 7.8mm	12.6mm x 5.3mm
	PW（TSSOP，20）	6.50mm x 6.4mm	6.50mm x 4.40mm
SNx4HC240	J（CDIP，20）	24.2mm x 7.62mm	24.2mm x 6.92mm
	FK（LCCC，20）	8.9mm x 8.9mm	8.9mm x 8.9mm
	W（CFP，20）	13.09mm x 8.13mm	13.09mm x 6.92mm

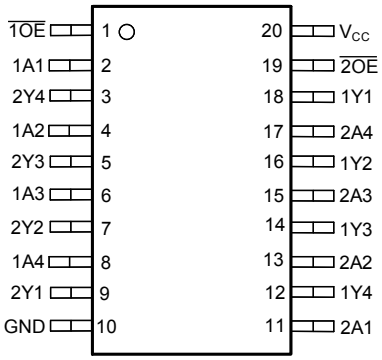
(1) 有关更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



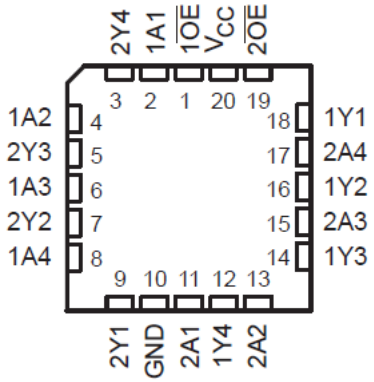
功能方框图

内容

3 引脚配置和功能



J、W、DB、DGS、DW、N、NS 或 PW 封装
20 引脚 CDIP、CFP、SSOP。SOIC、PDIP、SO、TSSOP
（顶视图）



FK 封装
20 引脚 LCCC
（顶视图）

表 3-1. 引脚功能

名称 [1]	引脚	类型	说明
1OE	1	I	输出使能 1
1A1	2	I	1A1 输入
2Y4	3	O	2Y4 输出
1A2	4	I	1A2 输入
2Y3	5	O	2Y3 输出
1A3	6	I	1A3 输入
2Y2	7	O	2Y2 输出
1A4	8	I	1A4 输入
2Y1	9	O	2Y1 输出
GND	10	—	接地引脚
2A1	11	I	2A1 输入
1Y4	12	O	1Y4 输出
2A2	13	I	2A2 输入
1Y3	14	O	1Y3 输出
2A3	15	I	2A3 输入
1Y2	16	O	1Y2 输出
2A4	17	I	2A4 输入
1Y1	18	O	1Y1 输出
2OE	19	I	输出使能 2
VCC	20	—	电源引脚

1. I = 输入、O = 输出、P = 电源、FB = 反馈、GND = 接地、N/A = 不适用

4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
I_{IK}	输入钳位电流(2)	$V_I < 0$ 或 $V_I > V_{CC}$		±20	mA
I_{OK}	输出钳位电流(2)	$V_O < 0$ 或 $V_O > V_{CC}$		±20	mA
I_O	持续输出电流	$V_O = 0$ 至 V_{CC}		±35	mA
	通过 V_{CC} 或 GND 的持续电流			±70	mA
T_J	结温			150	°C
T_{stg}	贮存温度范围		-65	150	°C
	引线温度（焊接 10s）（SOIC - 仅限引线尖端）			300	°C

(1) 超出*最大绝对额定值*下列出的值的应力可能会对器件造成永久损坏。这些仅为在应力额定值下的工作情况，对于额定值下的器件的功能性操作以及在超出*推荐的运行条件*下标明的任何其它条件下的操作，在此并未说明。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，有可能超过输入负电压和输出电压额定值。

4.2 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN54HC240			SN74HC240			单位
			最小值	标称值	最大值	最小值	标称值	最大值	
V_{CC}	电源电压		2	5	6	2	5	6	V
V_{IH}	高电平输入电压	V_{CC} = 2V	1.5			1.5			V
		V_{CC} = 4.5V	3.15			3.15			
		V_{CC} = 6V	4.2			4.2			
V_{IL}	低电平输入电压	V_{CC} = 2V			0.5			0.5	V
		V_{CC} = 4.5V			1.35			1.35	
		V_{CC} = 6V			1.8			1.8	
V_I	输入电压		0		V_{CC}	0		V_{CC}	V
V_O	输出电压		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	输入转换上升和下降时间	V_{CC} = 2V			1000			1000	ns
		V_{CC} = 4.5V			500			500	
		V_{CC} = 6V			400			400	
T_A	自然通风条件下的工作温度范围		-55		125	-40		85	°C

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢或悬空的影响*，文献编号 SCBA004。

4.3 热性能信息

热指标		SN74HC240						单位
		DW (SOIC)	DB (SSOP)	DGS (VSSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	
$R_{\theta JA}$	结至环境热阻 (1)	109.1	122.7	130.6	84.6	113.4	131.8	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	76	81.6	68.7	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	结至电路板热阻	77.6	77.5	85.4	65.3	78.4	82.8	°C/W
Ψ_{JT}	结至顶部特征参数	51.5	46.1	10.5	55.3	47.1	21.5	°C/W

4.3 热性能信息（续）

热指标		SN74HC240 DW (SOIC) 20 引脚	DB (SSOP) 20 引脚	DGS (VSSOP) 20 引脚	N (PDIP) 20 引脚	NS (SOP) 20 引脚	PW (TSSOP) 20 引脚	单位
Ψ_{JB}	结至电路板特征参数	77.1	77.1	85.0	65.2	78.1	82.4	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	不适用	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *半导体和 IC 封装热指标* 应用报告。

4.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件		V_{CC}	T_A = 25°C 最小值	典型值	最大值	SN54HC240 最小值	最大值	SN74HC240 最小值	最大值	单位
V_{OH}	$V_I = V_{IH}$ 或 V_{IL}	I_{OH} = -20μA	2V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6V	5.9	5.999		5.9		5.9		
		I_{OH} = -6mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH} = -7.8mA	6V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ 或 V_{IL}	I_{OL} = 20μA	2V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6V		0.001	0.1		0.1		0.1	
		I_{OL} = 6mA	4.5V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8mA	6V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ 或 0		6V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ 或 0		6V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ 或 0， I_O = 0		6V			8		160		80	μA
C_i			2V 至 6V		3	10		10		10	pF

4.5 开关特性

在自然通风条件下的建议工作温度范围内测得，C_L = 50pF（除非另有说明）（请参阅图 5-1）

参数	从（输入）	至（输出）	V_{CC}	T_A = 25°C 最小值	典型值	最大值	SN54HC240 最小值	最大值	SN74HC240 最小值	最大值	单位
t_{pd}	A	Y	2V		50	100		150		125	ns
			4.5V		10	20		30		25	
			6V		9	17		25		21	
t_{en}	$\overline{OE}$	Y	2V		75	150		225		190	ns
			4.5V		15	30		45		38	
			6V		13	26		38		32	
t_{dis}	$\overline{OE}$	Y	2V		44	150		225		190	ns
			4.5V		22	30		45		38	
			6V		21	26		38		32	
t_t		Y	2V		28	60		90		75	ns
			4.5V		8	12		18		15	
			6V		6	10		15		13	

4.6 开关特性

在自然通风条件下的建议工作温度范围内测得，C_L = 150pF（除非另有说明）（请参阅图 5-1）

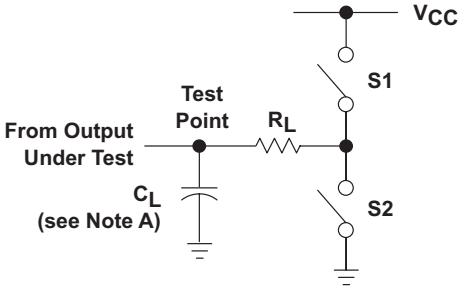
参数	从（输入）	至（输出）	V_{CC}	T_A = 25°C			SN54HC240		SN74HC240		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	2V		75	150		225		190	ns
			4.5V		15	30		45		38	
			6V		13	26		38		32	
t_{en}	$\overline{OE}$	Y	2V		100	200		300		250	ns
			4.5V		20	40		60		50	
			6V		17	34		51		43	
t_t		Y	2V		45	210		315		265	ns
			4.5V		17	42		63		53	
			6V		13	36		53		45	

4.7 工作特性

T_A = 25°C

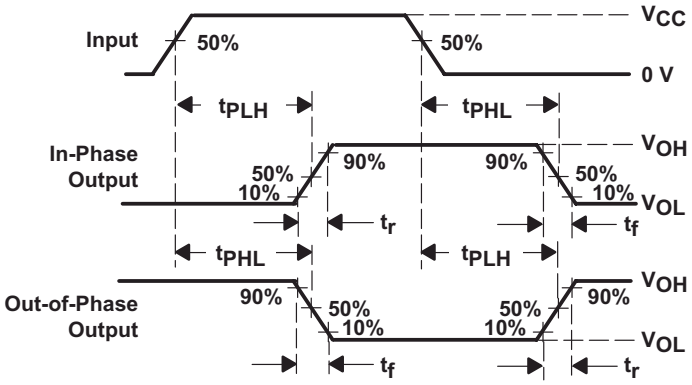
参数		测试条件	典型值	单位
C_{pd}	每个缓冲器/驱动器的功率耗散电容	空载	35	pF

5 参数测量信息

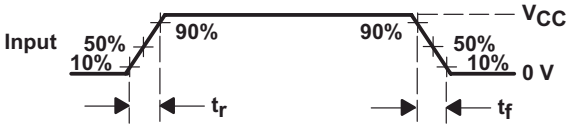


LOAD CIRCUIT

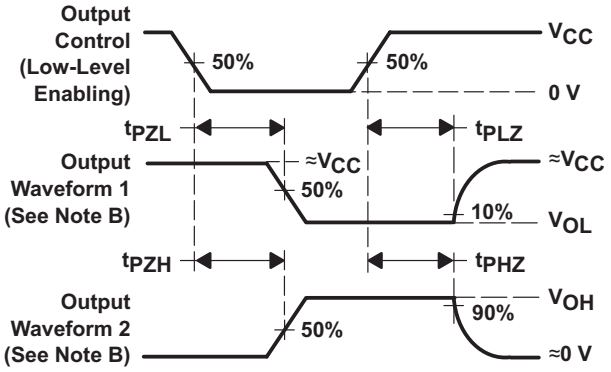
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

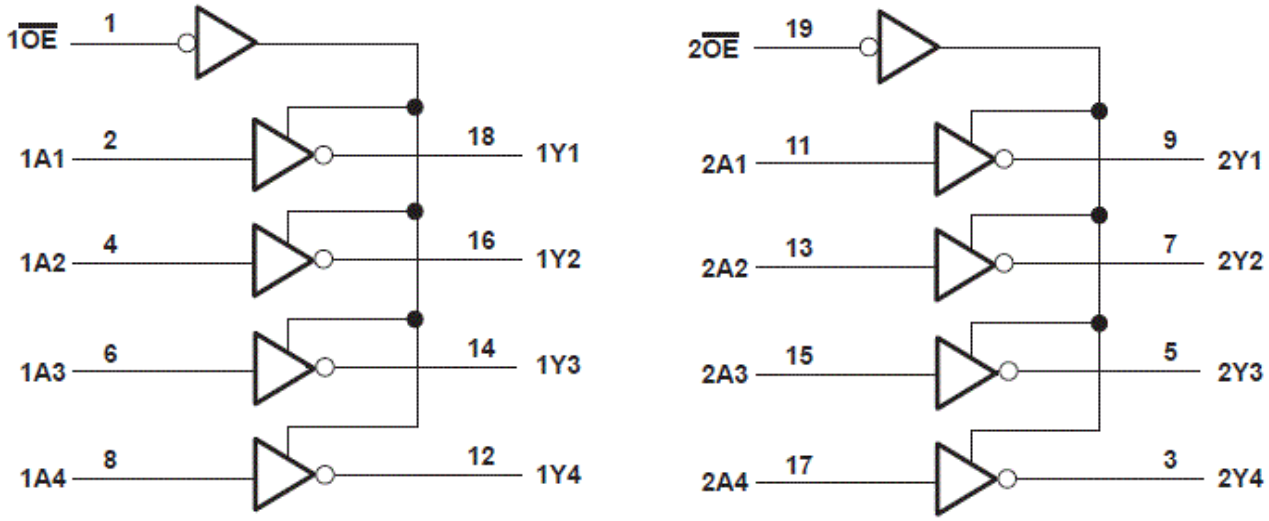
图 5-1. 负载电路和电压波形

6 详细说明

6.1 概述

这些八路缓冲器和线路驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。’HC240 器件配置为两个具有独立输出使能 ($\overline{OE}$) 输入的 4 位缓冲器/驱动器。当 $\overline{OE}$ 为低电平时，该器件将来自 A 输入的反相数据传递到 Y 输出。当 $\overline{OE}$ 为高电平时，输出处于高阻态。

6.2 功能方框图



6.3 器件功能模式

表 6-1. 功能表
（每个缓冲器/驱动器）

输入		输出
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 电源相关建议

电源可以是*建议运行条件* 中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。建议为该器件使用 0.1 µF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

7.2 布局

7.2.1 布局指南

使用多输入和多通道逻辑器件时，输入不得悬空。在许多情况下，未使用数字逻辑器件的全部或部分功能；例如，仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个。此类未使用的输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的操作状态。数字逻辑器件的所有未使用输入必须连接到由输入电压规范定义的逻辑高电平电压或逻辑低电平电压，以防止其悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，输入连接到 GND 或 V_{CC}，以对逻辑功能更有意义或更方便者为准。

8 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

8.1 文档支持

8.1.1 相关文档

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (April 2022) to Revision H (August 2024)	Page
• 向*器件信息* 表、*引脚配置和功能* 部分以及*热性能信息* 表中添加了 DGS 封装	1
• 向*器件信息* 表添加了封装尺寸	1
• 添加了*引脚功能* 表	3

Changes from Revision F (December 2021) to Revision G (April 2022)	Page
• 添加了*应用和实施* 部分	9

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84074012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84074012A SNJ54HC 240FK
8407401RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407401RA SNJ54HC240J
8407401SA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407401SA SNJ54HC240W
JM38510/65703B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65703B2A
JM38510/65703B2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65703B2A
JM38510/65703BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65703BRA
JM38510/65703BRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65703BRA
M38510/65703B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65703B2A
M38510/65703BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65703BRA
SN54HC240J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC240J
SN54HC240J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC240J
SN74HC240DBR	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SN74HC240DBR.A	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SN74HC240DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC240
SN74HC240DGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC240
SN74HC240DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 85	HC240
SN74HC240DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SN74HC240DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SN74HC240N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC240N
SN74HC240N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC240N
SN74HC240NE4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC240N
SN74HC240NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC240NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SN74HC240PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SN74HC240PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SN74HC240PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC240
SNJ54HC240FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84074012A SNJ54HC 240FK
SNJ54HC240FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84074012A SNJ54HC 240FK
SNJ54HC240J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407401RA SNJ54HC240J
SNJ54HC240J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407401RA SNJ54HC240J
SNJ54HC240W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407401SA SNJ54HC240W
SNJ54HC240W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407401SA SNJ54HC240W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54HC240, SN74HC240 :

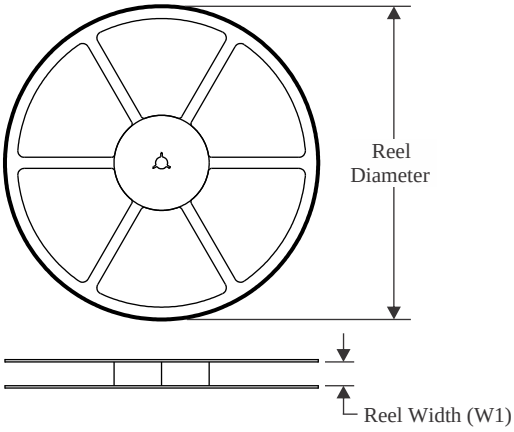
- Catalog : SN74HC240
- Military : SN54HC240

NOTE: Qualified Version Definitions:

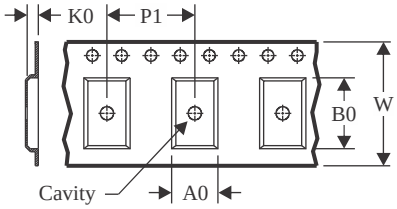
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

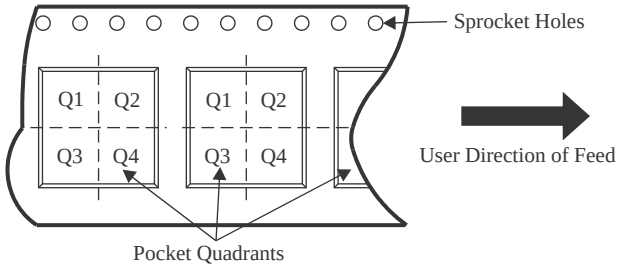


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

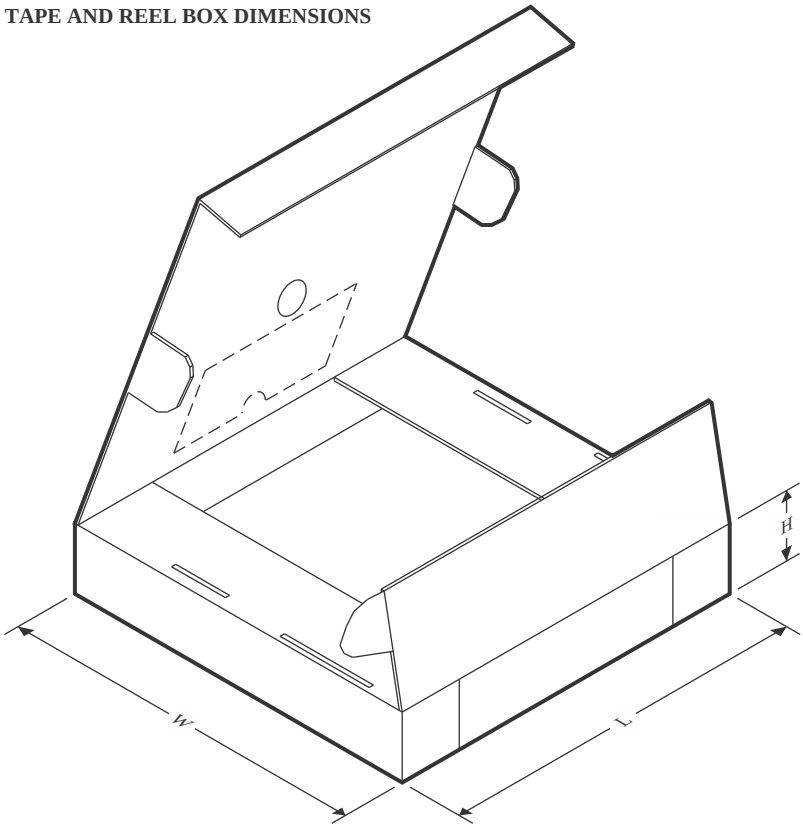
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC240DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74HC240DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC240NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

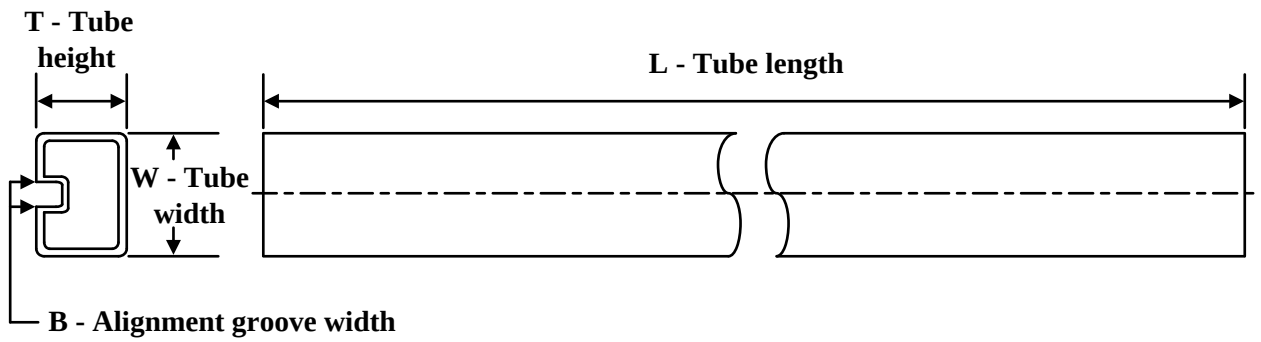
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC240DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74HC240DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74HC240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC240NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74HC240PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

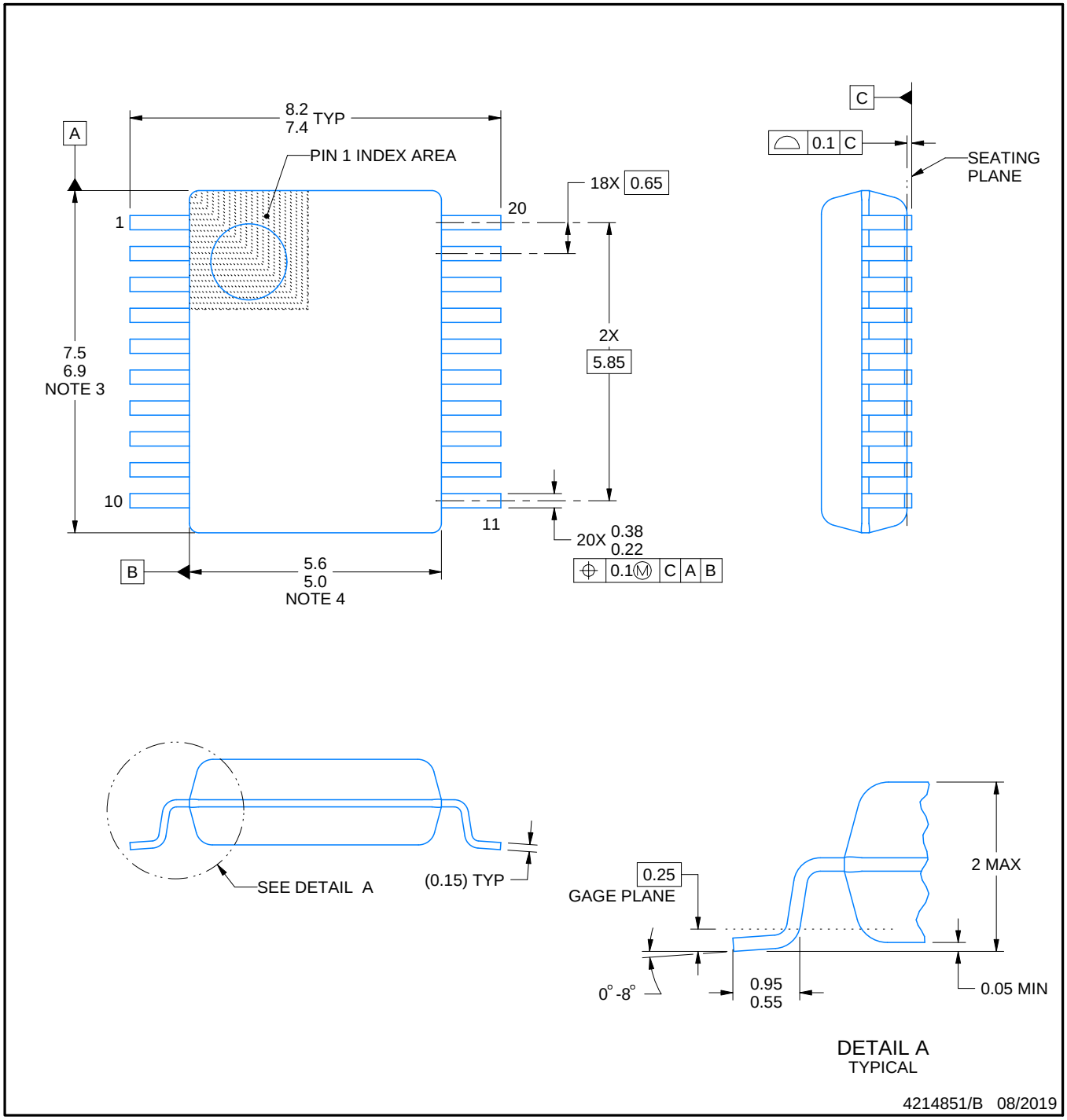
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
84074012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8407401SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/65703B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65703B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/65703B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC240N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC240N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC240NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC240FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC240FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC240W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54HC240W.A	W	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DB0020A

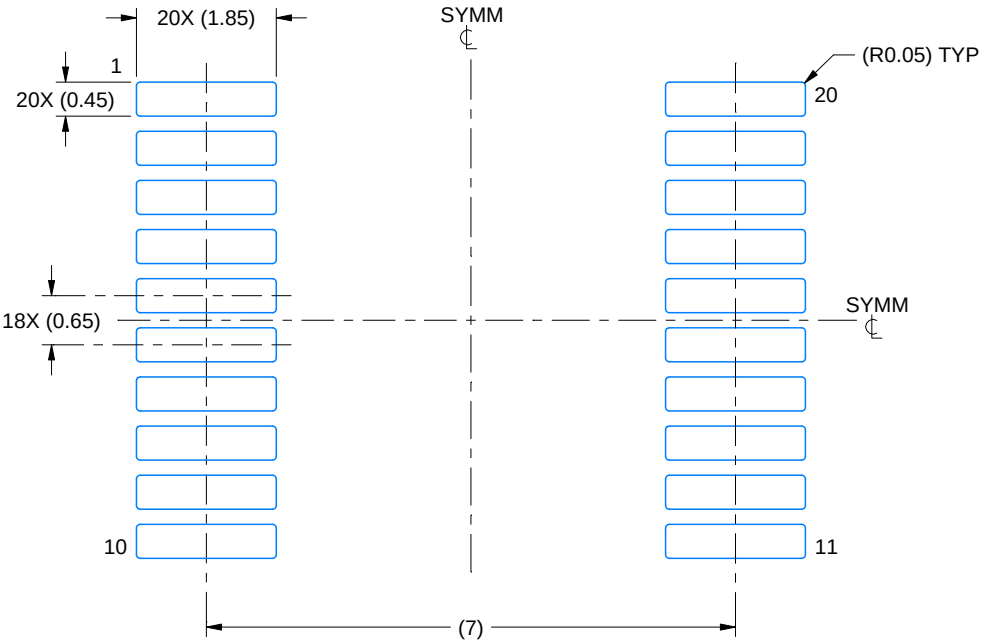
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

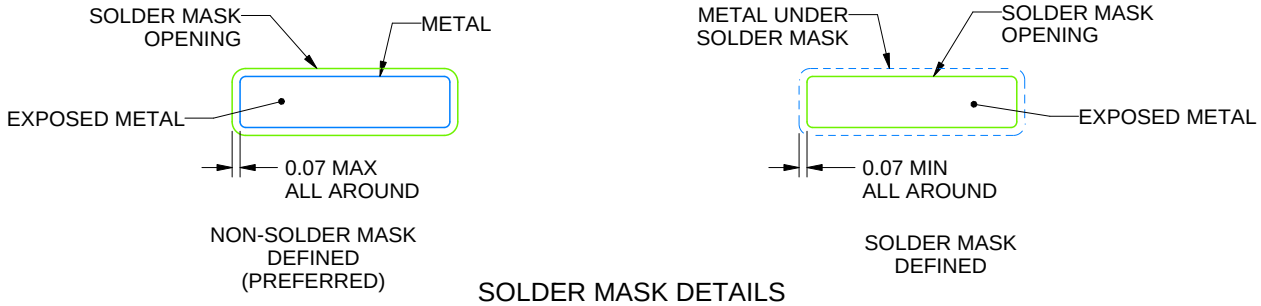


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

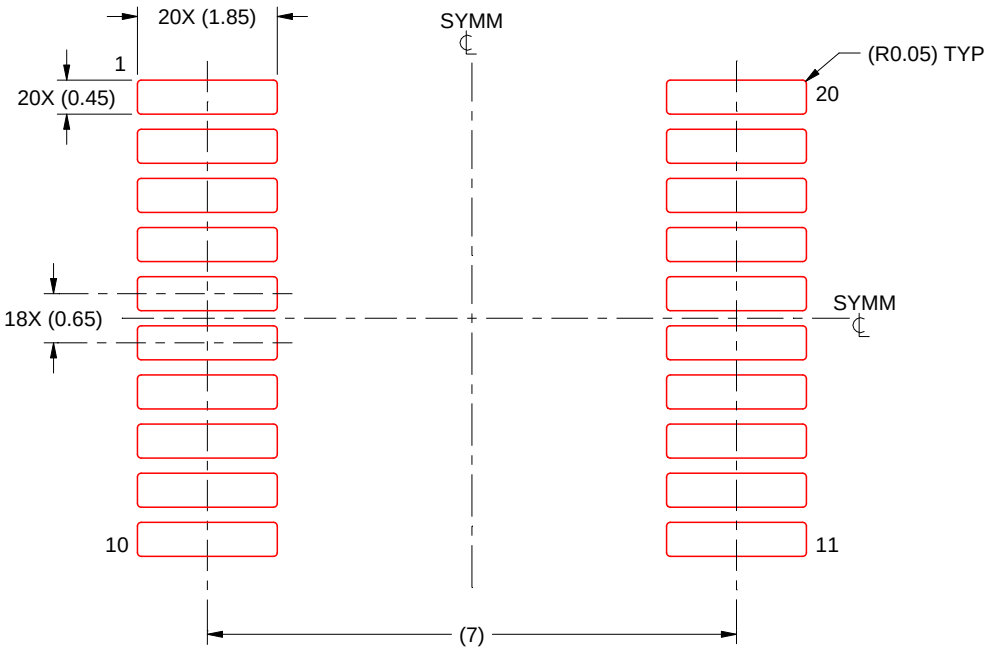
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

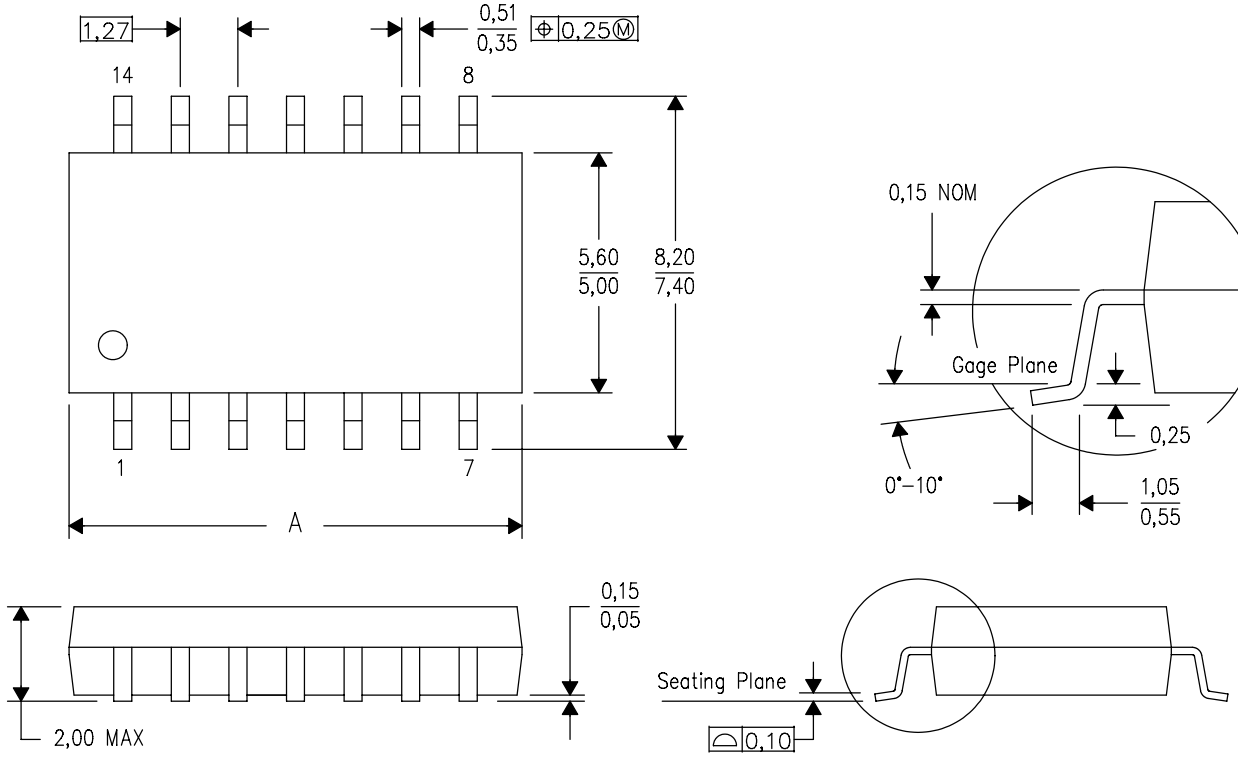
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

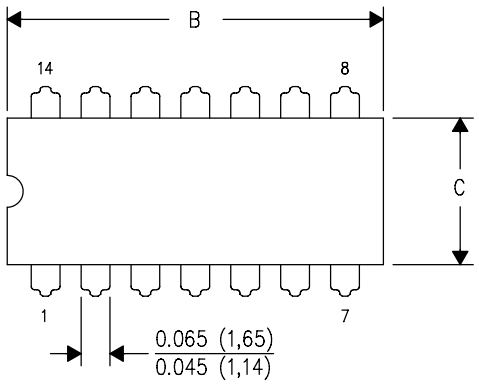
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

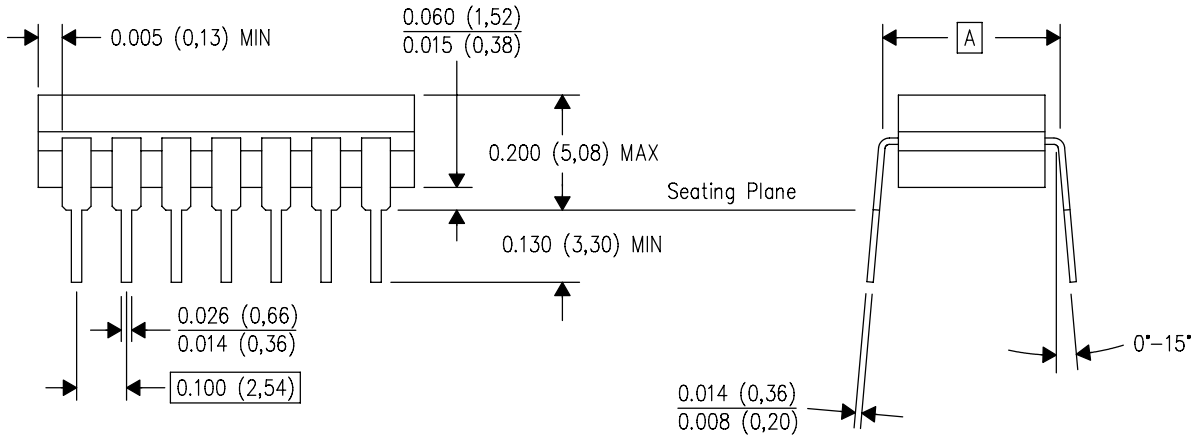
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

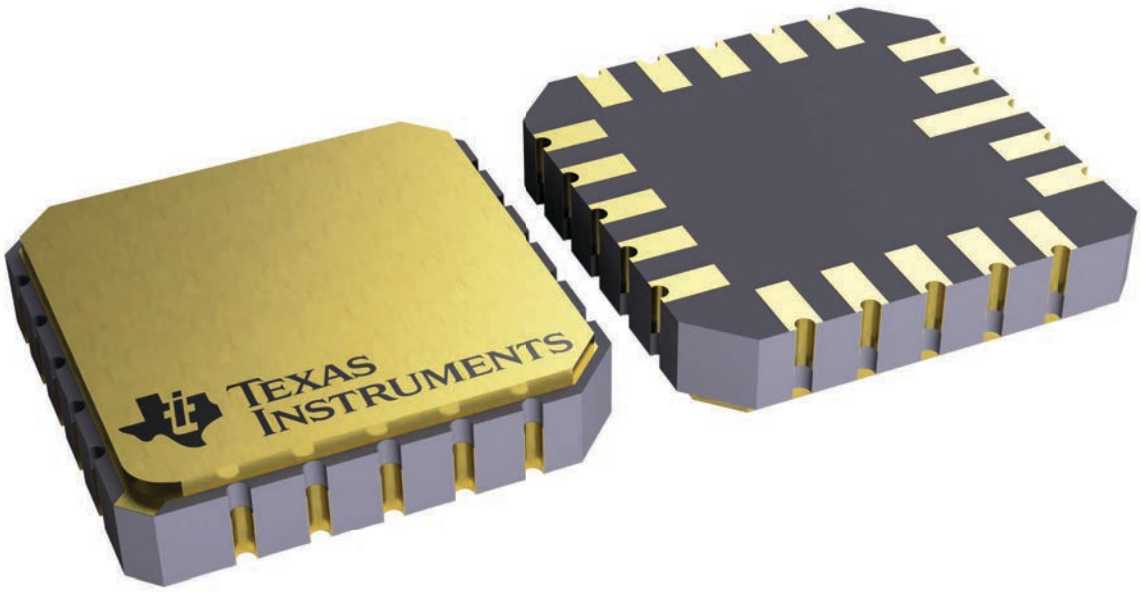
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

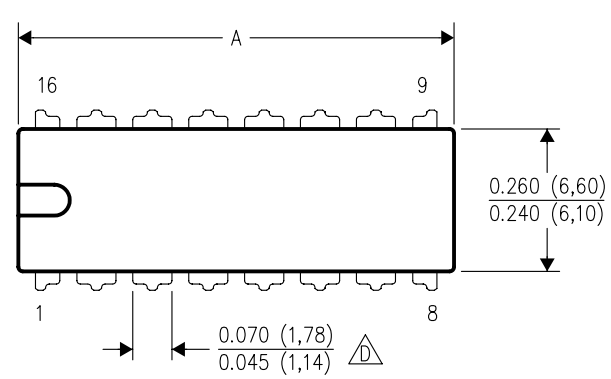


4229370VA\

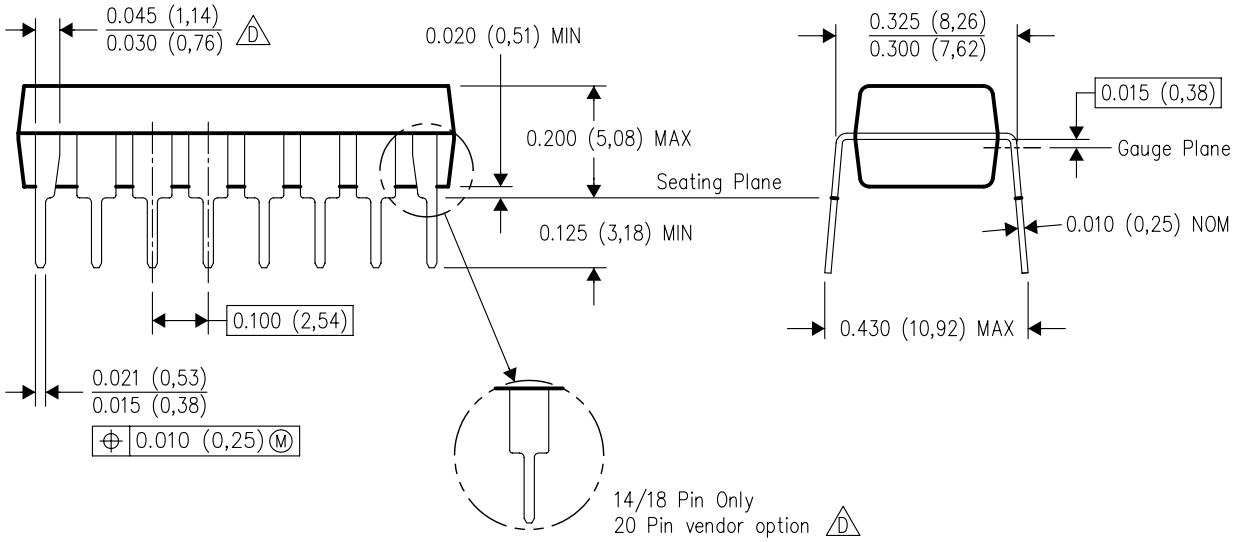
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

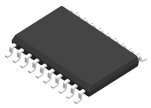


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

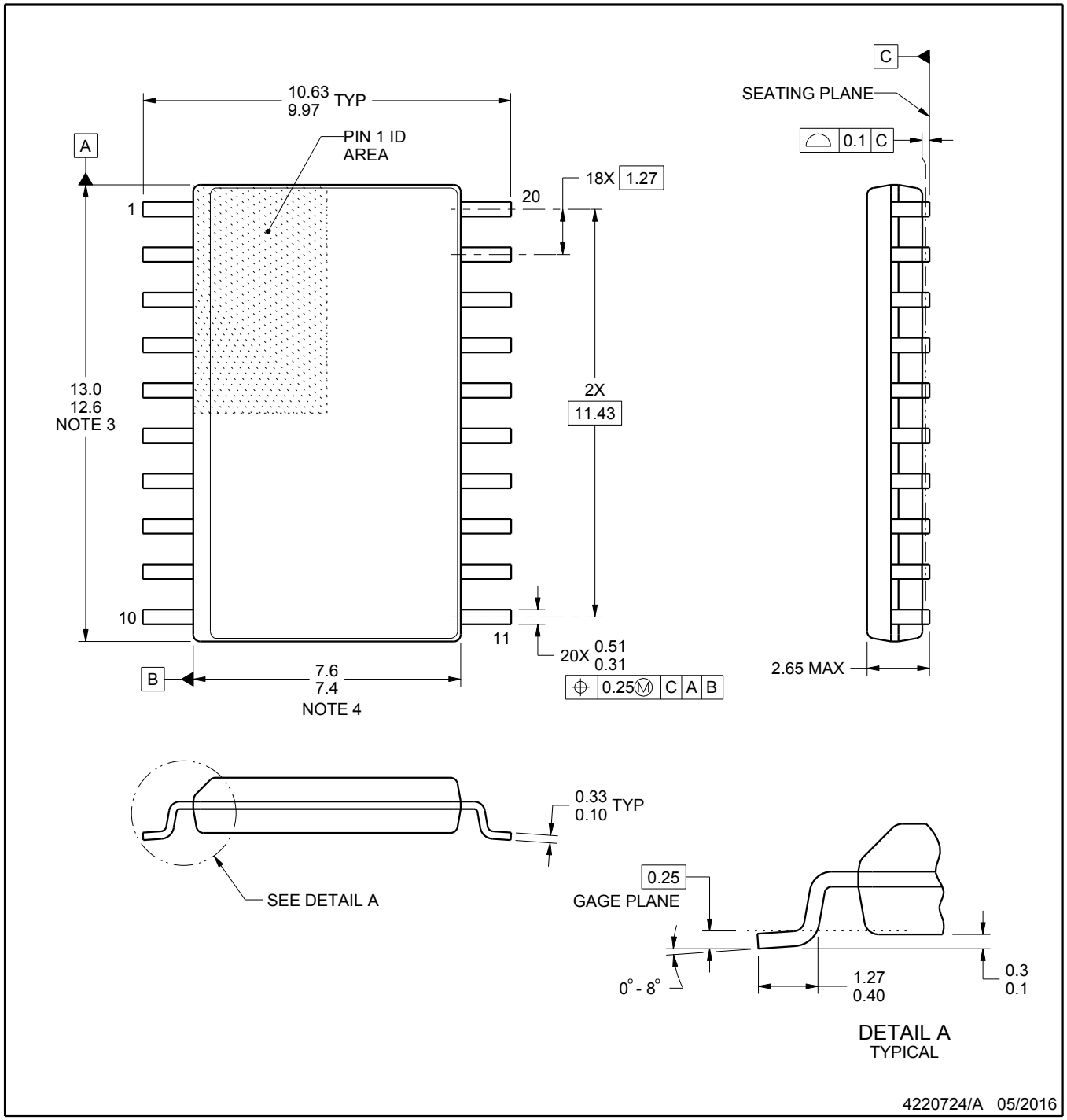


PACKAGE OUTLINE

DW0020A

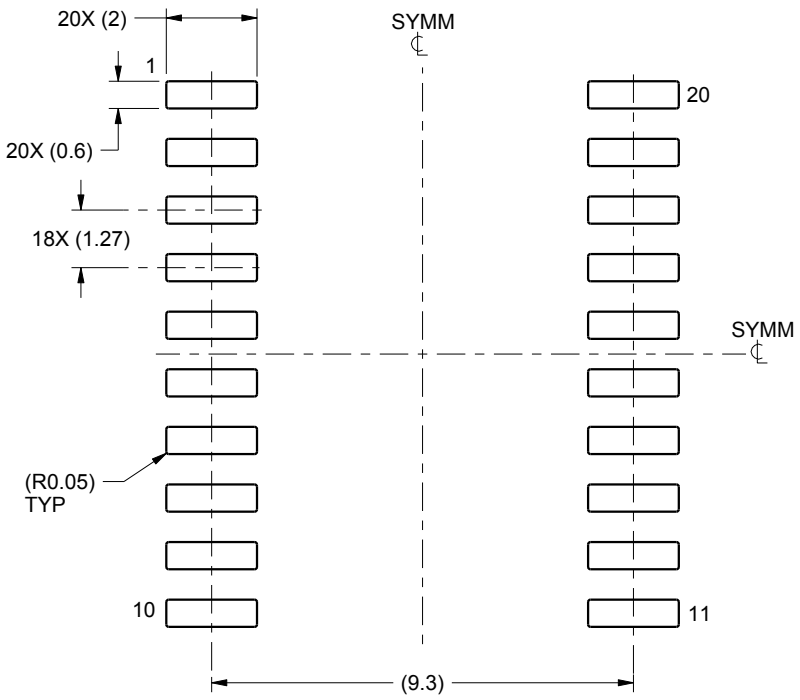
SOIC - 2.65 mm max height

SOIC

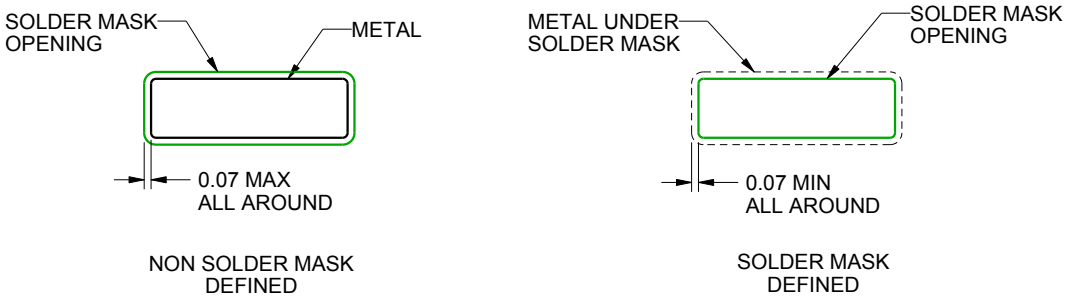


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

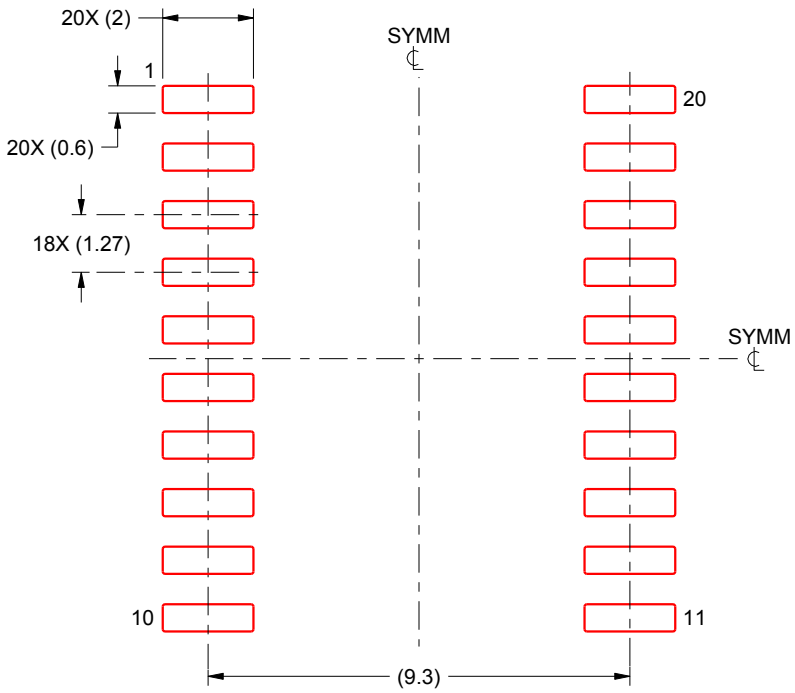


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



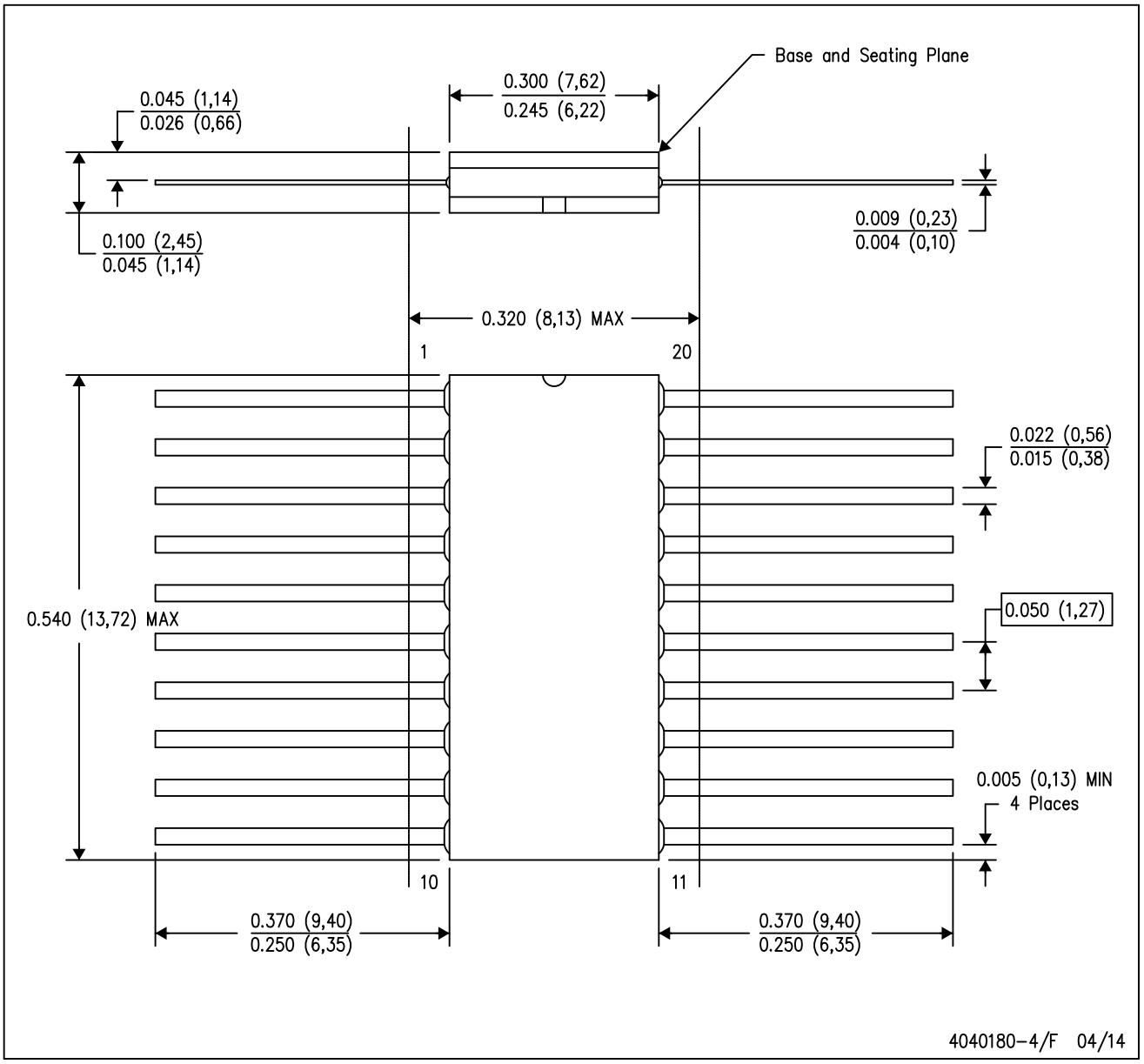
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



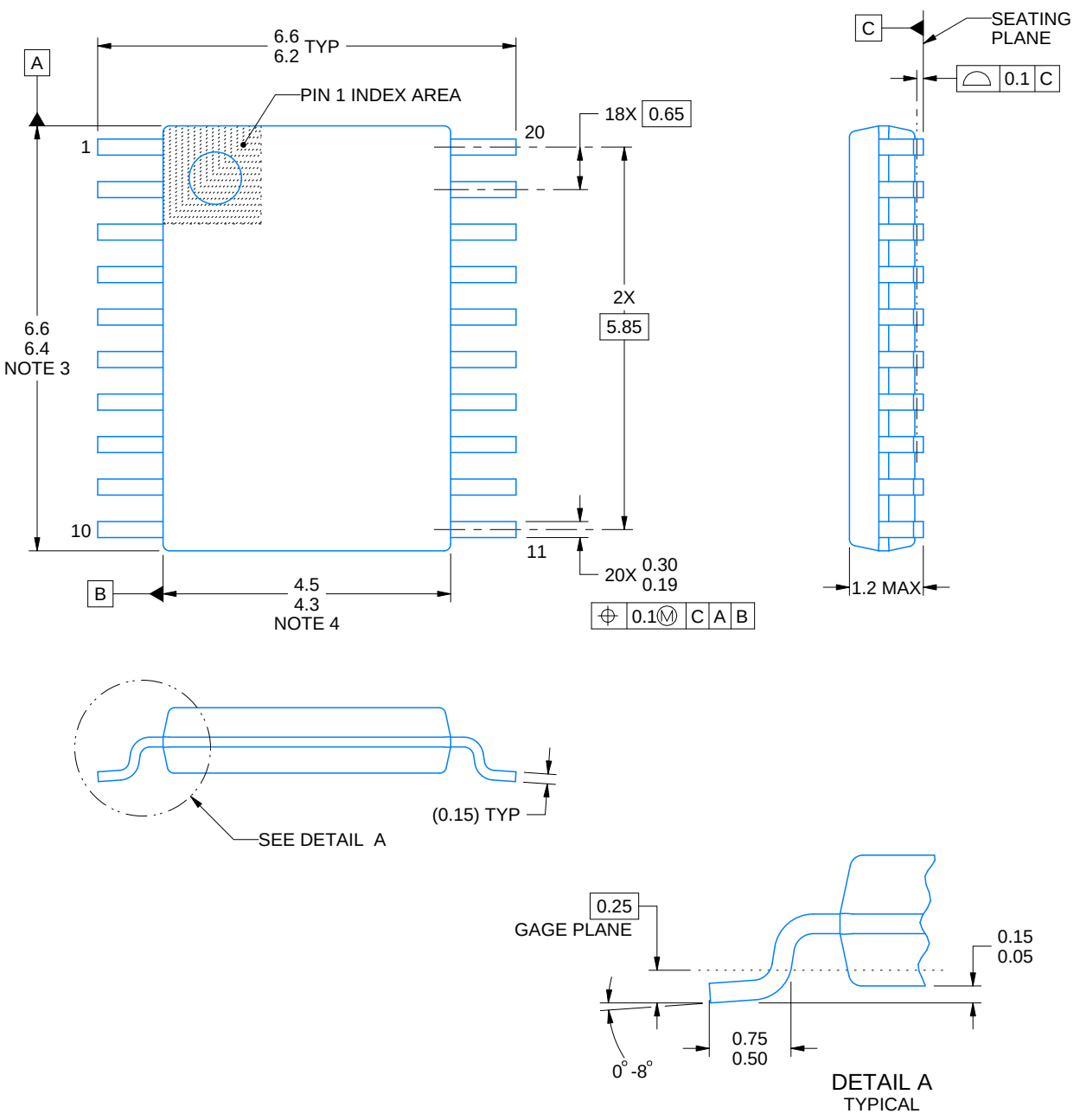
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

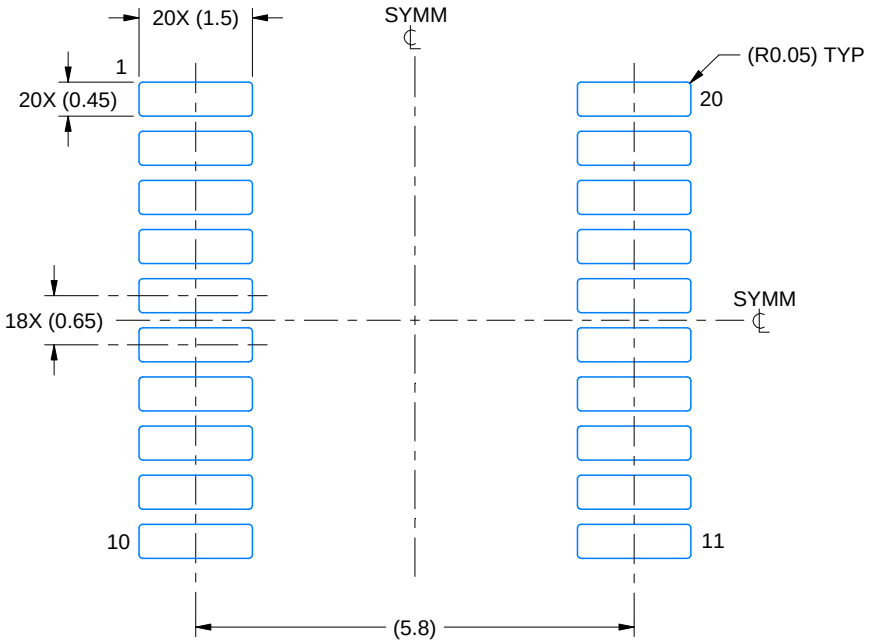
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



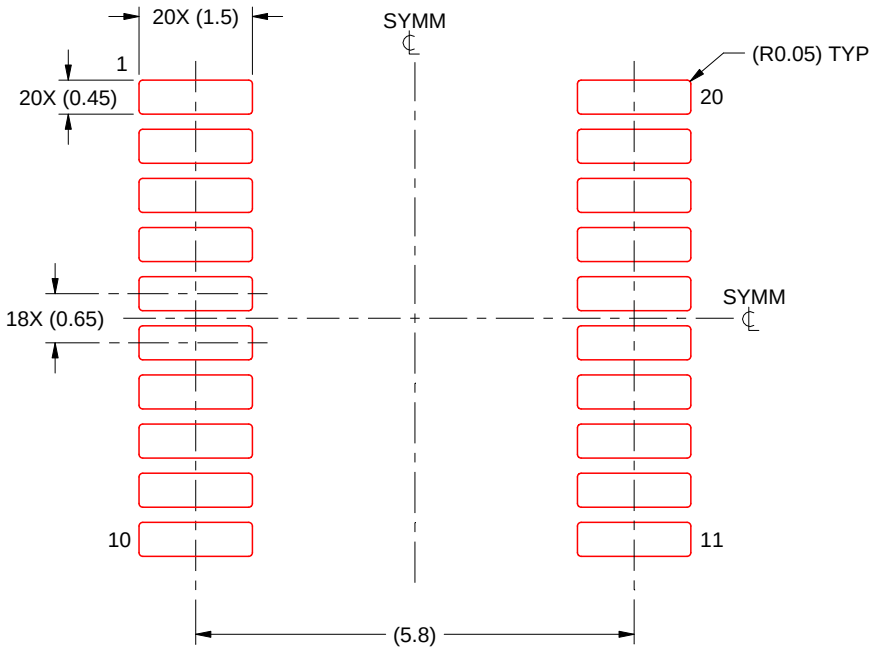
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

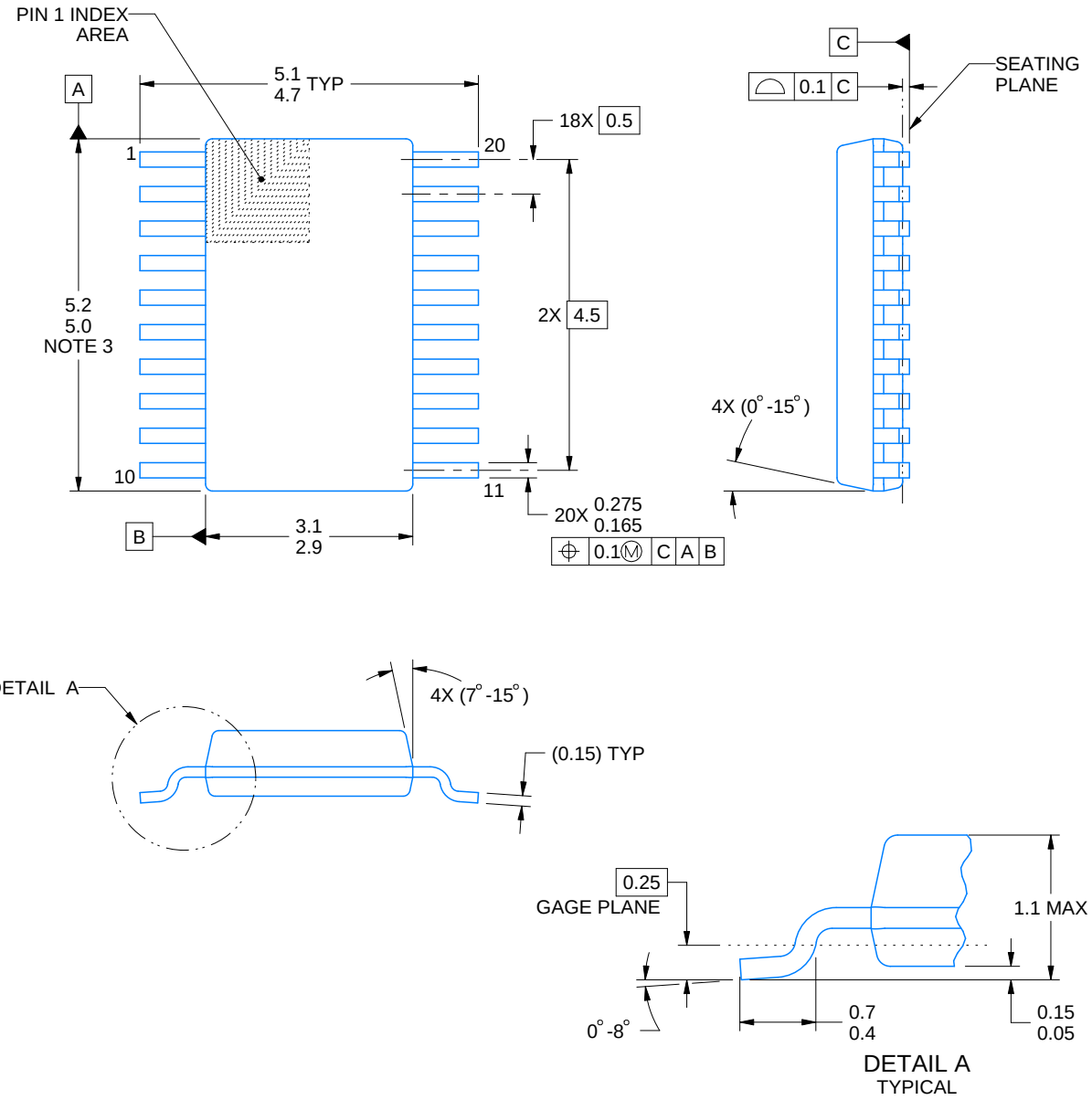
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

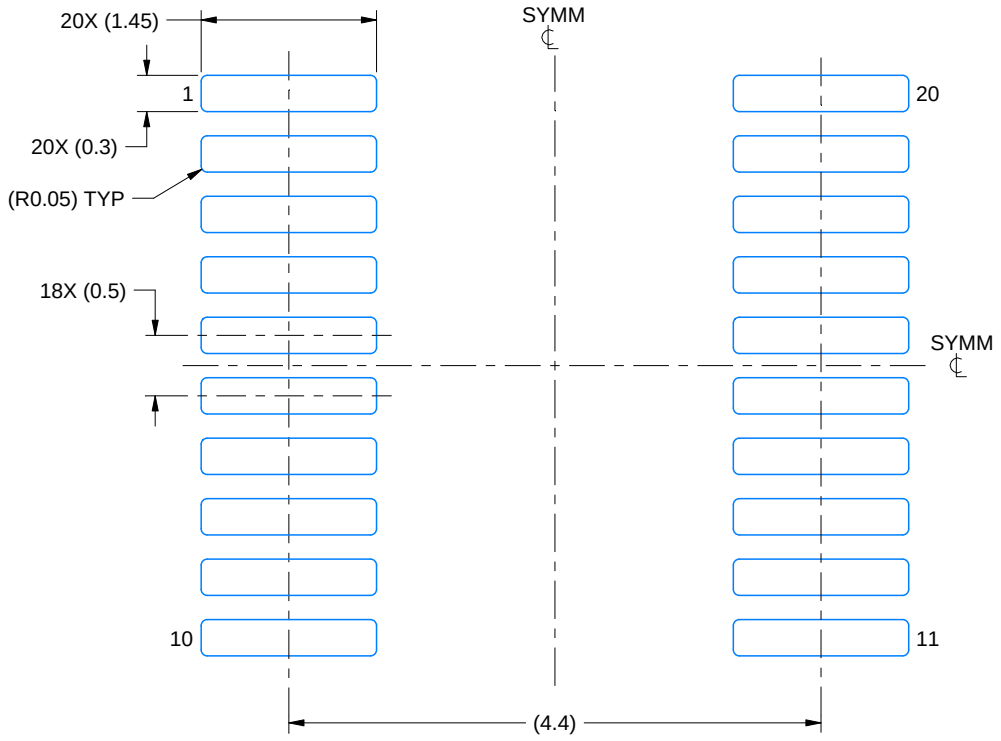
SMALL OUTLINE PACKAGE



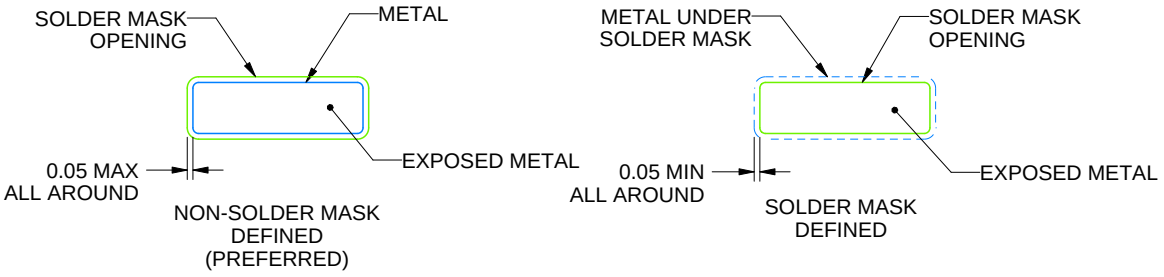
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

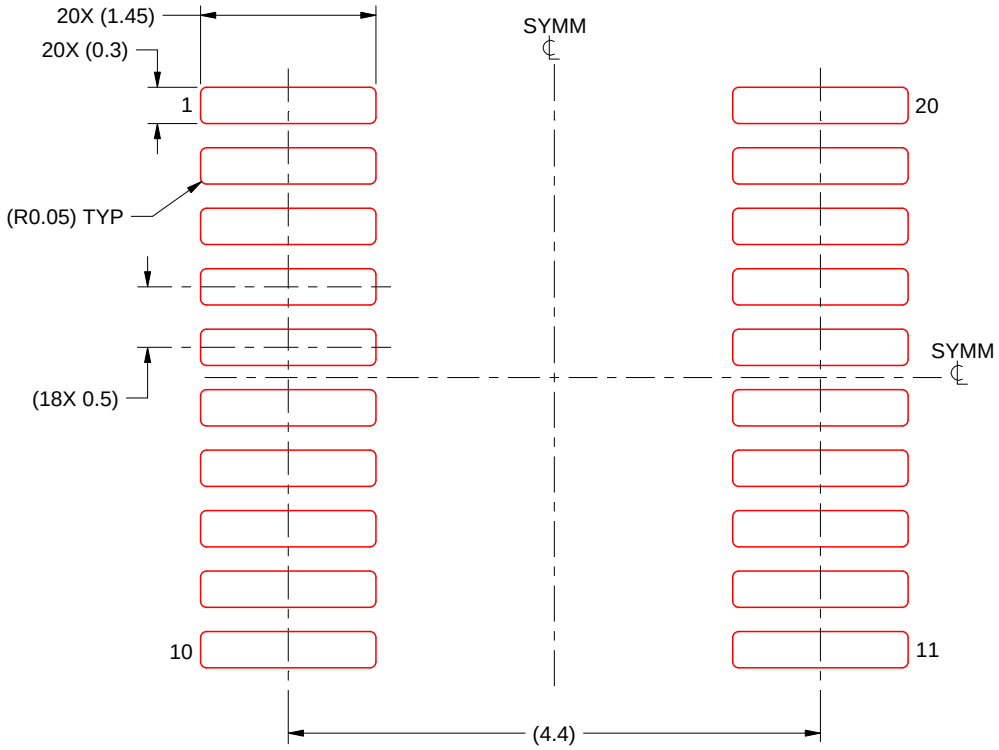


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月