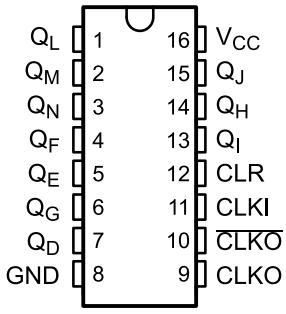
14级异步二进制计数器和振荡器

查询样品: SN74HC4060-Q1

特性

- 符合汽车应用要求
- **2V**至**6V**的宽运行电压范围
- 输出可驱动多达**10**个低功耗肖特基晶体管逻辑电路**(LSTTL)**负载
- 低功耗，I_{CC}最大**80μA**
- t_{pd}典型值 **= 14 ns**
- **±4mA** 输出驱动 （在 **5V** 时）
- 低输出电流，最大值**1 μA**
- 实现相移振荡电路**(RC)-**或者晶体振荡器电路的设计

SN74HC4060-Q1（**D** 封装）
(顶视图**)**



说明

HC4060-Q1器件包含一个振荡器部分和14个纹波进位二进制计数器级。 此振荡器配置可实现RC-或者晶体振荡器电路设计。 时钟(CLKI)输入上的高到低转换增加了计数器的值。 清除(CLR)输入上的高电平会关闭振荡器（$\overline{\text{CLKO}}$变为高电平而CLKO变为低电平）并且将计数器复位清零（所有的Q输出为低电平）。

订购信息

T_A	封装(1)		可订购部件号	正面标记
－40°C 至 125°C	小尺寸集成电路(SOIC) - D	2500 卷带	SN74HC4060QDRQ1	HC4060Q

(1) 封装图示，标准包装数量，散热数据，符号以及 PCB 设计指南： 。

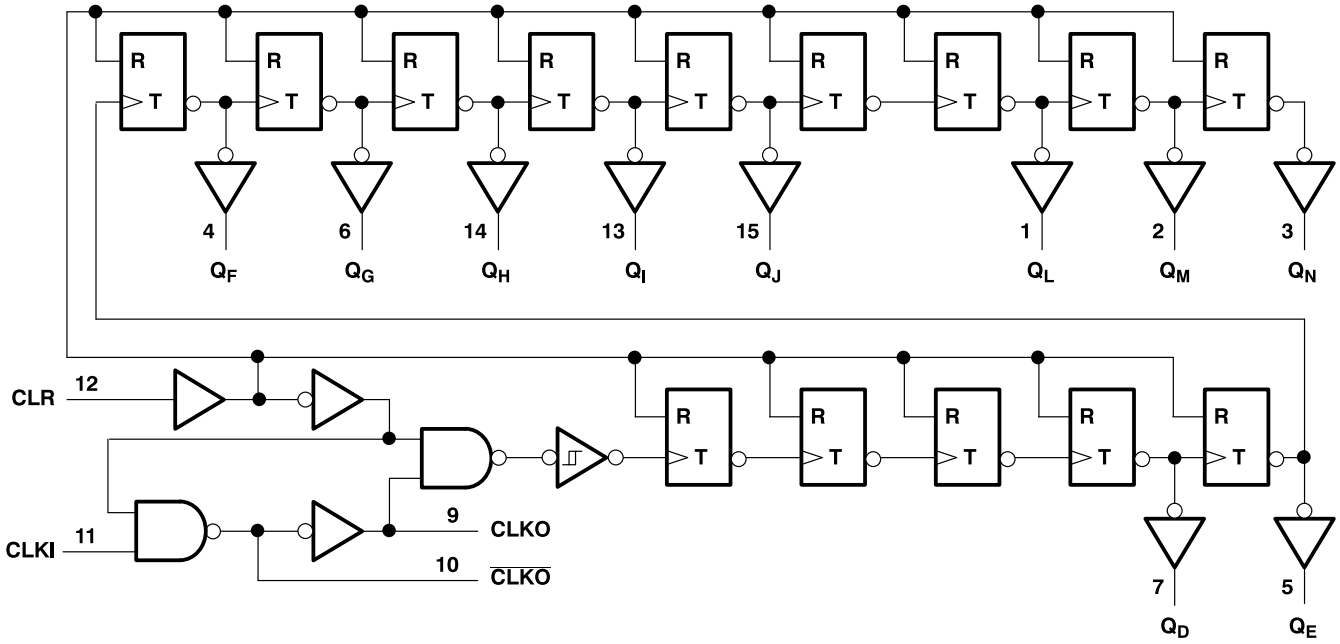
PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. FUNCTION TABLE (each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D package.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_{CC}	Supply voltage range		–0.5 to 7	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$ (2)	±20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$ (2)	±20	mA
I_O	Continuous output current	$V_O < 0$	±25	mA
θ_{JA}	Package thermal impedance	D package (3)	73	°C/W
T_{stg}	Storage temperature range		65 to 150	°C
	ESD rating:	Human Body Model (HBM)	2000	V
		Charged Device Model (CDM)	1000	V
		Machine Model (MM)	200	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

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RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.5			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Δt/Δv	Input transition rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			'HC4060-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}	All output	V_I = V_{IH} or V_{IL},	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		V
				4.5 V	4.4	4.499		4.4		
				6 V	5.9	5.999		5.9		
	Q outputs	V_I = V_{IH} or V_{IL}	I_{OH} = –4.5 mA	4.5 V	3.98	4.3		3.7		V
			I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		
V_{OL}	All output	V_I = V_{IH} or V_{IL},	I_{OL} = 20 μA	2 V		0.002	0.1		0.1	V
				4.5 V		0.001	0.1		0.1	
				6 V		0.001	0.1		0.1	
	Q outputs	V_I = V_{IH} or V_{IL}	I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4	V
			I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4	
I_I		V_I = V_{CC} or 0		6 V		±0.1	±100		±1000	nA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V			8		160	μA
C_i				2 V to 6 V		3	10		10	pF

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TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		'HC4060-Q1		
				MIN	MAX	MIN	MAX	UNIT
f_{clock}	Clock frequency		2 V		5.5		3.7	MHz
			4.5 V		28		19	
			6 V		33		22	
t_w	Pulse duration	CLKI high or low	2 V	90		135		ns
			4.5 V	18		27		
			6 V	15		23		
		CLR high	2 V	90		135		ns
			4.5 V	18		27		
			6 V	15		23		
t_{su}	Setup time, CLR inactive before CLKI↓		2 V	160		240		ns
			4.5 V	32		48		
			6 V	27		41		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			'HC4060-Q1		
				MIN	TYP	MAX	MIN	MAX	UNIT
f_{max}			2 V	5.5	10		3.7		MHz
			4.5 V	28	45		19		
			6 V	33	53		22		
t_{pd}	CLKI	QD	2 V		240	490		735	ns
			4.5 V		58	98		147	
			6 V		42	83		125	
t_{PHL}	CLR	Any Q	2 V		66	140		210	ns
			4.5 V		18	28		42	
			6 V		14	24		36	
t_t		Any	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	30		19	

OPERATING CHARACTERISTICS, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	88	pF

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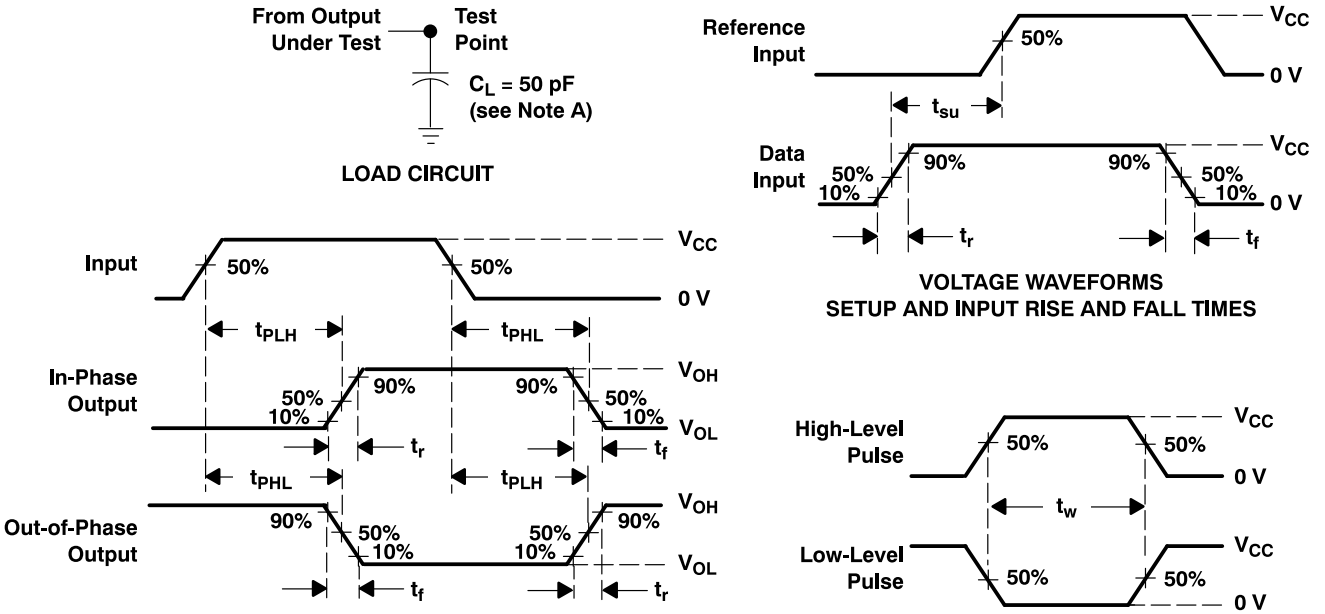
PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

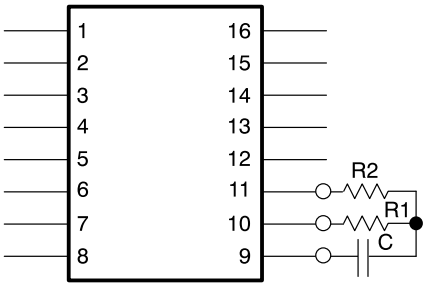
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

CONNECTING AN RC-OSCILLATOR CIRCUIT TO THE 'HC4060-Q1 DEVICE

The 'HC4060-Q1 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits.

When an RC-oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405\,R2}{R1 + R2} + 0.693\right)}$$

If R2 > > R1 (i.e., R2 = 10R1), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC4060QDRQ1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4060Q
SN74HC4060QDRQ1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4060Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74HC4060-Q1 :

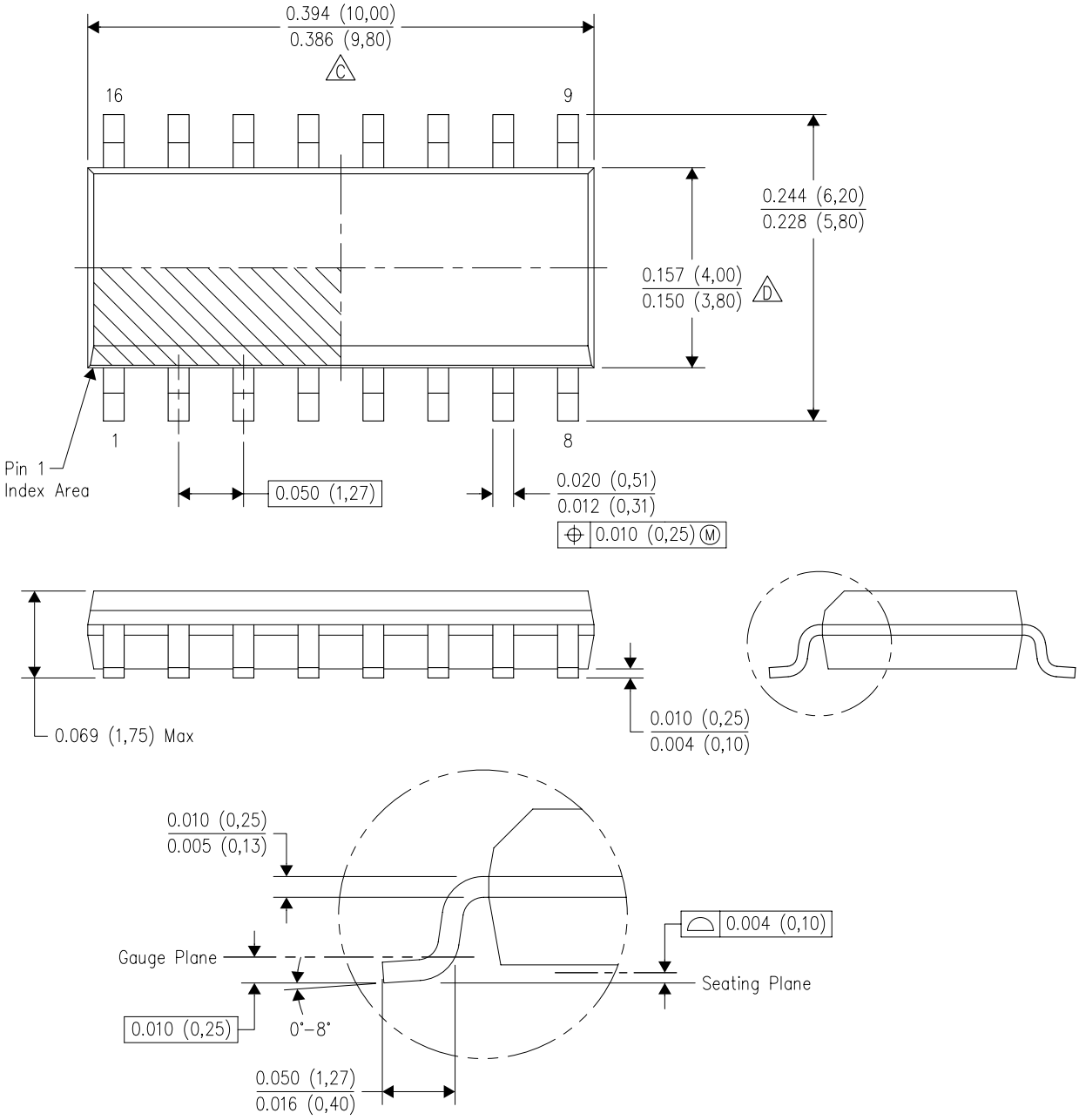
- Catalog : SN74HC4060

- Military : SN54HC4060

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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