# SN74HCS137 具有地址锁存器和施密特触发输入的 3 至 8 线解码器/多路信号分离器

## 1 特性

- 宽工作电压范围：2V 至 6V
- 施密特触发输入可实现慢速或高噪声输入信号
- 低功耗
  - $I_{CC}$ 典型值为 100nA
  - 输入泄漏电流典型值为 ±100nA
- 电压为 6V 时，输出驱动为 ±7.8mA
- 工作环境温度范围：–40°C 至 +125°C，$T_A$

## 2 应用

- 具有共享数据总线的存储器器件选项
- 减少片选应用所需的输出数量
- 路由数据

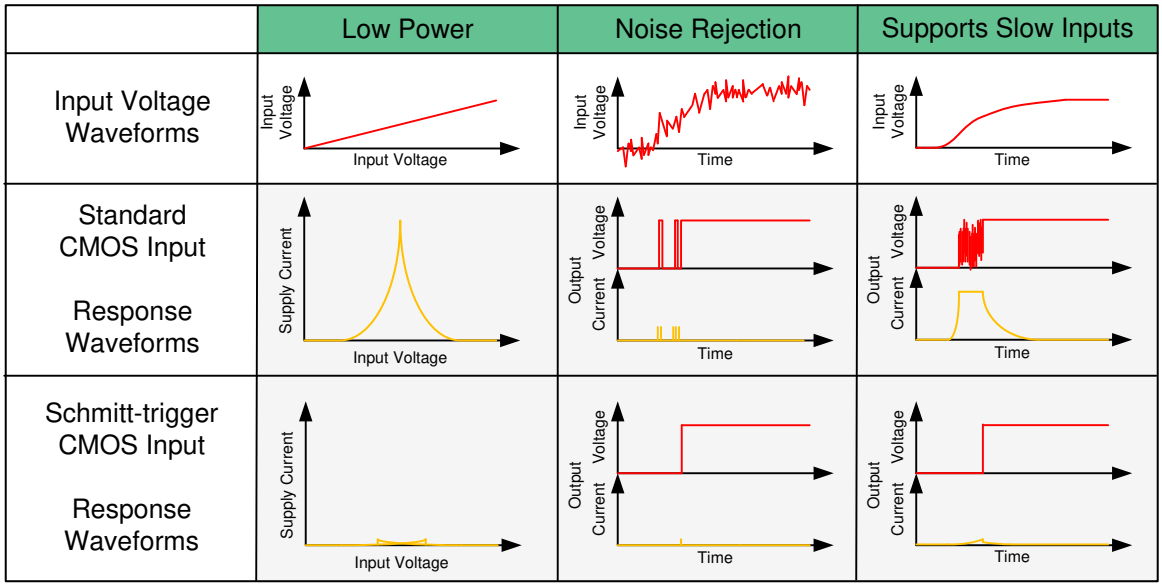
## 3 说明

SN74HCS137 是一款 3 线至 8 线解码器，具有锁存地址输入、一个标准输出选通 ($G_0$) 和一个低电平有效的输出选通 ($\overline{G}_1$)。当锁存使能 ($\overline{LE}$) 输入为低电平时，该器件充当标准 3 线至 8 线解码器。当锁存使能 ($\overline{LE}$) 输入为高电平时，地址锁存器保持其先前的状态。当输出受到任一选通输入控制时，这些输出全都强制进入高电平状态。当其中一个或两个选通输入未禁用输出时，只有选定输出为低电平，而所有其他输出为高电平。

**器件信息**

| 器件型号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| SN74HCS137PW | TSSOP (16) | 5.00mm × 4.40mm |
| SN74HCS137D | SOIC (16) | 9.90mm × 3.90mm |

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。




**施密特触发输入的优势**

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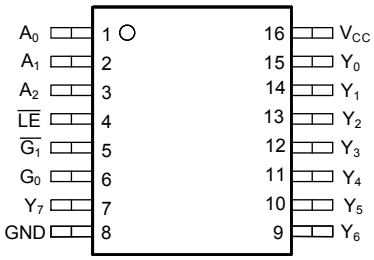
## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (September 2020) to Revision A (May 2021) | Page |
|---|---|
| • 在“说明”部分进行了以下更改。将“该器件充当标准 3 线至 8 线解码器”前面的”高电平”替换为”低电平”。将“地址锁存器保持其先前的状态”前面的”低电平”替换为”高电平”。 | 1 |
| • 为清楚起见，将高电平有效锁存使能引脚名称 (LE) 更改为低电平有效 ($\overline{LE}$)。受影响的部分：引脚排列图、引脚说明、时序特性表、开关特性表、功能方框图、器件功能模式、典型应用、应用曲线和布局示例 | 1 |
| • The following change was made in the overview section. Swapped "high" for "low" before, "the circuit functions as a normal one-of-eight decoder". Swapped "low" for "high" before, "the address latches will maintain their previous states" | 9 |

# 5 Pin Configuration and Functions




**D or PW Package 16-Pin SOIC or TSSOP Top View**

**表 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| SOIC or TSSOP NO. | NAME | | |
| 1 | $A_0$ | I | Address select 0 |
| 2 | $A_1$ | I | Address select 1 |
| 3 | $A_2$ | I | Address select 2 |
| 4 | $\overline{LE}$ | I | Latch enable, active low |
| 5 | $\overline{G}_1$ | I | Strobe input 1, active low |
| 6 | $G_0$ | I | Strobe input 0 |
| 7 | $Y_7$ | O | Output 7 |
| 8 | GND | — | Ground |
| 9 | $Y_6$ | O | Output 6 |
| 10 | $Y_5$ | O | Output 5 |
| 11 | $Y_4$ | O | Output 4 |
| 12 | $Y_3$ | O | Output 3 |
| 13 | $Y_2$ | O | Output 2 |
| 14 | $Y_1$ | O | Output 1 |
| 15 | $Y_0$ | O | Output 0 |
| 16 | $V_{CC}$ | — | Positive supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I$ < –0.5 V or $V_I$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_I$ < –0.5 V or $V_I$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Junction temperature(3) | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2 | 5 | 6 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | V |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74HCS137 | | UNIT |
|---|---|---|---|---|
| | | PW (TSSOP) | D (SOIC) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 141.2 | 122.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 78.8 | 80.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 85.8 | 80.6 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 27.7 | 40.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 85.5 | 80.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive switching threshold | | | 2 V | 0.7 | | 1.5 | V |
| | | | | 4.5 V | 1.7 | | 3.15 | |
| | | | | 6 V | 2.1 | | 4.2 | |
| $V_{T-}$ | Negative switching threshold | | | 2 V | 0.3 | | 1.0 | V |
| | | | | 4.5 V | 0.9 | | 2.2 | |
| | | | | 6 V | 1.2 | | 3.0 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$)(1) | | | 2 V | 0.2 | | 1.0 | V |
| | | | | 4.5 V | 0.4 | | 1.4 | |
| | | | | 6 V | 0.6 | | 1.6 | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 µA | 2 V to 6 V | $V_{CC}$ – 0.1 | $V_{CC}$ – 0.002 | | V |
| | | | $I_{OH}$ = -6 mA | 4.5 V | 4.0 | 4.3 | | |
| | | | $I_{OH}$ = -7.8 mA | 6 V | 5.4 | 5.75 | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V to 6 V | | 0.002 | 0.1 | V |
| | | | $I_{OL}$ = 6 mA | 4.5 V | | 0.18 | 0.30 | |
| | | | $I_{OL}$ = 7.8 mA | 6 V | | 0.22 | 0.33 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or 0 | | 6 V | | ±100 | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | | 6 V | | 0.1 | 2 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | | 5 | pF |

(1) Guaranteed by design.

## 6.6 Timing Characteristics

$C_L$ = 50 pF; over operating free-air temperature range (unless otherwise noted). See Parameter Measurement Information.

| PARAMETER | | | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | 25°C | | – 40°C to 125°C | | |
| | | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{LE}$ pulse width | 2 V | 6 | | 9 | | ns |
| | | | 4.5 V | 5 | | 7 | | |
| | | | 6 V | 5 | | 7 | | |
| $t_{su}$ | Setup time | $A_n$ to $\overline{LE}$ setup time | 2 V | 4 | | 5 | | ns |
| | | | 4.5 V | 3 | | 4 | | |
| | | | 6 V | 3 | | 4 | | |
| $t_h$ | Hold time | $A_n$ to $\overline{LE}$ hold time | 2 V | 4 | | 5 | | ns |
| | | | 4.5 V | 4 | | 5 | | |
| | | | 6 V | 4 | | 5 | | |

## 6.7 Switching Characteristics

$C_L$ = 50 pF; over operating free-air temperature range (unless otherwise noted). See Parameter Measurement Information.

| PARAMETER | | FROM | TO | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | – 40°C to 125°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | $A_n$ | $\overline{Y}$ | 2 V | | 17 | 35 | | | 51 | ns |
| | | | | 4.5 V | | 7 | 14 | | | 20 | |
| | | | | 6 V | | 6 | 12 | | | 17 | |
| | | G or $\overline{G}$ | $\overline{Y}$ | 2 V | | 15 | 30 | | | 48 | |
| | | | | 4.5 V | | 7 | 11 | | | 17 | |
| | | | | 6 V | | 6 | 9 | | | 15 | |
| | | $\overline{LE}$ | $\overline{Y}$ | 2 V | | 18 | 39 | | | 60 | |
| | | | | 4.5 V | | 8 | 16 | | | 24 | |
| | | | | 6 V | | 7 | 15 | | | 21 | |
| $t_t$ | Transition-time | | Any output | 2 V | | | 9 | | | 16 | ns |
| | | | | 4.5 V | | | 5 | | | 9 | |
| | | | | 6 V | | | 4 | | | 8 | |

## 6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | No load | 2 V to 6 V | | 40 | | pF |

## 6.9 Typical Characteristics

$T_A$ = 25°C

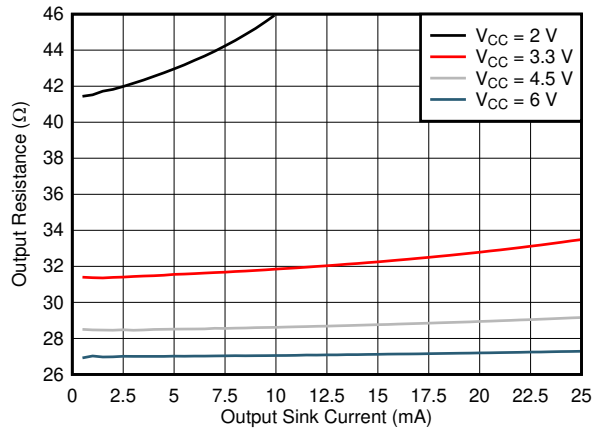



图 6-1. Output driver resistance in LOW state.

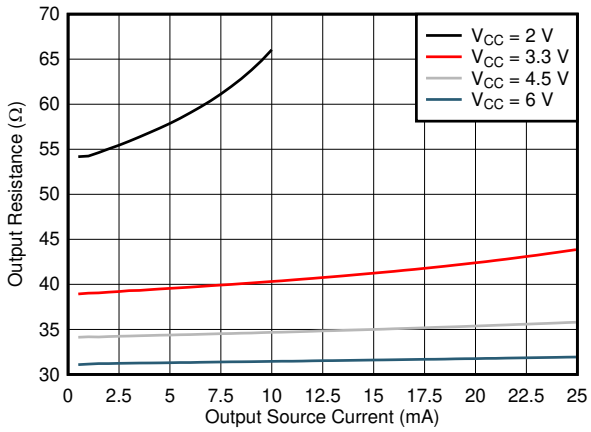



图 6-2. Output driver resistance in HIGH state.

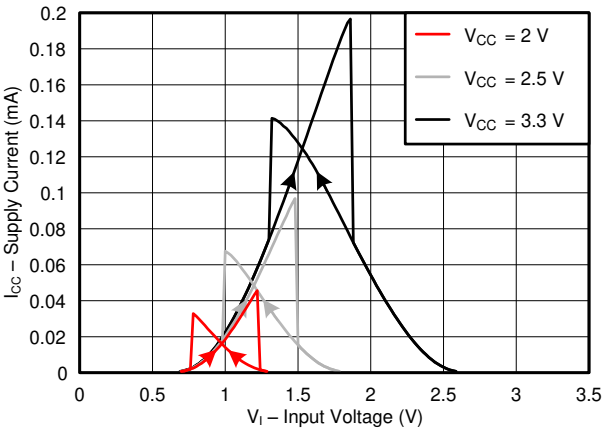



图 6-3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

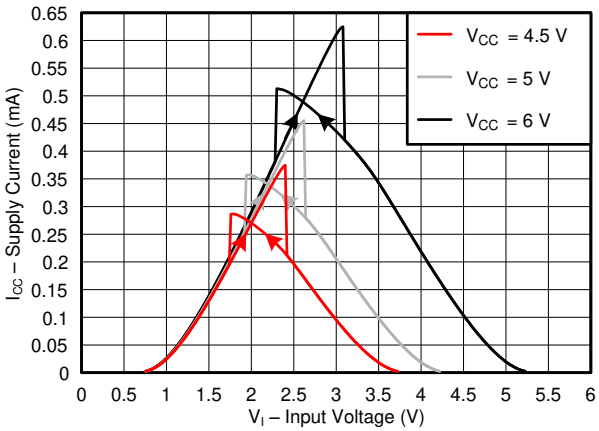


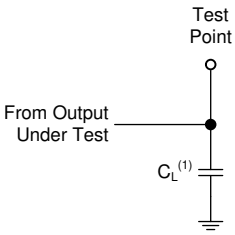

图 6-4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 2.5 ns.

For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.




(1) $C_L$ includes probe and test-fixture capacitance.

**图 7-1. Load Circuit for Push-Pull Outputs**

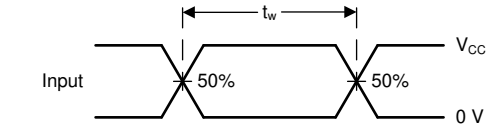



**图 7-2. Voltage Waveforms, Pulse Duration**

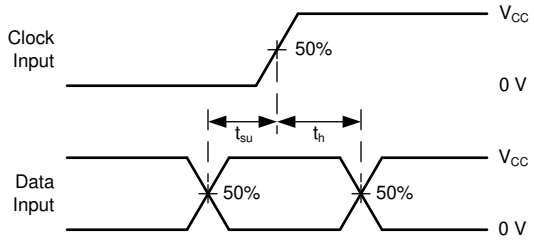
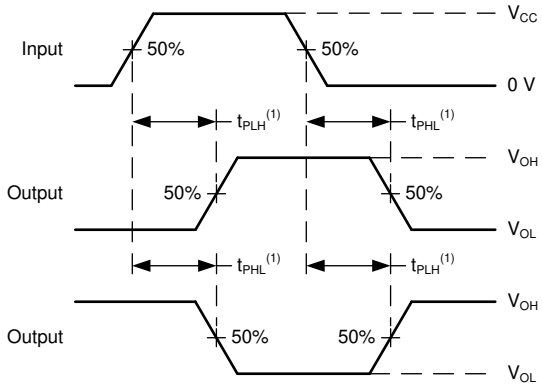
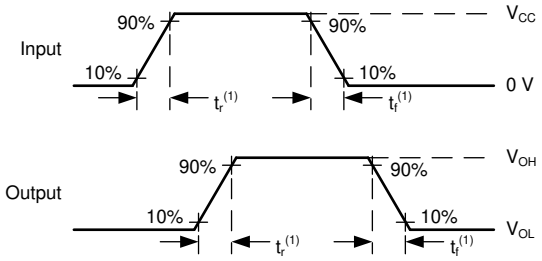



**图 7-3. Voltage Waveforms, Setup and Hold Times**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**图 7-4. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**图 7-5. Voltage Waveforms, Input and Output Transition Times**

# 8 Detailed Description

## 8.1 Overview

The SN74HCS137 is a high speed silicon gate CMOS decoder well suited to memory address decoding or data routing applications. It contains a single 3:8 decoder. All inputs include Schmitt-triggers allowing for slow input transitions and providing additional noise margin.

The SN74HCS137 has three address select inputs ($A_2$, $A_1$, and $A_0$). When the latch enable ($\overline{LE}$) input is low, the circuit functions as a normal one-of-eight decoder. When the latch enable ($\overline{LE}$) input is high, the address latches will maintain their previous states, regardless of any changes at the address select inputs.

Two strobe inputs ($\overline{G}_1$ and $G_0$) are provided to simplify cascading and to facilitate demultiplexing. When any input strobe is active, all outputs are forced into the high state.

The demultiplexing function is accomplished by first using the select inputs to choose the desired output, and then using one of the strobe inputs as the data input.

The outputs for the SN74HCS137 are normally high, and low when selected.

## 8.2 Functional Block Diagram

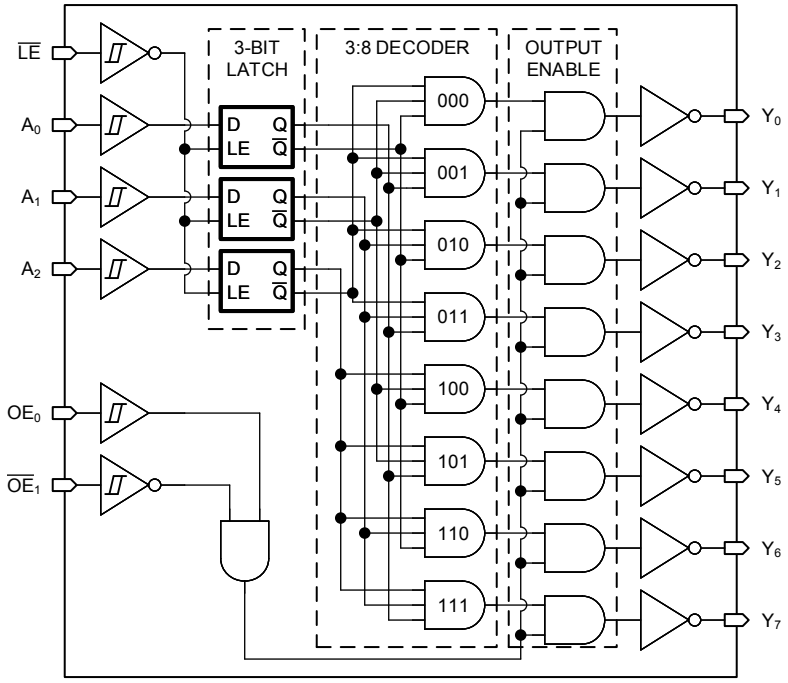



**图 8-1. Logic Diagram (Positive Logic) for the SN74HCS137**

## 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Electrical Placement of Clamping Diodes for Each Input and Output.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

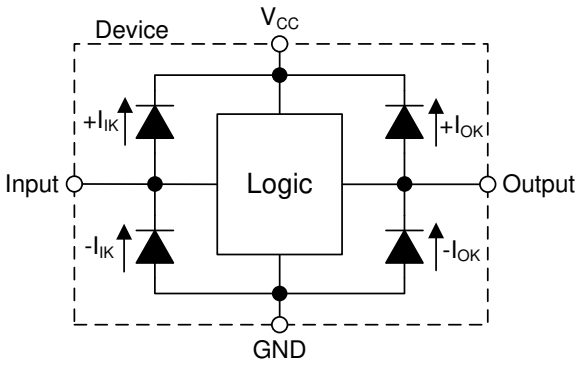



**图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

Function Table lists the functional modes of the SN74HCS137.

**表 8-1. Function Table**

| INPUTS(1) | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{LE}$ | $G_0$ | $\overline{G}_1$ | $A_2$ | $A_1$ | $A_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | Depends upon the address previously applied while $\overline{LE}$ was at a logic low. | | | | | | | |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

# 9 Application and Implementation

**备注**

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

The SN74HCS137 is used to control multiple devices that operate on a shared data bus. A decoder provides the capability to have a binary encoded input activate only one of the device's outputs. This is ideal for solid state memory applications where multiple devices have to be read or written to with a limited number of GPIO pins used on the system controller. The decoder is used to activate the chip select (CS) input to the selected memory device, and the controller can then read or write from that device alone when using a shared bus.

## 9.2 Typical Application

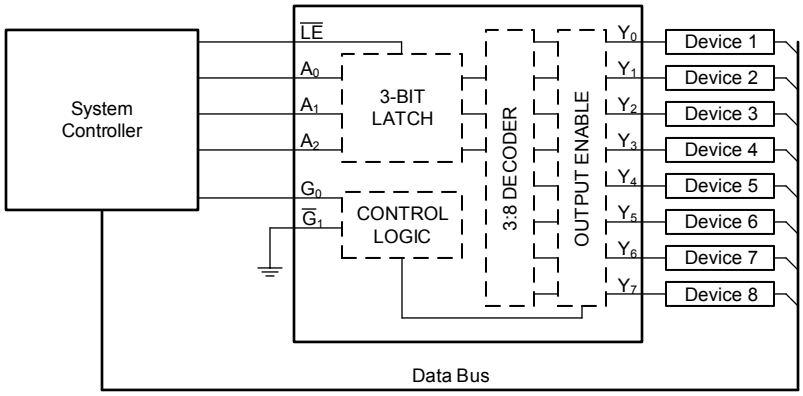



**图 9-1. Typical application block diagram**

### 9.2.1 Design Requirements

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS137 plus the maximum static supply current, $I_{CC}$, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS137 plus the maximum supply current, $I_{CC}$, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS137 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS137 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### *9.2.1.2 Input Considerations*

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS137, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS137 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### *9.2.1.3 Output Considerations*

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq$ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS137 to the receiving device(s).

3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

### 9.2.3 Application Curve

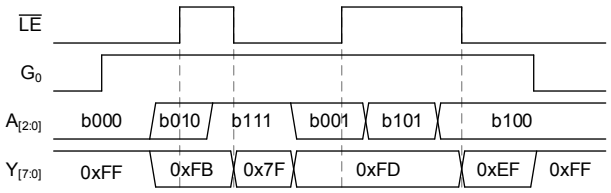



**图 9-2. Application timing diagram**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

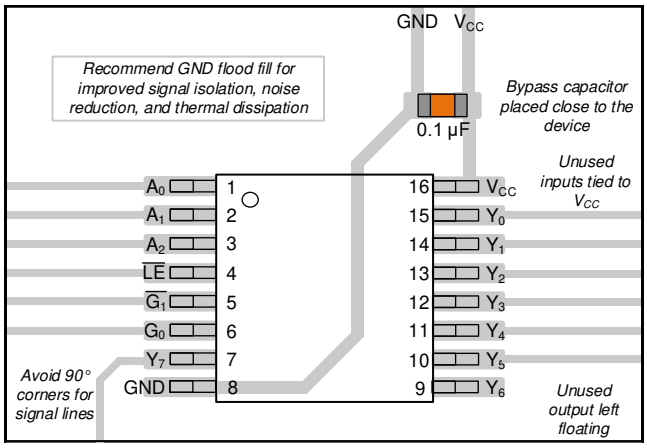



**图 11-1. Example layout for the SN74HCS137 in the PW package.**

# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

## 12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 12.4 Trademarks

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## 12.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCS137DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS137 | Samples |
| SN74HCS137PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS137 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN74HCS137 :**

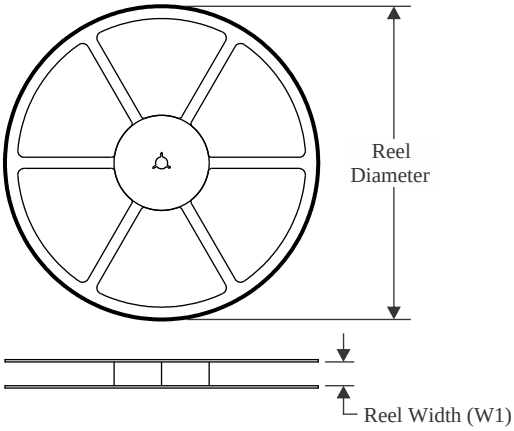
- Automotive : SN74HCS137-Q1

NOTE: Qualified Version Definitions:

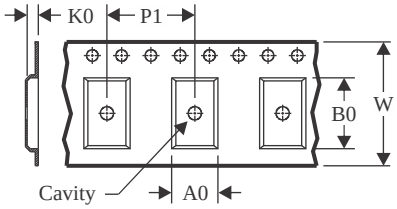
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

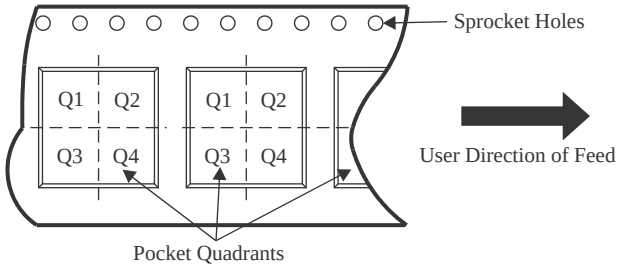



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

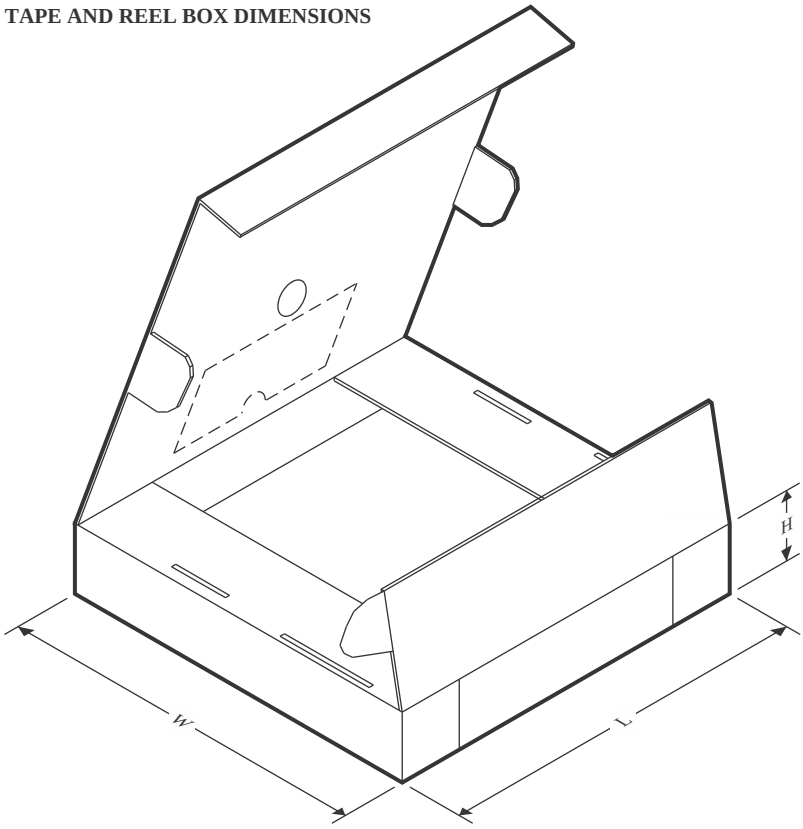
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCS137DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCS137DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCS137PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCS137PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.85 | 5.45 | 1.6 | 8.0 | 12.0 | Q1 |

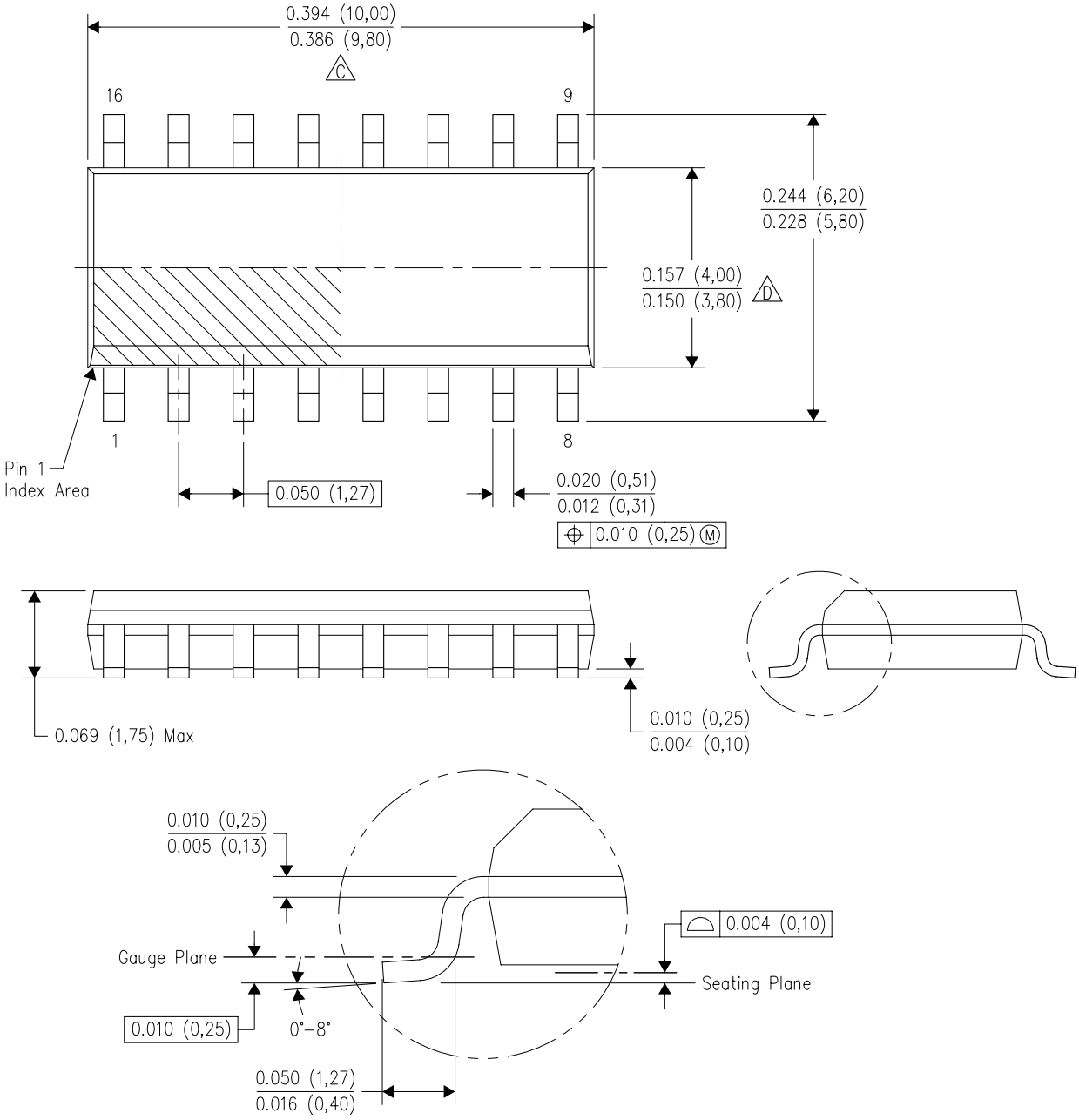
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HCS137DR | SOIC | D | 16 | 2500 | 366.0 | 364.0 | 50.0 |
| SN74HCS137DR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74HCS137PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCS137PWR | TSSOP | PW | 16 | 2000 | 366.0 | 364.0 | 50.0 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



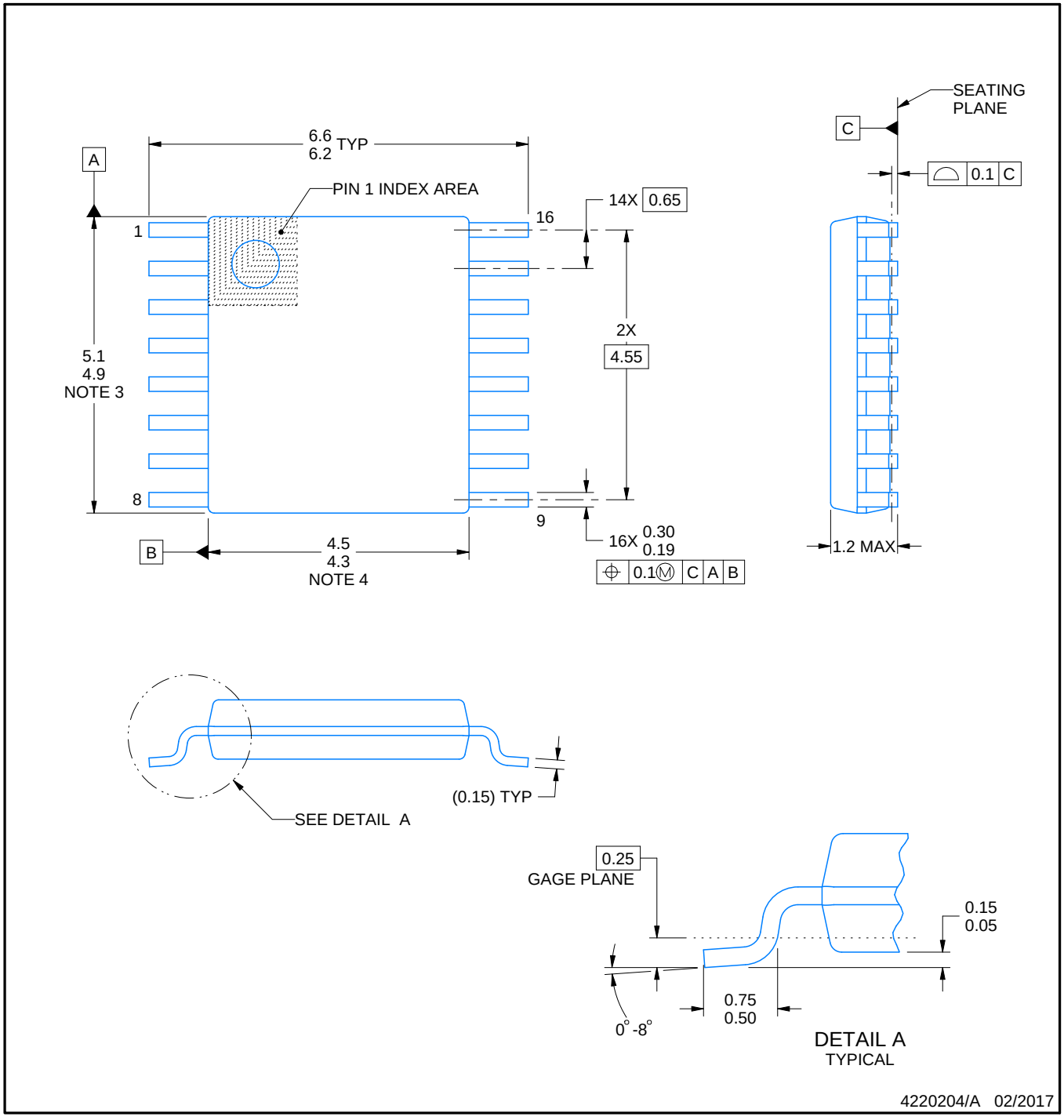

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# PACKAGE OUTLINE

## PW0016A

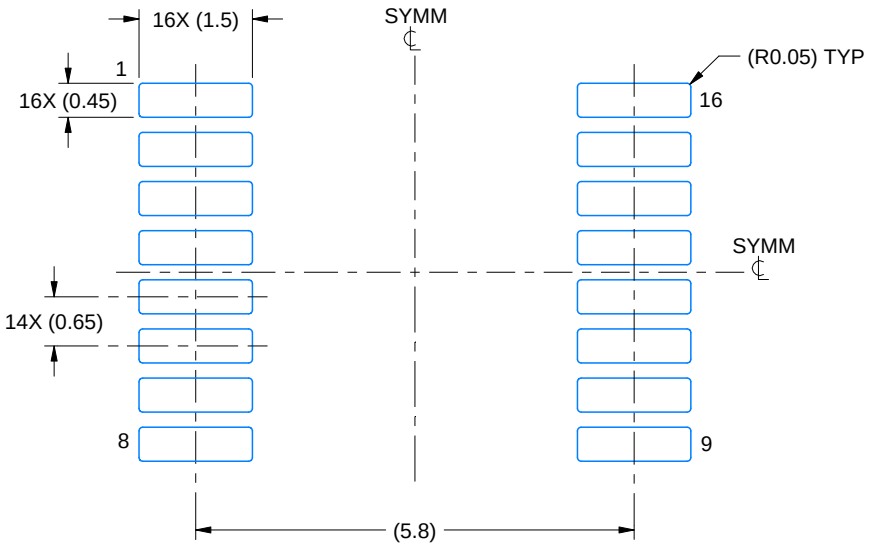
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

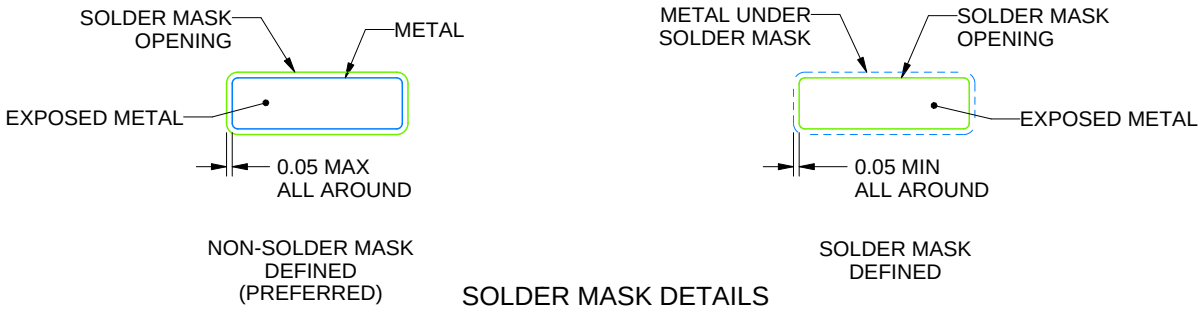



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

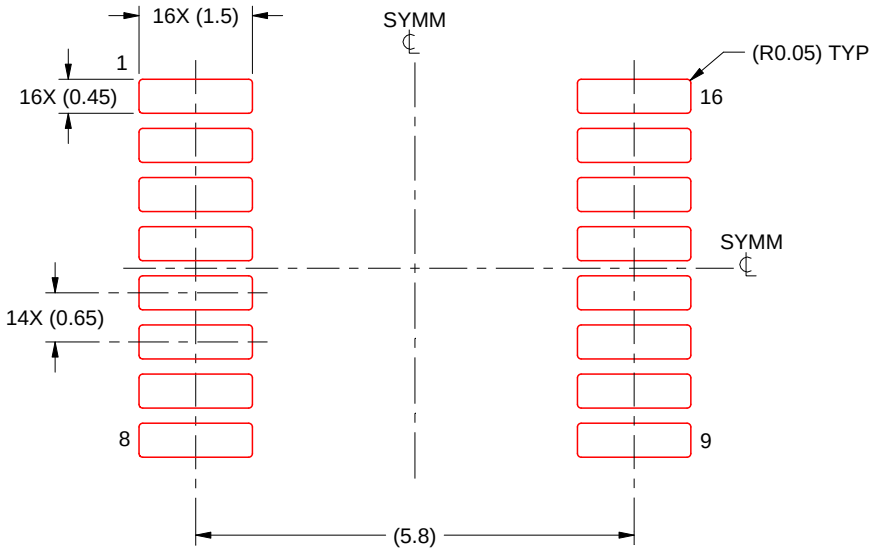



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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