

The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

# SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

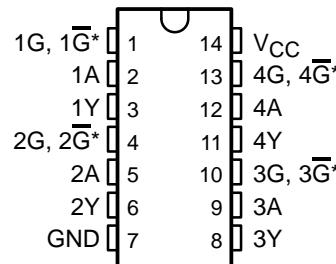
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- Quad Bus Buffers
- 3-State Outputs
- Separate Control for Each Channel

## description

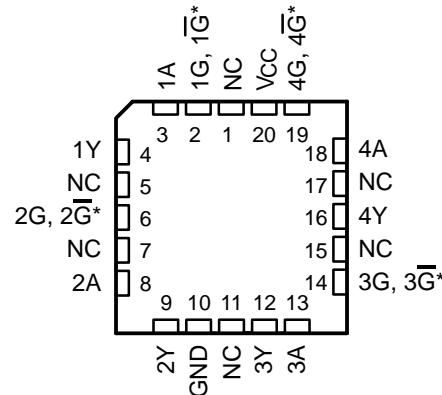
These bus buffers feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pullup resistors. When disabled, both output transistors are turned off, presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The '125 and 'LS125A devices' outputs are disabled when  $\bar{G}$  is high. The '126 and 'LS126A devices' outputs are disabled when G is low.

SN54125, SN54126, SN54LS125A, SN54LS126A . . . J OR W PACKAGE  
SN74125, SN74126 . . . N PACKAGE  
SN74LS125A, SN74LS126A . . . D, N, OR NS PACKAGE  
(TOP VIEW)



\* $\bar{G}$  on '125 and 'LS125A devices;  
G on 126 and 'LS126A devices

SN54LS125A, SN54LS126A . . . FK PACKAGE  
(TOP VIEW)



\* $\bar{G}$  on '125 and 'LS125A devices;  
G on 126 and 'LS126A devices  
NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54125, SN54126, SN54LS125A, SN54LS126A,  
SN74125, SN74126, SN74LS125A, SN74LS126A  
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**

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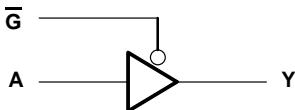
**ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS125AN	SN74LS125AN
		Tube	SN74LS126AN	SN74LS126AN
	SOIC – D	Tube	SN74LS125AD	LS125A
		Tape and reel	SN74LS125ADR	
		Tube	SN74LS126AD	LS126A
		Tape and reel	SN74LS126ADR	
	SOP – NS	Tape and reel	SN74LS125ANSR	74LS125A
		Tape and reel	SN74LS126ANSR	74LS126A
-55°C to 125°C	CDIP – J	Tube	SN54LS125AJ	SN54LS125AJ
		Tube	SNJ54LS125AJ	SNJ54LS125AJ
	CFP – W	Tube	SNJ54LS125AW	SNJ54LS125AW
	LCCC – FK	Tube	SNJ54LS125AFK	SNJ54LS125AFK

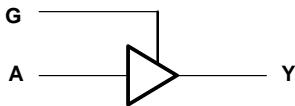
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**logic diagram (each gate)**

'125, 'LS125A



'126, 'LS126A

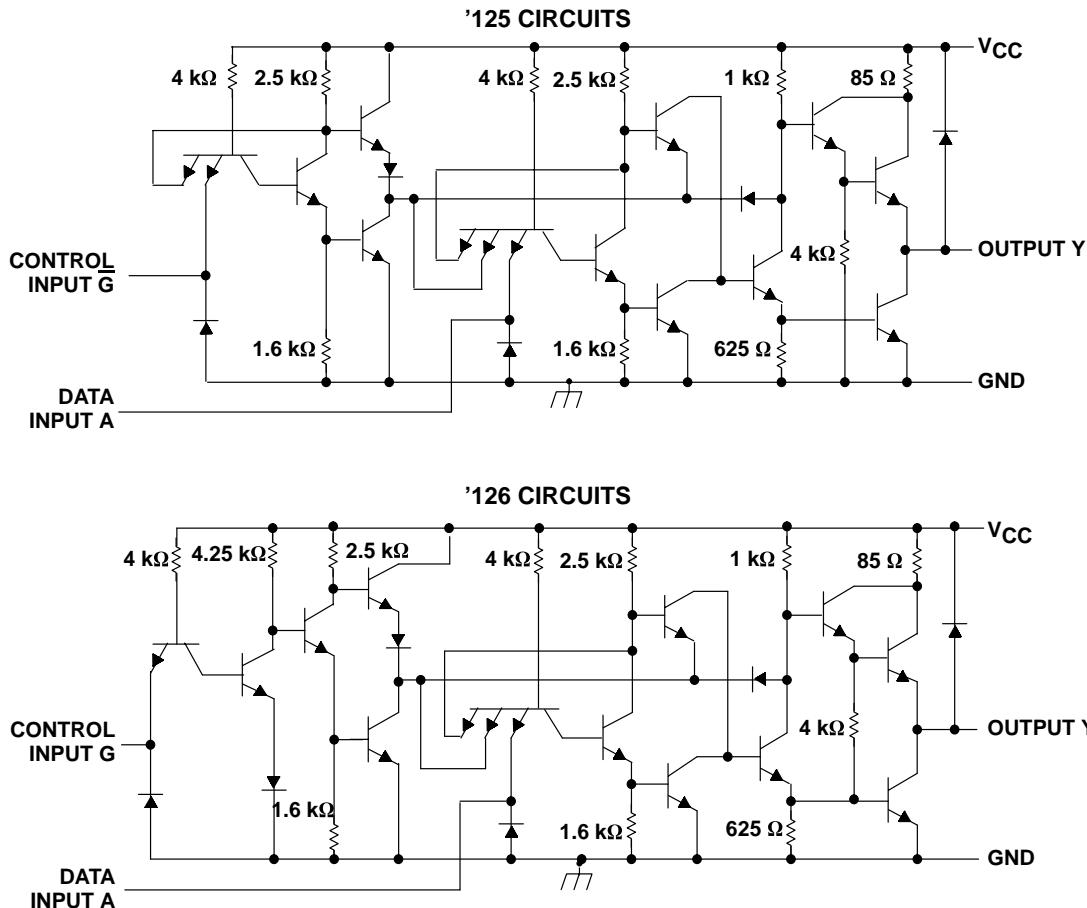


Y = A

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**SN54125, SN54126, SN54LS125A, SN54LS126A,  
SN74125, SN74126, SN74LS125A, SN74LS126A**  
**QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**  
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schematics (each gate)



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**  
('125 and '126)

Supply voltage, V <sub>CC</sub> (see Note 1) .....	7 V
Input voltage, V <sub>I</sub> .....	5.5 V
Package thermal impedance, θ <sub>JA</sub> (see Note 2): N package .....	80°C/W
Storage temperature range, T <sub>stg</sub> .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

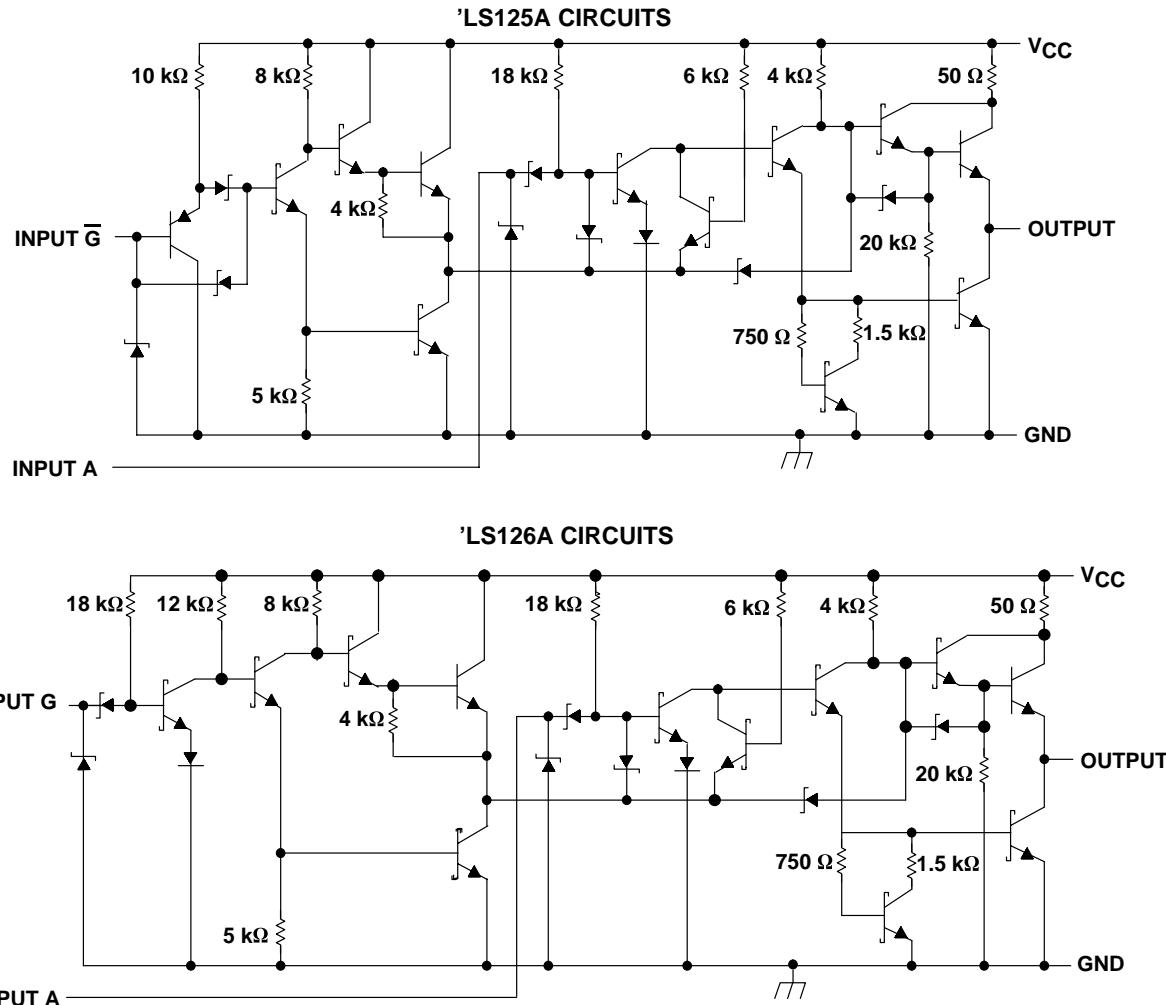
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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**The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.**

## schematics (each gate)



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**  
(**'LS125A** and **'LS126A**)

Supply voltage, $V_{CC}$ (see Note 1) . . . . .	7 V
Input voltage, $V_I$ . . . . .	7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package . . . . .	86°C/W
N package . . . . .	80°C/W
NS package . . . . .	76°C/W
Storage temperature range, $T_{stg}$ . . . . .	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

**SN54125, SN54126, SN54LS125A, SN54LS126A,  
SN74125, SN74126, SN74LS125A, SN74LS126A**  
**QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**  
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**recommended operating conditions**

		SN54125 SN54126			SN74125 SN74126			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-2			-5.2	mA
I <sub>OL</sub>	Low-level output current			16			16	mA
T <sub>A</sub>	Operating free-air temperature	-55	125	0	0	70	°C	

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>			SN54125 SN54126		SN74125 SN74126		UNIT
				MIN	TYP <sup>‡</sup>	MAX	MIN	
V <sub>IK</sub>	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -12 mA			-1.5		-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	I <sub>OH</sub> = -2 mA		2.4	3.3			V
		I <sub>OH</sub> = -5.2 mA				2.4	3.1	
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.8 V,			0.4		V
I <sub>OZ</sub>	V <sub>CC</sub> = MAX V <sub>IL</sub> = 0.8 V	V <sub>IH</sub> = 2 V,	V <sub>O</sub> = 2.4 V		40		40	μA
		V <sub>IL</sub>	V <sub>O</sub> = 0.4 V		-40		-40	
I <sub>I</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 6.5 V			1		1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.4 V			40		40	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V			-1.6		-1.6	mA
I <sub>OS</sub> <sup>§</sup>	V <sub>CC</sub> = MAX			-30	-70	-28	-70	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX (see Note 3)	'125		32	54	32	54	mA
		'126		36	62	36	62	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time.

NOTE 3: Data inputs = 0 V; output control = 4.5 V for '125 and 0 V for '126.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER	TEST CONDITIONS	SN54125 SN74125			SN54126 SN74126			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 50 pF		8	13		8	13	ns
t <sub>PHL</sub>			12	18		12	18	
t <sub>PZH</sub>	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 50 pF		11	17		11	18	ns
t <sub>PZL</sub>			16	25		16	25	
t <sub>PHZ</sub>	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 5 pF		5	8		10	16	ns
t <sub>PLZ</sub>			7	12		12	18	

**SN54125, SN54126, SN54LS125A, SN54LS126A,  
SN74125, SN74126, SN74LS125A, SN74LS126A  
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**

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**recommended operating conditions**

		SN54LS125A SN54LS126A			SN74LS125A SN74LS126A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage		0.7			0.8		V
I <sub>OH</sub>	High-level output current		-1			-2.6		mA
I <sub>OL</sub>	Low-level output current		12			24		mA
T <sub>A</sub>	Operating free-air temperature	-55	125	0	0	70	°C	

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS <sup>†</sup>			SN54LS125A SN54LS126A		SN74LS125A SN74LS126A		UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5				-1.5	V	
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V	V <sub>IL</sub> = 0.7 V, I <sub>OH</sub> = -1 mA	2.4					V	
		V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -2.6 mA				2.4			
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V	V <sub>IL</sub> = 0.7 V, I <sub>OL</sub> = 12 mA	0.25	0.4				V	
		V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 12 mA				0.25	0.4		
		V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 24 mA				0.35	0.5		
I <sub>OZ</sub>	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.7 V	V <sub>O</sub> = 2.4 V	20				μA	
			V <sub>O</sub> = 0.4 V	-20					
		V <sub>IL</sub> = 0.8 V	V <sub>O</sub> = 2.4 V			20			
			V <sub>O</sub> = 0.4 V			-20			
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1			0.1		mA	
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20			20		μA	
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	'LS125A-G inputs	-0.2			-0.2		mA	
		'LS125A-A inputs; 'LS126A All inputs	-0.4			-0.4		mA	
I <sub>OS</sub> <sup>§</sup>	V <sub>CC</sub> = MAX		-40	-225	-40	-225		mA	
I <sub>CC</sub>	V <sub>CC</sub> = MAX (see Note 4)	'LS125A	11	20	11	20		mA	
		'LS126A	12	22	12	22			

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 4: Data inputs = 0 V; output control = 4.5 V for 'LS125A and 0 V for 'LS126A.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER		TEST CONDITIONS			SN54LS125A SN74LS125A		SN54LS126A SN74LS126A		UNIT
		MIN	TYP	MAX	MIN	TYP	MAX		
t <sub>PLH</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF		9	15	9	15		ns	
			7	18	8	18			
t <sub>PHL</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF		12	20	16	25		ns	
			15	25	21	35			
t <sub>PZH</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF		20		25			ns	
			20		25				
t <sub>PZL</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF		20		25				
			20		25				
t <sub>PHZ</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF		20		25			ns	
			20		25				
t <sub>PLZ</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF		20		25				
			20		25				

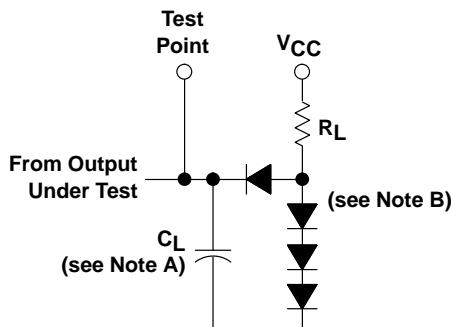


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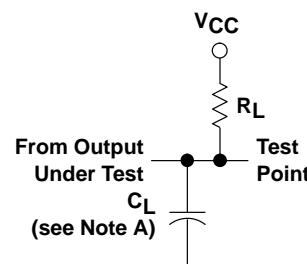
The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

**SN54125, SN54126, SN54LS125A, SN54LS126A,  
SN74125, SN74126, SN74LS125A, SN74LS126A**  
**QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**  
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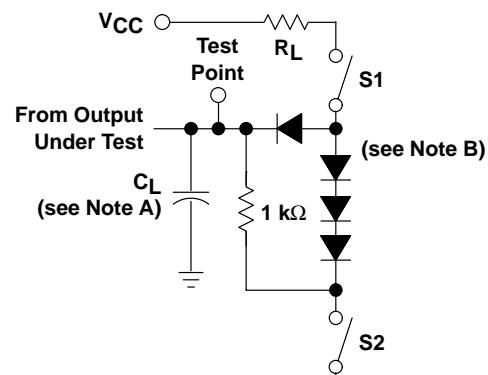
**PARAMETER MEASUREMENT INFORMATION  
SERIES 54/74 DEVICES**



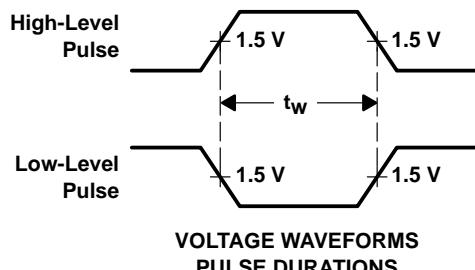
LOAD CIRCUIT  
FOR 2-STATE TOTEM-POLE OUTPUTS



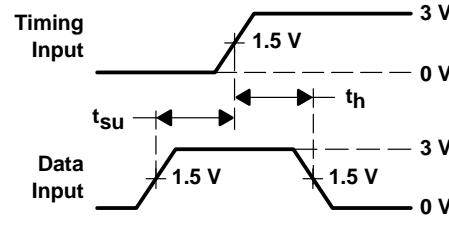
LOAD CIRCUIT  
FOR OPEN-COLLECTOR OUTPUTS



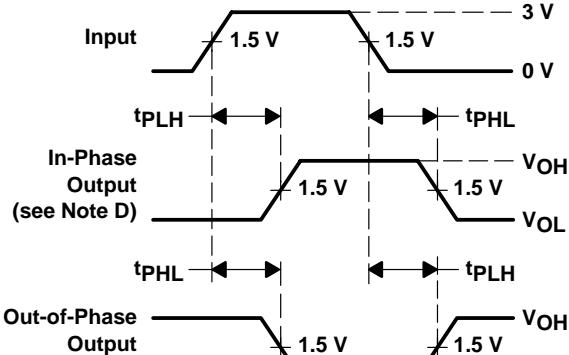
LOAD CIRCUIT  
FOR 3-STATE OUTPUTS



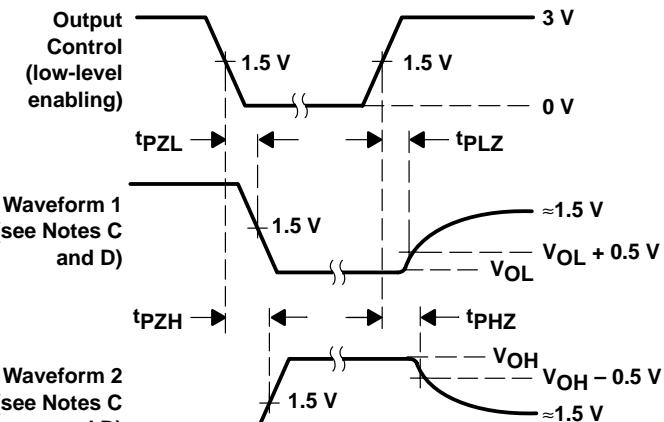
VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N3064 or equivalent.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PZH}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PLZ}$ .  
E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq 7 \text{ ns}$  for Series 54/74 devices and  $t_r$  and  $t_f \leq 2.5 \text{ ns}$  for Series 54S/74S devices.  
F. The outputs are measured one at a time with one input transition per measurement.

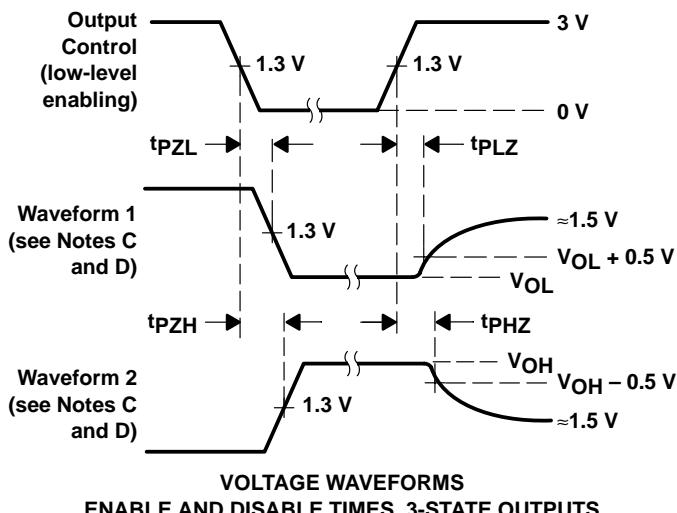
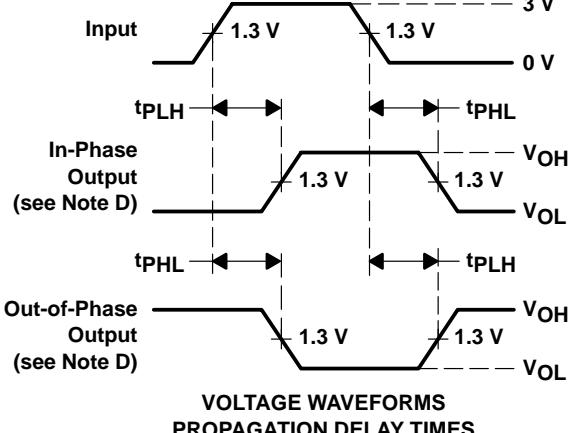
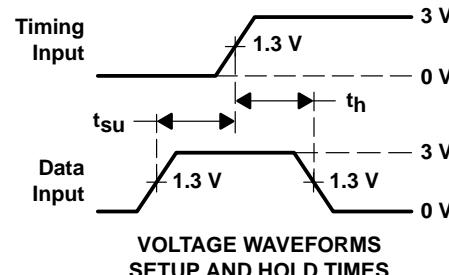
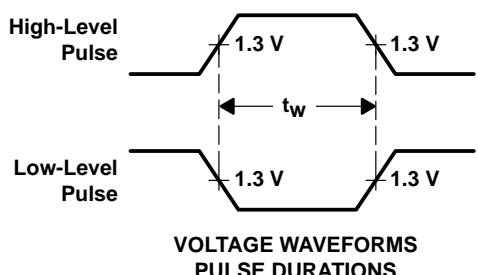
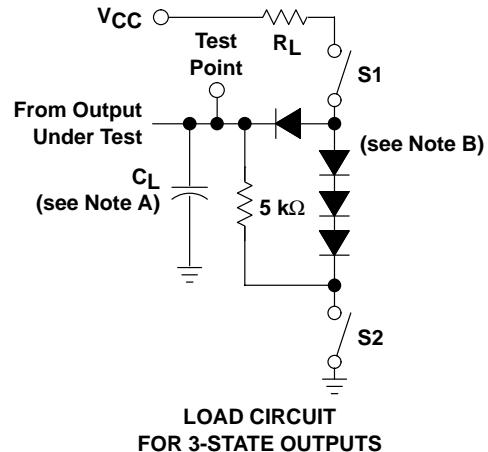
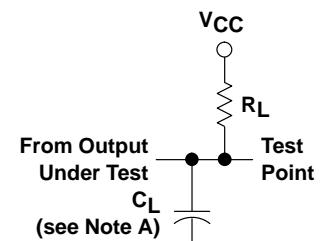
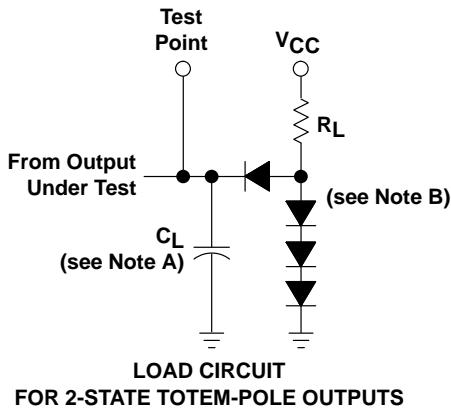
Figure 1. Load Circuits and Voltage Waveforms

**SN54125, SN54126, SN54LS125A, SN54LS126A,  
SN74125, SN74126, SN74LS125A, SN74LS126A  
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54LS/74LS DEVICES**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N3064 or equivalent.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.  
F. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.  
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/32301B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301B2A
JM38510/32301B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301B2A
JM38510/32301BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BCA
JM38510/32301BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BCA
JM38510/32301BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BDA
JM38510/32301BDA.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BDA
M38510/32301B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301B2A
M38510/32301BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BCA
M38510/32301BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 32301BDA
SN54LS125AJ	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS125AJ
SN54LS125AJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS125AJ
SN74LS125AD	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	LS125A
SN74LS125ADBR	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS125A
SN74LS125ADBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS125A
SN74LS125ADR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS125A
SN74LS125ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS125A
SN74LS125ADRE4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS125A
SN74LS125AN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS125AN
SN74LS125AN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS125AN
SN74LS125ANSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS125A
SN74LS125ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS125A
SN74LS126AD	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	LS126A

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LS126ADR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS126A
<a href="#">SN74LS126ADR.A</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS126A
<a href="#">SN74LS126AN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS126AN
<a href="#">SN74LS126AN.A</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS126AN
<a href="#">SN74LS126ANSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS126A
<a href="#">SN74LS126ANSR.A</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS126A
<a href="#">SNJ54LS125AJ</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS125AJ
<a href="#">SNJ54LS125AJ.A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS125AJ
<a href="#">SNJ54LS125AW</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS125AW
<a href="#">SNJ54LS125AW.A</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS125AW

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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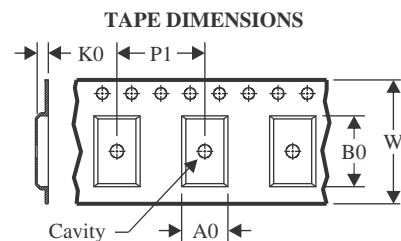
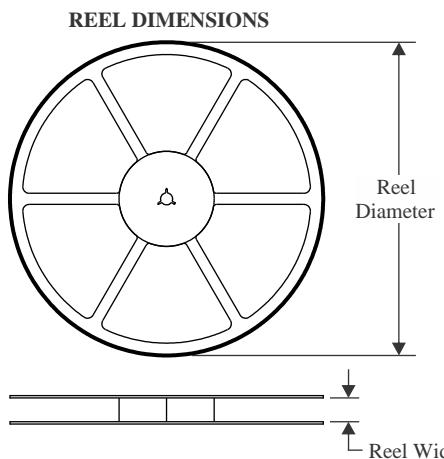
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS125A, SN74LS125A :**

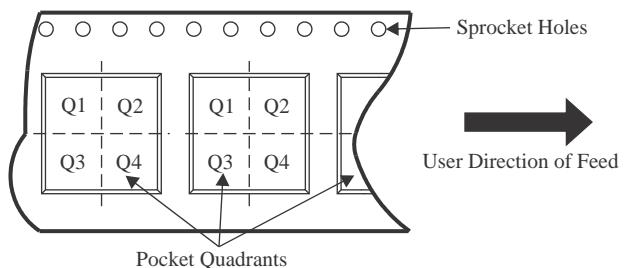
- Catalog : [SN74LS125A](#)
- Military : [SN54LS125A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


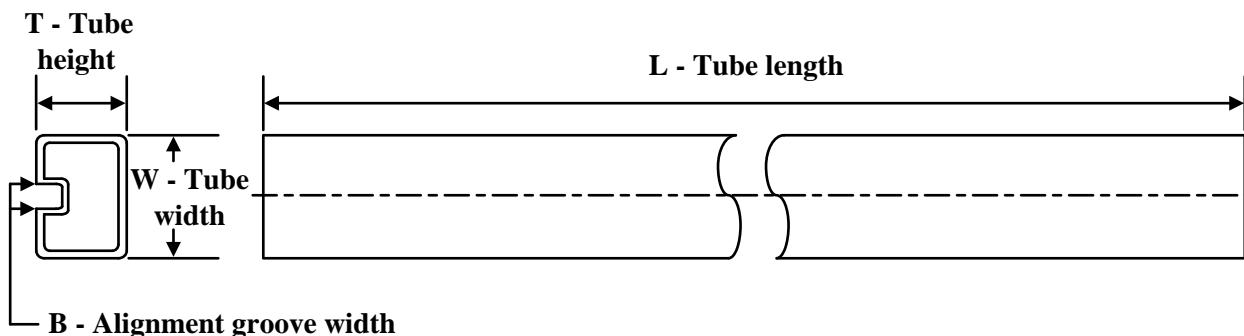
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS125ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS125ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LS126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS126ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS125ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LS125ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LS125ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LS126ADBR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LS126ANSR	SOP	NS	14	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

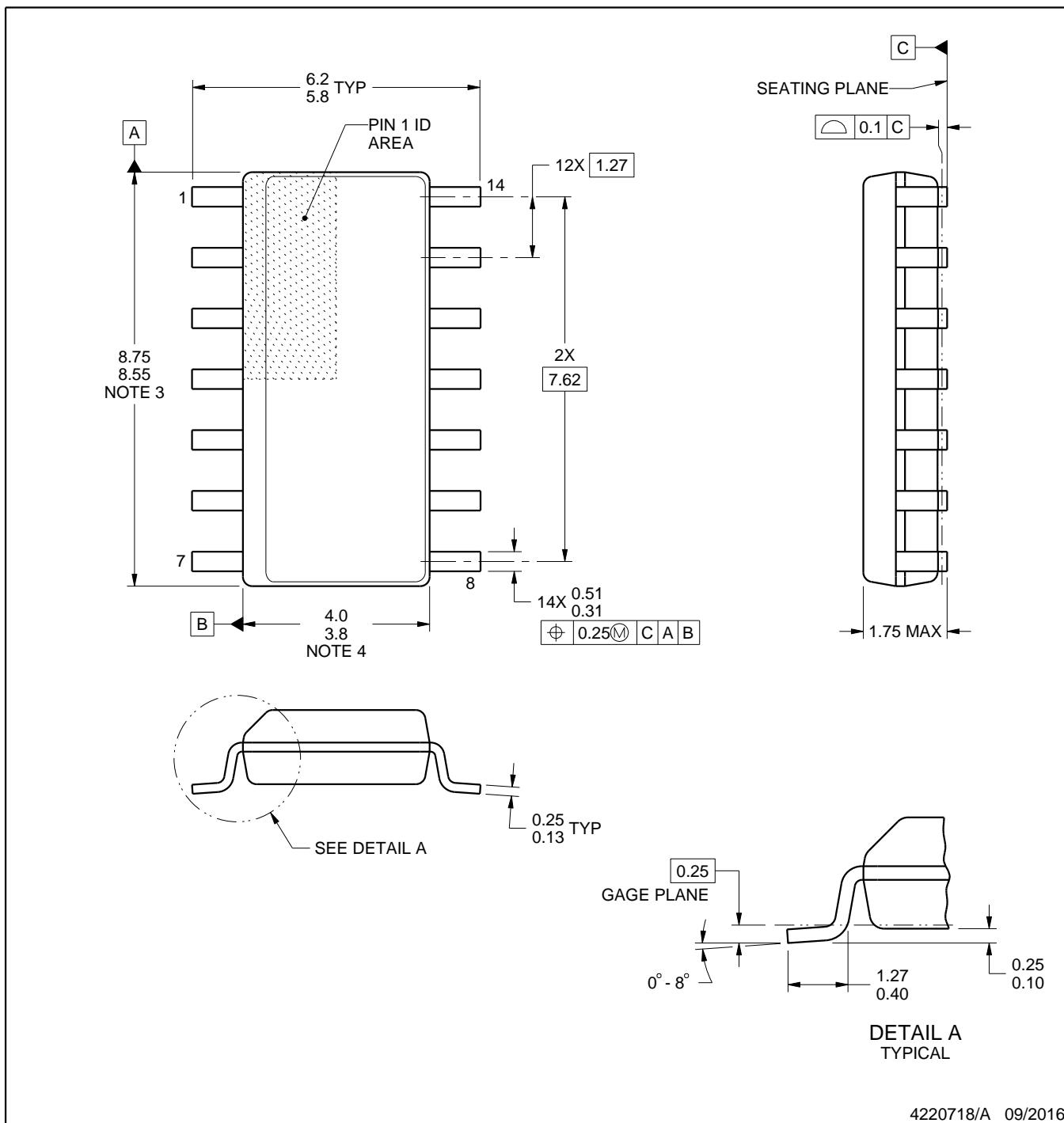
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/32301B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/32301B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/32301BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/32301BDA.A	W	CFP	14	25	506.98	26.16	6220	NA
M38510/32301B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/32301BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS125AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS125AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS126AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS126AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS126AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS126AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS125AW	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS125AW.A	W	CFP	14	25	506.98	26.16	6220	NA

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

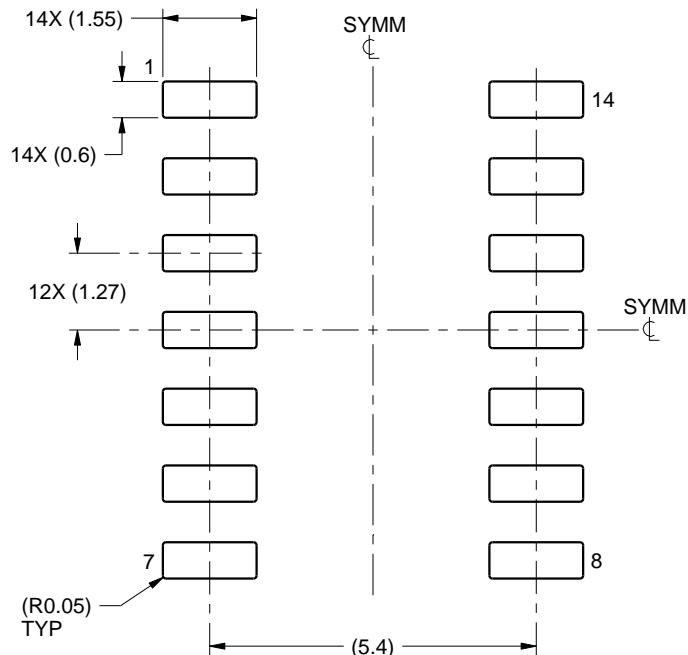
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

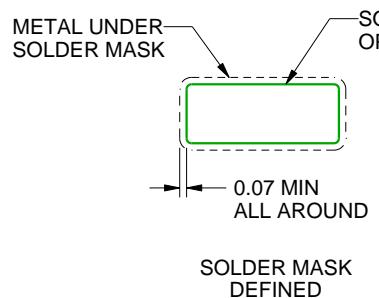
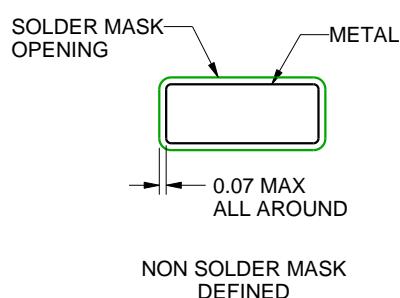
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

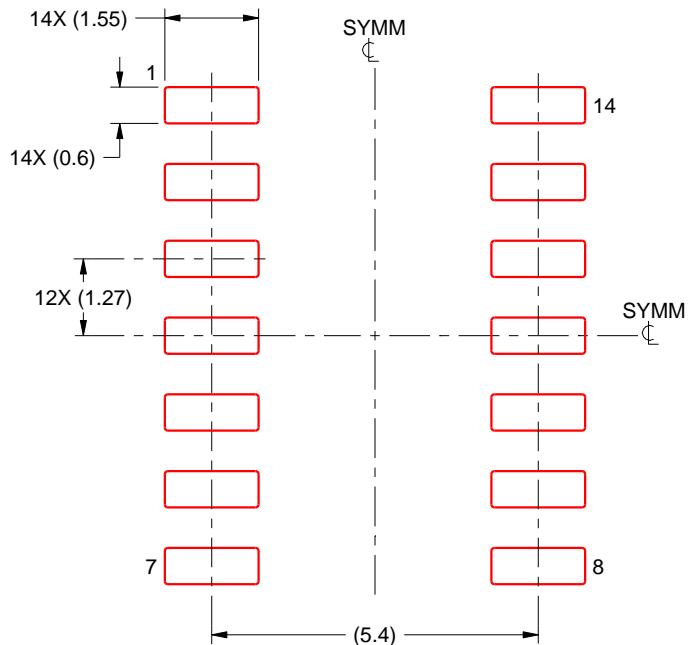
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

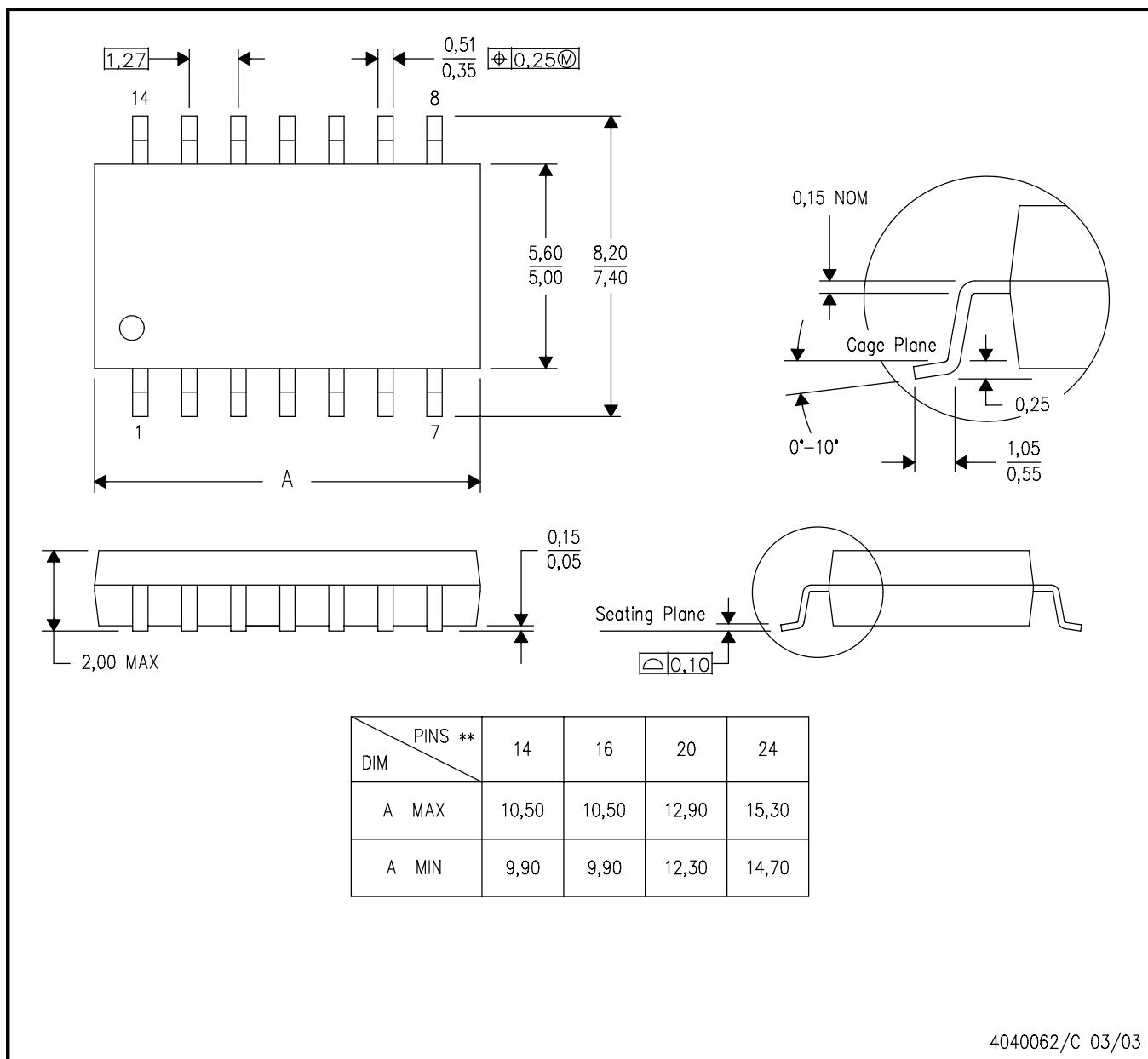
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

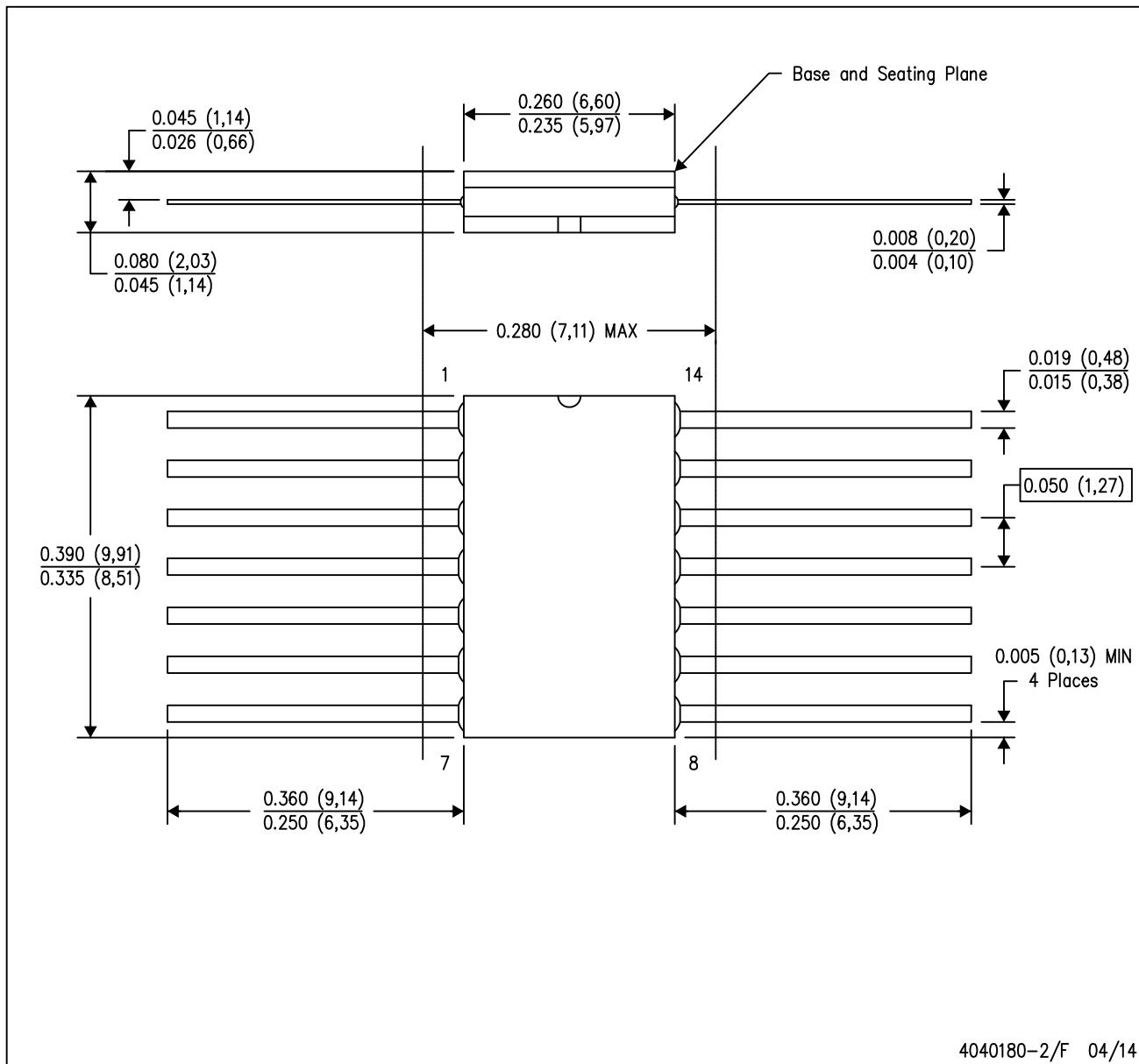


4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

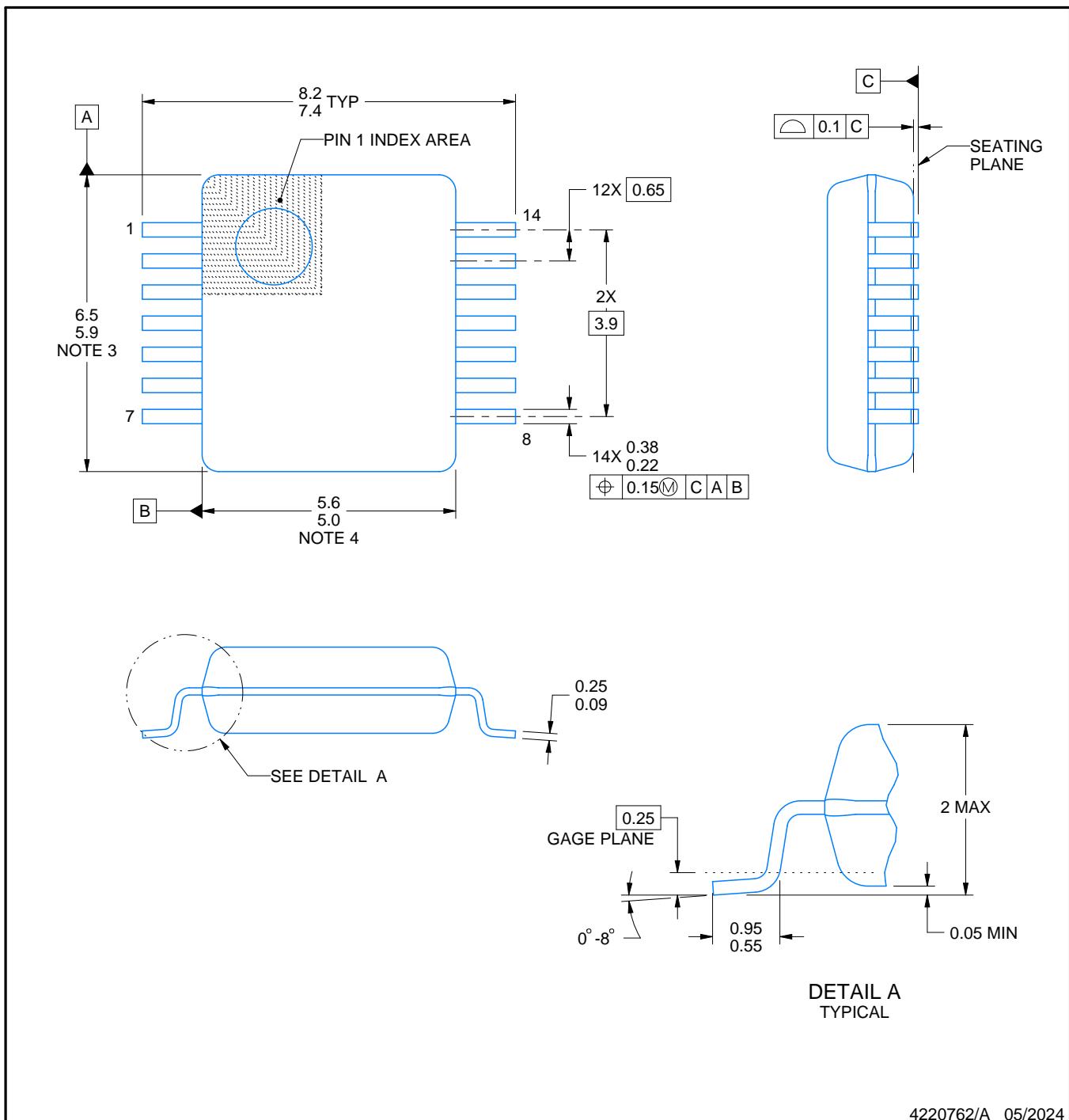
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

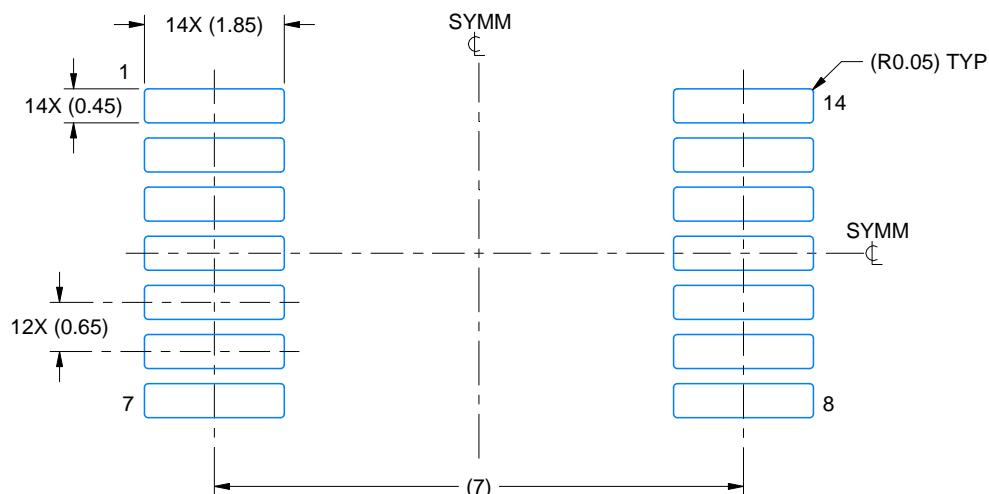
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

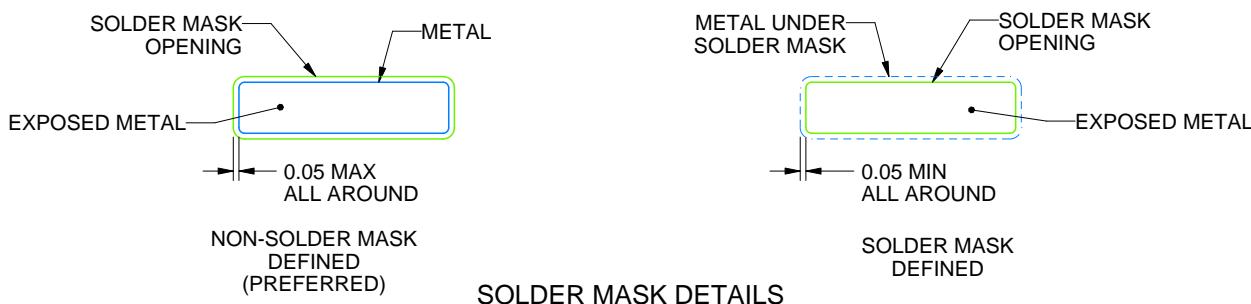
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

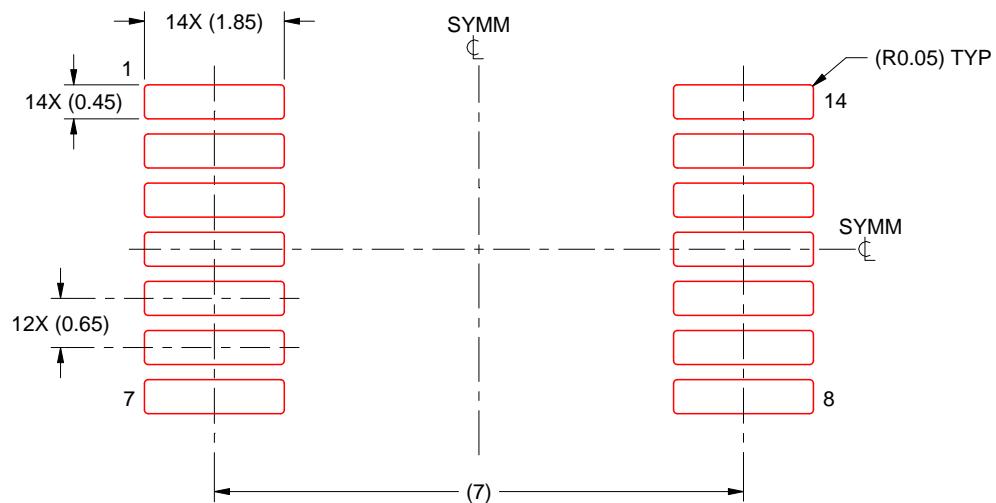
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

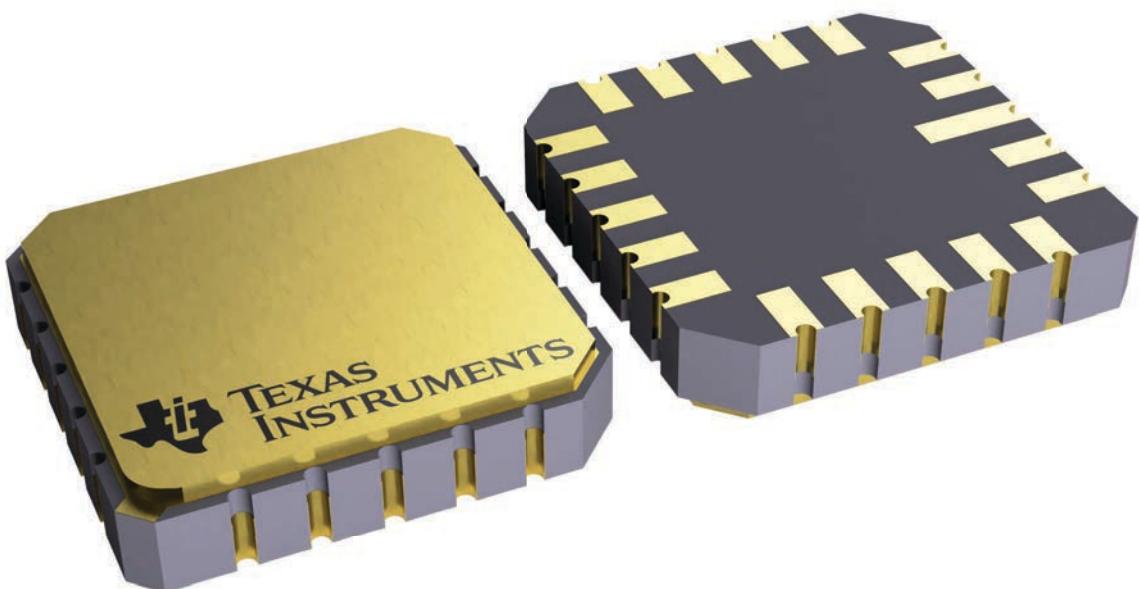
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



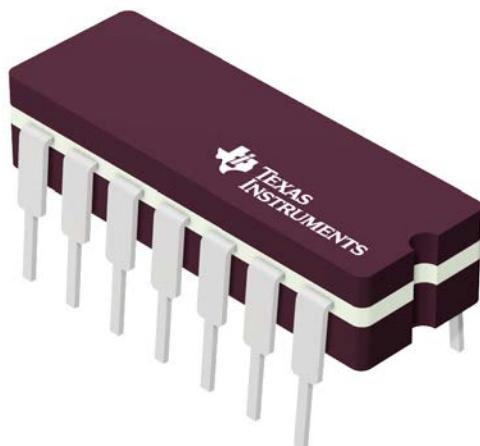
4229370VA\

# GENERIC PACKAGE VIEW

**J 14**

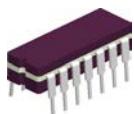
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

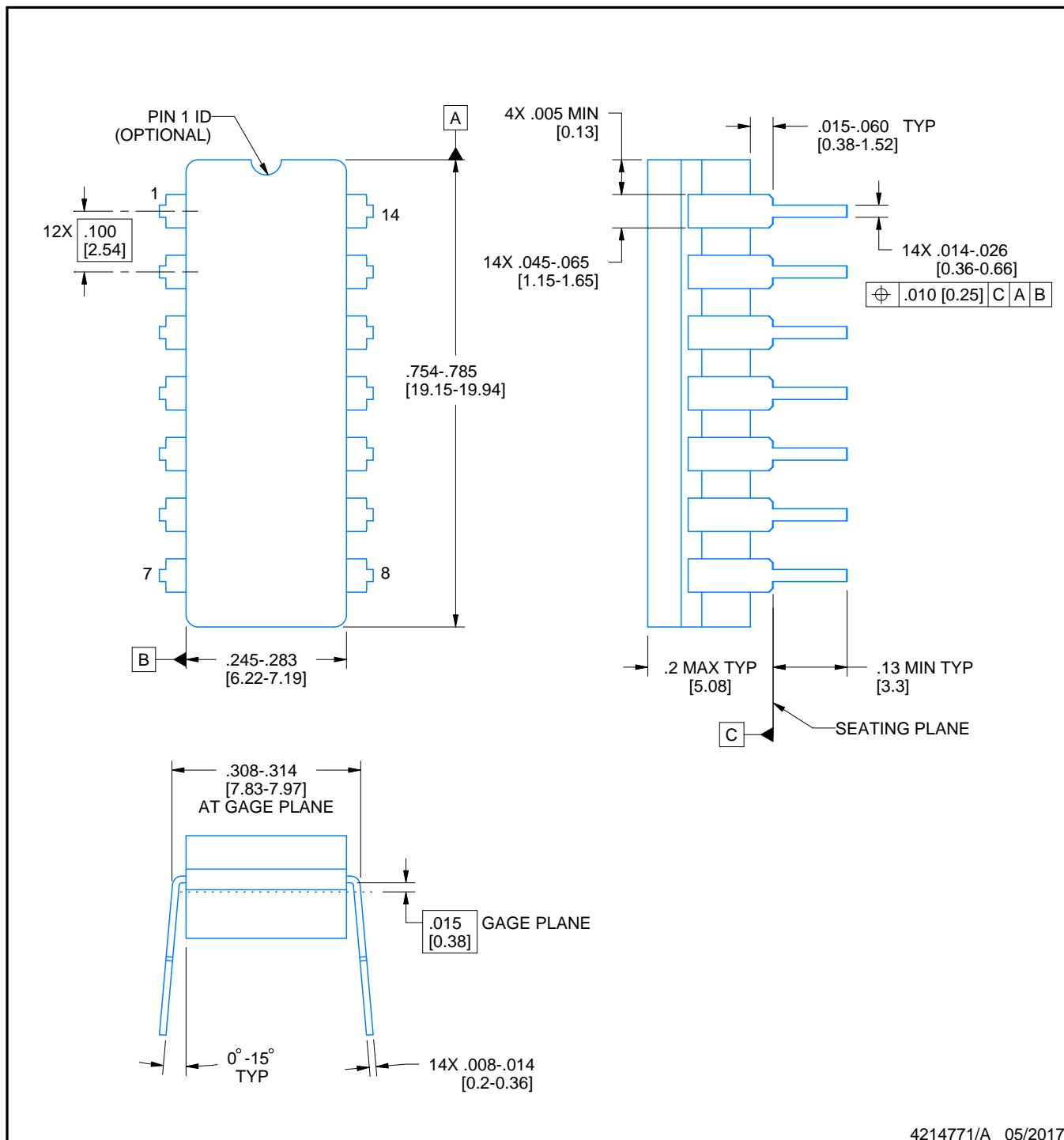


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

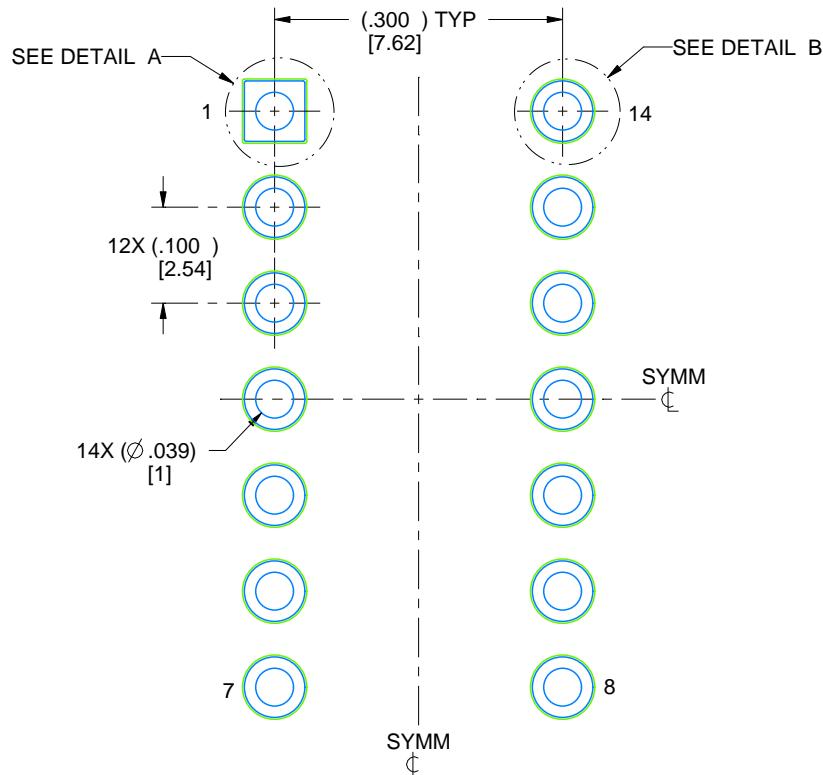
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

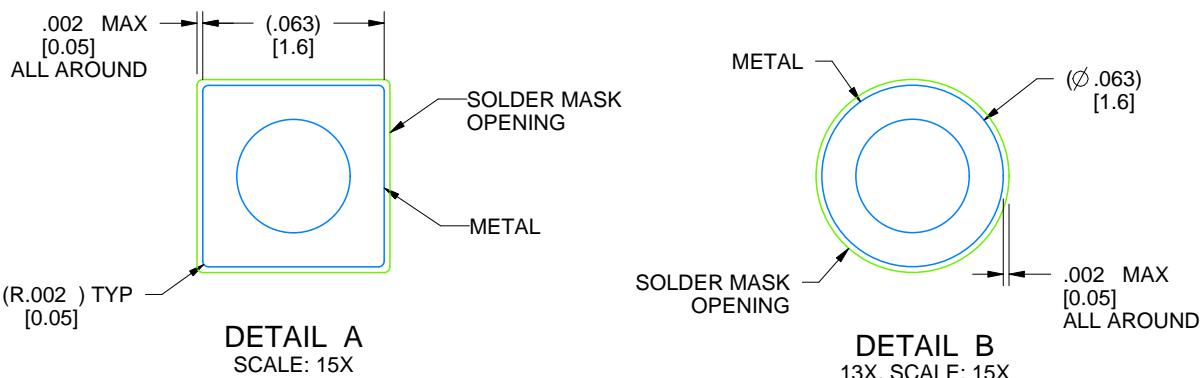
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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